EdgeBoard AI Box & Accelerator Card（FZ5）Hardware Manual

Version V1.0

Revision History

Version	Description	Date
V1.0	Initial Version	2020/08/10

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Chapter 1 Overview

1.1 Product Description

Baidu Brain EdgeBoard AI box / Accelerator Card is a high performance, high reliability AI box / accelerator card jointly launched by Baidu and Myir. This product is based on Xilinx zynq ultrascale + MPSoC series FPGA scalable computing architecture, can support secondary development and high-precision model / multi model deployment. Meanwhile, it is equipped with Baidu Brain PaddlePaddle AI framework, which can seamlessly connect Baidu Brain AI open ability and tool platform. It adopts wide temperature design and integrated fan free passive cooling, can adapt to the harsh environment of industrial scene. It is an excellent choice for batch AI project landing.

1.2 Picture

Figure 1-2

Product difference	
FZ5C-BOX	ZU5EV / 4GB DDR4 / 32GB eMMC
FZ5D-BOX	ZU5EV / 8GB DDR4 / 32GB eMMC
FZ5C-CARD	ZU5EV / 4GB DDR4 / 32GB eMMC
FZ5D-CARD	ZU5EV / 8GB DDR4 / 32GB eMMC

Table 1-2

Chapter 2 SOC introduction

2.1 SoC features

The XCZU5EV used in this development platform belongs to the Zynq UltraScale + MPSoC series SoC, integrating ARM quad-core Cortex-A53 (PS), dual-core Cortex-R5 (PS), Mali-400 MP2 graphics processing unit, VCU hardware codec unit and Kintex Ultrascale + FPGA (PL). The quad-core Cortex-A53 has powerful computing capabilities, the dual-core Cortex-R5 can be used for real-time processing applications, the Mali-400 MP2 can be used to accelerate graphics processing, and the FPGA is fully programmable. With the expandable I / O ports, it can adapt to a variety of application AI development scenarios.

The main chip of the AI development platform uses Xilinx XCZU5EV-2SFVC784I devices with a speed grade of -2. XCZU5EV-2SFVC784I supports 1.5GHz (max -2) APU speed, 600MHz (max -2) RPU speed, 667MHz (max -2) GPU speed, and DDR4 speed up to 2400Mbps. The XCZU5EV-2SFVC784I device has the following resources:

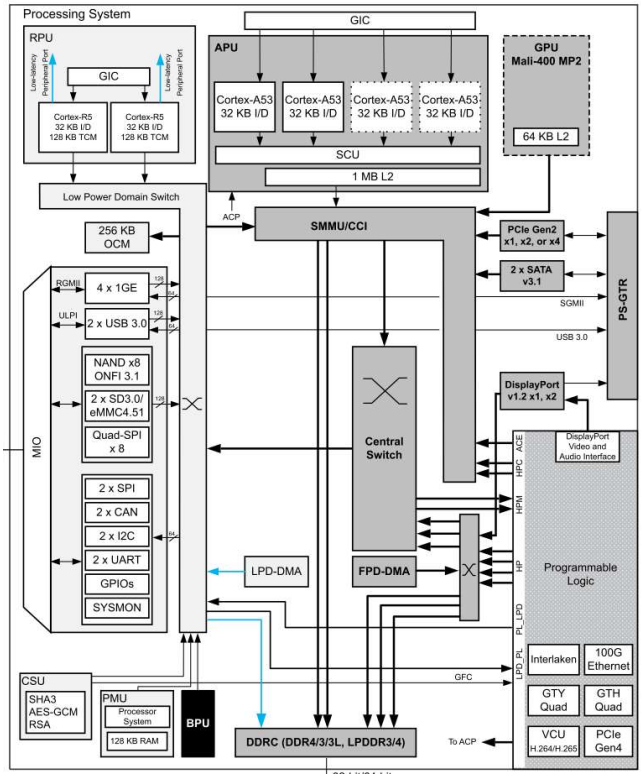


Figure 2-1

➢ **Processing System (PS)**

- **Processor Core:** Quad-core ARM Cortex-A53 MPCore up to 1.5GHz
- **Maximum Frequency:** 1.5Ghz
- **APU:** L1 Cache 32KB I / D per core, L2 Cache 1MB.
- **RPU：** L1 Cache 32KB I / D per core.
- **On-Chip Memory:** 256 KB
- **External Memory:** LPDDR4， DDR4， DDR3, DDR3L LPDDR3 with ECC
- **External Static Memory:** 2x Quad-SPI, NAND, NOR
- **DMA Channels:** 8 Programmable Logic（4 for PL）
- **Video Encoder/Decoder (VCU):** Accessible from either PS or PL, Simultaneous encode and decode, 264 and H.265 support
- **Peripherals:**
  - High speed: PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet.
  - Regular speed: 2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO

➢ **Programmable Logic (PL)**

	XCZU5EV
Logic Equivalent	Xilinx Kintex Ultrascale+®FPGA
Programmable Logic Cells	256K
Look-Up Tables	117K
Flip-Flops	234K
Block RAM	Distributed RAM 5.1Mb/ Block RAM 18.0Mb
DSP slice	1248
AMS-System Monitor	1

Table 2-1

2.2 SoC BANK

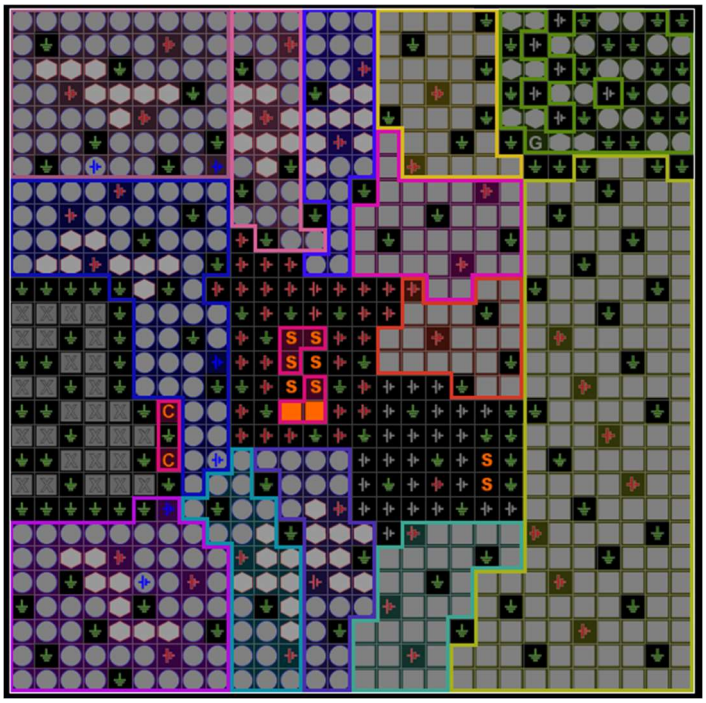


Figure 2-2 XCZU5EV SFVC784 Banks

- **BANK 0 :** humidity Sensor, XADC , Other configuration signals
- **BANK 24： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 25： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 26： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 44： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 64： PL** HP BANK, 52Pin(26 pairs of differential signal)
- **BANK 65： PL** HP BANK, 52Pin(26 pairs of differential signal)
- **BANK 66： PL** HP BANK, 52Pin(26 pairs of differential signal)
- **BANK 500:** PS side, MIO[00:25] 26pin， multiplex pin
- **BANK 501:** PS side, MIO[26:51] 26pin， multiplex pin
- **BANK 502:** PS side, MIO[52:77] 26pin， multiplex pin
- **BANK 503:** PS side, PS configuration pin, includeJTAG boot configuration reset, etc.
- **BANK 504:** PS side, DDR BANK
- **BANK 505:** PS side, MGTR BANK
- **BANK 224:** PL side， MGTH BANK

Chapter 3 Onboard Resources

3.1 Hardware resources

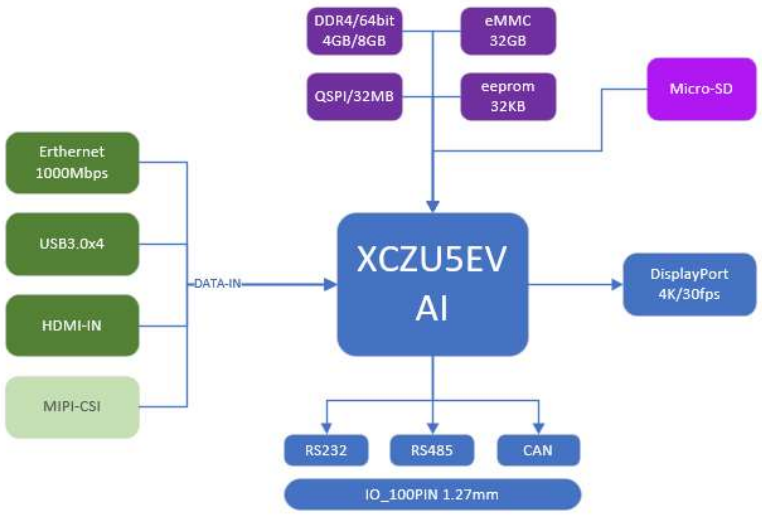


Figure 3-1

➢ Hardware resources

- 4GB/8GB DDR4 SDRAM（64bit 2400Mbps）
- 32GB eMMC
- 32MB QSPI
- Gigabit Ethernet
- RS232 * 1，RS485 * 1，CAN *1

➢ Peripheral interface and resources

- 1 Channel SD/MMC interface
- 4 Channel USB3.0 tyepA
- 1 Channel RJ45 Ethernet interface
- 1 Channel Mini Displayport interface
- 1 Channel HDMI in interface
- 1 System reset key，1 FPGA reset key
- 1 Channel MIPI-CSI interface

- 1 Channel JTAG interface，1 Channel USB to UART debug interface
- 1 Channel 100PIN 1.27mm spacing IO expander
- 3 onboard LED status, 2 indicators LED.

3.2 Boot Mode & JTAG Mode

The development board provides two boot modes by default. Users can select to boot the system from the TF CARD or the QSPI flash. For detailed information, refer to the table below.

Name	PS_MODE0	PS_MODE1	PS_MODE2	PSMODE3
SW1	1	2	3	4
JTAG	ON	ON	ON	ON
QSPI32	ON	OFF	ON	ON
SD1	OFF	ON	OFF	ON

Table 3-2

PS: OFF=1.ON=0

3.3 DDR4

The development Board incorporates four Micron DDR4 memory chips (MT40A512M16LY-062E IT:E) forming a 512M x 64-bit interface with a total of 4GB RAM(optional 8GB). The DDR4 memorys are connected to the memory controller in the PS of the Zynq® UltraScale+™ MPSoC, which supports access speed up to 2400 MT/s。

3.4 Storage

3.4.1 SPI Flash

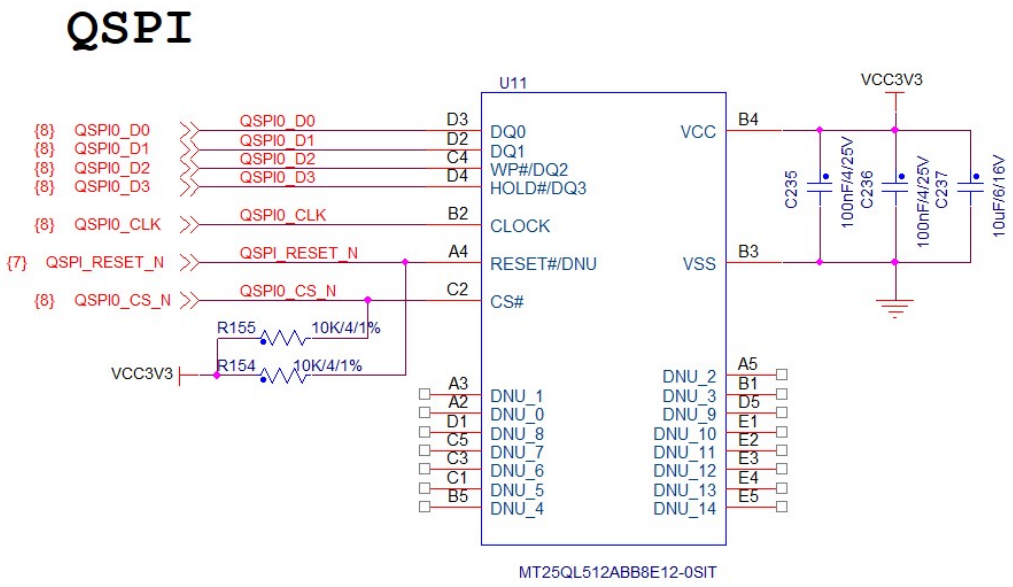


Figure 3-4-1

The development Board incorporates 1 Quad-SPI Flash(MT25QL512ABB8E12-0SIT), Connect to the QSPI0 interface of the CPU—PS_MIO0 ~ PSMIO5 pins of BANK500:

Zynq name	Net	Ball
PS_MIO0	QSPI_LOWER_SCK	AG15
PS_MIO1	QSPI_LOWER_D1	AG16
PS_MIO2	QSPI_LOWER_D2	AF15
PS_MIO3	QSPI_LOWER_D3	AH15
PS_MIO4	QSPI_LOWER_D0	AH16
PS_MIO5	QSPI_LOWER_CS	AD16

Table 3-4-1

It can be used to initialize the PS subsystem and configure the PL subsystem (bitstream).

3.4.2 eMMC

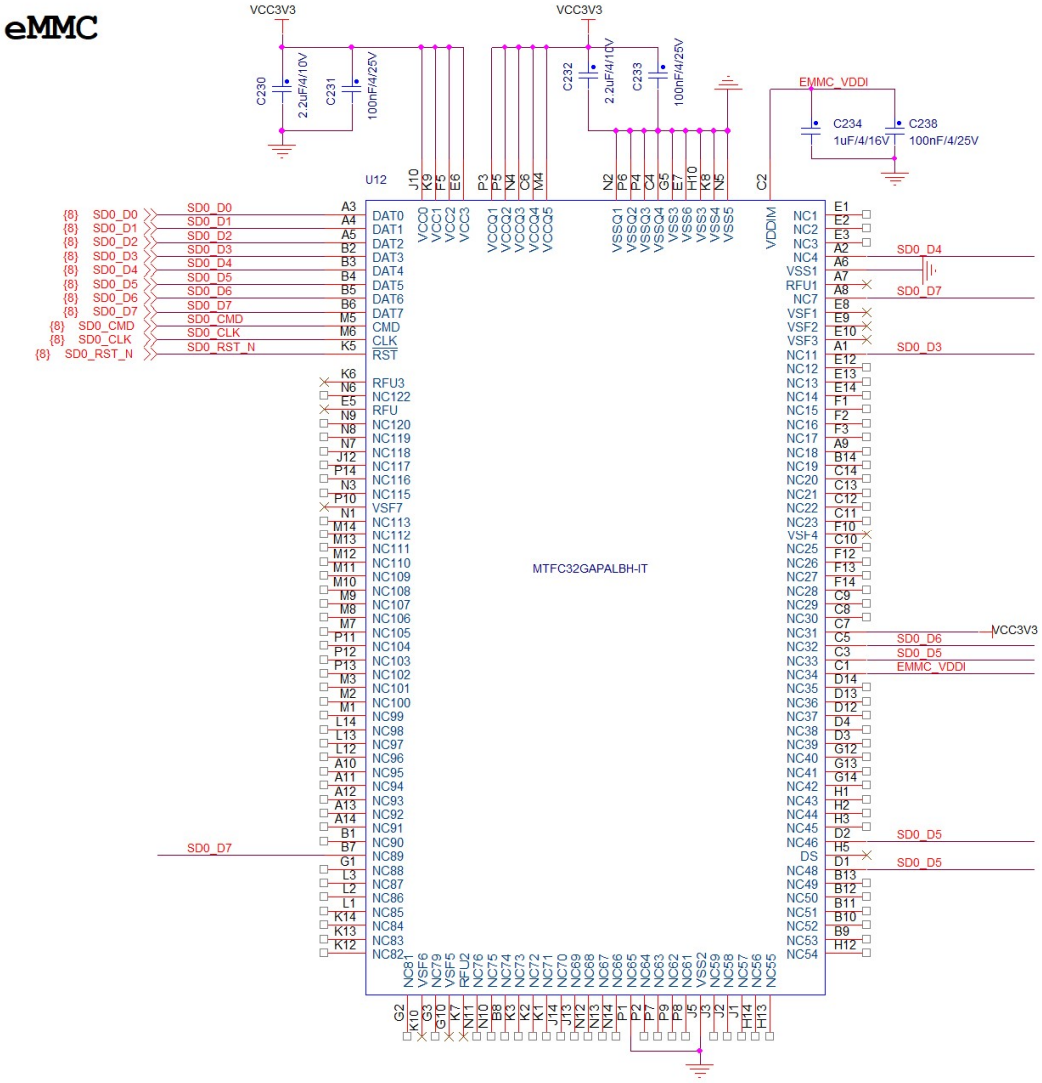


Figure 3-4-2

Onboard Micron 32GB eMMC -- MTFC32GAPALBH-IT，8 bit interface，Connectted to CPU SDIO0-- PS_MIO13 ~ PS_MIO23 pins of BANK500:

Zynq name	Net	Ball
PS_MIO13	SD0_D0	AH18
PS_MIO14	SD0_D1	AG18
PS_MIO15	SD0_D2	AE18
PS_MIO16	SD0_D3	AF18
PS_MIO17	SD0_D4	AC18
PS_MIO18	SD0_D5	AC19
PS_MIO19	SD0_D6	AE19
PS_MIO20	SD0_D7	AD19

PS_MIO21	SD0_CMD	AC21
PS_MIO22	SD0_CLK	AB20
PS_MIO23	SD0_RST_N	AB18

Table 3-4-2

3.4.3 eeprom

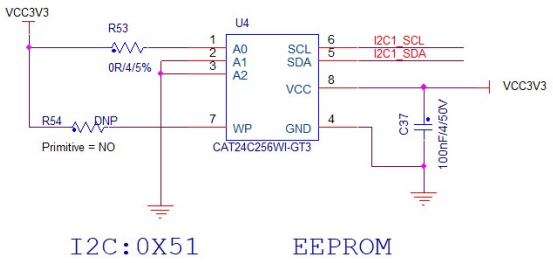


Figure 3-4-3

Onboard 32KB eeprom -- CAT24C256WI-GT3，connected to the I2C1 bus and used to store system data, such as ethernet mac address, product serial number, etc.

Zynq name	Net	Ball
PS_MIO24	I2C1_SCL	AB19
PS_MIO25	I2C1_SDA	AB21

Table 3-4-3

3.5 Ethernet

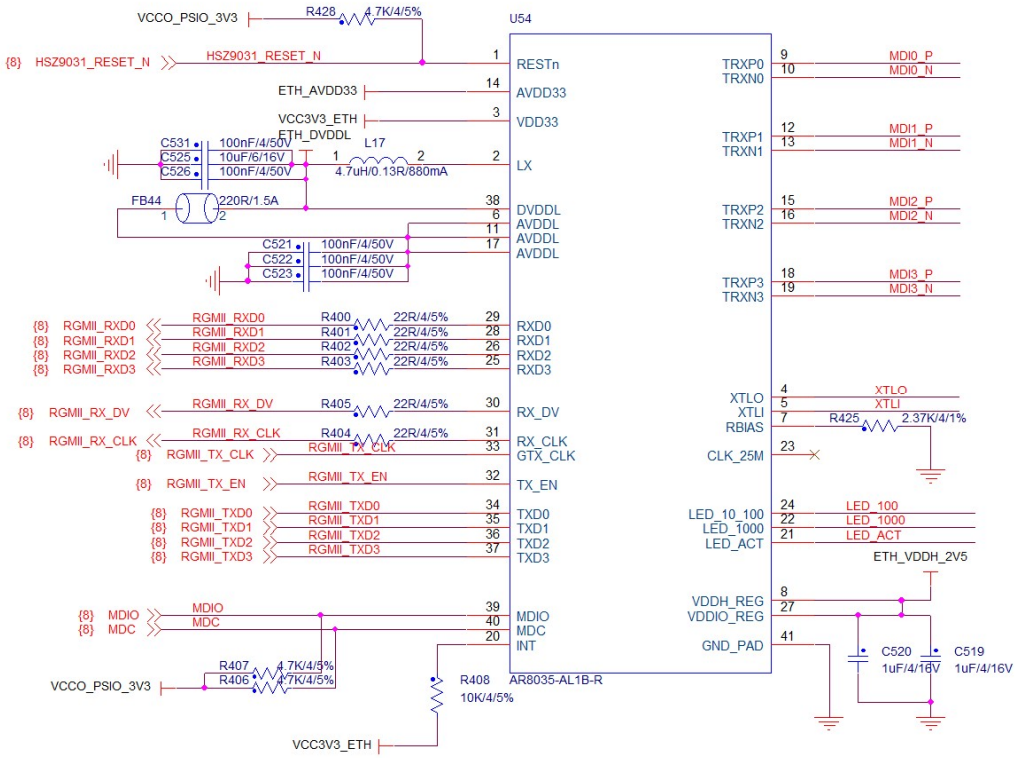


Figure 3-5

The PS unit of Zynq UltraScale + contains a Gigabit Ethernet MAC hardware controller, and an Ethernet physical layer transmission chip needs to be connected to the outside. The development board uses AR8035-AL1B-R as the PHY, and uses the PS RGMII interface to connect a Gigabit Ethernet mouth. The IIC address of PHY is 0x4.

AR8035-AL1B-R is connected to the PS_MIO64 ~ PS_MIO77 pins of the CPU's ETH0-BANK501:

Zynq name	Net	Ball
PS_MIO64	RGMII_TX_CLK	E19
PS_MIO65	RGMII_TXD0	A18
PS_MIO66	RGMII_TXD1	G19
PS_MIO67	RGMII_TXD2	B18
PS_MIO68	RGMII_TXD3	C18
PS_MIO69	RGMII_TX_EN	D19
PS_MIO70	RGMII_RX_CLK	C19
PS_MIO71	RGMII_RXD0	B19

PS_MIO72	RGMII_RXD1	G20
PS_MIO73	RGMII_RXD2	G21
PS_MIO74	RGMII_RXD3	D20
PS_MIO75	RGMII_RX_DV	A19
PS_MIO76	MDC	B20
PS_MIO77	MDIO	F20
PS_MIO30	HSZ9031_RESET_N	F16

Table 3-5

3.6 USB

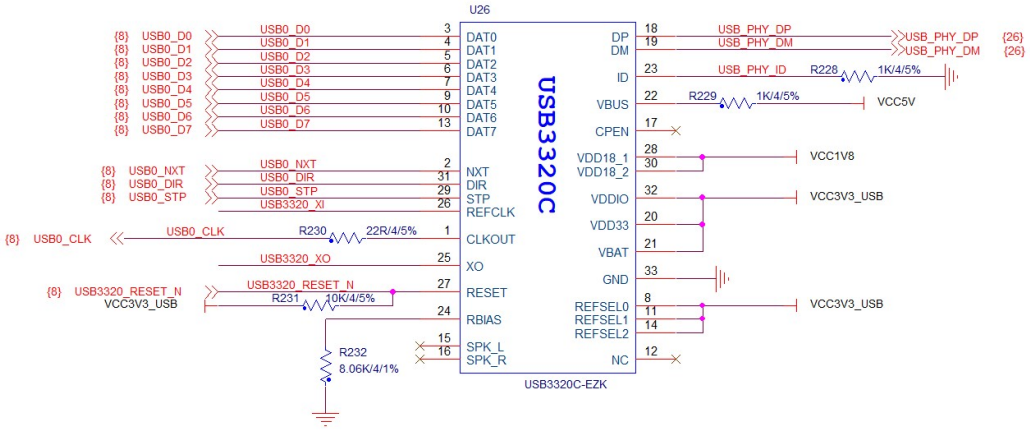


Figure 3-6

Zynq ’s PS-side USB controller is connected to a SMSC company ’s USB PHY chip USB3320C to form a USB 2.0 port as a USB Host, and then expands four USB2.0 ports through GL852G. One of the port signals is combined with the PS 3.0 USB port Together form a USB3.0 port, and several other ports are led out as separate USB2.0 ports.

USB3320C is connected to the PS_MIO52 ~ PS_MIO63 pins of the USB0-BANK501 of the CPU.

Zynq name	Net	Ball
PS_MIO52	USB0_CLK	G18
PS_MIO53	USB0_DIR	D16
PS_MIO54	USB0_D2	F17
PS_MIO55	USB0_NXT	B16

PS_MIO56	USB0_D0	C16
PS_MIO57	USB0_D1	A16
PS_MIO58	USB0_STP	F18
PS_MIO59	USB0_D3	E17
PS_MIO60	USB0_D4	C17
PS_MIO61	USB0_D5	D17
PS_MIO62	USB0_D6	A17
PS_MIO63	USB0_D7	E18

Table 3-6

3.7 Multi-channel programmable clock generator

This development platform has a programmable IDT SI5332 I2C programmable clock generator. This clock IC generates the necessary clock for the entire system through external 26 MHz crystal oscillator after frequency multiplication and frequency division processing. The schematic diagram is as follows:

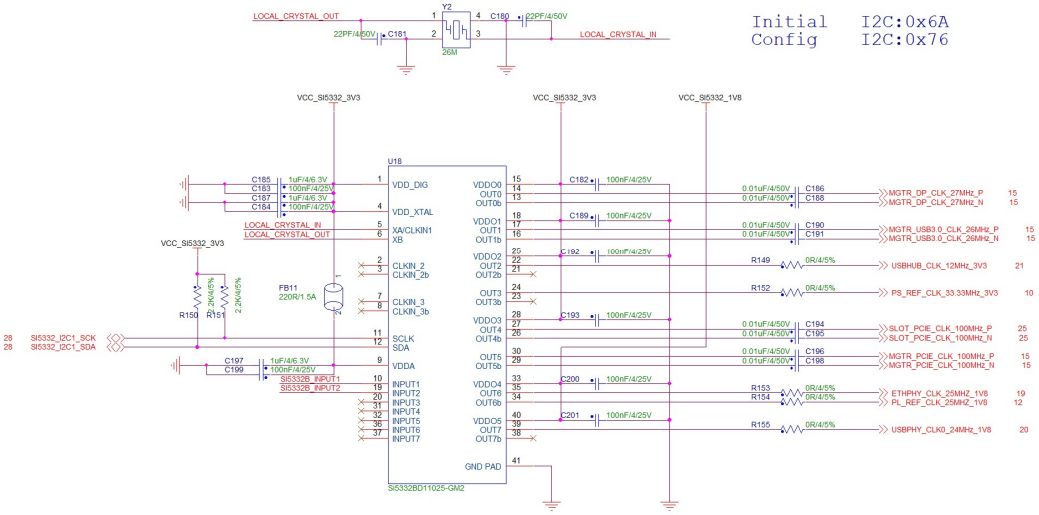


Figure 3-7-1

3.8 External watchdog and reset

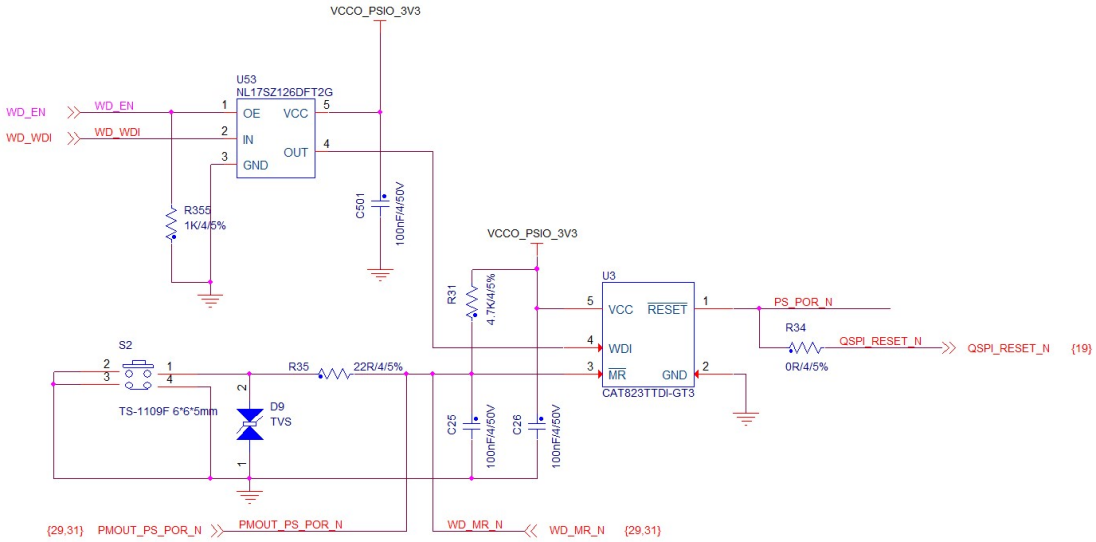


Figure 3-8-1

This development platform uses the external watchdog chip CAT823TTDI-GT3. The feeding pin of the chip is connected to the PS_MIO38 pin of the CPU, and the watchdog switch is set through PS_MIO33. The watchdog is closed by default. If you want to turn on the watchdog, set MIO33 to high.

Chapter 4 Hardware Interface

4.1 Interface summary

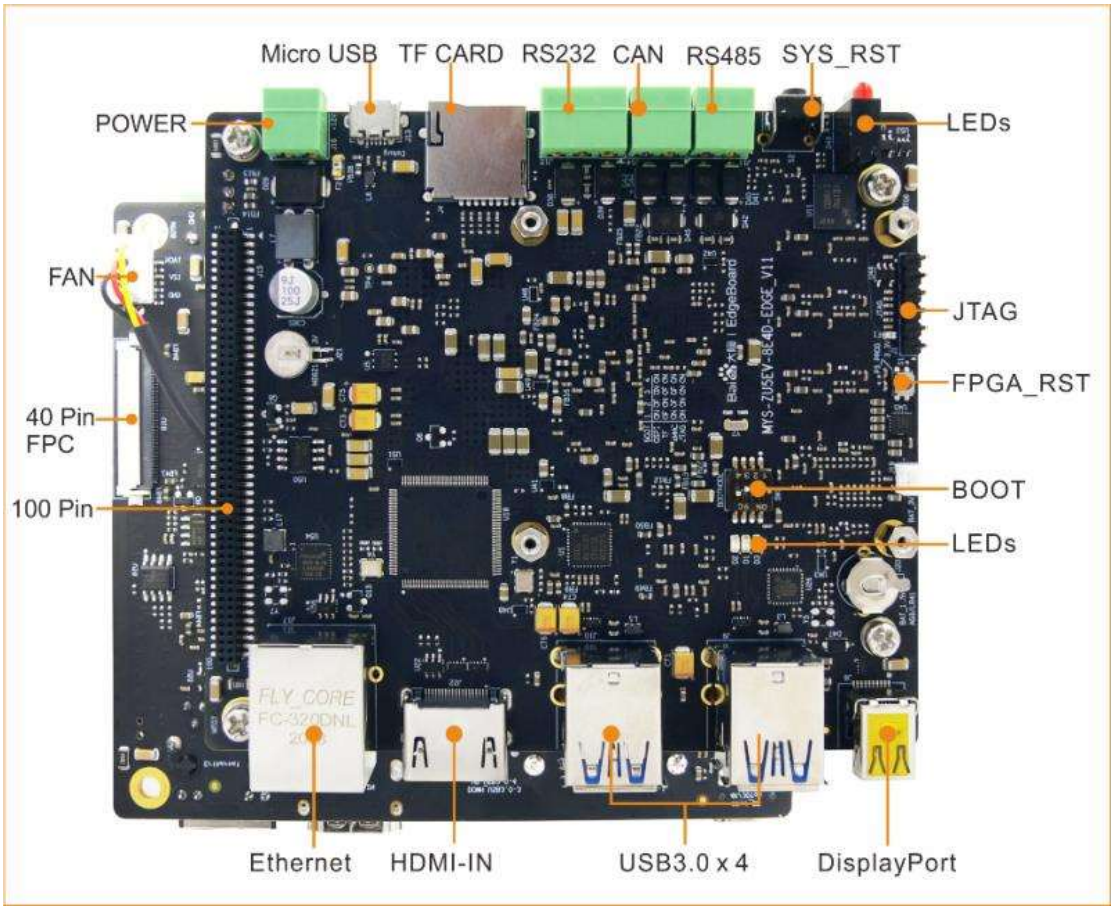


Figure 4-1

Num	Description
J16	POWER(12V/3A)
J13	Micro USB to uart
J4	TF card slot (PS)
J12	RS232
J14	CAN
J11	RS485
J6	DisplayPort (PS)
J9，J10	4xUSB3.0 (PS)
J22	HDMI input
J17	Ethernet (PS)
J15	100PIN expansion IO
J10	MIPI-CSI input (PL)

Num	Description
J2	FAN connector
J1	JTAG
J19	3V BAT connector
J20	1.5V BAT connector

Table 4-1

4.2 PS Unit

4.2.1 DisplayPort

One DisplayPort 1.2a interface, led from PS-side GTR, supports 4K / 30fps video output. The port is J6.

4.2.2 Ethernet

One 10/100 / 1000Mbps Ethernet RJ45 interface, the port is J17.

4.2.3 USB3.0 HOST

One USB 2.0 and one USB3.0 join together then connected to USB3.0 hub USB5744, Expand 4 USB3.0 ports TYPE-A interface, as HOST, the interface is J9 and J10.

4.2.4 TF Card

One TF card slot, used for startup or storage, the interface is J4.

TF card		
Zynq name	Net	Ball
PS_MIO45	SD1_CD	K20
PS_MIO46	SD1_D0	L20
PS_MIO47	SD1_D1	H21
PS_MIO48	SD1_D2	J21
PS_MIO49	SD1_D3	M18
PS_MIO50	SD1_CMD	M19
PS_MIO51	SD1_CLK	L21

Table 4-2-3

4.2.5 RS232

One Standard RS232 interface, used for external communication, the interface is J12.

4.2.6 CAN

One CAN interface, used for external communication, the interface is J14.

4.2.7 RS485

One standard RS485 interface, used for external communication, the interface is J11.

4.2.8 MicroUSB to UART

One MicroUSB to UART interface for debugging, the interface is J13.

4.2.9 JTAG

One 14 Pin ARM standard JTAG, can debug PS and PL unit, the corresponding pin signal name is marked on the back of the PCB, the port is J1.

J1	
1	VREF_3.3V
2	TDI
3	TDO
4	TCK
5	TMS
6	GND

Table 4-2-9

4.3 PL Unit

4.3.1 HDMI input

1 HDMI input interface, the control chip is ADV7619, connected to the PL, and supports the input resolution up to 4K/30fps. The port is J22.

4.3.2 MIPI-CSI

This development board has a MIPI-CSI interface on the PL end, and the MIPI signal directly passes through the IO on the PL end and enters the FPGA for decoding. For detailed IO details, please refer to the PINMAP. The posr is U18.

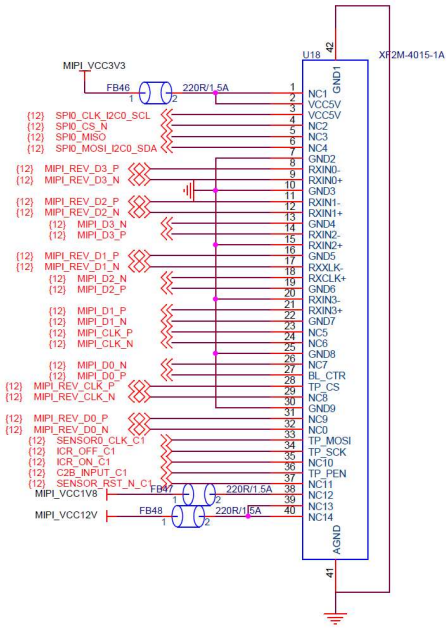


Figure 4-3-1

4.3.3 Expansion IO

This FZ5C uses a 2x50PIN 1.27 pin header for IO expansion, which includes 12V, 5V, 3.3V, 1.8V and other power outputs, including 5 PSMIO, 69 PL IO and other signals. The interface is J15. For detailed connector IO details, please refer to the FZ5C_PINMAP table. Please refer to the CD-ROM for some applicable connector specifications.

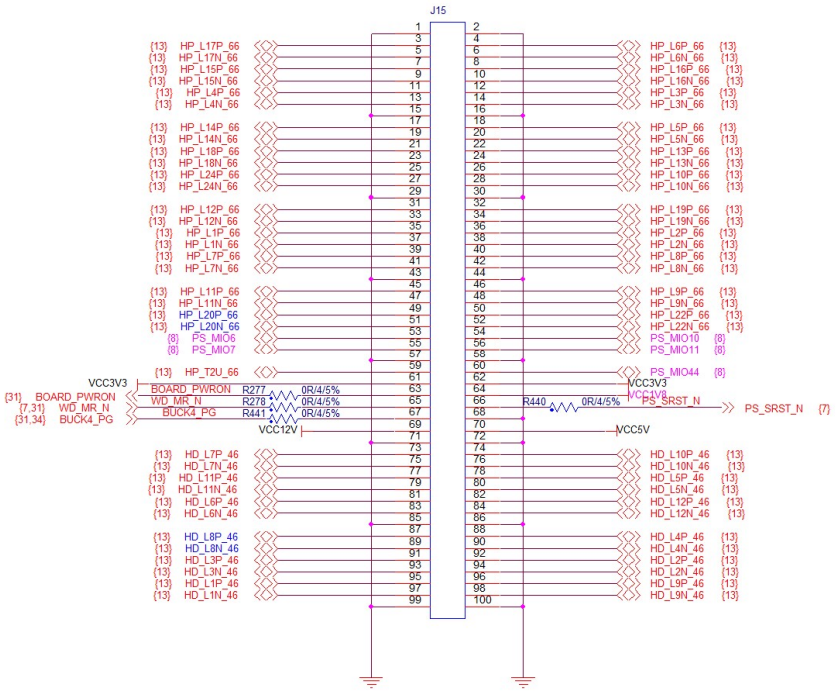


Figure 4-3-3

4.4 Other interface

4.4.1 Power input

The power input interface of this development board defaults to 12V input, and the overcurrent protection is 8A. It is recommended to use 12V / 3A power input. The interface is J16.

4.4.2 RTC bat connector

This development board has an onboard rechargeable battery, the model is MS621T (3V, position J21), or you can also use ordinary non-rechargeable 3V (terminal 1.27mm, position J19) or 1.5V (AG3/LR41, position J20) type battery.

4.4.3 Fan connector

This development board has a fan interface, which is powered by 12V by default. The fan speed can be detected through the PL terminal IO. The interface is J2.

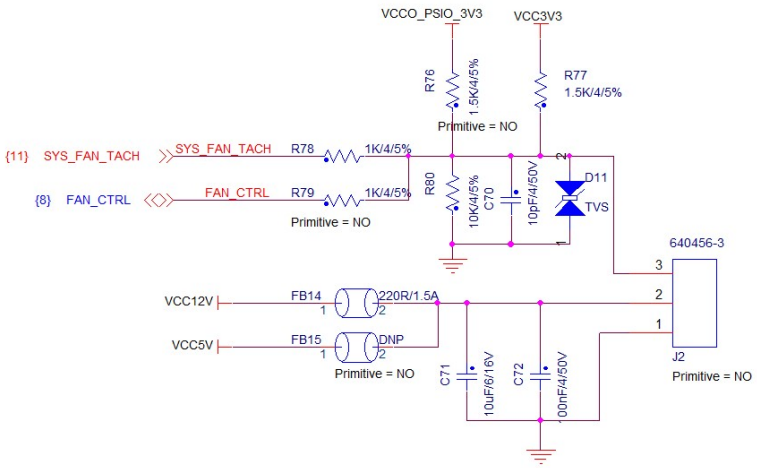


Figure 4-4-3

4.4.4 KEY&LED

This development platform has 2 buttons, an external button S2 is the system reset button, used to reset the entire system, and an internal button S1, used to reset the FPGA part. Two external LED status indicators, the red is the power indicator (the power is on when the power is running normally), and the green is the system operating status indicator (software control is required).

The functions of the onboard LED are described in the following table:

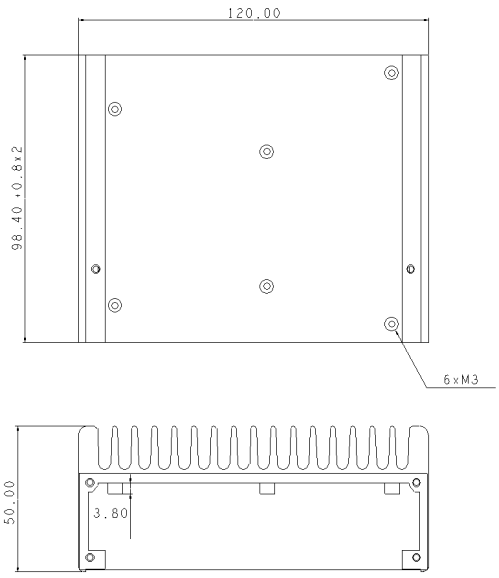
D1	PS_ERROR_OUT	RED
D2	PS_ERROR_STATUS	RED
D3	PS_DONE	GREEN
D46	POWER	RED
	RUN	GREEN

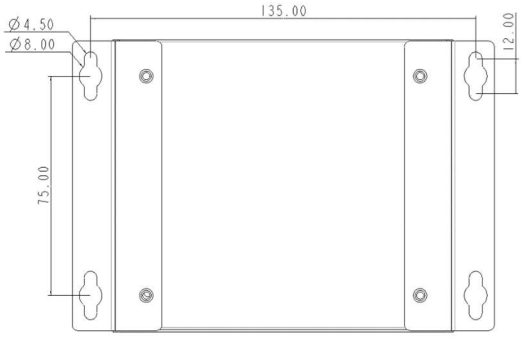
Table 4-4-4

NOTE: For the specific access pins of the signal, please refer to the Schematic and PINMAP table on the CD. There are detailed definitions and related trace length data.

Chapter 5 Mechanical parameters

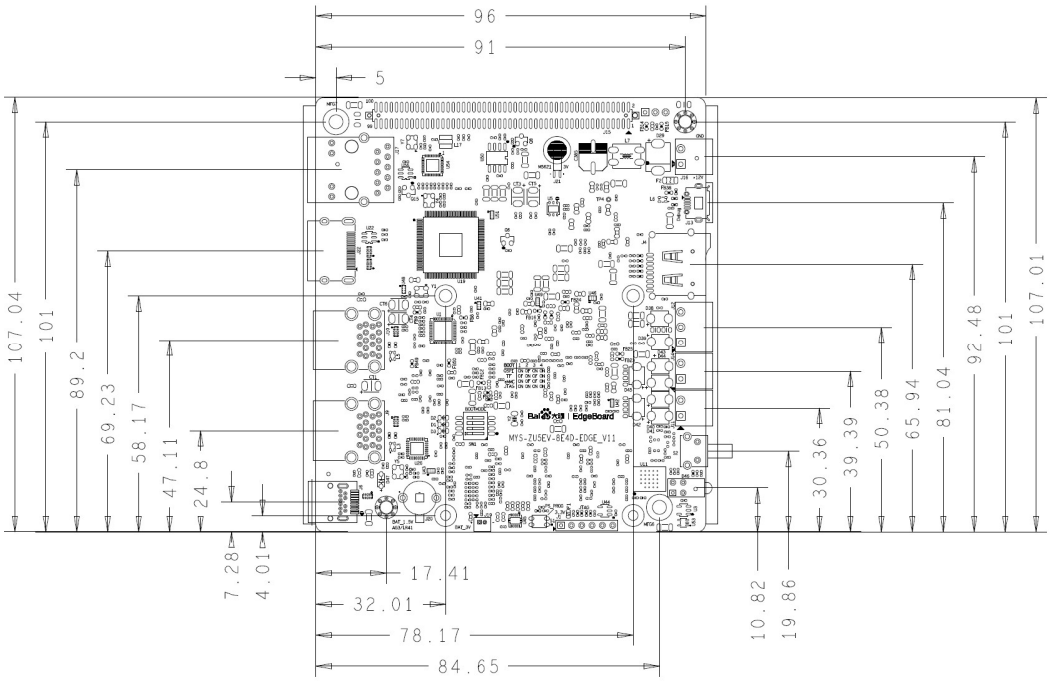
BOX:





- Operating Temperature：
  - Industrial：-40°C ~ +70°C
- Humidity：20%~90%
- Power Supply：
  - Board：12V/3A
  - RTC bat：1.5V/3V
- PCB layer：
  - 14 layer，Immersion Gold, Lead free
- Dimensions：
  - PCB：107mm x 96 mm
  - BOX：60 mm x 52 mm

Card:



- Operating Temperature：
  - Industrial：-40°C ~ +85°C
- Humidity：20%~90%
- Power Supply：
  - Board：12V/3A
  - RTC bat：1.5V/3V
- PCB layer：
  - 14 layer，Immersion Gold, Lead free
- Dimensions：
  - PCB：107mm x 96 mm
  - FAN：60 mm x 52 mm

Appendix 1 Warranty & Technical Support Services

MYIR Tech Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always

four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

1. Technical support service

a) MYIR offers technical support for the hardware and software materials which have provided to customers;

b) To help customers compile and run the source code we offer;

c) To help customers solve problems occurred during operations if users follow the user manual documents;

d) To judge whether the failure exists;

e) To provide free software upgrading service.

However, the following situations are not included in the scope of our free technical support service:

a) Hardware or software problems occurred during customers' own development;

b) Problems occurred when customers compile or run the OS which is tailored by themselves;

c) Problems occurred during customers' own applications development;

d) Problems occurred during the modification of MYIR's software source code.

2. After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

a) The warranty period is expired;

b) The customer cannot provide proof-of-purchase or the product has no serial number;

c) The customer has not followed the instruction of the manual which has caused the damage the product;

d) Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;

e) Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;

f) Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;

g) Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

1) MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.

2) Please do not use finger nails or hard sharp object to touch the surface of the LCD.

3) MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.

4) Do not clean the surface of the screen with chemicals.

5) Please read through the product user manual before you using MYIR's products.

6) For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

3. Maintenance period and charges

a) MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers

to confirm the maintenance period.

b) For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

4. Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

5. Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

1. MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
2. MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
3. MYIR provides other products supporting services like power adapter, LCD panel, etc.
4. ODM/OEM services.

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