

Ref	PIN	Net Name	BGA	Type	PIN MODE 0	PIN MODE 1	PIN MODE 2	PIN MODE 3	PIN MODE 4	PIN MODE 5	PIN MODE 6	PIN MODE 7
	1	+5V		PWR								
	2	+5V		PWR								
	3	+5V		PWR								
	4	+5V		PWR								
	5	GND		GND								
	6	GND		GND								
	7	GND		GND								
	8	GND		GND								
	9	NC										
	10	VRTC		PWR								
	11	NC										
	12	VDD_3V3B		PWR								
	13	NC										
	14	NC										
	15	LCD_DATA0	R1	I/O	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpw m2A		pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2_6
	16	LCD_DATA1	R2	I/O	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpw m2B		pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2_7
	17	LCD_DATA2	R3	I/O	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpw m2_tripzone_input		pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2_8
	18	LCD_DATA3	R4	I/O	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpw m0_synco		pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2_9
	19	LCD_DATA4	T1	I/O	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in		pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2_10
	20	LCD_DATA5	T2	I/O	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in		pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2_11
	21	LCD_DATA6	T3	I/O	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2_12
	22	LCD_DATA7	T4	I/O	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2_13
	23	NC										
	24	NC										
	25	LCD_DATA8	U1	I/O	lcd_data8	gpmc_a12	ehrpw m1_tripzone_input	mcasp0_aclcx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2_14

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	26	LCD_DATA9	U2	I/O	lcd_data9	gpmc_a13	ehrpw m0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio2_15
	27	LCD_DATA10	U3	I/O	lcd_data10	gpmc_a14	ehrpw m1A	mcasp0_axr0		pr1_mii0_rxd1	uart3_ctsn	gpio2_16
	28	LCD_DATA11	U4	I/O	lcd_data11	gpmc_a15	ehrpw m1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio2_17
	29	LCD_DATA12	V2	I/O	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlk	uart4_ctsn	gpio0_8
	30	LCD_DATA13	V3	I/O	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio0_9
	31	LCD_DATA14	V4	I/O	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	gpio0_10
	32	LCD_DATA15	T5	I/O	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio0_11
	33	NC										
	34	NC										
	35	LCDPCLK	V5	O	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out_4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio2_24
	36	LCDVSYNC	U5	O	lcd_vsync	gpmc_a8	gpmc_a1	pr1_edio_data_in2	pr1_edio_data_out_2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2_22
	37	LCDDE	R6	O	lcd_ac_bias_en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out_5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r31_11	gpio2_25
	38	LCDVHYNC	R5	O	lcd_hsync	gpmc_a9	gpmc_a2	pr1_edio_data_in3	pr1_edio_data_out_3	pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	gpio2_23
	39	NC										
	40	NC										
	41	NC										
	42	NC										
	43	MMC2_CLK	V12	O	gpmc_clk	lcd_memory_clk	gpmc_wait1	mmc2_clk	pri_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	gpio2_1
	44	MMC2_CMD	T13	O	gpmc_csn3	gpmc_a3	rmii2_crs_dv	mmc2_cmd	pr1_mii0_crs	pr1_mdio_data	EMU4	gpio2_0
	45	MMC2_DAT0	T12	I/O	gpmc_ad12	lcd_data19	mmc1_dat4	mmc2_dat0	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r30_14	gpio1_12
	46	MMC2_DAT1	R12	I/O	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30_15	gpio1_13
	47	MMC2_DAT2	V13	I/O	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31_14	gpio1_14
	48	MMC2_DAT3	U13	I/O	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_c_apin_apw_m_o	pr1_pru0_pru_r31_15	gpio1_15
	49	USER_BUTTON1	U10	O	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpw m2A	pr1_mii_mt0_clk		gpio0_22
	50	USER_BUTTON2	T10	O	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpw m2B	pr1_mii0_col		gpio0_23

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	51	GPIO0_26	T11	O	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpw m2_tripzone_input	pr1_mii0_txen		<a href="#">gpio0_26</a>
	52	GPIO0_27	U12	O	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpw m0_synco	pr1_mii0_txd3		<a href="#">gpio0_27</a>
	53	NC										
	54	NC										
	55	MMC1_DAT0	U7	I/O	gpmc_ad0	<a href="#">Mmc1_dat0</a>						Gpio1[0]
	56	MMC1_DAT1	V7	I/O	Gpmc_ad1	<a href="#">Mmc1_dat1</a>						Gpio1[1]
	57	MMC1_DAT2	R8	I/O	Gpmc_ad2	<a href="#">Mmc1_dat2</a>						Gpio1[2]
	58	MMC1_DAT3	T8	I/O	Gpmc_ad3	<a href="#">Mmc1_dat3</a>						Gpio1[3]
	59	MMC1_DAT4	U8	I/O	Gpmc_ad4	<a href="#">Mmc1_dat4</a>						Gpio1[4]
	60	MMC1_DAT5	V8	I/O	Gpmc_ad5	<a href="#">Mmc1_dat5</a>						Gpio1[5]
	61	MMC1_DAT6	R9	I/O	Gpmc_ad6	<a href="#">Mmc1_dat6</a>						Gpio1[6]
	62	MMC1_DAT7	T9	I/O	Gpmc_ad7	<a href="#">Mmc1_dat7</a>						Gpio1[7]
	63	NC										
	64	NC										
	65	GMII2_TXEN	R13	O	gpmc_a0	<a href="#">gmii2_txen</a>	rgmii2_tctl	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpw m1_tripzone_inp	gpio1_16
	66	GMII2_RXDV	V14	O	gpmc_a1	<a href="#">gmii2_rxdv</a>	rgmii2_rctl	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpw m0_synco	gpio1_17
	67	GMII2_TXD3	U14	O	gpmc_a2	<a href="#">gmii2_txd3</a>	rgmii2_td3	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpw m1A	gpio1_18
	68	GMII2_TXD2	T14	O	gpmc_a3	<a href="#">gmii2_txd2</a>	rgmii2_td2	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpw m1B	gpio1_19
	69	GMII2_TXD1	R14	O	gpmc_a4	<a href="#">gmii2_txd1</a>	rgmii2_td1	rmii2_txd1	gpmc_a20	pr1_mii1_txd0	eQEP1A_in	gpio1_20
	70	GMII2_TXD0	V15	O	gpmc_a5	<a href="#">gmii2_txd0</a>	rgmii2_td0	rmii2_txd0	gpmc_a21	pr1_mii1_rxd3	eQEP1B_in	gpio1_21
	71	NC										
	72	NC										
	73	GMII2_TXCLK	U15	I	gpmc_a6	<a href="#">gmii2_txclk</a>	rgmii2_tclk	mmc2_dat4	gpmc_a22	pr1_mii1_rxd2	eQEP1_index	gpio1_22
	74	GMII2_RXCLK	T15	I	gpmc_a7	<a href="#">gmii2_rxclk</a>	rgmii2_rclk	mmc2_dat5	gpmc_a23	pr1_mii1_rxd1	eQEP1_strobe	gpio1_23
	75	GMII2_RXD3	V16	I	gpmc_a8	<a href="#">gmii2_rxd3</a>	rgmii2_rd3	mmc2_dat6	gpmc_a24	pr1_mii1_rxd0	mcasp0_aclkx	gpio1_24

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	76	GMII2_RXD2	U16	I	gpmc_a9	gmii2_rxd2	gmii2_rd2	mmc2_dat7 / rmii2_crs_dv	gpmc_a25	pr1_mii_mr1_clk	mcasp0_fsx	gpio1_25
	77	GMII2_RXD1	T16	I	gpmc_a10	gmii2_rxd1	rgmii2_rd1	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0	gpio1_26
	78	GMII2_RXD0	V17	I	gpmc_a11	gmii2_rxd0	rgmii2_rd0	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1	gpio1_27
	79	MDIO_CLK	M18	I	mdio_clk	timer5	uart5_txd	uart3_rtsn	mmc0_sdw p	mmc1_clk	mmc2_clk	gpio0_1
	80	MDIO_DATA	M17	I/O	mdio_data	timer6	uart5_rxd	uart3_ctsn	mmc0_sdc d	mmc1_cmd	mmc2_cmd	gpio0_0
	81	NC										
	82	NC										
	83	USB1_DP	R17	DIFF	USB1_DP							
	84	USB0_DRVVBUS	F16	O	USB0_DRVVBUS							GPIO0_18
	85	USB1_DM	R18	DIFF	USB1_DM							
	86	USB0_VBUS	P15	A	USB0_VBUS							
	87	NC										
	88	USB0_ID	P16	A	USB0_ID							
	89	USB0_DP	N17	DIFF	USB0_DP							
	90	USB0_CE	M15	A	USB0_CE							
	91	USB0_DM	N18	DIFF	USB0_DM							
	92	USB1_DRV	F15	O	USB1_DRV							GPIO3_13
	93	NC										
	94	USB1_VBUS	T18	A	USB1_VBUS							
	95											
	96	USB1_ID	P17	A	USB1_ID							
	97	GPMC_OEn_REn	T7	O	Gpmc_oen_ren		Timer7					GPIO2_3
	98	GPMC_BE0n_CLE	T6	O	Gpmc_be0n_cle		Timer5					GPIO2_5
	99	GPMC_ADVn_ALE	R7	O	Gpmc_advn_ale		Timer4					GPIO2_2
	100	GPMC_WEn	U6	O	Gpmc_wen		Timer6					GPIO2_4

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	101	NC										
	102	NC										
	103	MMC0_CLK	G17	O	<a href="#">mmc0_clk</a>	gpmc_a24	uart3_ctsn	uart2_rxd	dcan1_tx	pr1_pru0_pru_r30_12	pr1_pru0_pru_r31_12	gpio2_30
	104	MMC0_DAT0	G16	I/O	<a href="#">mmc0_dat0</a>	gpmc_a23	uart5_rtsn	uart3_txd	uart1_rin	pr1_pru0_pru_r30_11	pr1_pru0_pru_r31_11	gpio2_29
	105	MMC0_CMD	G18	O	<a href="#">mmc0_cmd</a>	gpmc_a25	uart3_rtsn	uart2_txd	dcan1_rx	pr1_pru0_pru_r30_13	pr1_pru0_pru_r31_13	gpio2_31
	106	MMC0_DAT1	G15	I/O	<a href="#">mmc0_dat1</a>	gpmc_a22	uart5_ctsn	uart3_rxd	uart1_dtrn	pr1_pru0_pru_r30_10	pr1_pru0_pru_r31_10	gpio2_28
	107	MCASP0_AHCLKX	A14	O	<a href="#">mcasp0_ahclkx</a>	eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3_21
	108	MMC0_DAT2	F18	I/O	<a href="#">mmc0_dat2</a>	gpmc_a21	uart4_rtsn	timer6	uart1_dsrn	pr1_pru0_pru_r30_9	pr1_pru0_pru_r31_9	gpio2_27
	109	NC										
	110	MMC0_DAT3	F17	I/O	<a href="#">mmc0_dat3</a>	gpmc_a20	uart4_ctsn	timer5	uart1_dcdn	pr1_pru0_pru_r30_8	pr1_pru0_pru_r31_8	gpio2_26
	111	NC										
	112	NC										
	113	NC										
	114	UART1_CTS	D18	O	<a href="#">uart1_ctsn</a>	timer6	dcan0_tx	I2C2_SDA	spi1_cs0	pr1_uart0_cts_n	pr1_edc_latch0_in	gpio0_12
	115	NC										
	116	UART1_RTS	D17	O	<a href="#">uart1_rtsn</a>	timer5	dcan0_rx	I2C2_SCL	spi1_cs1	pr1_uart0_rts_n	pr1_edc_latch1_in	gpio0_13
	117	UART0_TX	E16	O	<a href="#">uart0_txd</a>	spi1_cs1	dcan0_rx	I2C2_SCL	eCAP1_in_PWM1_out	pr1_pru1_pru_r30_15	pr1_pru1_pru_r31_15	gpio1_11
	118	UART1_TX	D15	O	<a href="#">uart1_txd</a>	mmc2_sdw p	dcan1_rx	I2C1_SCL		pr1_uart0_txd	pr1_pru0_pru_r31_16	gpio0_15
	119	UART0_RX	E15	I	<a href="#">uart0_rxd</a>	spi1_cs0	dcan0_tx	I2C2_SDA	eCAP2_in_PWM2_out	pr1_pru1_pru_r30_14	pr1_pru1_pru_r31_14	gpio1_10
	120	UART1_RX	D16	I	<a href="#">uart1_rxd</a>	mmc1_sdw p	dcan1_tx	I2C1_SDA		pr1_uart0_rxd	pr1_pru1_pru_r31_16	gpio0_14
	121	NC										
	122	NC										
	123	UART2_TX / UART5_RTS	J15	O	gmii1_rxerr	rmii1_rxerr	spi1_d1	I2C1_SCL	mcasp1_fsx	uart5_rtsn	<a href="#">uart2_txd</a>	gpio3_2
	124	UART3_TX	C18	O	eCAP0_in_PWM0_out	<a href="#">uart3_txd</a>	spi1_cs1	pr1_ecap0_ecap_capin_apw m_o	spi1_sclk	mmc0_sdw p	xdma_event_intr2	gpio0_7
	125	UART2_RX / UART5_CTS	H17	I	gmii1_crs	rmii1_crs_dv	spi1_d0	I2C1_SDA	mcasp1_ackx	uart5_ctsn	<a href="#">uart2_rxd</a>	gpio3_1

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