TC358774XBG/75XBG

DSI2LVDS Low Power Bridge Chip

TOSHIBA

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HISTORY

Revision	Date	Note
Rev 0.1	4/18/2012	Init
Rev 0.2	5/16/2012	1. Change PD pin to STBY pin to reflect its function and changed polarity to active “low” 2. Add Power State Diagram 3. Updated power on/off sequence 4. Replace Pin GPIO[4] with STBY, not “muxed”. No need for register bit 0x0400[7] 5. Reduce 0x0450[VSDelay] field to 10 bit 6. Add DSI debug register, 0x05A8
Rev 0.3	5/18/2012	Typo Corrections Remove GPIO[4] related register bits Update debug register 0x05A8
Rev 0.4	6/11/2012	1. All the reserved bits in register 0x0450 are defaulted to “0”. 2. Updated to match with RTL codes 3. Typo corrections
Rev 0.5	6/21/2012	1. Typo Correction 2. Remove CLKPOL1/2 bits. Update Register LVCFG and Fig 5-12
Rev 0.6	7/12/2012	1. Remove fields [13:10] in register I2CTIMCTRL (0x0540) 2. Remove registers DSIStart (0x0204) and DSIBusy (0x0208).
Rev 0.7	7/17/2012	1. Minimum values in register fields H/VTIM1/2 are ‘1’, not ‘0’ 2. Update clock structure Figure 5-5 3. Remove Modification #8 requirement in Rev 0.0 above
Rev 0.8	9/20/2012	1. Change register 0x0230 from R/W to RO 2. Update “RESTRICTIONS ON PRODUCT USE” page 3. Update registers 0x0224 4. Update LVDS IP info
Rev 0.9	10/31/2012	1. Typo Fixed 2. Update LVDS PHY 3. RDATAQ register address corrected to 0x54a 4. Typical Power Consumption updated
Rev 1.0	01/15/2013	1. Update section 5.2.3.6: using RefClk is option 2. Change max LVDS Clk from 85MHz to 135MHz.
Rev 1.1	02/25/2013	1. Update package info in Chapter 7 2. Update Table 5-3, 10-bit Slave address
Rev 1.2	02/25/2013	1. Remove “Draft” watermark
Rev 1.3	04/12/2013	1. Remove section 8.3.4 LVDS Transmitter Supply Current 2. Emphasize “don’t changes” on certain D-PHY register bits 3. HPW minimum requirement is 8-pixel
Rev 1.4	05/29/2013	Update Footer page

REFERENCE

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI Alliance Specification for DSI version 1.01, Feb 2008
3. MIPI Alliance Specification for DPI version 2.0, Sep, 2005
4. An Introduction to FPD-Link, AN-1032, Application Note, National Semiconductor 2009
5. DS90C383/DS90CF384 LVDS Transmitter 24-Bit FPD Link, Data Sheet, National Semiconductor 2000
6. THC63LVD823 Single/Dual Link LVDS Transmitter, Data Sheet, Thine Electronics, 2000-2003.
7. SN75LVDS83 FlatLink Transmitter, Data Sheet, Texas Instrument, 1997-2009.

Precautions and Usage Considerations Specific to Application Specific Standard Products and General-Purpose Linear Ics

1. ⚠ CAUTION

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

a. If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. For details on how to connect a protection circuit such as a current limiting resistor or back electromotive force adsorption diode, refer to individual IC datasheets or the IC databook. IC breakdown may cause injury, smoke or ignition.

b. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

c. Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

2. Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

3. Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the Thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

4. Heat Radiation Design
When using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These

Contents

List of Figures

List of Tables

1 Introduction

The TC358774/75XBG Functional Specification defines operation of the DSI2LVDS low power chip (or more abbreviated, 775XBG chip). 775XBG is the follow-up chip of TC358764/65XBG, which:

1. Is pin compatible to TC358764/65XBG
2. Exhibit LVDS Tx block operates at 1.8V @135 MHz to reduce operation power
3. Update 4-lane DSI Rx max bit rate @ 1 Gbps/lane to support 1920 x 1200 x 24 @60fps
4. Add STBY pin with to enable turning on VDDIO power first before other power supplies.

The primary function of this chip is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1600x1200 24-bit pixel resolution for single-link LVDS and up to WUXGA (1920x1200 24-bit pixels) resolution for dual-link LVDS. As a secondary function, the chip also supports an I2C Master which is controlled by the DSI link; this may be used as an interface to any other control functions through I2C.

The chip can be configured through the DSI link by sending write register commands through DSI Generic Long Write-packets. It can also be configured through the I2C Slave interface. I2C slave address of 775XBG is 8'b0001_111X, where X = 0/1 for write/read to/from 775XBG operation.

This specification provides description of two product versions:

TC358774XBG-49: In BGA49 package, it supports DSI-RX with up to 4 data lanes, and outputs to Single-Link LVDS.

TC358775XBG-64: In BGA64 package, it supports DSI-RX with up to 4 data lanes, and outputs to Dual-Link LVDS.

1.1 Scope

This document details the operation of the chip, description of each major function that the chip supports, description of the configuration register set, and includes pinout, package, and electrical characteristics information.

1.2 Purpose

This document serves as the vehicle for exchanging detailed technical information of the 775XBG chip and its usage within the target application systems at the customer side. It also serves as the chip functional specification for design implementation and verification.

2 Device Overview

The 775XBG chip functions primarily as a DSI-to-LVDS communication protocol bridge, enabling video streaming from a Host processor over DSI link to drive LVDS-compatible display panels. In other words, the chip receives video stream input through its DSI receiver (DSI-RX), buffers the received pixel data in a buffer, and then re-transmits the video stream out through the LVDS transmitter.

As a secondary function, the chip also ports an I2C Master which is controlled by the DSI link; this may be used as a programming interface to other peripherals in the system.

The chip is configured through the DSI link. Alternatively, it can optionally be configured through the I2C Slave interface; in such case, the I2C Master function would be disabled.

The reference video pixel clock for the LVDS link is sourced either from an external clock via input pin EXTCLK or derived from DSICLK. The chip integrates a PLL which synthesizes the high-speed clock for use solely to serialize video data over the LVDS link.

The DSI-RX receiver supports from 1- to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in video mode. In video mode, Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only 1024-pixel of video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The LVDS transmitter supports a clock frequency of up to 135 MHz for either single- or dual-link.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption states by using ULPS signaling over DSI link and/or STBY pin.

3 Features

- **DSI Receiver**
  - Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
  - Maximum bit rate of 1 Gbps/lane
  - Video input data formats:
    - RGB565 16 bits per pixel
    - RGB666 18 bits per pixel
    - RGB666 loosely packed 24 bits per pixel
    - RGB888 24 bits per pixel.
  - Video frame size:
    - Up to 1600x1200 24-bit/pixel resolution to single-link LVDS display panel, limited by 135 MHz LVDS speed
    - Up to WUXGA resolutions (1920x1200 24-bit pixels) to dual-link LVDS display panel, limited by 4 Gbps DSI link speed
  - Supports Video Stream packets for video data transmission.
  - Supports generic long packets for accessing the chip's register set
  - Supports the path for Host to control the on-chip I2C Master

- **LVDS FPD Link Transmitter**
  - Supports single-link or dual-link
  - Maximum pixel clock frequency of 135 Mhz.
  - Maximum pixel clock speed of 135 MHz for single-link or 270 MHz for dual-link
  - Supports display up to 1600x1200 24-bit/pixel resolution for single-link, or up to 1920x1200 24-bit resolutions for dual-link
  - Supports the following pixel formats:
    - RGB666 18 bits per pixel
    - RGB888 24 bits per pixel.
  - Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality equivalent to that of an RGB888 24-bit panel
  - Flexible mapping of parallel data input bit ordering
  - Supports programmable clock polarity
  - Supports two power saving states
    - Sleep state, when receiving DSI ULPS signaling
    - Standby state, entered by STBY pin assertion

- **System Operation**
  - Host configures the chip through DSI link
  - Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses
  - Includes an I2C Master function which is controlled by Host through DSI link (multi-master is not supported)
  - Power management features to save power
  - Configuration registers is also accessible through I2C Slave interface

- **Clock Source**

- LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
- A built-in PLL generates the high-speed LVDS serializing clock requiring no external components

- **Digital Input/Output Signals**
  - All Digital Input signals are 3.3V tolerant
  - All Digital Output signals can output ranging from 1.8V to 3.3V depending on IO supply voltage

- **Power supply**
  - MIPI DSI D-PHY: 1.2 V
  - LVDS PHY: 1.8 V
  - I/O: 1.8 V - 3.3V (all IO supply pins must be same level)
  - Digital Core: 1.2 V

- **Power Consumption**
  - Power Down State is achieved by:
    1. Reset asserted
    2. EXTCLK not toggling
    3. STBY=0
    4. DSI in ULPS Drive

Reduced Mode							
	VDDC	VDDS	DSI	LVDS		TOTAL Power	Unit
	VDDC	VDDIO	VDD1	LVDS1.2	LVDS1.8		
	1.2	1.8	1.2	1.2	1.8		V
720x480x18 @26 MHz	8.60	0.11	8.40	3.60	10.00		mA
	10.32	0.20	10.08	4.32	18.00	42.92	mW
1366x768x18 @85 MHz	17.2	0.13	14.6	8.3	11.1		mA
	20.64	0.23	17.52	9.96	19.98	68.33	mW
1920 x 1080x18 Dual Link @74MHz	18.57	0.092	19.77	8.123	22.4		mA
	22.28	0.17	23.72	9.75	40.32	96.24	mW
Power Down	0.03	0.01	0.02	0.01	0.02		mA
	0.04	0.02	0.02	0.01	0.04	0.09	mW

- **Packaging Information**

  - BGA64 (0.65mm ball pitch)
    - Supports DSI-RX 4-data-lanes + Dual-Link LVDS-TX
    - 6.0mm x 6.0mm x 1.2mm

  - BGA49 (0.65mm ball pitch)
    - Supports DSI-RX 4-data-lanes + Single-Link LVDS-TX
    - 5.0mm x 5.0mm x 1.2mm

4 Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8
VSS_LVDS2_12	LVTX2AN	LVTX2BN	LVTX2CN	LVTX2DN	LVTX2EN	VSS_LVDS2_18	VSS_LVDS1_12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**
VDD_LVDS2_12	LVTX2AP	LVTX2BP	LVTX2CP	LVTX2DP	LVTX2EP	VDD_LVDS2_18	VDD_LVDS1_12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**
VSSIO	VDDIO	STBY	GPIO3	VDD_LVDS2_18	VSS_LVDS2_18	LVTX1AP	LVTX1AN
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**
EXTCLK	GPIO2	GPIO1	RESX	TM	VDD_LVDS1_18	LVTX1BP	LVTX1BN
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**
VSSC	VDDC	GPIO0	VDDC	VSSC	VSS_LVDS1_18	LVTX1CP	LVTX1CN
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**
VSSIO	VDDIO	VDD_MIPI	VSS_MIPI	VSS_MIPI	VDD_MIPI	LVTX1DP	LVTX1DN
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**
I2C_SCL	DSRXD0P	DSRXD1P	DSRXCP	DSRXD2P	DSRXD3P	LVTX1EP	LVTX1EN
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**
I2C_SDA	DSRXD0M	DSRXD1M	DSRXCM	DSRXD2M	DSRXD3M	VDD_LVDS1_18	VSS_LVDS1_18

Figure 4-1 TC358775XBG Chip Pin Layout (BGA64 – Top View)

A1	A2	A3	A4	A5	A6	A7
VSSIO	VDDIO	RESX	GPIO0	VSSC	VDDC	VSSC
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**
EXTCLK	VDDC	VSSC	TM	VDD_LVDS1_12	LVTX1AP	LVTX1AN
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**
I2C_SDA	GPIO3	GPIO2	GPIO1	VSS_LVDS1_12	LVTX1BP	LVTX1BN
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
I2C_SCL	STBY	VSS_MIPI	VDD_MIPI	VSS_LVDS1_18	LVTX1CP	LVTX1CN
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**
VDDIO	VSSIO	VSS_MIPI	VDD_MIPI	VDD_LVDS1_18	LVTX1DP	LVTX1DN
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**
DSRXD0P	DSRXD1P	DSRXCP	DSRXD2P	DSRXD3P	LVTX1EP	LVTX1EN
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**
DSRXD0M	DSRXD1M	DSRXCM	DSRXD2M	DSRXD3M	VDD_LVDS1_18	VSS_LVDS1_18

Figure 4-2 TC358774XBG Chip Pin Layout (BGA49 – Top View)

4.1 BGA64 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	Power Supply Voltage
DSI RX IF	DSICP	DSI-PHY	1	DSI clock signal - positive	1.2 V
	DSICM	DSI-PHY	1	DSI clock signal - negative	1.2 V
	DSIDP[3:0]	DSI-PHY	4	DSI data lane - positive	1.2 V
	DSIDM[3:0]	DSI-PHY	4	DSI data lane - negative	1.2 V
	VDD_MIPI	Power	2	MIPI Analog Power Supply	1.2 V
	VSS_MIPI	Ground	2	MIPI Analog Ground	GND
First-Link LVDS TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	1.8 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	1.8 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	1.8 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	1.8 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	1.8 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	1.8 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	1.8 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	1.8 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	1.8 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E – negative	1.8 V
	VDD_LVDS1_18	Power	2	First-link LVDS 1.8V Power Supply	1.8 V
	VSS_LVDS1_18	Ground	2	First-link LVDS 1.8V Ground	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2V Power Supply	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2V Ground	GND
2nd-Link LVDS TX IF	LVTX2AP	LVDS-PHY	1	LVDS second-link data channel A - positive	1.8 V
	LVTX2AN	LVDS-PHY	1	LVDS second-link data channel A - negative	1.8 V
	LVTX2BP	LVDS-PHY	1	LVDS second-link data channel B - positive	1.8 V
	LVTX2BN	LVDS-PHY	1	LVDS second-link data channel B - negative	1.8 V
	LVTX2CP	LVDS-PHY	1	LVDS second-link data channel C - positive	1.8 V
	LVTX2CN	LVDS-PHY	1	LVDS second-link data channel C - negative	1.8 V
	LVTX2DP	LVDS-PHY	1	LVDS second-link data channel D (Clock) - positive	1.8 V
	LVTX2DN	LVDS-PHY	1	LVDS second-link data channel D (Clock) -negative	1.8 V
	LVTX2EP	LVDS-PHY	1	LVDS second-link data channel E - positive	1.8 V
	LVTX2EN	LVDS-PHY	1	LVDS second-link data channel E – negative	1.8 V
	VDD_LVDS2_18	Power	2	Second-link LVDS 1.8V Power Supply	1.8 V
	VSS_LVDS2_18	Ground	2	Second-link LVDS 1.8V Ground	GND
	VDD_LVDS2_12	Power	1	Second-link LVDS 1.2V Power Supply	1.2 V
	VSS_LVDS2_12	Ground	1	Second-link LVDS 1.2V Ground	GND
I2C IF	I2C_SCL	S-OD	1	I2C Master or Slave interface clock signal	1.8V-3.3V
	I2C_SDA	S-OD	1	I2C Master or Slave interface data signal	1.8V-3.3V
GPIO	GPIO[3:0]	N_{PD}	4	GPIO bits 3-0	1.8V-3.3V
SYSTEM	RESX	N	1	Hardware reset, low active	1.8V-3.3V

	EXTCLK	N	1	External pixel clock source	1.8V-3.3V
	STBY	N	1	Standby pin, low active	1.8V-3.3V
	TM	N_{PD}	1	Test mode select	1.8V-3.3V
	VDDIO	Power	2	IO Power Supply	1.8-3.3V
	VSSIO	Ground	2	IO Ground	GND
	VDDC	Power	2	Digital Core Power Supply	1.2 V
	VSSC	Ground	2	Digital Core Ground	GND

Buffer Type Abbreviation:

N: Normal IO
N_{PD}: Normal IO with weak Internal Pull-Down
N_{PU}: Normal IO with weak Internal Pull-Up
S-OD: Pseudo open-drain output, schmidtt input
SCHMIDTT: Fail Safe schmidtt input buffer
DSI-PHY: front-end analog IO for DSI
LVDS-PHY: front-end analog IO for LVDS
A: Analog pad

4.2 TC358775 BGA64 Pin Count Summary

Table 4-1 BGA64 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
DSI-RX IF	14	Include DSI Power & Ground
LVDS-TX IF	32	Include LVDS Power & Ground
I2C	2	
GPIOx	4	
POWER	4	System Power
GROUND	4	System Ground
Total Pin Count	64	

4.3 BGA49 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	Power Supply Voltage
DSI RX IF	DSICP	DSI-PHY	1	DSI clock signal - positive	DSICP
	DSICM	DSI-PHY	1	DSI clock signal - negative	DSICM
	DSIDP[3:0]	DSI-PHY	4	DSI data lane - positive	DSIDP[3:0]
	DSIDM[3:0]	DSI-PHY	4	DSI data lane - negative	DSIDM[3:0]
	VDD_MIPI	Power	2	MIPI Analog Power Supply	1.2 V
	VSS_MIPI	Ground	2	MIPI Analog Ground	GND
First-Link LVDS TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	1.8 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	1.8 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	1.8 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	1.8 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	1.8 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	1.8 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	1.8 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	1.8 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	1.8 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E – negative	1.8 V
	VDD_LVDS1_18	Power	2	First-link LVDS 1.8V Power Supply	1.8 V
	VSS_LVDS1_18	Ground	2	First-link LVDS 1.8V Ground	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2V Power Supply	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2V Ground	GND
I2C IF	I2C_SCL	S-OD	1	I2C Master or Slave interface clock signal	1.8V-3.3V
	I2C_SDA	S-OD	1	I2C Master or Slave interface data signal	1.8V-3.3V
GPIO	GPIO[3:0]	N_{PD}	4	GPIO bits 3-0	1.8V-3.3V
SYSTEM	RESX	N	1	Hardware reset, low active	1.8V-3.3V
	EXTCLK	N	1	External pixel clock source	1.8V-3.3V
	STBY	N	1	Standby pin, low active	1.8V-3.3V
	TM	N_{PD}	1	Test mode select	1.8V-3.3V
	VDDIO	Power	2	IO Power Supply	1.8-3.3V
	VSSIO	Ground	2	IO Ground	GND
	VDDC	Power	2	Digital Core Power Supply	1.2 V
	VSSC	Ground	3	Digital Core Ground	GND

Buffer Type Abbreviation:

N: Normal IO
S-OD: Pseudo open-drain output, schmidtt input
SCHMIDTT: Fail Safe schmidtt input buffer
DSI-PHY: front-end analog IO for DSI
LVDS-PHY: front-end analog IO for LVDS
A: Analog pad

4.4 TC358774 BGA49 Pin Count Summary

Table 4-2 BGA49 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
DSI-RX IF	14	Include DSI Power & Ground
LVDS-TX IF	16	Include LVDS Power & Ground
I2C	2	
GPIOx	4	
POWER	4	System Power
GROUND	5	System Ground
Total Pin Count	49	

5 Operations

The system operation of the 775XBG Bridge Chip is overviewed from the user application point of view in this section.

Following diagram illustrates the functional blocks of the chip and the major data paths interconnecting them.

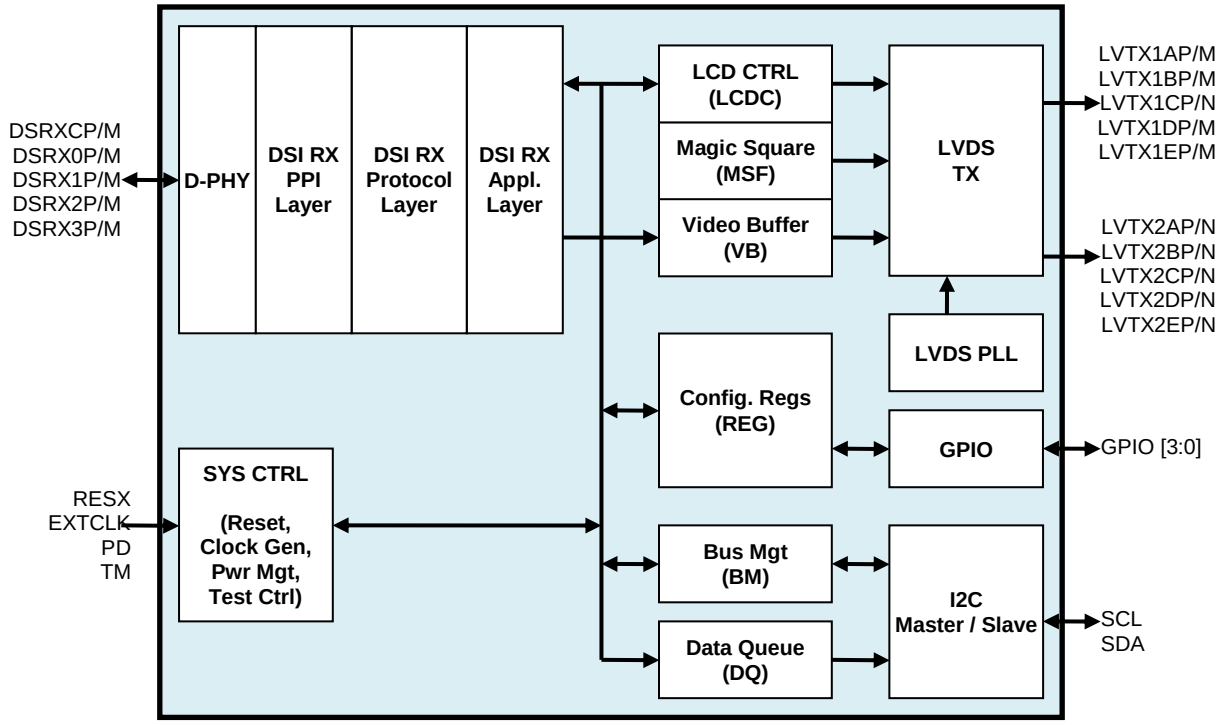

Figure 5-1 TC358775XBG Bridge Chip Functional Block Diagram

System operation of the chip consists of the following major segments and will be described in that order:

- Power on
- Reset
- Hardware mode selection
- Initial chip configuration
- DSI-RX operation
- Write and read access to the chip configuration and status registers
- Streaming video to LVDS FPD display panels
- Control of the I2C Master Interface port
- Enter and exit chip Sleep state

- Enter and exit chip StandBy state
- DSI packet support
- Reverse low-power transmission
- LVDS-TX operation
- Power management

In this section, description will be limited to system application which is more useful for the system users. These operation segments are implemented by a collection of major functional blocks in the chip as depicted in the functional block diagram above.

5.1 Power On

The 775XBG Bridge Chip is powered by three supply voltages, 1.2V, 1.8-3.3V and 1.8V, required by different blocks of the chip. If the digital I/Os is powered by 1.8V supply voltage, the number of supply voltages can be reduced to two, 1.2V and 1.8V. Please keep all the input signals at either "Hi-z" or "logic low" state before powering on 775XBG.

The power on/off sequence and input STBY and RESX signals are discussed in section 8.4.5.

After power is applied, the chip input pins should be driven to some deterministic states. Input or bi-directional pins with standard CMOS buffer types should be driven (or weakly pulled) high or low. DSI-RX PHY pins should be driven to LP-11 (stop) state.

5.2 Reset

775XBG chip has external hardware reset which distributed to the sub modules inside the 775XBG chip.

Individual software reset control is also supported for the main functions in the chip. These reset control bits are defined in the SYSRST register.

5.3 DSI-RX Interface Operation

Following reset de-assertion, the chip is ready to receive low-power (LP) mode communication transactions from Host over the DSI link over data lane 0.

Initial transactions are typically those that write to the chip configuration registers to configure the chip and to activate various functions of the chip.

Accessing the chip configuration registers can be performed in low-power (LP) mode over only data lane 0, or in high-speed (HS) mode over one or more data lanes.

Initially, since only data lane 0 is enabled for LP mode reception, DSI-RX configuration registers must be written in LP mode. Then, after DSI-RX is configured and enabled for high-speed reception, subsequent transactions can be in either LP or HS mode.

The DSI-RX interface is capable of supporting LP mode transactions at data bit rate up to 10 Mbps (lane 0 only) for receive and transmit, and HS mode transactions over one and up to four data lanes, at data bit rate up to 1 Gbps per data lane.

The DSI-RX Interface is used for four purposes:

Write and read access to the chip configuration and status registers

Streaming video to LVDS FPD display panels

Control of the I2C Master Interface port

Enter and exit chip ultra-low power state (ULPS) or Sleep state

5.3.1 Write and Read Access to Chip Configuration Registers

The 775XBG Bridge Chip makes use of DSI Generic Long packets for Host to write and read to its register set. Format of these packets is defined in the DSI specification. The payload of these packets is further defined here and is specific to the 775XBG Bridge Chip.

5.3.1.1 Write Access

Host sends a DSI Generic Long Write packet (Data ID = 0x29) over the DSI link for each write access transaction to the chip configuration registers. Payload of this packet is further defined as follows:

First two bytes of the payload specifies the chip register 16-bit address, hence the address field. The first byte corresponds to address bits [7:0]. The following byte corresponds to address bits [15:8].

Next four bytes specifies the 32-bit data to be written to the address specified in the address field. The first of the four bytes corresponds to data bits [7:0]; next byte corresponds to data bits [15:8]; …; last byte corresponds to data bits [31:24].

"Address auto-increment" capability is supported. That means Host can write to contiguous register address locations with one single packet. The address field specifies the address of the first register to be written to. Each group of following 4 bytes in the payload constitutes the 32-bit data to be written to each of the registers in the group starting with that addressed by the address field.

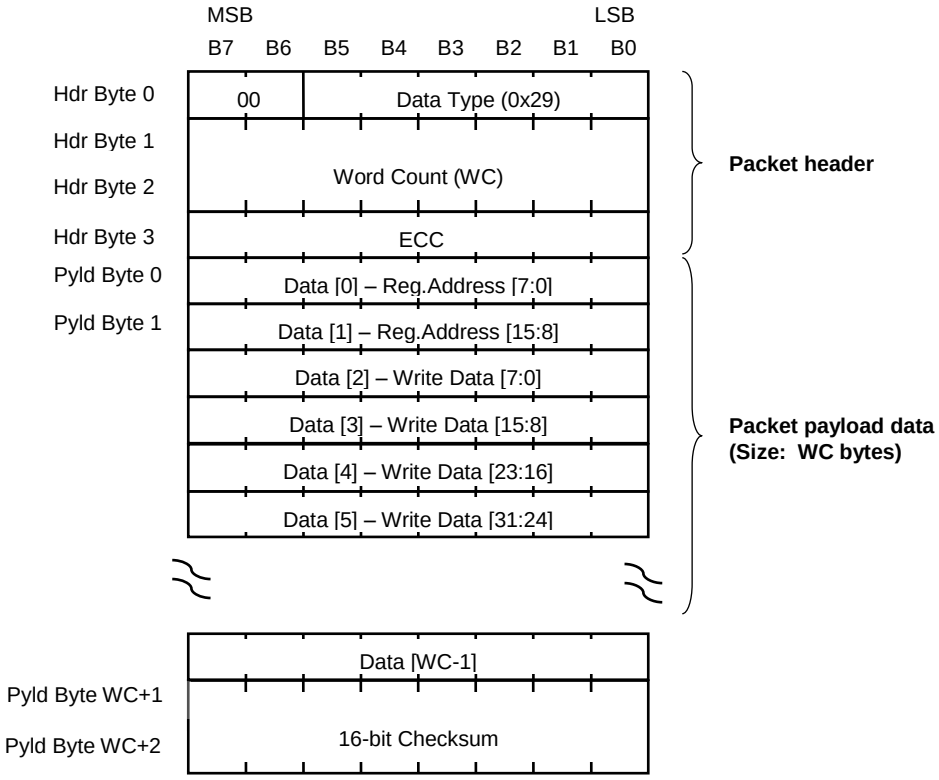

Figure 5-2 DSI Long Generic Write Packet

5.3.1.2 Read Access

Host sends a DSI Generic Read packet (Data ID = 0x24) over the DSI link for each read request transaction to the chip configuration registers. Payload of this packet is further defined as follows:

The two data bytes of the packet specify the chip register 16-bit address, hence the address field. Data byte 0 corresponds to address bits [7:0]. Data byte 1 corresponds to address bits [15:8].

Immediately after sending this packet, Host performs a Bus-Turn-Around (BTA) sequence to transfer the DSI link ownership to the 775XBG Bridge Chip for it to send a read response packet. (If a BTA does not immediately follow the read request packet, then the read transaction will be abandoned and no read response will be returned.)

The chip detects the BTA sequence and takes one of the following actions:

If the read request packet arrived with no errors (and there are no previously stored errors since the last reverse communication with Host), the chip forms and sends a Generic Long Read Response packet (Data ID = 0x1A) which returns the 4-byte content of the register being addressed (one register access per read)

If errors are detected during reception of the read request packet (or there are no previously stored errors since the last reverse communication with Host), the chip sends Host an “Acknowledge and Error Report” packet (Data ID = 0x02). Please refer to MIPI DSI Spec. version 1.01 for the details of the error packet.

If an ECC correctible error in the request was detected and corrected, the chip forms and sends the Generic Long Read Response packet (same as in case 1) followed by the “Acknowledge and Error Report” packet.

After sending the response, the chip performs its own BTA sequence to give the DSI link ownership back to the Host.

The Generic Short Read Request packet structure is shown in the following figure.

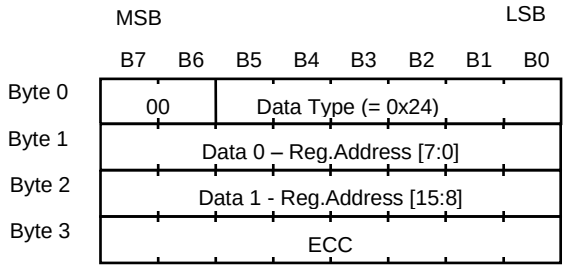

Figure 5-3 DSI Generic Short Read Request Packet

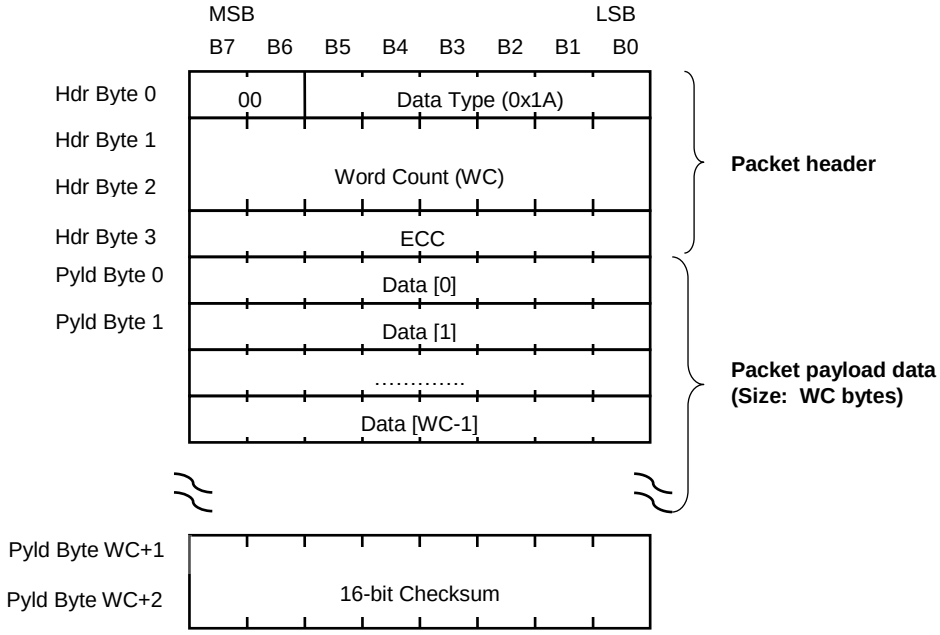

Figure 5-4 DSI Generic Long Read Response packet

5.3.2 Streaming Video

Video stream from Host over the DSI link will be described in the following context:

1. DSI packets for video transmission
2. Mode of transmission, video mode only
3. Picture resolution and timing parameters
4. Pixel format

5. Video data buffering
6. DSI clock and display pixel clock

5.3.2.1 DSI Packets for Video Transmission

DSI packets pertaining to video transmission are listed in the following table:

Table 5-1 DSI Packets Pertaining to Video Transmission

Data Type	Short/Long Packet	Description	Supported
6'h01	Short	Vsync start	Yes
6'h11	Short	Vsync end	Yes
6'h21	Short	Hsync start	Yes
6'h31	Short	Hsync end	Yes
6'h09	Long	Null packet	Yes
6'h19	Long	Blanking Packet	Yes
6'h0E	Long	Pixel Stream, 16-bit RGB-565 format	Yes
6'h1E	Long	Pixel Stream, 18-bit RGB-666 Packed format	Yes
6'h2E	Long	Pixel Stream, 18-bit RGB-666 Loosely Packed format	Yes
6'h3E	Long	Pixel Stream, 24-bit RGB-888 format	Yes

5.3.2.2 Mode of Transmission

The 775XBG Bridge Chip supports only one mode of video transmission: Video mode.

In Video mode, Host is expected to transmit all video timing events and pixel data in proper sequence and time. Video timing events are transmitted in these DSI short packets: VSYNC Start (VSS), VSYNC End, HSYNC Start (HSS), and HSYNC End. They must be multiplexed with null (or blank) packets (or transitioned to LP idle cycle) and pixel data packets in the DSI serial link such that their reception at the chip will reflect in signal transition on VSYNC and HSYNC at proper timing for the receiving display panel.

Pixel data is expected to be transmitted using Pixel Stream packet types (Data Type ID = 0x0E, 0x1E, 0x2E or 0x3E.). Pixel data can be transmitted in non-burst or burst fashion. Non-burst refers to pixel data packet transmission time on DSI link being roughly the same (to account for packet overhead time) as active video line time on LVDS output (i.e. DE = 1). And burst refers to pixel data packet transmission time on DSI link being less than the active video line time on LVDS output.

Video mode transmission is further differentiated by the types of timing events being transmitted. Video pulse mode refers to the case where both sync start and sync end events (for frame and line) are transmitted. Video event mode refers to the case where only sync start events are transmitted.

The 775XBG chip operates as event mode only. It ignores VSYNC End and HSYNC End packets. Host is expected to program Hsync and Vsync width in registers HTIM1[HPW] and VTIM1[VPW], respectively.

5.3.2.3 Video Picture Resolution and Timing Parameters

The maximum display resolution is limited by the data bandwidth available on the LVDS link in single LVDS link case. While it is limited by the data bandwidth available on the DSI link in dual LVDS link case.

Host is expected to program LVDS timing registers HTIM1/2 and VTIM1/2 before sending video data packets. Host is responsible to control frame/line time with VSS/HSS packets. It is also required to feed video data packets to 775XBG chip in time to prevent data underflow.

775XBG chip follows timing parameters set in registers HTIM1/2 and VTIM1/2 to output LVDS stream with panel timing requirement. 775XBG synchronizes its output timing with Host either at frame boundary (VSS) or line boundary (HSS) as programed in register bit VPCTRL[FrameSync]. Please refer to section 5.5.1 for more information.

5.3.2.4 Pixel Format

The chip supports RGB-565, RGB-666 packed or loose, and RGB-888 pixel formats in video data packets received from Host.

In video mode transmission, pixel format is differentiated by the data type ID in the header of pixel stream packets received.

5.3.2.5 Video Data Buffering

A Video Line Buffer is provided to buffer the incoming video data due to the speed mismatch between DSI and LVDS links. To a lesser degree, it is also required to absorb the latency caused by de-serialization and pipelining along the data path.

During DSI link speed is slower than that of LVDS link's, data needs to be buffer within 775XBG before outputting to prevent data from underflow. Register field VPCTRL[VSDELAY] is used to for this purpose.

Pixel data received over the DSI link are always stored in the video line buffer as 24 bits per pixel. Each color component of incoming RGB-565 or packed RGB-666 pixel data is stored as left justified byte.

5.3.2.6 Clock Structure

The 775XBG chip has two clocks source, DSICLK and EXTCLK. The latter is optional.

DSICLK, or DSI clock, refers to the DSI bit clock used in HS mode transmission of video packets over the DSI link. All video related packets must be transmitted in high-speed mode to ensure the relationships discussed below.

Either EXTCLK or DSICLK can be used for display pixel clock source, or PCLK. In the case of LVDS Single-Link, PCLK refers to the clock used to transfer one pixel per PCLK period out to the display panel interface and its frequency matches the picture resolution and refresh-timing parameters of the display panel being driven. It is sourced from EXTCLK input pin. For LVDS Dual-Link, two pixels are transmitted to LVDS per PCLK period.

After reset, If EXTCLK toggles then EXTCLK is selected as pixel clock source, else DSICLK is selected (LVCFG register describes the DSICLK divide options).

Pixel clock source implies continuous clocking. That means clock pulses must be continuously present during normal operation.

DSI bit clock must be present when Host issues I2C transactions to the chip even if EXTCLK is present.

Following diagram illustrates the clock source to the internal functional blocks of the chip.

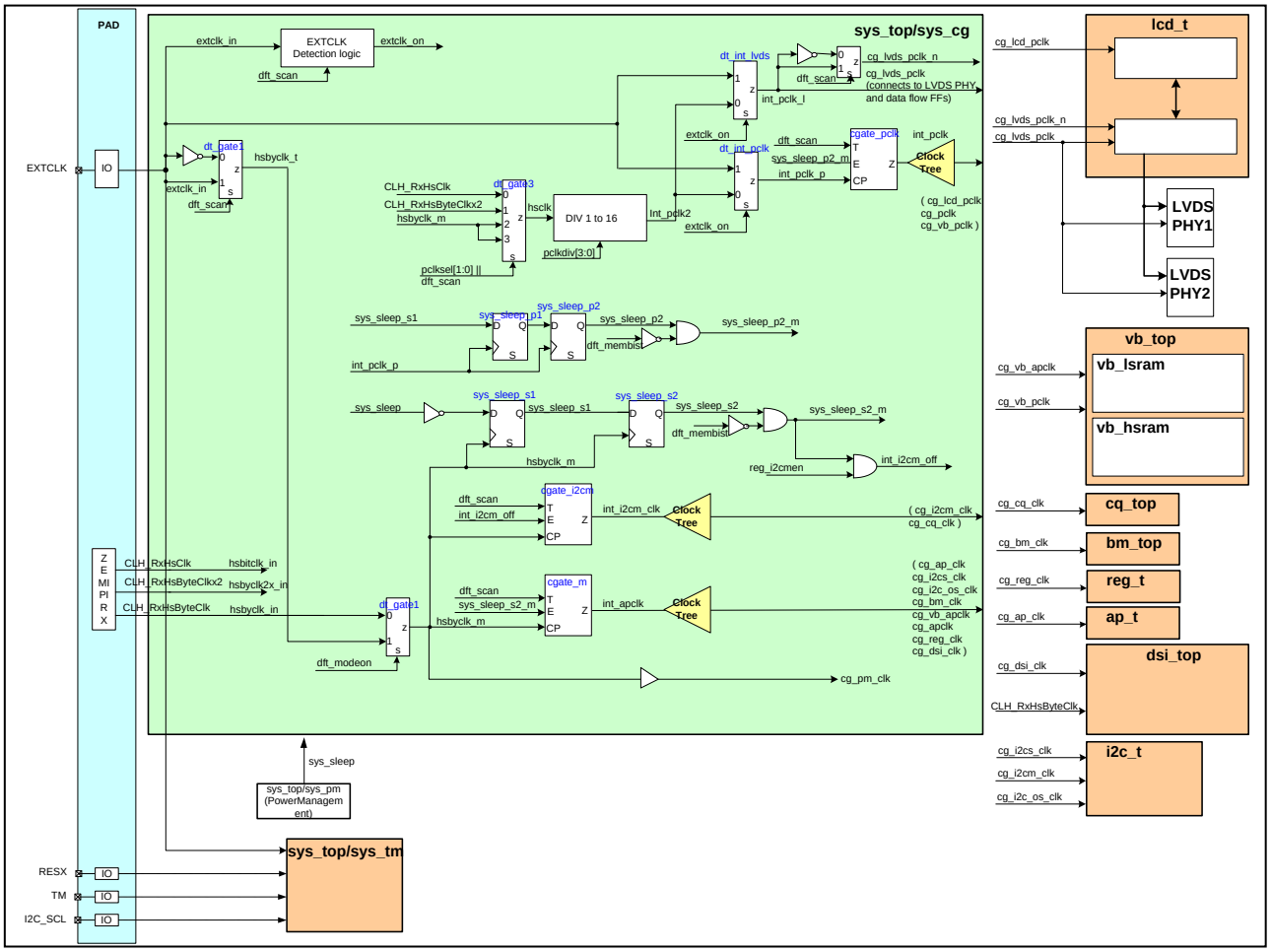

Figure 5-5 Clock Mode Selection and Clock Sources

Thus, the 775XBG chip receives video data over the DSI link which is synchronous to DSICLK, and it in turn re-transmits video out to LVDS link which is synchronous to PCLK. In between, the input video data is temporarily held in a 1024-pixel FIFO buffer.

5.3.3 Enter and Exit Chip Sleep Mode

When the display is turned off and the video path from Host to the display panel through 775XBG Bridge Chip is not active, Host sends a ULPS Entry command to instruct the chip to transition into Sleep state. Upon receiving this command, the chip powers down all of its functions except for the DSI low-power receive function which is used to listen to a ULPS Exit command. Subsequently, upon receiving the ULPS Exit command, the chip will exit the ULPS state and transition to standby state.

No (re-)initialization of 775XBG chip is necessary when exiting Sleep state. 775XBG is ready to transfer data when its PLL/Multiplier is stable.

5.3.4 Enter and Exit Chip Standby State

Host asserts/de-asserts STBY pin to instruct 775XBG goes into/out of StandBy state.

1. Before assertion of STBY pin, Host DSI link is recommended to go to LP00/ULPS mode.
   a. Host can disable its DSI Tx to float DSI link after asserting STBY.
2. After de-assertion of STBY pin, Host DSI link should go to LP11 mode
   a. It is necessary to re-initialize 775XBG before it can function probably, toggling RESX is recommended.
   b. RESX toggling needs to be performed while DSI Link, both data and clock lanes are in LP11 mode.

5.3.5 Control of the I2C Master Interface Port

Host can issue commands to the I2C Master Interface Port of the 775XBG Bridge Chip by transmitting DSI Generic Long Write packets writing to appropriate registers of the 775XBG chip. I2C Master Write commands and Read commands are discussed in the sections below.

5.3.5.1 I2C Master Write

The I2C master in 775XBG requires software to setup the following register fields before initiating an I2C write transfer on the I2C bus:

I2CMADDR.I2CSB

I2CMADDR.I2CASEL

I2CMADDR.I2CADD

Software will then write to the WDATAQ register with the data to be transferred on to the I2C bus; this is done via DSI Generic Long Write packets. Each read transaction must be encapsulated in one DSI packet. 775XBG will ensure that the DSI packet is received with no CRC errors before forwarding the request to the I2C master; otherwise, no action takes place. Depending on the register setting of registers I2CMADDR, the I2C master will create an internal I2C message before sending WDATAQ data on the I2C bus. Note that LSB data within WDATAQ entry is sent out first.

Table 5-2 I2C controller write message formatting

Register Field		Internal I2C Message						
I2CSB	I2CASEL	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	…	Byte n
0	0	S + I2CADD[6:0] + 1'b0	WDATAQ byte 0	WDATAQ byte1	WDATAQ byte 2	WDATAQ byte 3	…	WDATAQ byte n + P
0	1	S + 6'b11110 + I2CADD[9:8] + 1'b0	I2CADDR[7:0]	WDATAQ byte 0	WDATAQ byte1	WDATAQ byte 2		WDATAQ byte n + P
1	0	S + 8'h01	Sr + I2CADD [6:0] + 1'b0	WDATAQ byte 0	WDATAQ byte1	WDATAQ byte 2	…	WDATAQ byte n + P
1	1	S + 8'h01	Sr + 6'b11110 + I2CADD[9:8] + 1'b0	I2CADD [7:0]	WDATAQ byte 0	WDATAQ byte1	…	WDATAQ byte n + P

Where S is an I2C Start condition, Sr is an I2C repeated start condition and P is an I2C Stop condition.

The I2C master controller ignores I2C slave NACK (not acknowledge) and continues transmitting the internal I2C message as defined in Table 5-2 until the STOP condition is asserted on the I2C bus. 775XBG I2C Master regards an I2C slave NACK as an error and sets an I2CERR bit and the byte number of the internal I2C message where the first NACK was received. The following diagram illustrates the control flow of the I2C Master in 775XBG.

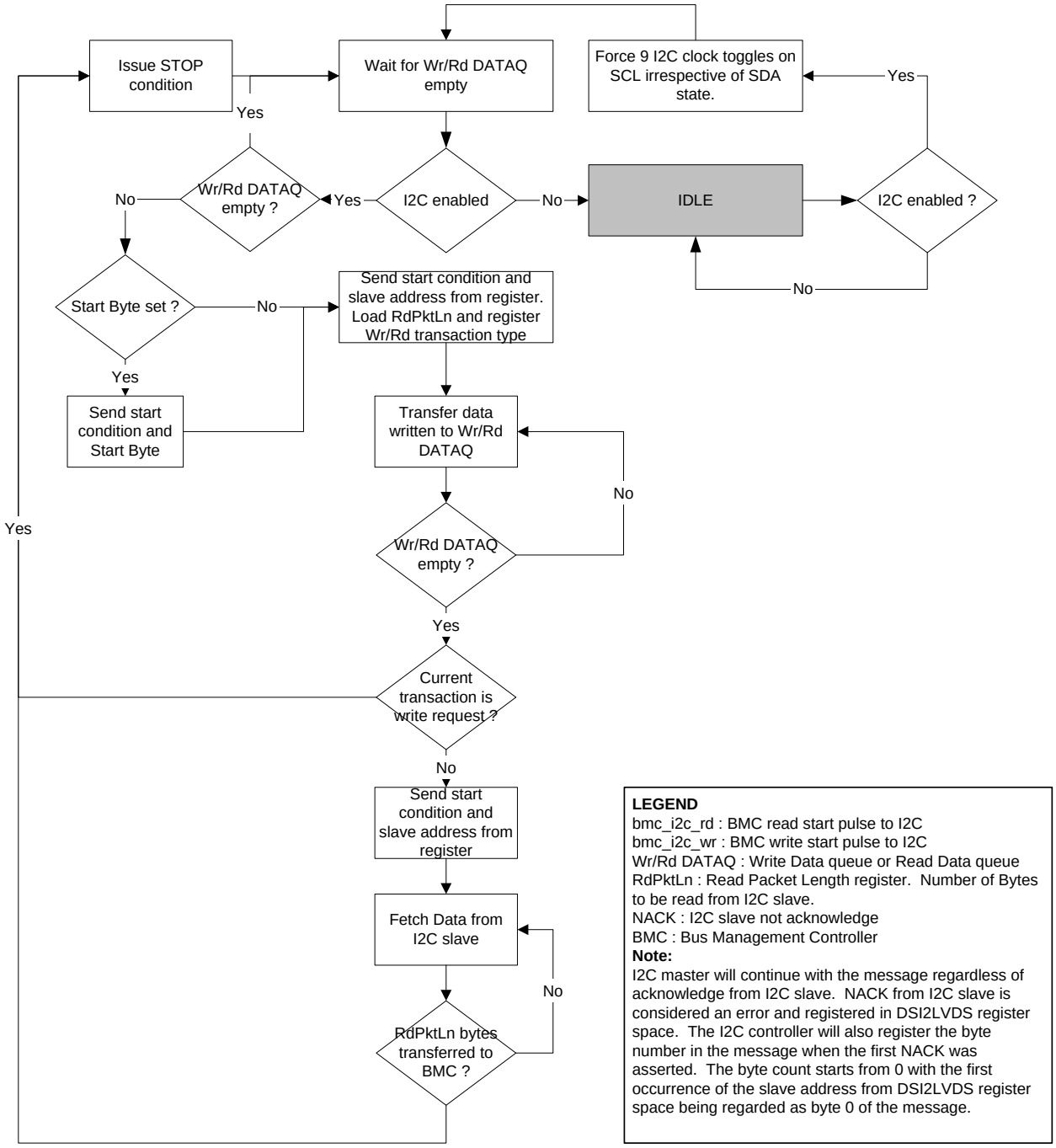

Figure 5-6 I2C master control flow diagram

5.3.5.2 I2C Master Read

The I2C master in 775XBG requires software to setup the following register fields before initiating an I2C read transfer on the I2C bus:

I2CMADDR. I2CSB

I2CMADDR. I2CASEL

I2CMADDR. I2CADD

RDPKTLN.RDPKTLN

Software will then write to the RDATAQ register with the data to be transferred on to the I2C bus as part of the I2C Read transfer; this is done via DSI Generic Long Write packets. Between one to four bytes can be written to RDATAQ. Each read transaction must be encapsulated in one DSI packet. 775XBG will ensure that the DSI packet is received with no CRC errors before forwarding the request to the I2C master; otherwise, no action takes place. Depending on the values of register I2CMADDR, the I2C Master will create an internal I2C message (Table 5-3) before sending RDATAQ data on the I2C bus. When all data in RDATAQ have been sent, the I2C master will issue I2C read cycles for the number of bytes defined in RDPKTLN register. All except the last byte of data returned by the slave will be acknowledged by the I2C master. The last byte as defined in the RDPKTLN register will not be acknowledged and is followed by a stop condition. See Figure 5-6 for more details on I2C master control flow. Note that LSB data within RDATAQ entry is sent out first.

Table 5-3 I2C controller internal I2C read message format

Register Field		Internal I2C message								
I2C SB	I2C ASEL	Byte 0	Byte 1	Byte 2	Byte 3	…	Byte n	Byte n+1	…	Byte n+m
0	**0**	S + I2CADD[6:0] + 1'b0	RDATAQ byte 0	RDATAQ byte1	RDATAQ byte 2	…	RDATAQ byte n	Sr + I2CADD [6:0] + 1'b1	…	I2C Slave data (RDPKTLN) + P
0	**1**	S + 6'b11110 + I2CADD[9:8] + 1'b0	I2CADD[7:0]	RDATAQ byte 0	RDATAQ byte1		RDATAQ byte n	Sr+5'b11110+I2CADD[9:8]+1'b1	…	I2C Slave data (RDPKTLN) + P
1	**0**	S + 8'h01	Sr + I2CADD[6:0] + 1'b0	RDATAQ byte 0	RDATAQ byte1	…	RDATAQ byte n	Sr + I2CADD [6:0] + 1'b1	…	I2C Slave data (RDPKTLN) + P
1	**1**	S + 8'h01	Sr + 6'b11110 + I2CADD[9:8] + 1'b0	I2CADD [7:0]	RDATAQ byte 0	…	RDATAQ byte n	Sr + I2CADD [6:0] + 1'b1	…	I2C Slave data (RDPKTLN) + P

Notation: In the above table:

S is an I2C START condition,

Sr is an I2C repeated START condition and

P is an I2C STOP condition.

m = RDPKTLN + 1

5.3.6 DSI Packet Type Support

Following tables summarize the DSI packet types that the chip supports. Unrecognized or unsupported packet types will be treated as no-ops and error status will be saved and reported.

Table 5-4 Forward-Link DSI Packet Support

Data Type	Short/Long Packet	Description	Supported
6'h01	**Short**	**Vsync start**	**Yes**
6'h11	**Short**	**Vsync end**	**Yes**
6'h21	**Short**	**Hsync start**	**Yes**
6'h31	**Short**	**Hsync end**	**Yes**
6'h08	**Short**	**EoT packet**	**Yes**
6'h02	Short	Color Mode Off Command	No
6'h12	Short	Color Mode On Command	No
6'h22	Short	shut down peripheral	No
6'h32	Short	turn on peripheral	No
6'h03	Short	Generic short write, no parameters	No
6'h13	Short	Generic short write, 1 parameter	No
6'h23	Short	Generic short write, 2 parameters	No
6'h04	Short	Generic Read, no parameters	No
6'h14	Short	Generic Read, 1 parameter	No
6'h24	**Short**	**Generic Read, 2 parameters**	**Yes**
6'h05	Short	DCS write, no parameters	No
6'h15	Short	DCS write, 1 parameter	No
6'h06	Short	DCS read	No
6'h37	**Short**	**Set Maximum Return Packet Size**	**Yes**
6'h09	**Long**	**Null packet, no data**	**Yes**
6'h19	**Long**	**Blanking Packet, no data**	**Yes**
6'h29	**Long**	**Generic Long Write**	**Yes**
6'h0E	**Long**	**Packed Pixel Stream, 16-bit RGB, 565 format**	**Yes**
6'h1E	**Long**	**Packed Pixel Stream, 18-bit RGB, 666 format**	**Yes**
6'h2E	**Long**	**Loosely Packed Pixel Stream, 18-bit 666 RGB format**	**Yes**
6'h3E	**Long**	**Packed Pixel Stream, 24-bit RGB, 888 format**	**Yes**

Table 5-5 Reverse-Link DSI Packet Support

Data Type	Packet Size	Description	Supported
00h – 01 h	Short	Reserved	
02h	**Short**	**Acknowledge and Error Report**	**Yes**
03h – 7h		Reserved	
08h	**Short**	**End of Transmission packet (Eotp)**	**Yes**
09h – 10h		Reserved	
11h	**Short**	**Generic Short Read Response, 1 byte returned**	**Yes**
12h	**Short**	**Generic Short Read Response, 2 bytes returned**	**Yes**
13 – 19h		Reserved	
1Ah	**Long**	**Generic Long Read Response**	**Yes**
1Bh		Reserved	
1Ch	Long	DCS Long Read Response	**No**
1Dh – 20h		Reserved	
21h	Short	DCS Short Read Response, 1 byte returned	**No**
22h	Short	DCS Short Read Response, 2 bytes returned	**No**
23h – 3Fh		**Reserved**	

Note: EoT Packet: No action is required at Application Layer.

5.3.7 Reverse Low Power Transmission

The chip supports reverse Low Power transmission as described in the MIPI DSI Specification for the following types of transactions:

Acknowledge. A Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication has been received with no errors.

Acknowledge and Error Report. A Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.

Read Response. May be a Short or Long packet that returns data requested by the preceding read request command from Host.

The control flow of which packets to be returned is shown the following figure.

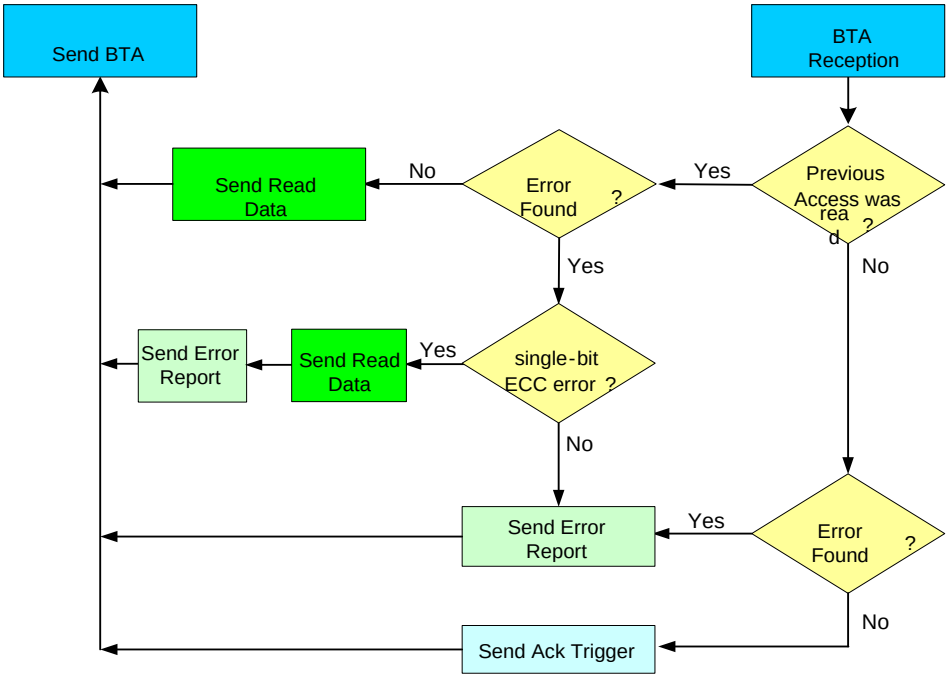

Figure 5-7 Control Flow of Reverse-Link Transactions

5.4 Initial Chip Configuration

As described earlier, following power up resets sequence, the DSI-RX interface is initially enabled for receiving LP mode transactions. Host can completely configure the chip using LP mode transactions. Afterward, Host configures it for 1-, 2-, 3-, or 4-lane HS mode reception for video streaming, depending on data bandwidth required for the display resolution. Alternative, Host can immediately configure the chip for HS mode reception over 1-, 2-, 3-, or 4-lane. Then, any subsequent transactions can be performed in either LP or HS mode. Needless to say, video streaming must be in HS mode to keep up with the required display data rate.

Besides the DSI-RX function, other functions must be configured and enabled (by writing to appropriate configuration registers) before video streaming should start:

Video related function: Pixel processing (Magic Square Algorithm) and timing generation

LVDS-TX function: Transmitter function that drives the LVDS interface with the display panel

5.5 Video Related Operation

5.5.1 Video Timing Generation

In order to transmit video data over LVDS link, three video timing control signals are required, VSYNC, HSYNC, and DE (data enable signal). Host is Not responsible to generate LVDS Panel's timing requirements. It is 775XBG which drives LVDS link according to panel's timing requirement. After programming the timing requirement to 775XBG, Host is recommended to burst data into 775XBG within the panel's desired line width time.

775XBG chip incorporates a Video Timing Gen (VTGEN) module that can generate these timing signals according to the video parameters programmed in the video timing registers VTIM1, VTIM2, HTIM1, HTIM2 and VPCTRL.

- In FrameSync mode: VTGEN honors all the timing register values, it synchronized with Host only at each frame boundary, i.e. each Vsync Start (VSS) packet.
- In LineSync mode: VTGEN ignores value in register field HTIM2[HFPR]. In this mode 775XBG synchronized with Host at each line, i.e. each Hsync Start (HSS) and VSS packet.

DSI packet input and LVDS link output timing parameter/diagram is shown graphically in Figure 5-8 above.

- In FrameSync Mode, VTGEN synchronizes with Host only at VSS. New line starts when VTGEN finishes counting HFPR (Δ is kept at zero). HSS to HPW delayed, VSDelay is maintained when VPW is delayed by VSDelay with respect to VSS.
- In LineSync Mode, VTGEN synchronizes with Host only at each HSS (including VSS). VTGEN starts new lines when detecting HSS arrives and delays by VSDelay cycles. HFPR values vary among each lines with Δ amount, which could be a negative value.

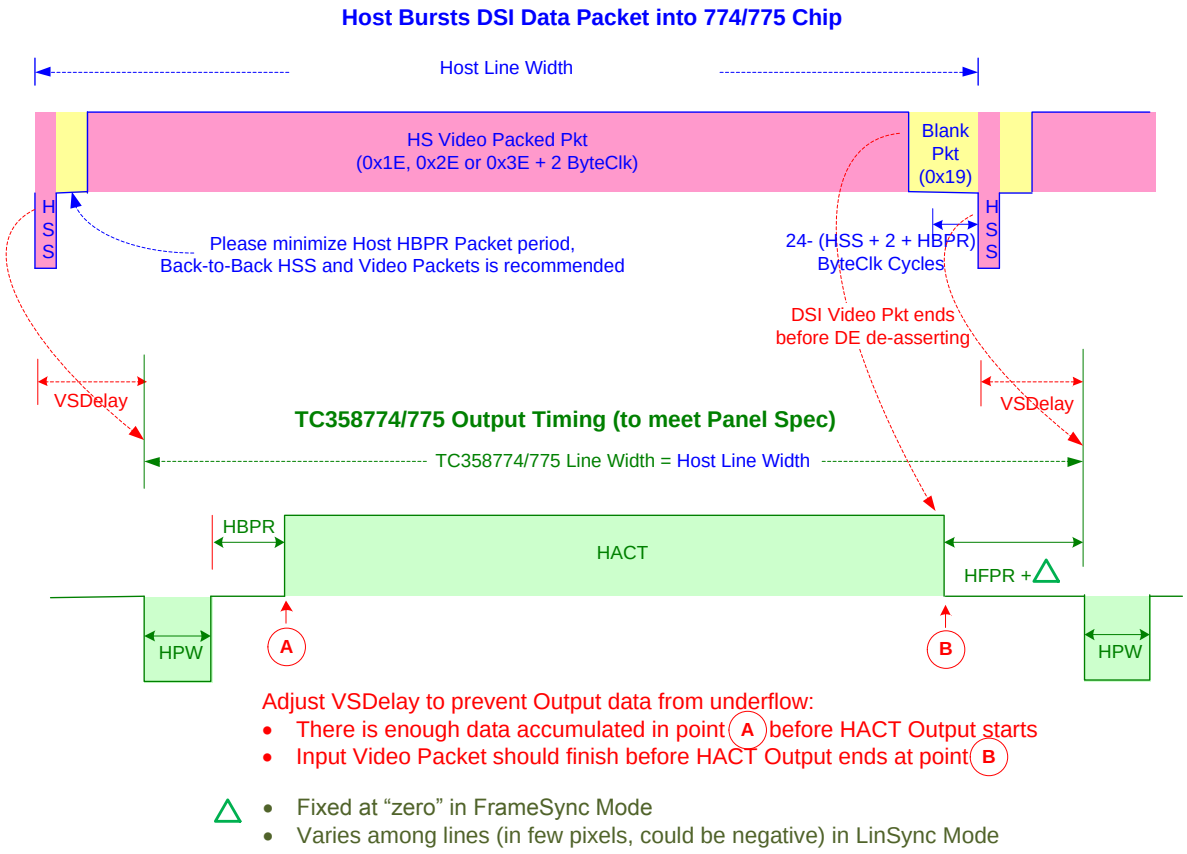

Figure 5-8 Input vs Output Timing Diagram

To help avoid long term time drift (between Host's DSI clock and 775XBG's pixel clock), it is recommended to use LineSync mode. If it is necessary to use FrameSync mode, please:

1. Ground EXTCLK and use divided down DSIClk to drive LVDS' PClk, or
2. Use Host generated clock (same source as DSIClk) to drive EXTCLK, or
3. High precision OSCs (<50 ppm) are required to generate DSIClk and LVDS EXTCLK

5.5.2 Pixel Format Translation

As discussed earlier, the chip can receive video data from Host in one of these formats: 16-bit RGB565, 18-bit RGB666 (Packed), 24-bit RGB666 (Loosely Packed), and 24-bit RGB888.

Pixel data are always stored in the video line buffer as 24-bit. When 16-bit RGB565 or 18-bit RGB666 data are received, each color component will be padded with 0 in its LSB bit positions.

The received video data can be re-transmitted to LVDS link in either 18-bit RGB666 or 24-bit RGB888. The following pixel translation paths are possible:

Table 5-6 Pixel Translation Paths

Received Pixel Format	Re-transmitted Pixel Format
16-bit RGB565	24-bit RGB888 Or 18-bit RGB666
18-bit RGB666 (Packed)	
24-bit RGB666 (Loosely Packed)	
24-bit RGB888	

5.5.3 Magic Square Algorithm

When the display panel's color depth capability is less than that of the input data, say sending RGB888 data to 18-bit display panel, the number of bits of display need to be reduced. With the Toshiba Magic Square algorithm, an RGB666 18-bit LCD panel can produce a display quality equivalent to that of an RGB888 24-bit LCD panel.

For example, when Magic Square algorithm is enabled the red component of the RGB666 output becomes either "R [7:2]" or "R [7:2] + 1". The ratio of these two values depends on the horizontal and vertical position and the display timing. With this changing pixel value, human eye senses the red color component as "R [7:2]", "R [7:2] + 0.25", "R [7:2] + 0.5" and "R [7:2] + 0.75". Therefore, the color depth for the human eye becomes almost those of RGB888 data.

By employing Toshiba's Magic Square algorithm the color graduation is increased significantly compared to 18-bit RGB666 data. The following figure shows 2 conceptual examples of the effect from the Magic Square algorithm.

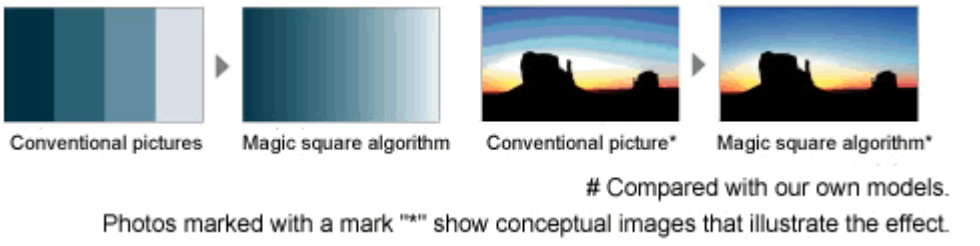

Figure 5-9 Magic Square Algorithm Effect

Thus, Magic Square algorithm may be enabled when the chip drives the LVDS output in RGB666 format.

5.6 LVDS-TX Interface Operation

Video data received over DSI link is re-transmitted to the display panel through LVDS-TX interface port.

The LVDS Transmitter supports both single-link and dual-link operation.

In single-link operation, the LVDS Transmitter converts parallel video data and 3 control data bits into four LVDS serial data channels. The pixel clock, PCLK, is transmitted differentially in parallel with the four LVDS data channels over a fifth LVDS channel. In every pixel clock period, one pixel sample consisting of 24 data bits and 3 control bits is transmitted. Optionally, if RGB666 output format is selected, the fourth serial data channel would be disabled.

In dual-link operation, the LVDS Transmitter converts parallel video data of two pixels and 3 control data bits into eight LVDS serial data channels. The pixel clock, PCLK, is transmitted differentially in parallel with the eight LVDS data channels over two additional LVDS channels. In every pixel clock period, two pixel samples consisting of 2x 24 data bits and 3 control bits are transmitted.

An on-chip PLL synthesizes from PCLK a 7x transmit clock, LVDS_TXCLK, to serialize the data over the LVDS link.

The LVDS interface port configuration is controlled by a set of configuration registers accessible through DSI link. That includes sleep/power-down mode control. Following power-on, the port is defaulted in sleep mode: All of the LVDS outputs are tri-stated.

Video Signal Mapping

LVDS FPD Link is an industry de-facto standard which does not benefit from an industry-wide standardization. At the PHY level, there is strong compatibility between chip vendors due to common adoption of Low-Voltage Differential Signalling data interface standard which is defined in the IEEE 1596.3 standards. However, at the functional signaling level, there is no standard mapping of the order of signals to be serialized over LVDS link. For example, there is no standardized color naming convention between 6-bit and 8-bit color data with regards to LSB and MSB bit ordering.

While there is no standardization, the industry has aligned over the years on certain bit meaningful bit ordering. The following tables detail the industry-aligned bit mapping for all cases that the 775XBG chip supports. They contain a number of bit-mapping information, assuming that each LVDS link takes in a 28-bit bus IN27 to IN0:

The mapping (or connectivity) of pixel data bits to input bits of LVDS Transmitter for the case of LSB bits being mapped to the 4th LVDS channel, JEIDA standard (775XBG is default).

The mapping (or connectivity) of pixel data bits to input bits of LVDS Transmitter for the case of MSB bits being mapped to the 4th LVDS channel Bit, VESA standard. When connecting to VESA standard panels please set the following registers.

LVMX0300 = 0x03020100;
LVMX0704 = 0x08050704;
LVMX1108 = 0x0F0E0A09;
LVMX1512 = 0x100D0C0B;
LVMX1916 = 0x12111716;
LVMX2320 = 0x1B151413;
LVMX2724 = 0x061A1918;

The mapping of bits transmitted on the four channels of an LVDS single-link, and over 8 channels of an LVDS dual-link

The order of bits being transmitted on LVDS link.

Table 5-7 LVDS Single-Link Bit Mapping

LVDS Bit Tx Order	28 bits of LVDS TX Input				JEDEC Pixel Data Bit Mapping LSB on 4th Channel (Ch.D)				VESA Pixel Data Bit Mapping MSB on 4th Channel (Ch.D)			
	LVDS Channel ID				LVDS Channel ID				LVDS Channel ID			
	Ch.A	Ch.B	Ch.C	Ch.D	Ch.A	Ch.B	Ch.C	Ch.D	Ch.A	Ch.B	Ch.C	Ch.D
First	IN7	IN18	IN26	IN23	G2	B3	DE	RSVD	G0	B1	DE	RSVD
	IN6	IN15	IN25	IN17	R7	B2	VSYNC	B1	R5	B0	VSYNC	B7
	IN4	IN14	IN24	IN16	R6	G7	HSYNC	B0	R4	G5	HSYNC	B6
	IN3	IN13	IN22	IN11	R5	G6	B7	G1	R3	G4	B5	G7
	IN2	IN12	IN21	IN10	R4	G5	B6	G0	R2	G3	B4	G6
	IN1	IN9	IN20	IN5	R3	G4	B5	R1	R1	G2	B3	R7
Last	IN0	IN8	IN19	IN27	R2	G3	B4	R0	R0	G1	B2	R6

Note:

- IN27-IN0 are 28 input bits of an LVDS single-link transmitter
- R7-R0, G7-G0, B7-B0 are the three color components of one pixel
- VSYNC, HSYNC, DE are video timing control signals
- RSVD is fixed to logic level 0.

Table 5-8 LVDS Dual-Link Bit Mapping

LVDS Bit Tx Order	52 bits of LVDS TX Input				JEDEC Pixel Data Bit Mapping LSB on 4th Channel (Ch.D)				VESA Pixel Data Bit Mapping MSB on 4th Channel (Ch.D)			
	LVDS First-Link Channel ID				LVDS First-Link Channel ID				LVDS First-Link Channel ID			
	Ch.A	Ch.B	Ch.C	Ch.D	Ch.A	Ch.B	Ch.C	Ch.D	Ch.A	Ch.B	Ch.C	Ch.D
First	IN7	IN18	IN26	IN23	G12	B13	DE	RSVD	G10	B11	DE	RSVD
	IN6	IN15	IN25	IN17	R17	B12	VSYNC	B11	R15	B10	VSYNC	B17
	IN4	IN14	IN24	IN16	R16	G17	HSYNC	B10	R14	G15	HSYNC	B16
	IN3	IN13	IN22	IN11	R15	G16	B17	G11	R13	G14	B15	G17
	IN2	IN12	IN21	IN10	R14	G15	B16	G10	R12	G13	B14	G16
	IN1	IN9	IN20	IN5	R13	G14	B15	R11	R11	G12	B13	R17
Last	IN0	IN8	IN19	IN27	R12	G13	B14	R10	R10	G11	B12	R16
	LVDS Second-Link Channel ID				LVDS Second-Link Channel ID				LVDS Second-Link Channel ID			
	Ch.A	Ch.B	Ch.C	Ch.D	Ch.A	Ch.B	Ch.C	Ch.D	Ch.A	Ch.B	Ch.C	Ch.D
First	IN7	IN18	IN26	IN23	G22	B23	DE	RSVD	G20	B21	DE	RSVD
	IN6	IN15	IN25	IN17	R27	B22	VSYNC	B21	R25	B20	VSYNC	B27
	IN4	IN14	IN24	IN16	R26	G27	HSYNC	B20	R24	G25	HSYNC	B26
	IN3	IN13	IN22	IN11	R25	G26	B27	G21	R23	G24	B25	G27
	IN2	IN12	IN21	IN10	R24	G25	B26	G20	R22	G23	B24	G26
	IN1	IN9	IN20	IN5	R23	G24	B25	R21	R21	G22	B23	R27
Last	IN0	IN8	IN19	IN27	R22	G23	B24	R20	R20	G21	B22	R26

Note:

- IN27-IN0 are 28 input bits of each link of a dual-link LVDS transmitter
- R17-R10, G17-G10, B17-B10 are the three color components of one pixel. R27-R20, G27-G20, B27-B20 are the three color components of the next pixel
- VSYNC, HSYNC, DE are video timing control signals
- RSVD is fixed to logic level 0.

In order to maintain maximum flexibility, the 775XBG Bridge Chip features complete flexibility of how parallel input signals are mapped to the input of the LVDS transmitter. Every bit of the parallel input into an LVDS link can be configured to receive any of the 28 input video pixel and control signals (24-bit pixel data, VSYNC, HSYNC, DE).

When interfacing to an 18-bit RGB666 display panel, the configuration register bit "Output Pixel Format" (VPCTRL.OPXLFMT) should be set to 0, selecting RGB666 format. In such case, only 3 channels of an LVDS link are active; the 4th channel is disabled.

Note that as described in earlier section, incoming pixel data from DSI link are always stored in the video buffer as 24 bits per pixel for all input formats.

The following diagram illustrates the multiplexing logic in front of each of the LVDS link.

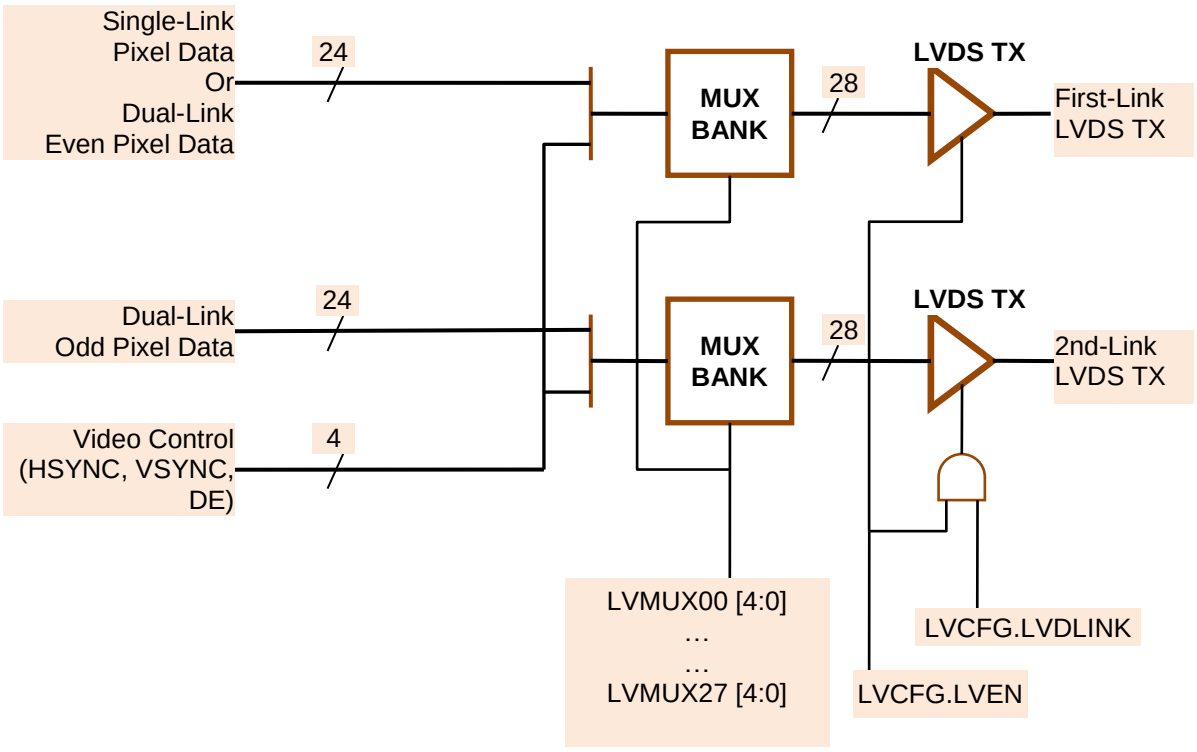

Figure 5-10 LVDS Link Input Multiplexing Logic

In the above diagram, the mux bank consists of 28 28-to-1 muxes where each of the muxes connectivity is shown below. The default reset values for the mux select control LVMUXi [4:0] signals are chosen to reflect the case of pixel data LSBs being mapped to the fourth channel.

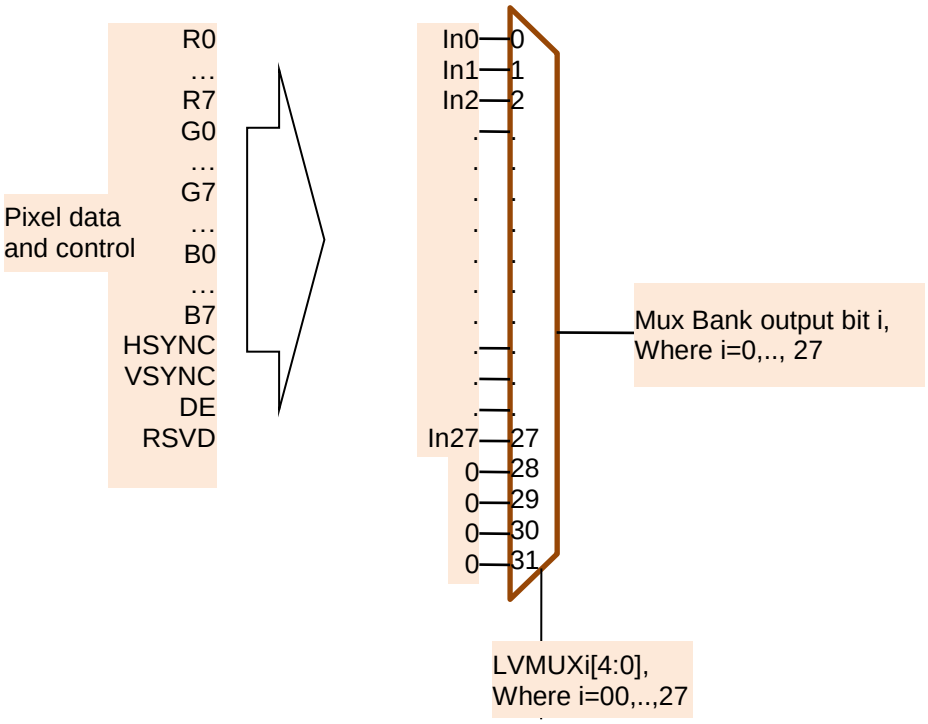

Figure 5-11 Mux 28-to-1 Connectivity

Following figure shows the relationship of parallel input data bits to the LVDS link.

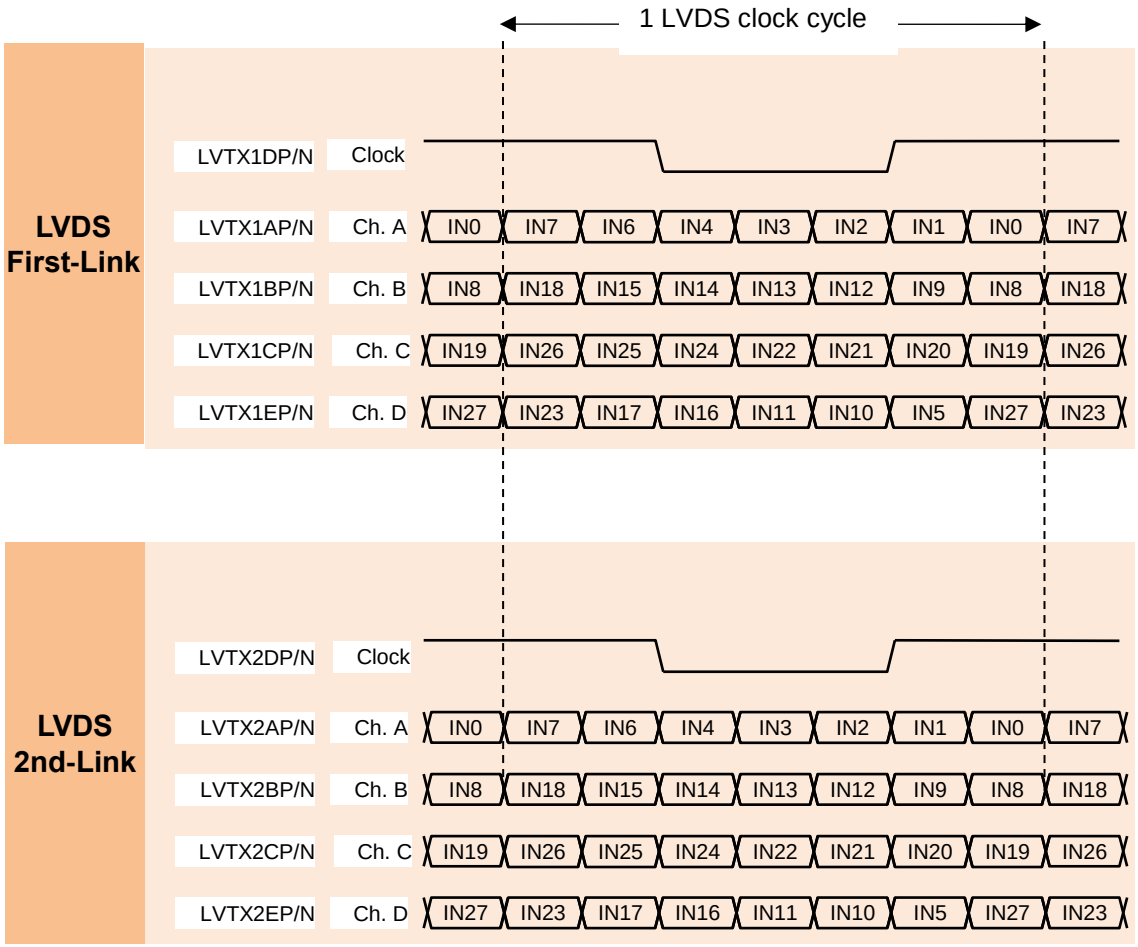

Figure 5-12 Relationship of Parallel Input Data to LVDS Link

5.7 I2C Master Interface Operation

The I2C Master Interface port is controlled by Host as described in the DSI-RX operation above, and incorporates the following features:

Fail safe I2C pad operation

3.3V tolerant I/O buffers

Up to 400 KHz fast mode operation

High speed tolerant; can be plugged into a I2C high speed capable system without disturbing the high speed transmission

Single master operation

Supports slave initiation of clock stretching and wait state generation

Supports 7- and 10-bit slave device address generation

The I2C bus consists of 2 active wires. The active wires, called SDA and SCL, are both bi-directional. SDA is the serial data line, and SCL is the Serial clock line.

All I2C transfers follow the same scheme. First, the I2C master will issue a START condition. This acts as a cue to all of the connected devices. All I2C modules on the bus will listen to the bus for incoming data.

The master next sends the ADDRESS of the device it wants to access, along with an indication whether the access is a Read or Write operation. Having received the address, an I2C slave compares this with its pre-assigned address (for example, the slave device address for 775XBG is “0001_111X”). If there is no match, it simply waits until the bus is released by the stop condition (see below). If the address matches the I2C slave module will produce a response called the ACKNOWLEDGE signal.

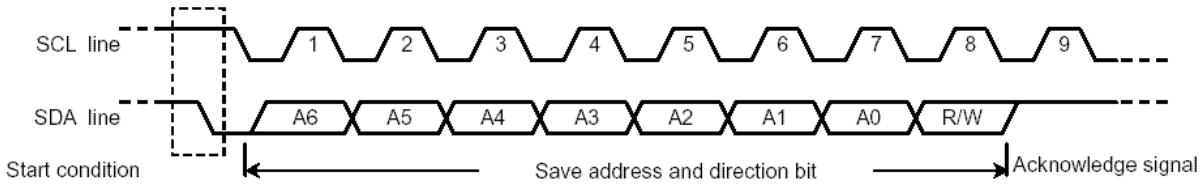

Figure 5-13 Start of an I2C transfer

Once the I2C master receives the ACKNOWLEDGE signal, it can start transmitting or receiving DATA. To transmit data to a device, the master places the first bit onto the SDA line and generates a clock pulse to transmit the bit across the bus to the slave. To receive data from a device, the master releases the SDA line, allowing the slave to take control of it. The master generates a clock pulse on the SCL line for each bit, reading the data while the SCL line is high (the I2C slave is not allowed to change SDA line state while SCL is high). The I2C master will issue the STOP condition once its transmission has finished. This STOP condition is a signal that the bus has been released and that the connected I2C module may expect other transmissions.

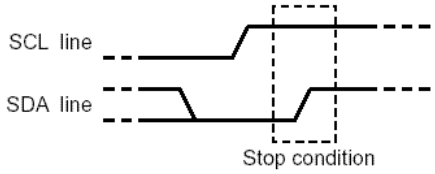

Figure 5-14 I2C stop state

The following figure shows I2C data format for addressing.

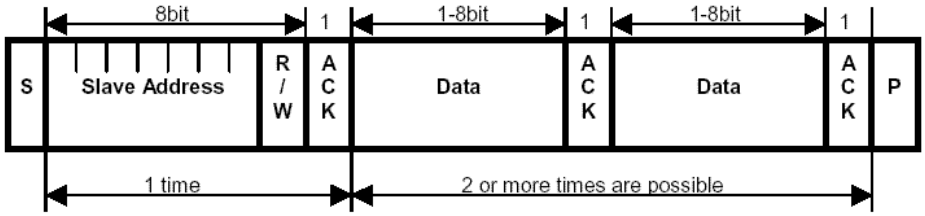

Figure 5-15 I2C data format

The implemented I2C master controller operates on the bus only as a single master. Multi-master mode is not supported.

The I2C Master function is disabled by default to save power. It must be enabled by writing 1 to register bit I2CTIMCTRL.I2CMEN before issueing any transactions to it.

The I2C protocol specification states that the I2C module that initiates a data transfer on the bus is considered the bus master. All the other I2C modules on the same bus are regarded to be bus slaves. Thus, when Host drives the I2C port, it must ensure that bus conflict due to simultaneous transactions by Host I2C Master and 775XBG I2C Master would not arise.

5.8 I2C Slave Interface Operation

The 775XBG Bridge Chip incorporates an I2C Slave Interface port which Host can drive to configure registers in the chip.

The following features are supported:

- Fail safe I2C pad operation
- Up to 400 KHz fast mode operation
- High speed tolerant, can be plugged into a I2C high speed capable system without disturbing the high speed transmission
- 7-bit slave address recognition

The I2C Slave interface port shares the same two pins, SCL and SDA, as that of the I2C Master Interface port.

The I2C slave device address for 775XBG chip is hardcoded to be “0001_111X” (0x0F). Bit[0] defines Write or Read access.

Internally to 775XBG chip, the I2C Slave interface port is sampled by a clock which is derived from the DSI high-speed clock, DSICLK. Thus, before Host issues an I2C Slave transaction to the 775XBG chip, it must first activate the DSICLK and maintain it for the duration of the transaction. At other times, DSICLK may be stopped.

It should be cautioned also that Host must not issue an I2C slave transaction to the chip while another register access from DSI link is taking place; and vice versa.

For I2C Slave write transaction, the order of data in the transaction is illustrated below:

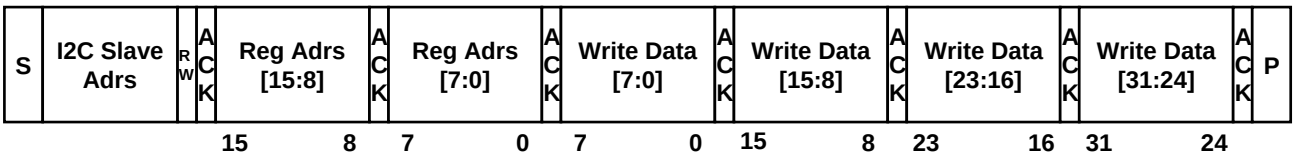

Figure 5-16 I2C Slave Write Transaction

5.9 GPIO

The 775XBG supports 4 GPIO pins that are individually configurable as either input or output.

- Host configured the direction of GPIO pins by writing to register GPC. By default the GPIOs are in input mode.
- As input, the logic state on the GPIO pins are reflected in the register GPI which Host can read.
- When configured as output, the GPIO pins are driven by the state of register GPO which Host can write to.

5.10 Power Management

In general, the chip exhibits the following power states: Power Off, StandBy/STBY, Reset, Init, Normal Sleep/ULPS and Normal state. Transition between the six states, as illustrated in diagram below, is controlled by four mechanisms: Hardware reset (power-on reset and input pin RESX reset), STBY pin, Power suppliers and ULPS trigger messages over the DSI link.

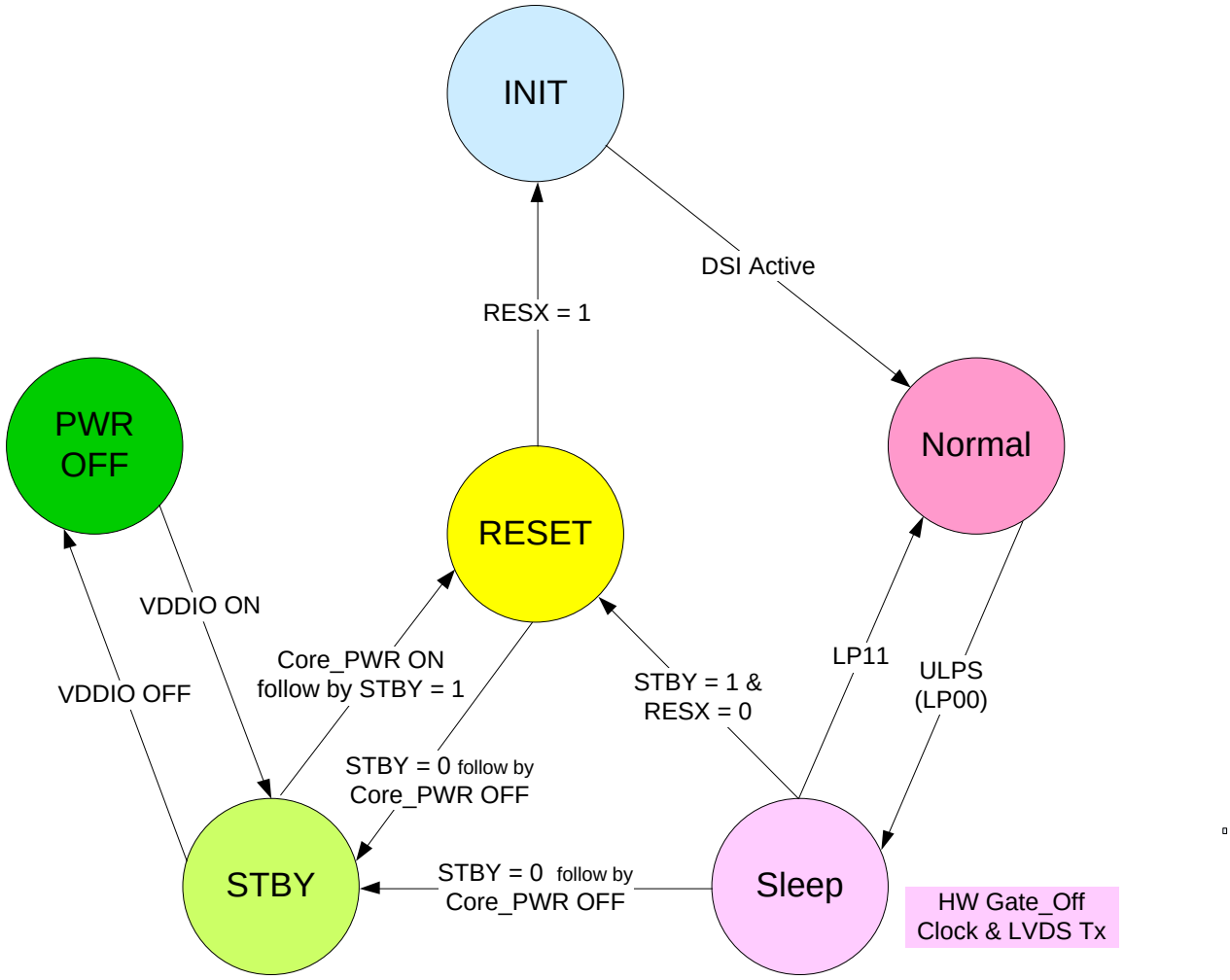

Figure 5-17 Power State Transition Diagram

Following table summarizes the active state of major components in the chip under the four power states.

Table 5-9 Component Power State Summary

Component Name	RESET	StandBy	Sleep/ULPS	NORMAL
DSI LP RX PHY	OFF	OFF	ON	ON
DSI HS RX PHY	OFF	OFF	OFF	ON when enabled (register controlled)
I2C Slave	OFF	OFF	OFF	ON
LVDS TX (PHY: PLL + Serializer + IO buffer)	OFF	OFF	OFF	ON when enabled (register controlled)
I2C Master	OFF	OFF	OFF	ON when enabled (register controlled)
Digital Core Clock PCLK	OFF	OFF	OFF	ON
Register Values	Reset Default	Reset Default	Maintain value. Inaccessible.	Host accessible
FSM State	Reset	Reset	Idle	Active state

6 Registers

6.1 Summary of Register Address

Address	Neumonic	R/W	Default	Register Description
DSI D-PHY Layer Registers				
0x0004	**D0W_DPHYCONTTX**	R/W	0x0000_0002	Data Lane 0 DPHY Tx Control register
0x0020	**CLW_DPHYCONTRX**	R/W	0x0000_A002	Clock Lane DPHY Rx Control register
0x0024	**D0W_DPHYCONTRX**	R/W	0x0000_A002	Data Lane 0 DPHY Rx Control register
0x0028	**D1W_DPHYCONTRX**	R/W	0x0000_A002	Data Lane 1 DPHY Rx Control register
0x002C	**D2W_DPHYCONTRX**	R/W	0x0000_A002	Data Lane 2 DPHY Rx Control register
0x0030	**D3W_DPHYCONTRX**	R/W	0x0000_A002	Data Lane 3 DPHY Rx Control register
0x0038	**COM_DPHYCONTRX**	R/W	0x0000_0000	DPHY Rx Common Control register
0x0040	**CLW_CNTRL**	R/W	0x0000_0000	Clock Lane Control register
0x0044	**D0W_CNTRL**	R/W	0x0000_0000	Data Lane 0 Control register
0x0048	**D1W_CNTRL**	R/W	0x0000_0000	Data Lane 1 Control register
0x004C	**D2W_CNTRL**	R/W	0x0000_0000	Data Lane 2 Control register
0x0050	**D3W_CNTRL**	R/W	0x0000_0000	Data Lane 3 Control register
0x0054	**DFTMODE_CNTRL**	R/W	0x0000_0000	DFT Mode Control register
DSI PPI Layer Registers				
0x0104	**PPI_STARTPPI**	R/W	0x0000_0000	START control bit of PPI-TX function.
0x0108	**PPI_BUSYPPI**	RO	0x0000_0000	After writing 1 to START bit, this bit is set until RESET_N is asserted.
0x0110	**PPI_LINEINITCNT**	R/W	0x0000_208E	Line Initialization Wait Counter
0x0114	**PPI_LPTXTIMECNT**	R/W	0x0000_0001	The counter generates a timing signal for the period of T_{LPX}.
0x0134	**PPI_LANEENABLE**	R/W	0x0000_0003	Enables the operation of each lane at the PPI layer.
0x013C	**PPI_TX_RX_TA**	R/W	0x0008_0008	DSI Bus Turn Around timing parameters
0x0140	**PPI_CLS_ATMR**	R/W	0x0000_0000	Analog timer function enable, Delay for Clock Lane in LPRX
0x0144	**PPI_D0S_ATMR**	R/W	0x0000_0000	Analog timer function enable, Delay for Data Lane 0 in LPRX
0x0148	**PPI_D1S_ATMR**	R/W	0x0000_0000	Analog timer function enable, Delay for Data Lane 1 in LPRX
0x014C	**PPI_D2S_ATMR**	R/W	0x0000_0000	Analog timer function enable, Delay for Data Lane 2 in LPRX
0x0150	**PPI_D3S_ATMR**	R/W	0x0000_0000	Analog timer function enable, Delay for Data Lane 3 in LPRX
0x0164	**PPI_D0S_CLRSIPOCOUNT**	R/W	0x0000_0019	For lane 0, this counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Set the counter value between 85 ns + 6*UI and 145ns + 10*UI.
0x0168	**PPI_D1S_CLRSIPOCOUNT**	R/W	0x0000_0019	For lane 1
0x016C	**PPI_D2S_CLRSIPOCOUNT**	R/W	0x0000_0019	For lane 2
0x0170	**PPI_D3S_CLRSIPOCOUNT**	R/W	0x0000_0019	For lane 3

0x0180	**CLS_PRE**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x0184	**D0S_PRE**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x0188	**D1S_PRE**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x018C	**D2S_PRE**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x0190	**D3S_PRE**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01A0	**CLS_PREP**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01A4	**D0S_PREP**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01A8	**D1S_PREP**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01AC	**D2S_PREP**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01B0	**D3S_PREP**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01C0	**CLS_ZERO**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01C4	**D0S_ZERO**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01C8	**D1S_ZERO**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01CC	**D2S_ZERO**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01D0	**D3S_ZERO**	R/W	0x0000_0000	Digital Counter inside of PHY IO
0x01E0	**PPI_CLRFLG**	R/W	0x0000_0000	PRE Counters has reached set values
0x01E4	**PPI_CLRSIPO**	R/W	0x0000_0155	Clear SIPO values, Slave mode use only. HSRX use only.
0x01F0	**HSTIMEOUT**	R/W	0x0000_0000	HS Rx Time Out Counter
0x01F4	**HSTIMEOUTENABLE**	R/W	0x0000_0000	Enable HS Rx Time Out Counter
DSI Protocol Layer Registers				
0x0210	**DSI_LANEENABLE**	R/W	0x0000_0002	Enables the operation of each lane at the Protocol layer.
0x0214	**DSI_LANESTATUS0**	RO	0x0000_0000	Displays dynamically when a lane is in HS RX mode.
0x0218	**DSI_LANESTATUS1**	RO	--	Displays dynamically if a lane is in ULPS or STOP state
0x0220	**DSI_INTSTATUS**	RO	0x0000_0000	Interrupt Status
0x0224	**DSI_INTMASK**	R/W	0xF07F_AFFF	Interrupt Mask
0x0228	**DSI_INTCLR**	WO	0x0000_0000	Interrupt Clear
0x0230	**DSI_LPTXTO**	R0	0xFFFF_FFFF	Low Power Tx Time Out Counter
DSI General Registers				
0x0300	**DSIERRCNT**	R/W	0xC080_0000	DSI Error Count Register
DSI Application Layer Registers				
0x0400	**APLCTRL**	R/W	0x0000_0000	Application Layer Control Register
0x0404	**RDPKTLN**	R/W	0x0000_0003	Command/Register Read Packet Length Register
Video Path Registers				
0x0450	**VPCTRL**	R/W	0x0050_0000	Video Path Control Register
0x0454	**HTIM1**	R/W	0x0004_0008	Horizontal Timing Control Register 1
0x0458	**HTIM2**	R/W	0x0004_00A0	Horizontal Timing Control Register 2
0x045C	**VTIM1**	R/W	0x0008_0010	Vertical Timing Control Register 1
0x0460	**VTIM2**	R/W	0x0008_00F0	Vertical Timing Control Register 2
0x0464	**VFUEN**	R/W	0x0000_0000	Video Frame Timing Update Enable Register
LVDS Registers				
0x0480	**LVMX0003**	R/W	0x0504_0302	Mux Input Select for LVDS LINK Input Bit 0 to 3

0x0484	**LVMX0407**	R/W	0x0A07_0106	Mux Input Select for LVDS LINK Input Bit 4 to 7
0x0488	**LVMX0811**	R/W	0x0908_0C0B	Mux Input Select for LVDS LINK Input Bit 8 to 11
0x048C	**LVMX1215**	R/W	0x120F_0E0D	Mux Input Select for LVDS LINK Input Bit 12 to 15
0x0490	**LVMX1619**	R/W	0x1413_1110	Mux Input Select for LVDS LINK Input Bit 16 to 19
0x0494	**LVMX2023**	R/W	0x1B17_1615	Mux Input Select for LVDS LINK Input Bit 20 to 23
0x0498	**LVMX2427**	R/W	0x001A_1918	Mux Input Select for LVDS LINK Input Bit 24 to 27
0x049C	**LVCFG**	R/W	0x0000_0820	LVDS Configuration Register
0x04A0	**LVPHY0**	R/W	0x0004_4106	LVDS PHY Register 0
0x04A4	**LVPHY1**	R/W	0x0000_0000	LVDS PHY Register 1
System Registers				
0x0500	**SYSSTAT**	RO	0x0000_0000	System Status Register
0x0504	**SYSRST**	WO	0x0000_0000	System Reset Register
GPIO Registers				
0x0520	**GPIOC**	R/W	0x0000_0000	GPIO Control Register
0x0524	**GPIOO**	R/W	0x0000_0000	GPIO Output Register
0x0528	**GPIOI**	RO	0x0000_000X	GPIO Input Register
I2C Registers				
0x0540	**I2CTIMCTRL**	R/W	0x0080_0080	I2C IF Timing and Enable Control Register
0x0544	**I2CMADDR**	R/W	0x0000_0000	I2C Master Addressing Register
0x0548	**WDATAQ**	WO	-	Write Data Queue
0x054A	**RDATAQ**	WO	-	Read Data Queue
Chip/Rev Registers				
0x0580	**IDREG**	RO	0x0000_7500	Chip ID and Revision ID
Debug Registers				
0x05A0	**DEBUG00**	R/W	0x0000_0008	Debug Register
0x05A4	**DEBUG01**	R/W	0x0000_1F63	LVDS Data register
0x05A8	**DEBUG02**	R/W	0x0000_0000	DSI Input Debug register

6.2 DSI PHY Layer Registers

6.2.1 D0W_DPHYCONTTX Register

Mnemonic	D0W_DPHYCONTTX (Adrs = 0x0004)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	---							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						LPTXCURR1EN	LPTXCURR0EN
Access	---						R/W	R/W
Default	0x00						1	0

Field Name	Bit	Description
Reserved	[31:2]	
D0W_LPTXCURR1EN	1	**D0W_LPTXCURR1EN:** Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
D0W_LPTXCURR0EN	0	**D0W_LPTXCURR0EN:** Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. Setting it to “00” makes rise/fall time longer, and setting to “11” makes it shorter.		

6.2.2 CLW_DPHYCONTRX Register

Mnemonic	CLW_DPHYCONTRX (Adrs = 0x0020)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Resvd	Resvd	HSRXTUNE1	HSRXTUNE0	Resvd	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Resvd	Resvd	CLW_CURSEL	LPRXVTHLOW	Resvd	ATMREN	ATMR1	ATMR0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Field Name	Bit	Description
Reserved	[31:14]	
CLW_HSRXTUNE	[13:12]	**CLW_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Clock Lane**. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	11	
CLW_DLYCNTRL	[10:8]	**CLW_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)}$ x 20ps for Clock Lane in HSRX**. 3'b000: (Temporary default)
Reserved	[7:6]	
CLW_CURSEL	5	**CLW_CURSEL: LPRXVTHLOW Selection** 1:LPRXVTHLOW value is set by CUTR cell 0:LPRXVTHLOW value is set by CLW_LPRXVTHLOW
CLW_LPRXVTHLOW	4	**CLW_LPRXVTHLOW: LPRX input threshold select for Clock Lane**. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary default)
Reserved3	3	
CLW_ATMREN	2	**CLW_ATMREN: Analog timer function enable for Clock Lane in HSRX.** 0: analog timer function off (default) 1: analog timer function on This bit is valid only in TESTMODE=1. When TESTMODE=0, this bit can be written or read but it does not affect any function.
CLW_ATMR	[1:0]	**CLW_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Clock Lane in HSRX**. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (default) (ATMR1, ATMR0) = (1,1): delay = D3

NOTE:

1. Please do not change the values in bits 15, 14 and 11
2. In the description for DSI-RX related registers, TESTMODE and TESTMODEREGEN refer to the chip internal test mode signals, and should be treated as for internal test purpose only.

6.2.3 D0W_DPHYCONTRX Register

Mnemonic	D0W_DPHYCONTRX (Adrs = 0x0024)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Resvd	Resvd	HSRXTUNE1	HSRXTUNE0	Resvd	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Resvd	Resvd	CURSEL	LPRXVTHLOW	Resvd	ATMREN	ATMR1	ATMR0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Field Name	Bit	Description
Reserved	[31:14]	
D0W_HSRXTUNE	[13:12]	**D0W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 0**. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	11	
D0W_DLYCNTRL	[10:8]	**D0W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)}$ x 20ps for Data Lane 0 in HSRX**. 3'b000: (Temporary default)
Reserved	[7:6]	
D0W_CURSEL	5	**D0W_CURSEL: LPRXVTHLOW Selection** 1:LPRXVTHLOW value is set by CUTR cell 0:LPRXVTHLOW value is set by D0W_LPRXVTHLOW
D0W_LPRXVTHLOW	4	**D0W_LPRXVTHLOW: LPRX input threshold select for Data Lane 0**. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary default)
Reserved3	3	
D0W_ATMREN	2	**D0W_ATMREN: Analog timer function enable for Data Lane 0 in HSRX**. 0: analog timer function off (default) 1: analog timer function on This bit is valid only in TESTMODE=1. When TESTMODE=0, this bit can be written or read but it does not affect any function.
D0W_ATMR	[1:0]	**D0W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Clock Lane 0 in HSRX**. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (default) (ATMR1, ATMR0) = (1,1): delay = D3

NOTE: Please do not change the values in bits 15, 14 and 11

6.2.4 D1W_DPHYCONTRX Register

Mnemonic	D1W_DPHYCONTRX (Adrs = 0x0028)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Resvd	Resvd	HSRXTUNE1	HSRXTUNE0	Resvd	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Resvd	Resvd	CURSEL	LPRXVTHLOW	Resvd	ATMREN	ATMR1	ATMR0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Field Name	Bit	Description
Reserved	[31:14]	
D1W_HSRXTUNE	[13:12]	**D1W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 1**. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	11	
D1W_DLYCNTRL	[10:8]	**D1W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)}$ x 20ps for Data Lane 1 in HSRX**. 3'b000: (Temporary default)
Reserved	[7:6]	
D1W_CURSEL	5	**D1W_CURSEL: LPRXVTHLOW Selection** 1:LPRXVTHLOW value is set by CUTR cell 0:LPRXVTHLOW value is set by D1W_LPRXVTHLOW
D1W_LPRXVTHLOW	4	**D1W_LPRXVTHLOW: LPRX input threshold select for Data Lane 1**. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary default)
Reserved3	3	
D1W_ATMREN	2	**D1W_ATMREN: Analog timer function enable for Data Lane 1 in HSRX**. 0: analog timer function off (default) 1: analog timer function on This bit is valid only in TESTMODE=1. When TESTMODE=0, this bit can be written or read but it does not affect any function.
D1W_ATMR	[1:0]	**D1W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Data Lane 1 in HSRX**. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (default) (ATMR1, ATMR0) = (1,1): delay = D3

NOTE: Please do not change the values in bits 15, 14 and 11

6.2.5 D2W_DPHYCONTRX Register

Mnemonic	D1W_DPHYCONTRX (Adrs = 0x002C)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Resvd	Resvd	HSRXTUNE1	HSRXTUNE0	Resvd	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Resvd	Resvd	CURSEL	LPRXVTHLOW	Resvd	ATMREN	ATMR1	ATMR0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Field Name	Bit	Description
Reserved	[31:14]	
D2W_HSRXTUNE	[13:12]	**D2W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 2**. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	11	
D2W_DLYCNTRL	[10:8]	**D2W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)}$ x 20ps for Data Lane 2 in HSRX**. 3'b000: (Temporary default)
Reserved	[7:6]	
D2W_CURSEL	5	**D2W_CURSEL: LPRXVTHLOW Selection** 1:LPRXVTHLOW value is set by CUTR cell 0:LPRXVTHLOW value is set by D2W_LPRXVTHLOW
D2W_LPRXVTHLOW	4	**D2W_LPRXVTHLOW: LPRX input threshold select for Data Lane 2**. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary default)
Reserved3	3	
D2W_ATMREN	2	**D2W_ATMREN: Analog timer function enable for Data Lane 2 in HSRX**. 0: analog timer function off (default) 1: analog timer function on This bit is valid only in TESTMODE=1. When TESTMODE=0, this bit can be written or read but it does not affect any function.
D2W_ATMR	[1:0]	**D2W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Data Lane 2 in HSRX**. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (default) (ATMR1, ATMR0) = (1,1): delay = D3

NOTE: Please do not change the values in bits 15, 14 and 11

6.2.6 D3W_DPHYCONTRX Register

Mnemonic	D3W_DPHYCONTRX (Adrs = 0x0030)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Resvd	Resvd	HSRXTUNE1	HSRXTUNE0	Resvd	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Resvd	Resvd	CURSEL	LPRXVTHLOW	Resvd	ATMREN	ATMR1	ATMR0
Access	--	--	R/W	R/W	--	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Field Name	Bit	Description
Reserved	[31:14]	
D3W_HSRXTUNE	[13:12]	**D3W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 3**. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	11	
D3W_DLYCNTRL	[10:8]	**D3W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)}$ x 20ps for Data Lane 3 in HSRX**. 3'b000: (Temporary default)
Reserved	[7:6]	
D3W_CURSEL	5	**D3W_CURSEL: LPRXVTHLOW Selection** 1:LPRXVTHLOW value is set by CUTR cell 0:LPRXVTHLOW value is set by D3W_LPRXVTHLOW
D3W_LPRXVTHLOW	4	**D3W_LPRXVTHLOW: LPRX input threshold select for Data Lane 3**. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary default)
Reserved3	3	
D3W_ATMREN	2	**D3W_ATMREN: Analog timer function enable for Data Lane 3 in HSRX**. 0: analog timer function off (default) 1: analog timer function on This bit is valid only in TESTMODE=1. When TESTMODE=0, this bit can be written or read but it does not affect any function.
D3W_ATMR	[1:0]	**D3W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Data Lane 3 in HSRX**. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (default) (ATMR1, ATMR0) = (1,1): delay = D3

NOTE: Please do not change the values in bits 15, 14 and 11

6.2.7 COM_DPHYCONTRX Register

Mnemonic	COM_DPHYCONTRX (Adrs = 0x0038)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	---							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						LPRXCALRES	LPRXCALEN
Access	---						R/W	R/W
Default	0x00						0	0

Field Name	Bit	Description
Reserved	[31:2]	
LPRXCALRES	1	**LPRXCALRES: LPRX Calibration Reset.** 0: Not Reset 1: Resets high LPRXVTHLOW Reset with this bit set to 1 requires the bit remains set to 1 for 500us or more.
LPRXCALEN	0	**LPRXCALEN: LPRX Calibration Enable** 0: Calibration Switch OFF 1: Calibration Switch ON Calibration with this bit set to 1 requires the bit remains set to 1 for 500us or more

6.2.8 CLW_CNTRL Register

Mnemonic	CLW_CNTRL (Adrs = 0x0040)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	LaneEnDFT	Reserved						
Access	R/W	---						
Default	0	0x00						
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							LaneDisable
Access	---							R/W
Default	0x00							0

Field Name	Bit	Description
Reserved	[31:16]	
LaneEnDFT	[15]	**LaneEnDFT: Force Lane Enable for DFT** The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D0W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (default)
Reserved	[14:1]	
LaneDisable	0	**LaneDisable: Force Lane Disable for Clock Lane.** 1'b1 : Force Lane Disable 1'b0 : Bypass Lane Enable (default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

6.2.9 D0W_CNTRL Register

Mnemonic	D0W_CNTRL (Adrs = 0x0044)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	LaneEnDFT	Reserved						
Access	R/W	---						
Default	0	0x00						
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							LaneDisable
Access	---							R/W
Default	0x00							0

Field Name	Bit	Description
Reserved	[31:16]	
LaneEnDFT	[15]	**LaneEnDFT: Force Lane Enable for DFT** The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D0W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (default)
Reserved	[14:1]	
LaneDisable	0	**LaneDisable: Force Lane Disable for Data Lane 0.** 1'b1 : Force Lane Disable 1'b0 : Bypass Lane Enable (default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

NOTE: Please do not change the values in bits 9 and 8

6.2.10 D1W_CNTRL Register

Mnemonic	D1W_CNTRL (Adrs = 0x0048)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LaneEnDFT	Reserved						
Access	R/W	---						
Default	0	0x00						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							LaneDisable
Access	---							R/W
Default	0x00							0

Field Name	Bit	Description
Reserved	[31:16]	
LaneEnDFT	[15]	**LaneEnDFT: Force Lane Enable for DFT** The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D1W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (default)
Reserved	[14:1]	
LaneDisable	0	**LaneDisable: Force Lane Disable for Data Lane 1.** 1'b1 : Force Lane Disable 1'b0 : Bypass Lane Enable (default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

NOTE: Please do not change the values in bits 9 and 8

6.2.11 D2W_CNTRL Register

Mnemonic	D2W_CNTRL (Adrs = 0x004C)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LaneEnDFT	Reserved						
Access	R/W	---						
Default	0	0x00						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							LaneDisable
Access	---							R/W
Default	0x00							0

Field Name	Bit	Description
Reserved	[31:16]	
LaneEnDFT	[15]	**LaneEnDFT: Force Lane Enable for DFT** The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D2W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (default)
Reserved	[14:1]	
LaneDisable	0	**LaneDisable: Force Lane Disable for Data Lane 2.** 1'b1 : Force Lane Disable 1'b0 : Bypass Lane Enable (default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

NOTE: Please do not change the values in bits 9 and 8

6.2.12 D3W_CNTRL Register

Mnemonic	D3W_CNTRL (Adrs = 0x0050)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LaneEnDFT	Reserved						
Access	R/W	---						
Default	0	0x00						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							LaneDisable
Access	---							R/W
Default	0x00							0

Field Name	Bit	Description

Field Name	Bit	Description
Reserved	[31:16]	
LaneEnDFT	[15]	**LaneEnDFT: Force Lane Enable for DFT** The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D3W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (default)
Reserved	[14:1]	
LaneDisable	0	**LaneDisable: Force Lane Disable for Data Lane 3.** 1'b1 : Force Lane Disable 1'b0 : Bypass Lane Enable (default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

NOTE: Please do not change the values in bits 9 and 8

6.2.13 DFT Mode Control Register

Mnemonic	DFTMODE_CNTRL (Adrs = 0x0054)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							DFTMUXMODE_EN
Access	---							R/W
Default	0x00							0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	DFT_BYTECLK_EN	TESTLANESEL		Reserved	PCEN	TEST_INTLB	Reserved
Access	---	R/W	R/W		---	R/W	R/W	---
Default	0	0	00		0	0	0	0

Field Name	Bit	Description
Reserved	[31:9]	
DFTMUXMODE_EN	8	DFTMUXMODE_EN: DFT Mux Test Mode Data Enable. 1'b1: Enable The test mode is enabled. 1'b0: Disable
Reserved	7	
DFT_BYTECLK_EN	6	DFT_BYTECLK_EN: DFT_CLH_RxHsByteClk Enable 1'b1: Enable 1'b0: Disable
TESTLANESEL	[5:4]	TESTLANE_SEL: Input Lane Select for Internal Loopback The bit enabled when TEST_INTLB = 1'b1. 11: DataLane 3 Select 10: DataLane 2 Select 01: DataLane 1 Select 00: DataLane 0 Select
Reserved	3	
PCEN	2	Pattern Capture Enable: Used when DFTMUXMODE_EN = 1. 1'b1: Pattern Capture Enable. D-PHY IO is programmed to be HSRX. 1'b0: Disable
TEST_INTLB	1	TEST_INTLB: Internal Loopback select. 1'b1: Internal Loopback 1'b0: External Loopback
Reserved	0	

NOTE: Please do not change the value in bit 0

6.3 DSI PPI Layer Registers

6.3.1 PPI_STARTPPI Register

Mnemonic	PPI_STARTPPI (Adrs = 0x0104)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Access	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							StartPPI
Access	RO							WO
Default	0x00							0

Field Name	Bit	Description
Reserved	[31:1]	
startPPI	0	**startPPI** START control bit of PPI-TX function. By writing 1 or 0 to this bit, the values of initial registers are latched inside of PPI, and PPI starts function. Once START bit is set to high, the change of the register bits does not affect to function. 0: (Default) Stop function. Writing 0 is invalid and the bit can be set to zero by system reset only. 1: Start function.

6.3.2 PPI_BUSYPPI Register

Mnemonic	PPI_BUSYPPI (Adrs = 0x0108)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Access	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name								BusyPPI
Access								RO
Default								0

Field Name	Bit	Description
Reserved	[31:1]	
BusyPPI	0	**BUSY** After writing 1 to START bit in STARTPPI register, this bit is set until RESET_N is asserted. 0: Not Busy. (default) 1: Busy.

6.3.3 PPI_LINEINITCNT Register

Mnemonic	PPI_LININITCNT (Adrs = 0x0110)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LINEINITCNT[15:8]							
Access	R/W							
Default	0x20							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LININITCNT[7:0]							
Access	R/W							
Default	0x8E							

Field Name	Bit	Description
Reserved	[31:16]	
LINEINITCNT	[15:0]	LINEINITCNT Line Initialization Wait Counter This counter is used for line initialization. MIPI specification requires that slave device needs to observe LP-11 for 100 us and ignore the received data before the period at initialization time. The count value depends on HSByteClk and the value needs to be set to achieve more than 100 us. The counter starts after STARTPPI bit of STARTPPI register is set. Master device needs to output LP-11 for 100 us in order for slave device to observe LP-11 for the period. For example, in order to set 100 us when the period of HSByteClk is 12 ns, the counter value should be more than 8333.3 = 0x208D (100 us / 12 ns). Default is 0x208E.

6.3.4 PPI_LPTXTIMECNT Register

Mnemonic	PPI_LPTXCNT (Adrs = 0x0114)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name						LPTXCNT[10:8]		
Access						R/W		
Default						0x00		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXCNT[7:0]							
Access	R/W							
Default	0x01							

Field Name	Bit	Description
Reserved	[31:11]	
	[10:0]	**LPTXTIMECNT** SYSLPTX Timing Generation Counter The counter generates a timing signal for the period of T_{LPX}. The counter is counted by HSByteClk. And the count up value is changed to one pulse of SYSTEM clock, and it is used as SYSLPTX timing enable. SYSLPTX clock domain block works by the every active timing of SYSLPTX Timing enable, which is the counted value of this register. The SYSLPTX Timing enable is one pulse of SYSTEM clock. Default value is one. Setting zero is prohibited and the working when set to zero is not guaranteed. The timing signal frequency should be not more than 20MHz to comply with MIPI specification in which T_{LPX} should be more than 50ns.

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.3.5 PPI_LANEENABLE Register

Mnemonic	PPI_LANEENABLE (Adrs = 0x0134)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Access	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				L3EN	L2EN	L1EN	L0EN	CLEN
Access				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	1	1

Field Name	Bit	Description
Reserved	[15:3]	
L3EN	2	**L3 Lane Enable** Data Lane 3 Enable 0: Lane operation disabled (default) 1: Lane operation enabled
L2EN	1	**L2 Lane Enable** Data Lane 2 Enable 0: Lane operation disabled (default) 1: Lane operation enabled
L1EN	2	**L1 Lane Enable** Data Lane 1 Enable 0: Lane operation disabled (default) 1: Lane operation enabled
L0EN	1	**L0 Lane Enable** Data Lane 0 Enable 0: Lane operation disabled 1: Lane operation enabled (default)
CLEN	0	**Clock Lane Enable** Clock Lane 0 Enable 0: Lane operation disabled 1: Lane operation enabled (default)

This register controls the lane operation at the PPI layer within the DSI-RX module.
In a typical configuration sequence, this register is programmed before StartPPI register. Once StartPPI register is enabled and BusyPPI status indicates busy, user should only reprogram the setting of this register with great care. The following constraints are advised:

Modification to allow the change during busy is considered acceptable with following limitations.
1) There must be sufficient length (minimum 100us) of LP11 period before and after the register change such that internal data transfer within the DSI-RX pipeline has been flushed out.
2) Switching lane 0 during BTA (when the lane is TX) is not allowed.

6.3.6 PPI_TX_RX_TA Register

Mnemonic	PPI_TX_RX_TA (Adrs = 0x013C)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved					TXTAGOCNT[10:8]		
Access	RO					RW		
Default	0x00					0x0		
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	TXTAGOCNT[7:0]							
Access	RW							
Default	0x08							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved					TXTASURECNT[10:8]		
Access	RO					RW		
Default	0x00					0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TXTASURECNT[7:0]							
Access	R/W							

Default	0x8

Field Name	Bit	Description
Reserved	[31:27]	
TXTAGOCNT[10:0]	[26:16]	TXTAGOCNT is used to configure the TTA-GET timing as specified by the MIPI DPHY specification on Global Operation Timing Parameters. TTA-GET is defined as the time that the new transmitter drives the bridge state (LP-00) afer accepting control during a Link Turn Around. This register field should be set to be = (5 * PPI_LPTXTIMECNT – 3) / 4.
Reserved	[15:11]	
TXTASURECNT [10:0]	[10:0]	TXTASURECNT is used to configure the TTA-SURE timing as specified by the MIPI DPHY specification on Global Operation Timing Parameters. TTA-SURE is defined as the time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turn Around. This register field should be set to be = 1.5 * PPI_LPTXTIMECNT

6.3.7 PPI_CLS_ATMR Register

Mnemonic	PPI_CLS_ATMR (Adrs = 0x0140)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name						CLS_ATMREN	CLS_ATMR	
Access						R/W		
Default						0	0	0

Field Name	Bit	Description
Reserved	[31:3]	
CLS_ATMREN	2	Analog timer function enable for Data Lane 0 in LPRX.
CLS_ATMR	[1:0]	**CLS_ATMR[1:0]** Selection of different delay times for tuning of Analog Timer for Clock Lane in LPRX. (0,0): Bypass mode (0,1): delay = D1 (1,0): delay = D2 (default) (1,1): delay = D3

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)
Analog Timer (ATMR) function in the D-PHY is not used by the DSI-RX in this chip. Please set CLS_ATMREN = 0, CLS_ATMR [1:0] =”00”.

6.3.8 PPI_D0S_ATMR Register

Mnemonic	PPI_D0S_ATNR (Adrs = 0x0144)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name						D0S_ATMREN	D0S_ATMR	
Access						R/W	R/W	R/W
Default						0	0	0

Field Name	Bit	Description
Reserved	[31:3]	
D0S_ATMREN	2	D0S_ATMREN: Analog timer function enable for Data Lane 0 in LPRX. 0: analog timer function off (default) 1:analog timer function on
D0S_ATMR	[1:0]	D0S_ATMR[1:0] Selection of different delay times for tuning of Analog Timer for Data Lane 0 in LPRX. (0,0): Bypass mode (0,1): delay = D1 (1,0): delay = D2 (default) (1,1): delay = D3

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)
Analog Timer (ATMR) function is not used. Please set D0S_ATMREN = 0, D0S_ATMR [1:0] =”00”.

6.3.9 PPI_D1S_ATMR Register

Mnemonic	PPI_D1S_ATMR (Adrs = 0x0148)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name						D1S_ATMREN	D1S_ATMR	
Access						R/W	R/W	R/W
Default						0	0	0

Field Name	Bit	Description
Reserved	[31:3]	
D1S_ATMREN	2	**D1S_ATMREN:** Analog timer function enable for Data Lane 1 in LPRX. 0: analog timer function off (default) 1:analog timer function on
D1S_ATMR	[1:0]	**D1S_ATMR[1:0]** Selection of different delay times for tuning of Analog Timer for Data Lane 1 in LPRX. (0,0): Bypass mode (0,1): delay = D1 (1,0): delay = D2 (default) (1,1): delay = D3

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)
Analog Timer (ATMR) function is not used. Please set D1S_ATMREN = 0, D1S_ATMR [1:0] =”00”.

6.3.10 PPI_D2S_ATMR Register

Mnemonic	PPI_D2S_ATMR (Adrs = 0x014C)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name						D2S_ATMREN	D2S_ATMR	
Access						R/W	R/W	R/W
Default						0	0	0

Field Name	Bit	Description
Reserved	[31:3]	
D2S_ATMREN	2	**D2S_ATMREN:** Analog timer function enable for Data Lane 2 in LPRX. 0: analog timer function off (default) 1:analog timer function on
D2S_ATMR	[1:0]	**D2S_ATMR[1:0]** Selection of different delay times for tuning of Analog Timer for Data Lane 2 in LPRX. (0,0): Bypass mode (0,1): delay = D1 (1,0): delay = D2 (default) (1,1): delay = D3

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)
Analog Timer (ATMR) function is not used. Please set D2S_ATMREN = 0, D2S_ATMR [1:0] =”00”.

6.3.11 PPI_D3S_ATMR Register

Mnemonic	PPI_D3S_ATMR (Adrs = 0x0150)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name						D3S_ATMREN	D3S_ATMR	
Access						R/W	R/W	R/W
Default						0	0	0

Field Name	Bit	Description
Reserved	[31:3]	
D3S_ATMREN	2	**D3S_ATMREN: Analog timer function enable for Data Lane 3 in LPRX.** 0: analog timer function off (default) 1:analog timer function on
D3S_ATMR	[1:0]	**D3S_ATMR[1:0]** Selection of different delay times for tuning of Analog Timer for Data Lane 3 in LPRX. (0,0): Bypass mode (0,1): delay = D1 (1,0): delay = D2 (default) (1,1): delay = D3

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)
Analog Timer (ATMR) function is not used. Please set D3S_ATMREN = 0, D3S_ATMR [1:0] =”00”.

6.3.12 PPI_D0S_CLRSIPOCOUNT Register

Mnemonic	PPI_D0S_CLRSIPOCOUNT (Adrs = 0x0164)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name			D0S_CLRSIPOCOUNT					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Default			0	1	1	0	0	1

Field Name	Bit	Description
Reserved	[31:6]	
D0S_CLRSIPOCOUNT	[5:0]	**D0S_CLRSIPOCOUNT** CLRSIPO counter for data lane 0. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value. Set the counter value between 85 ns + 6*UI and 145ns + 10*UI.

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.3.13 PPI_D1S_CLRSIPOCOUNT Register

Mnemonic	PPI_D1S_CLRSIPOCOUNT (Adrs = 0x0168)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name								
Access								
Default								
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name			D1S_CLRSIPOCOUNT					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Default			0	1	1	0	0	1

Field Name	Bit	Description
Reserved	[31:6]	
D1S_CLRSIPOCOUNT	[5:0]	**D1S_CLRSIPOCOUNT** CLRSIPO counter for data lane 0. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value. Set the counter value between 85 ns + 6*UI and 145ns + 10*UI.

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.3.14 PPI_D2S_CLRSIPOCOUNT Register

Mnemonic	PPI_D2S_CLRSIPOCOUNT (Adrs = 0x016C)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name			D2S_CLRSIPOCOUNT					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Default			0	1	1	0	0	1

Field Name	Bit	Description
Reserved	[31:6]	
D2S_CLRSIPOCOUNT	[5:0]	**D2S_CLRSIPOCOUNT** CLRSIPO counter for data lane 2. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value. Set the counter value between 85 ns + 6*UI and 145ns + 10*UI.

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.3.15 PPI_D3S_CLRSIPOCOUNT Register

Mnemonic	PPI_D3S_CLRSIPOCOUNT (Adrs = 0x0170)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name			D3S_CLRSIPOCOUNT					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Default			0	1	1	0	0	1

Field Name	Bit	Description
Reserved	[31:6]	
D3S_CLRSIPOCOUNT	[5:0]	**D3S_CLRSIPOCOUNT** CLRSIPO counter for data lane 3. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value. Set the counter value between 85 ns + 6*UI and 145ns + 10*UI.

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.3.16 CLS_PRE Register

Mnemonic	CLSPRE (Adrs = 0x0180)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CLS_PREEN			CLS_PREFLG			CLS_SETPRE	
Access	R/W			R			R/W	
Default	0			0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CLS_SETPRE							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
CLS_PREEN	15	**CLS_SETPREEN** CLS_SETPRE Register bit Enable. CLS_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of CLS_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
CLS_PREFLG	12	**CLS_PREFLG** Flag indicating counter value SETPRE has been reached for Clock Lane. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
CLS_SETPRE	[9:0]	**CLS_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Clock Lane. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.17 D0S_PRE Register

Mnemonic	D0SPRE (Adrs = 0x0184)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	D0S_PREEN			D0S_PREFLG			D0S_SETPRE	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D0S_SETPRE							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D0S_PREEN	15	**D0S_SETPREEN** D0S_SETPRE Register bit Enable. D0S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D0S_PREFLG	12	**D0S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 0. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D0S_SETPRE	[9:0]	**D0S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 0. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.18 D1S_PRE Register

Mnemonic	D1SPRE (Adrs = 0x0188)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D1S_PREEN			D1S_PREFLG			D1S_SETPRE	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D1S_SETPRE							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D1S_PREEN	15	**D1S_SETPREEN** D1S_SETPRE Register bit Enable. D1S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D1S_PREFLG	12	**D1S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 1. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D1S_SETPRE	[9:0]	**D1S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 1. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.19 D2S_PRE Register

Mnemonic	D2SPRE (Adrs = 0x018C)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D2S_PREEN			D2S_PREFLG			D2S_SETPRE	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D2S_SETPRE							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D2S_PREEN	15	**D2S_SETPREEN** D2S_SETPRE Register bit Enable. D2S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D2S_PREFLG	12	**D2S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 2. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D2S_SETPRE	[9:0]	**D2S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 2. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.20 D3S_PRE Register

Mnemonic	D3SPRE (Adrs = 0x0190)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D3S_PREEN			D3S_PREFLG			D3S_SETPRE	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D3S_SETPRE							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D3S_PREEN	15	**D3S_SETPREEN** D3S_SETPRE Register bit Enable. D3S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D3S_PREFLG	12	**D3S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 3. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D3S_SETPRE	[9:0]	**D3S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 3. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.21 CLS_PREP Register

Mnemonic	CLS_PREP (Adrs = 0x01A0)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	CLS_PREPEN			CLS_PREPFLG			CLS_SETPREP	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CLS_SETPREP							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
CLS_PREPEN	15	**CLS_SETPREEN** CLS_SETPREP Register bit Enable. CLS_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of CLS_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
CLS_PREPFLG	12	**CLS_PREPFLG** Flag indicating counter value SETPREP has been reached for Clock Lane. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
CLS_SETPREP	[9:0]	**CLS_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Clock Lane. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.22 D0S_PREP Register

Mnemonic	D0S_PREP (Adrs = 0x01A4)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D0S_PREPEN			D0S_PREPFLG			D0S_SETPREP	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D0S_SETPREP							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D0S_PREPEN	15	**D0S_SETPREPEN** D0S_SETPREP Register bit Enable. D0S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D0S_PREPFLG	12	**D0S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 0. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D0S_SETPREP	[9:0]	**D0S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 0. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.23 D1S_PREP Register

Mnemonic	D1S_PREP (Adrs = 0x01A8)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D1S_PREPEN			D1S_PREPFLG				
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D1S_SETPREP							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D1S_PREPEN	15	**D1S_SETPREP Register bit Enable.** D1S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D1S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D1S_PREPFLG	12	**D1S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 1. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D1S_SETPREP	[9:0]	**D1S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 1. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.24 D2S_PREP Register

Mnemonic	D2S_PREP (Adrs = 0x01AC)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D2S_PREPEN			D2S_PREPFLG			D2S_SETPREP	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D2S_SETPREP							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D2S_PREPEN	15	**D2S_SETPREP Register bit Enable.** D2S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D2S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D2S_PREPFLG	12	**D2S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 2. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D2S_SETPREP	[9:0]	**D2S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 2. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.25 D3S_PREP Register

Mnemonic	D3S_PREP (Adrs = 0x01B0)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D3S_PREPEN			D3S_PREPFLG			D3S_SETPREP	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D3S_SETPREP							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D3S_PREPEN	15	**D3S_SETPREP Register bit Enable.** D3S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D3S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D3S_PREPFLG	12	**D3S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 3. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D3S_SETPREP	[9:0]	**D3S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 3. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.26 CLS_ZERO Register

Mnemonic	CLS_ZERO (Adrs = 0x01C0)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	CLS_ZEROEN			CLS_ZEROFLG			CLS_SETZERO	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CLS_SETZERO							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
CLS_ZEROEN	15	**CLS_SETZERO Register bit Enable** CLS_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of CLS_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
CLS_ZEROFLG	12	**CLS_ZEROFLG** Flag indicating counter value SETZERO has been reached for Clock Lane. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
CLS_SETZERO	[9:0]	**CLS_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Clock Lane. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.27 D0S_ZERO Register

Mnemonic	D0S_ZERO (Adrs = 0x01C4)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D0S_ZEROEN			D0S_ZEROFLG			D0S_SETZERO	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D0S_SETZERO							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D0S_ZEROEN	15	**D0S_SETZEROEN** D0S_SETZERO Register bit Enable. D0S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D0S_ZEROFLG	12	**D0S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 0. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D0S_SETZERO	[9:0]	**D0S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 0. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.28 D1S_ZERO Register

Mnemonic	D1S_ZERO (Adrs = 0x01C8)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D1S_ZEROEN			D1S_ZEROFLG			D1S_SETZERO	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D1S_SETZERO							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D1S_ZEROEN	15	**D1S_SETZEROEN** D1S_SETZERO Register bit Enable. D1S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D1S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D1S_ZEROFLG	12	**D1S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 1. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D1S_SETZERO	[9:0]	**D1S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 1. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.29 D2S_ZERO Register

Mnemonic	D2S_ZERO (Adrs = 0x01CC)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	D2S_ZEROEN			D2S_ZEROFLG			D2S_SETZERO	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D2S_SETZERO							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D2S_ZEROEN	15	**D2S_SETZEROEN** D2S_SETZERO Register bit Enable. D2S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D2S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D2S_ZEROFLG	12	**D2S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 2. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D2S_SETZERO	[9:0]	**D2S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 2. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.30 D3S_ZERO Register

Mnemonic	D3S_ZERO (Adrs = 0x01D0)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	D3S_ZEROEN			D3S_ZEROFLG			D3S_SETZERO	
Access	R/W			R			R/W	
Default	0x0			0x0			0x00	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D3S_SETZERO							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:16]	
D3S_ZEROEN	15	**D3S_SETZEROEN** D3S_SETZERO Register bit Enable. D3S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D3S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D3S_ZEROFLG	12	**D3S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 3. It stops the counter. If write to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D3S_SETZERO	[9:0]	**D3S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 3. 10'b00_0000_0000: (Temporary default)

Can be modified while [BUSYPPI].BusyPpi is 1.
Since counter function is not used, do not change SETPREEN=0 setting.

6.3.31 PPI_CLRFLG Register

Mnemonic	PPI_CLRFLG (Adrs = 0x01E0)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name								
Access								
Default								
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name			D1_CLRFLGEN	D1_CLRFLG	D0_CLRFLGEN	D0_CLRFLG	CL_CLRFLGEN	CL_CLRFLG
Access			R/W					
Default			0x00					

NOTE: Please do not change the values in bits 9, 8, 7 and 6

Field Name	Bit	Description
Reserved	[31:6]	
D1_CLRFLGEN	5	**D1_CLRFLGEN** D1_CLRFLG Register bit Enable. D1_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of D1_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D1_CLRFLG	4	**D1_CLRFLG** Flag indicating counter value SETPRE has been reached for Data Lane 1. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D0_CLRFLGEN	3	**D0_CLRFLGEN** D0_CLRFLG Register bit Enable. D0_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of D0_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D0_CLRFLG	2	**D0_CLRFLG** Flag indicating counter value SETPRE has been reached for Data Lane 0. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
CL_CLRFLGEN	1	**CL_CLRFLGEN** CL_CLRFLG Register bit Enable. CL_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of CL_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
CL_CLRFLG	0	**CL_CLRFLG** Flag indicating counter value SETPRE has been reached for Clock Lane. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)

Since counter function is not used, do not change from initial setting.

6.3.32 PPI_CLRSIPO Register

Mnemonic	PPI_CLRSIPO (Adrs = 0x01E4)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name							D3_CLRSIPOEN	D3_CLRSIPO
Access							R/W	
Default							0x1	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D2_CLRSIPOEN	D2_CLRSIPO	D1_CLRSIPOEN	D1_CLRSIPO	D0_CLRSIPOEN	D0_CLRSIPO	CL_CLRSIPOEN	CL_CLRSIPO
Access	R/W							
Default	0x55							

Field Name	Bit	Description
Reserved	[31:6]	
D1_CLRSIPOEN	5	**D1_CLRSIPOEN** D1_CLRSIPO Register bit Enable. D1_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of D1_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D1_CLRSIPO	4	**D1_CLRSIPO** Flag indicating counter value SETPRE has been reached for Data Lane 1. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D0_CLRSIPOEN	3	**D0_CLRSIPOEN** D0_CLRSIPO Register bit Enable. D0_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of D0_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D0_CLRSIPO	2	**D0_CLRSIPO** Flag indicating counter value SETPRE has been reached for Data Lane 0. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
CL_CLRSIPOEN	1	**CL_CLRSIPOEN** CL_CLRSIPO Register bit Enable. CL_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of CL_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
CL_CLRSIPO	0	**CL_CLRSIPO** Flag indicating counter value SETPRE has been reached for Clock Lane. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)

6.3.33 HSTIMEOUT Register

Mnemonic	PPI_HSTIMEOUT (Adrs = 0x01F0)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name					HSTO[27:24]			
Access					R/W			
Default					0x00			
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	HSTO[23:16]							
Access	R/W							
Default	0x00							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	HSTO[15:8]							
Access	R/W							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	HSTO[7:0]							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	[31:28]	
HSTO	[27:0]	TimeOut for HS, upper Bytes

Cannot be overwritten wrile BusyPpi=1.
Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.3.34 HSTIMEOUTENABLE Register

Mnemonic	PPI_HSTIMEOUTENABLE (Adrs = 0x01F4)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	---							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							HSTmOutEn
Access	---							R/W
Default	0x00							0

Field Name	Bit	Description
Reserved	[31:1]	
HSTmOutEn	0	HSTmOutEnTimeOut Enable 0: disabled (default) 1: Enabled

Cannot be overwritten wrile BusyPpi=1.
Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

6.4 DSI Protocol Layer Registers

6.4.1 DSI_LANEENABLE Register

Mnemonic	DSI_LANEENABLE (Adrs = 0x0210)							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name								
Access								
Default								
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name				L3EN	L2EN	L1EN	L0EN	CLEN
Access				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	1	0

Field Name	Bit	Description
Reserved	[15:3]	
L3EN	2	**L3 Lane Enable** Data Lane 3 Enable 0: Lane operation disabled 1: Lane operation enabled
L2EN	1	**L2 Lane Enable** Data Lane 2 Enable 0: Lane operation disabled 1: Lane operation enabled
L1EN	2	**L1 Lane Enable** Data Lane 1 Enable 0: Lane operation disabled 1: Lane operation enabled
L0EN	1	**L0 Lane Enable** Data Lane 0 Enable 0: Lane operation disabled 1: Lane operation enabled
CLEN	0	**Clock Lane Enable** Clock Lane 0 Enable 0: Lane operation disabled 1: Lane operation enabled

This register controls the lane operation at the PPI layer within the DSI-RX module.
In a typical configuration sequence, this register is programmed before StartDSI register. Once StartDSI register is enabled and BusyDSI status indicates busy, user should only reprogram the setting of this register with great care. The following constraints are advised:

Modification to allow the change during busy is considered acceptable with following limitations.
1) There must be sufficient length (minimum 100us) of LP11 period before and after the register change such that internal data transfer within the DSI-RX pipeline has been flushed out.
2) Switching lane 0 during BTA (when the lane is TX) is not allowed.

6.4.2 DSI_LANESTATUS0 Register

Mnemonic	DSI_LANESTATUS0 (Adrs = 0x0214)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Access								
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				L3RxActiveHs	L2RxActiveHs	L1RxActiveHs	L0RxActiveHs	ClRxActiveHs
Access				RO	RO	RO	RO	RO
Default				0	0	0	0	0

Field Name	Bit	Description
Reserved	[31:3]	
L3RxActiveHS	2	**Data Lane 3 Rx Active HS mode status** 0: Lane 3 not in HS Mode 1: Lane 3 in HS Mode
L2RxActiveHS	1	**Data Lane 2 Rx Active HS mode status** 0: Lane 2 not in HS Mode 1: Lane 2 in HS Mode
L1RxActiveHS	2	**Data Lane 1 Rx Active HS mode status** 0: Lane 1 not in HS Mode 1: Lane 1 in HS Mode
L0RxActiveHS	1	**Data Lane 0 Rx Active HS mode status** 0: Lane 0 not in HS Mode 1: Lane 0 in HS Mode
ClRxActiveHS	0	**Clock Lane Rx Active HS mode status** 0: Clock Lane not in HS Mode 1: Clock Lane in HS Mode

Displays dynamically when a lane is in HS RX mode

6.4.3 DSI_LANESTATUS1 Register

Mnemonic	DSI_LANESTATUS1 (Adrs = 0x0218)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name				L3 UlpsEsc	L2 UlpsEsc	L1 UlpsEsc	L0 UlpsEsc	Cl UlpsEsc
Access				RO	RO	RO	RO	RO
Default				0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				L3Stop State	L2Stop State	L1Stop State	L0Stop State	ClStop State
Access				RO	RO	RO	RO	RO
Default				-	-	-	-	-

Field Name	Bit	Description

Field Name	Bit	Description
Reserved	[31:13]	
L3 UlpsEsc	12	L3UlpsEsc－Data Lane 3 Rx Ulps Esc
L2 UlpsEsc	11	L2UlpsEsc－Data Lane 2 Rx Ulps Esc
L1 UlpsEsc	10	L1UlpsEsc－Data Lane 1 Rx Ulps Esc
L0 UlpsEsc	9	L0UlpsEsc－Data Lane 0 Rx Ulps Esc
Cl UlpsEsc	8	ClUlpsEsc－Clock Lane Rx Ulps Esc
Reserved	[7:5]	
L3Stop State	4	Data Lane 3 in Stop State, initial value depends on the lane status
L2Stop State	3	Data Lane 2 in Stop State, initial value depends on the lane status
L1Stop State	2	Data Lane 1 in Stop State, initial value depends on the lane status
L0Stop State	1	Data Lane 0 in Stop State, initial value depends on the lane status
ClStop State	0	Clock Lane in Stop State, initial value depends on the lane status

6.4.4 DSI_INTSTATUS Register

Mnemonic	DSI_INTSTATUS (Adrs = 0x0220)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	ErrRxFifoOvf	ErrLpTxTo	ErrCntLP1	ErrCntLP0	Reserved			
Access	R							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Rsved	L0BTARequest	L0UlpsEscOFF	L0UlpsEscON	L0Trigger[3:0]			
Access	R							
Default	0x00							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	ErrDsiProtocol	Rsved	ErrInvalid	Rsved	ErrDataType	ErrCRC	ErrEccDbl	ErrEccCrctd
Access	R							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Rsved	ErrCntr	ErrHsRxTo	ErrSyncEsc	ErrEsc	ErrEotSyncHs	ErrSotSyncHs	ErrSotHs
Access	R							
Default	0x00							

Field Name	Bit	Description
ErrRxFifoOvf	31	**ErrRxFifoOvf－Fifo Overflow** This bit is set if the synchronization FIFO in PPI from HS data RX clock to system clock is full when an additional HS data is written. Assertion of this bit means there was an omission in RX data. An overflow may happen for example when the system clock is slower than the line rate byte clock
ErrLpTxTo	30	**ErrLpTxTo — LP Transmission Timeout Error** This bit indicates that an error has been detected at the point of LP TX timeout period ([LPTXTO].LpTxTo) during an LP transfer. The application layer must issue a BTA and return the bus to DSI-TX when it receives this error.
ErrCntLP1	29	**ErrCntLP1 — Contention Detection LP1 Error** This bit is set to 1 when a contention is detected during LP1 transfer.
ErrCntLP0	28	**ErrCntLP0 — Contention Detection LP0 Error** This bit is set to 1 when a contention is detected during LP1 transfer.
Reserved	[27:23]	
L0BTARequest	22	**L0BTARequest－Lane 0 BTA Request** This bit is set to 1 when Direction signal from PPI is changed from 1 (input) to 0 (output).
L0UlpsEscOFF	21	**L0UlpsEscOFF－Lane 0 ULPS OFF** This bit is set to 1 when UlpsActiveNot of lane 0 is deasserted from 0 to 1.
L0UlpsEscON	20	**L0UlpsEscON－Lane 0 ULPS ON** This bit is set to 1 when UlpsActiveNot of lane 0 is asserted from 1 to 0.
L0Trigger	[19:16]	**L0Trigger－Lane 0 Trigger** These bits are set to 1 when corresponding trigger is received. According to MIPI DSI specification [2], DSI-RX may only receive remote application reset trigger. [3] = Unknown-5 “10100000” [2] = Unknown-4 “00100001” [1] = Unknown-3 “01011101” [0] = Reset-Trigger [Remote Application] “01100010”
ErrDsiProtoco	15	**ErrDsiProtocol－DSI Protocol Violation** Flags an error when a MIPI specification violation of following two types is detected. EoT packet is not received before EoT sequence in HS transfer. (It is because EoT packet transfer in LP transfer is not recommended. This error is not detected in LP transfer mode.) BTA is not received though a read request command is received (this condition is not implemented)
Reserved	14	
ErrInvalid	13	**ErrInvalid－Invalid transmission length** Indicates an error is detected that LP-11 is observed before the payload of bytes described in head WC has been received, after a correct packet header is received. The received data before this error is detected is sent to upper layer.
Reserved	12	
ErrDataType	11	**ErrDataType－DSI Data Type Not Recognized** Indicates an error is detected that a packet of undefined Data Type in DSI-RX is received.
ErrCRC	10	**ErrCRC** Indicates CRC errors occur in the received DSI long packets

Field Name	Bit	Description
ErrEccDbl	9	**ErrEccDbl－Ecc Error can not be corrected** Indicates an uncorrectable error is detected in ECC
ErrEccCrctd	8	**ErrEccCrctd－Ecc Error corrected** Indicates a corrected error is detected in ECC.
Reserved	7	
ErrCntrl	6	**ErrCntrl－False Control Error** Indicates an error is detected that LP-10 is not detected after a valid escape sequence or a BTA sequence. Bit[5]： ErrHsRxTo－Hs Rx Time out Error
ErrHsRxTo	5	**ErrHsRxTo－Hs Rx Time out Error** Indicates an error is detected that HS RX timeout period is reached during HS transfer.
ErrSyncEsc	4	**ErrSyncEsc－LP Transmission Sync Error** Indicates an error is detected that the received data is not aligned to byte at the end of LP transfer.
ErrEsc	3	**ErrEsc－Escape Mode Entry Command Error** Indicates an error is detected that an entry command to unknown escape mode is received
ErrEotSyncHs	2	**ErrEotSyncHs－EoT Sync Error** Indicates an error is detected that the last bit of transferred data is not aligned to byte in EoT sequence of HS transfer.
ErrSotSyncHs	1	**ErrSotSyncHs－SoT Sync Error** Indicates an uncorrectable error is detected in SoT sequence of HS transfer.
ErrSotHs	0	**ErrSotHs－SoT Error** Indicates a corrected error is detected in SoT sequence of HS transfer.

6.4.5 DSI_INTMASK Register

Mnemonic	DSI_INTMASK (Adrs = 0x0224)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	MaskRxFifoOvf	MaskLpTxTo	Reserved					
Access	R/W	R/W	---					
Default	1	1	0x30					
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Rsved	MaskL0BTARequest	MaskL0UlpsEscOFF	MaskL0UlpsEscON	MaskL0Trigger[3:0]			
Access	-	R/W						
Default	0	1	1	1	0xF			
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	MaskDsiProtocol	Rsved	MaskInvalid	Rsved	MaskDataType	MaskCrc	MaskEccDbl	MaskEccCrctd
Access	R/W	-	R/W	-	R/W	R/W	R/W	R/W
Default	1	0	1	0	1	1	1	1
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Rsved	MaskCntr	MaskHsRxTo	MaskSyncEsc	MaskEsc	MaskEotSyncHs	MaskSotSyncHs	MaskSotHs
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

NOTE: Please do not change the values in bits 29, 28 and 7

Field Name	Bit	Description
MaskRxFifoOvf	31	**MaskRxFifoOvf—Fifo Overflow Mask** Masks FIFO overflow notification.
MaskLpTxTo	30	**MaskLpTxTo — LP Transmission Timeout Mask** Masks LP TX Timeout error notification.
Reserved	[29:23]	
MaskL0BTARequest	22	**MaskL0BTARequest—Lane 0 BTA Request Mask** Masks BTA request of lane 0.
MaskL0UlpsEscOFF	21	**MaskL0UlpsEscOFF—Lane 0 ULPS OFF Mask** Masks ULPS OFF notification of lane 0.
MaskL0UlpsEscON	20	**MaskL0UlpsEscON—Lane 0 ULPS ON Mask** Masks ULPS ON notification of lane 0.
MaskL0Trigger	[19:16]	**MaskL0Trigger—Lane 0 Trigger Mask** Masks trigger notification of lane 0
MaskDsiProtocol	15	**MaskDsiProtocol—DSI Protocol Violation Mask** This bit needs to be set to mask “EoT packet not received” error if the host device does not support EoT packet
Reserved	14	
MaskInvalid	13	**MaskInvalid—Invalid transmission length Mask** Masks invalid transmission length error notification.
Reserved	12	
MaskDataType	11	**MaskDataType—DSI Data Type Not Recognized Mask** Masks DSI Data Type error notification.
MaskCrc	10	**MaskCRC—CRC Error Mask** Masks CRC error notification
MaskEccDbl	9	**MaskEccDbl—Ecc Error can not be corrected Mask** Masks ECC uncorrectable error notification
MaskEccCrctd	8	**MaskEccCrctd—Ecc Error corrected Mask** Masks ECC correctable error notification.
Reserved	7	
MaskCntrl	6	**MaskCntrl—False Control Error Mask** Masks False Control error notification
MaskHsRxTo	5	**MaskHsRxTo—Hs Rx Time out Error Mask** Masks HS RX timeout notification.
MaskSyncEsc	4	**MaskSyncEsc—LP Transmission Sync Error Mask** Masks LP Transmission Sync Error notification.
MaskEsc	3	**MaskEsc—Escape Mode Entry Command Error Mask** Masks EoT Sync error notification.
MaskEotSyncHs	2	**MaskEotSyncHs—EoT Sync Error Mask** Masks EoT Sync error notification.
MaskSotSyncHs	1	**MaskSotSyncHs—SoT Sync Error Mask** Masksk SoT Sync error notification.
MaskSotHs	0	**MaskSotHs—SoT Error Mask** Masks SoT error notification.

6.4.6 DSI_INTCLR Register

Mnemonic	DSI_INTCLR (Adrs = 0x0228)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	ClrRxFifoOvf	ClrLpTxTo	Reserved					
Access	W	W	---					
Default	0	0	0x00					
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Rsved	ClrL0BTARequest	ClrL0UlpsEscOFF	ClrL0UlpsEscON	ClrL0Trigger[3:0]			
Access	-	W						
Default	0	0	0	0	0x0			
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	ClrDsiProtocol	Rsved	ClrInvalid	Rsved	ClrDataType	ClrCrc	ClrEccDbl	ClrEccCrctd
Access	W	-	W	-	W	W	W	W
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Rsved	ClrCntr	ClrHsRxTo	ClrSyncEsc	ClrEsc	ClrEotSyncHs	ClrSotSyncHs	ClrSotHs
Access	-	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Field Name	Bit	Description
ClrRxFifoOvf	31	**ClrRxFifoOvf—Clear Fifo Overflow** Clears FIFO overflow notification.
ClrLpTxTo	30	**ClrLpTxTo — Clear LP Transmission Timeout** Clears LP TX Timeout error notification.
Reserved	[29:23]	
ClrL0BTARequest	22	**ClrL0BTARequest—Clear Lane 0 BTA Request** Clears BTA request of lane 0.
ClrL0UlpsEscOFF	21	**ClrL0UlpsEscOFF—Clear Lane 0 ULPS OFF** Clears ULPS OFF notification of lane 0.
ClrL0UlpsEscON	20	**ClrL0UlpsEscON—Clear Lane 0 ULPS ON** Clears ULPS ON notification of lane 0.
ClrL0Trigger	[19:16]	**ClrL0Trigger—Clear Lane 0 Trigger** Clears trigger notification of lane 0
ClrDsiProtocol	15	**ClrDsiProtocol—Clear DSI Protocol Violation** Clears DSI protocol violation interrupt.
Reserved	14	
ClrInvalid	13	**ClrInvalid—Clear Invalid transmission length** Clears invalid transmission length error notification.
Reserved	12	
ClrDataType	11	**ClrDataType—Clear DSI Data Type Not Recognized** Clears DSI Data Type error notification.
ClrCrc	10	**ClrCrc—Clear Crc Error** Clears CRC error notification.
ClrEccDbl	9	**CLREccDbl—Clear Ecc Error can not be corrected** Clears ECC uncorrectable error notification
ClrEccCrctd	8	**ClrEccCrctd—Clear Ecc Error corrected** Clears ECC correctable error notification.
Reserved	7	
ClrCntrl	6	**ClrCntrl—Clear False Control Error** Clears False Control error notification
ClrHsRxTo	5	**ClrHsRxTo—Clear Hs Rx Time out Error** Clears HS RX timeout notification.
ClrSyncEsc	4	**ClrSyncEsc—Clear LP Transmission Sync Error** Clears LP Transmission Sync Error notification.
ClrEsc	3	**ClrEsc—Clear Escape Mode Entry Command Error** Clears EoT Sync error notification.
CLREotSyncHs	2	**ClrEotSyncHs—Clear EoT Sync Error** Clears EoT Sync error notification.
ClrSotSyncHs	1	**ClrSotSyncHs—Clear SoT Sync Error** Clearsk SoT Sync error notification.
ClrSotHs	0	**ClrSotHs—Clear SoT Error** Clears SoT error notification.

6.4.7 DSI_LPTXTO Register

Mnemonic	DSI_LPTXO (Adrs = 0x0230)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	LPTXTO[31:24]							
Access	RO							
Default	0xFF							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	LPTXTO[23:16]							
Access	RO							
Default	0xFF							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	LPTXTO[15:8]							
Access	RO							
Default	0xFF							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	LPTXTO[7:0]							
Access	RO							
Default	0xFF							

Field Name	Bit	Description
LPTXTO[31:0]	[31:0]	**LpTxTO — LP Transmission Timeout Value** Specify the LP TX timeout period in SYSCLK cycle. LP TX timeout counter counts by SYSCLK. DSI-RX counts the period in which Direction from PPI is 0 (output) and issues an interrupt ([INTSTATUS].ErrLpTxTo) to the application layer when the counter value reaches LpTxTo.

6.5 DSI General Registers

6.5.1 DSIERRCNT Register

Mnemonic	DSIERRCNT (Adrs = 0x0300)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Err_Mask							
Access	R/W							
Default	0xC0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Err_Mask							
Access	R/W							
Default	0x80							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Overflow	ErrCnt						
Access	RO	RO						
Default	1'b0	0x00						

Field Name	Bit	Description
ERR_MASK	[31:16]	**DSI Error mask** 0: enable 1: mask
Reserved	[15:8]	
Overflow	7	**Overflow** This bit is set is ErrCnt is overflowed. Similar to ErrCnt, It is cleared when it is read
ErrCnt	[6:0]	**DSI Error Count** Error count increment whenever the DSI Rx receives an error as defined in DSI standard. It is cleared after reading by the DSI host or I2C master.

Notes: - Use DSI command to clear the flag:

1. Issues Read command to this register – flag status return and then flag status will be clear after read cycle is completed.

- Use I2C command to clear the flag:

1. Set all DSIERRCNT[31:16] to "1"
2. Issues I2C Read command to this register – flag status return and then flag status will be clear after read cycle is completed.
3. Re-Program DSIERRCNT[31:16] back to its original value.

6.6 DSI Application Layer Registers

6.6.1 Application Layer Control Register

Mnemonic	APLCTRL (Adrs = 0x0400)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved					NOPKTENDMSK	CHKSUMMSK	ECCDBLMSK
Access	RO					R/W	R/W	R/W
Default	0x0					1’b0	1’b0	1’b0

Field Name	Bit	Description
Reserved	31:3	
NOPKTENDMSK	2	No dsapPktEnd error mask 1’b0: mask 1’b1: not mask
CHKSUMMSK	1	Checksum error mask 1’b0: mask 1’b1: not mask
ECCDBLMSK	0	Multi-bit ECC error mask 1’b0: mask 1’b1: not mask

This register is reserved for internal use only.

6.6.2 DSI Read Packet Length Register

Mnemonic	RDPKTLN (Adrs = 0x0404)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved					RDPKTLN		
Access	RO					R/W		
Default	0x00					0x3		

Field Name	Bit	Description
Reserved	31:3	
RDPKTLN	2:0]	DSI Read Packet Size. Configures the number of bytes that 775XBG chip is to return in the DSI read response packet. 3'b000: 1 byte 3'b001: 2 byte 3'b010: 3 byte :: 3'b111: 8 bytes Default is set to 3 (4 bytes) Notes: Must set to 3 when reading 775XBG internal register.

6.7 Video Path Configuration Registers

6.7.1 Video Path Control (VPCTRL)

Mnemonic	VPCTRL (Adrs = 0x0450)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved		VSDELAY[9:4]					
Access	RO		RW					
Default	0x0		0x0					
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	VSDELAY [3:0]				VSPOL	DEPOL	HSPOL	Resvd
Access	RW				RW	RW	RW	RO
Default	0x5				0x0	0x0	0x0	0x0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							OPXLFMT
Access	RO							RW
Default	0x00							0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Resvd			FrameSync	Resvd			MSF
Access	RO			RW	RO			RW
Default	3'b000			1'b0	0x0			0x0

Field Name	Bit	Description
reserved	31:30	
VSDELAY[9:0]	29:20	VSYNC Delay, 1 to 1023. “0” is not allowed
VSPOL	19	Polarity of VSYNC signal. 0: Active low 1; Active high
DEPOL	18	Polarity of DE signal 0: Active high 1; Active low
HSPOL	17	Polarity of HSYNC signal 0: Active low 1; Active high
reserved	16:9	
OPXLFMT	8	Output Pixel Format 1’b0: Selects RGB666 format for output on LVDS link. (default) 1’b1: Selects RGB888 format for output on LVDS link.
Reserved	7:5	
FrameSync	4	Video Timing Gen Enable 1’b0: LineSync mode (default) Register field HTIM2[HFPR] are ignored. New lines starts when VSS/HSS arrives 1’b1: FrameSync mode Starts new lines after counting in HTIM2[HFPR] or the arriving of VSS
Reserved	3:1	
MSF	0	MSF : Magic Square FRC 1’b0: Magic Square is disabled. (default) 1’b1: magic Square is enabled Applicable only when OPXLFMT is set to RGB666 format.

6.7.2 Horizontal Timing Control Register 1 (HTIM1)

Mnemonic	HTIM1 (Adrs = 0x0454)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							HBPR[8]
Access	RO							R/W
Default	0x0							0x0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	HBPR[7:0]							
Access	R/W							
Default	0x4							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							HPW[8]
Access	RO							R/W
Default	0x0							0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	HPW[7:0]							
Access	R/W							
Default	0x8							

Field Name	Bit	Description
Reserved	31:25	
HBPR	24:16	Horizontal Back Porch 9'h1: : 9'h4: Default : 9'h1ff: HBPR Max HBPR = 510 pixel Note: These bits must be multiple of even pixel
Reserved	15:9	
HPW	8:0	Horizontal Pulse Width 9'h8: Default : 9'h1ff: HPW Min HPW = 8, Max HPW = 510 pixel Note: These bits must be multiple of even pixel

6.7.3 Horizontal Timing Control Register 2 (HTIM2)

Mnemonic	HTIM2 (Adrs = 0x0458)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							HFPR[8]
Access	RO							R/W
Default	0x0							0x0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	HFPR[7:0]							
Access	R/W							
Default	0x4							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved					HACT[10:8]		
Access	RO					R/W		
Default	0x0					0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	HACT[7:0]							
Access	R/W							
Default	0xA0							

Field Name	Bit	Description
Reserved	31:25	
HFPR	24:16	Horizontal Front Porch 9'h1: : 9'h4: Default : 9'h1ff: HFPR Max HFPR = 510 pixel Note: These bits must be multiple of even pixel This bit field is used only in FrameSync mode
Reserved	15:11	
HACT	10:0	Horizontal Active video size 11'h1: : 11'ha0: Default : 11'h7ff: HDISPR Max HACT = 2046 pixel VTGEN uses this field to count DE length for both FrameSync and LineSync modes. DE should keep constant at this value and should not drop when VBuf is underflow.

6.7.4 Vertical Timing Control Register 1 (VTIM1)

Mnemonic	VTIM1 (Adrs = 0x045C)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	VBPR[7:0]							
Access	R/W							
Default	0x8							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VPW[7:0]							
Access	R/W							
Default	0x10							

Field Name	Bit	Description
Reserved	31:24	
VBPR[7:0]	23:16	Vertical Back Porch 8'h1: : 8'h08 : Default : 8'hff: VBPR Max VBPR = 255 line
Reserved	15:8	
VPW[7:0]	7:0	Vertical Sync Pulse Width 8'h1: : 8'h10 : Default : 8'hff: VPW Max VPW = 255 line

6.7.5 Vertical Timing Control Register 2 (VTIM2)

Mnemonic	VTIM2 (Adrs = 0x0460)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	VFPR[7:0]							
Access	R/W							
Default	0x8							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved					VACT[10:8]		
Access	RO					R/W		
Default	0x0					0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VACT[7:0]							
Access	R/W							
Default	0xF0							

Field Name	Bit	Description
Reserved	31:24	
VFPR[7:0]	23:16	Vertical Front Porch 8'h1: : 8'h08: Default : 8'hff: VFPR Max VFPR = 255 line
Reserved	15:11	
VACT[10:0]	10:0	Vertical Display Size 11'h1: : 11'hf0: Default : 11'h7ff: VACT Max VACT = 2047 line

6.7.6 Video Frame Timing Upload Enable (VFUEN)

Mnemonic	VFUEN (Adrs = 0x0464)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							VFUEN
Access	RO							W1S
Default	0x0							0x0

Field Name	Bit	Description
Reserved	31:1	
VFUEN	0	Video Frame Timing Upload Enable 0: No action 1: Upload enable After this bit has been written to 1, the chip will upload (copy) the newly programmed video timing parameters (HTIM1, HTIM2, VTIM1, and VTIM2) to the active set of video timing registers at the next VSYNC event. At that point, this bit will also be automatically cleared by hardware. This register must be programmed after the above video timing parameters have been programmed.

6.7.7 LVDS-TX Mux Input Select Control Register (LVMX0003)

Mnemonic	LVMX0003 (Adrs = 0x0480)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved			LVMX03[4:0]				
Access	RO			R/W				
Default	0x0			0x05				
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved			LVMX02[4:0]				
Access	RO			R/W				
Default	0x0			0x04				
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved			LVMX01[4:0]				
Access	RO			R/W				
Default	0x0			0x03				
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved			LVMX00[4:0]				
Access	RO			R/W				
Default	0x0			0x02				

Field Name	Bit	Description
Reserved	31:30	
LVMX03[4:0]	29:24	LVDS-TX Input 3 mux select control
Reserved	23:21	
LVMX02[4:0]	20:16	LVDS-TX Input 2 mux select control
Reserved	15:13	
LVMX01[4:0]	12:8	LVDS-TX Input 1 mux select control
Reserved	7:5	
LVMX00[4:0]	4:0	LVDS-TX Input 0 mux select control

Other registers, LVMX0407… to LVMX2427 are structured similarly.

There are 28 inputs to LVDS-TX transmitter, each of which is fed by one of 28 possible input signals R0-R7, G0-G7, B0-B7, HSYNC, VSYNC, DE, and RSV; the selection of such inputs is controlled by the collection of mux select control registers here. For each input i to LVDS-TX, the value of corresponding mux select control LVMXi [4:0] is defined as follows:

Value of LVMXi [4:0]	Assigned Meaning
0	Selects input R0
1	Selects input R1
2	Selects input R2
3	Selects input R3
4	Selects input R4
5	Selects input R5
6	Selects input R6
7	Selects input R7
8	Selects input G0
9	Selects input G1
10	Selects input G2
11	Selects input G3
12	Selects input G4
13	Selects input G5
14	Selects input G6
15	Selects input G7
16	Selects input B0
17	Selects input B1
18	Selects input B2
19	Selects input B3
20	Selects input B4
21	Selects input B5
22	Selects input B6
23	Selects input B7
24	Selects input HSYNC
25	Selects input VSYNC
26	Selects input DE
27	Selects logic 0
28 – 31	Undefined

The register default values are summarized here:

LVDS Mux Input Select Control Register Default Values			
Adrs	**Register**	**Description**	**Default Value**
0x0480	LVMX0003	Mux Input Select for LVDS LINK Input Bit 0 to 3	0x0504_0302
0x0484	LVMX0407	Mux Input Select for LVDS LINK Input Bit 4 to 7	0x0A07_0106
0x0488	LVMX0811	Mux Input Select for LVDS LINK Input Bit 8 to 11	0x0908_0C0B
0x048C	LVMX1215	Mux Input Select for LVDS LINK Input Bit 12 to 15	0x120F_0E0D
0x0490	LVMX1619	Mux Input Select for LVDS LINK Input Bit 16 to 19	0x1413_1110
0x0494	LVMX2023	Mux Input Select for LVDS LINK Input Bit 20 to 23	0x1B17_1615
0x0498	LVMX2427	Mux Input Select for LVDS LINK Input Bit 24 to 27	0x001A_1918

6.8 LVDS Configuration Registers

6.8.1 LVDS Configuration Register (LVCFG)

Mnemonic	LVCFG (Adrs = 0x049C)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved				PCLKSEL		Reserved	
Access	RO				R/W		RO	
Default	0x00				0x2		0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	PCLKDIV				Reserved		LVLINK	LVEN
Access	R/W				RO		R/W	R/W
Default	0x2				0x0		0x0	0x0

Field Name	Bit	Description
Reserved	31:12	
PCLKSEL	11:10	PCLK Selection 2'b00: DCLK = HSRCK (DSI_CLK) 2'b01: DCLK = HbyteHSClkx2 (DSI_CLK / 2) 2'b10: DCLK = ByteHsClk (DSI_CLK / 4) 2'b11: Reserved Note: These bits only used if EXTCLK is not available (LOW)
Reserved	9:8	
PCLKDIV	7:4	PCLK Divide Option (Divide down from DCLK to generate PCLK) 0: divide by 16 1: divide by 1 2: divide by 2 . . 15: divide by 15 Note: These bits only used if EXTCLK is not available (LOW)
Reserved	3:2	
LVDLINK	1	Configures LVDS transmitter as single or dual link. 0: Single-link LVDS transmitter 1: Dual-link LVDS transmitter
LVEN	0	Enables the LVDS transmitter. 0: LVDS transmitter is disabled. Its outputs are tri-stated. (default) 1: LVDS transmitter is enabled.

6.8.2 LVDS PHY Register 0 (LVPHY0)

Mnemonic	LVPHY0 (Adrs = 0x04A0)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved	LV_DIREN		LV_DIRIN				
Access	RO	R/W		R/W				
Default	0x0	0x0		0x0				
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved	LV_RST	LV_PRBSEN	LV_PRBS_ON				
Access	RO	R/W	R/W	R/W				
Default	0x0	0x0	0x0	0x04				
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	LV_IS		LV_MEAS	LV_HIZ	LV_EREN	LV_REN	LV_PRD	LV_BP
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Default	0x1		0x0	0x0	0x0	0x0	0x0	0x1
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	LV_FS		LV_ND				
Access	RO	R/W		R/W				
Default	0x0	0x0		0x6				

Field Name	Bit	Description
Reserved	31	
LV_DIREN	30:29	Direct Input Enable 2'b00: Normal operation 2'b01: PLL X7 Output 2'b10: "0" Fix 2'b11: DIRIN Output
LV_DIRIN	28:24	Test Signal Direct Input Pins Via only LVDS-Tx buffer
Reserved	23	
LV_RST	22	LV PHY reset 0: Normal 1: Reset
LV_PRBSEN	21	PRBS Pattern enable 0: Normal operation 1:PRBS Pattern input
LV_PRBS_ON	20:16	Clock/Data Flag Pins (with LV_PRBSEN ="1") (5 bits) 0: Clock Channel (Input Signal select) 1: Data Channel (PRBS signal select)
LV_IS	15:14	Charge pump current control pin for PLL portion 2'b00: X0.76 2'b01: X1 (Default) 2'b10: X1.5 2'b11: X3
LV_MEAS	13	Bang Gap voltage monitor 0: Normal Mode 1: measured through the VMID
LV_HIZ	12	Output Tristate 0: Normal output mode 1: Hi-Z output
LV_EREN	11	External Reference Enable 0: Normal operation External Reference (1.2V) ON (through the VMID)
LV_REN	10	Output Range select 0: Normal Range 1: Reduced Range
LV_PRD	9	Input Pre-Divider 0: Normal Mode (25Mhz – 85MHz) 1/1 dividing 1: Hi Frequency TEST mode ½ dividing
LV_BP	8	Bypass PLL clock 0: Normal operation mode (PLL clock input for p2s) 1: Bypass mode (outer clock direct input for p2s) – PLL Power Down Mode
Reserved	7	
LV_FS	6:5	Frequency Range Select (Output Divider Ratio) 2'b00: 60MHz – 85MHz 2'b01: 30MHz – 70MHz 2'b10: 25MHz – 35MHz 2'b11: Reserved
LV_ND	4:0	Frequency Range Select (Feed Back Divider Ratio)

Field Name	Bit	Description
		5'b01101: 85MHz ~ 5'b00110: 60MHz – 85MHz (Default) 5'b01101: 30Mhz – 70MHz 5'b11011: 25MHz – 35MHz Others: Reserved

6.8.3 LVDS PHY Register 1 (LVPHY1)

Mnemonic	LVPHY1 (Adrs = 0x04A4)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				LV_TEST			
Access	RO				R/W			
Default	0x0				0x0			

Field Name	Bit	Description
Reserved	[31:4]	
LV_TEST	[3:0]	0: Normal operation 1: PLL TEST Mode

6.9 System Registers

6.9.1 SYS Status Register

Mnemonic	SYSSTAT (Adrs = 0x0500)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved		I2CBERR					
Access	RO		RO					
Default	0x0		0x0					
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved		ERRID					
Access	RO		RO					
Default	0x0		0x00					
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved						VCERR	PKTERR
Access	RO						RO	RO
Default	0x0						0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved		I2CERR	I2CBUSY	Reserved	CQOVF	VBOVF	VBUNF
Access	RO		RO	RO	RO	RO	RO	RO
Default	0x0		0x0	0x0	0x00	0x0	0x0	0x0

Field Name	Bit	Description
Reserved	31:30	
I2CBERR	29:24	I2C Byte Error Byte position in the message when first NACK was received from i2C slave Note: See I2C master section for more description
Reserved	23:22	
ERRID	21:16	Un-Supported Packet ID This field is valid only when PKTERR is asserted
Reserved	15:10	
VCERR	9	Un-supported VC number This bit is asserted when receiving DSI Packets with VC field other than 0
PKTERR	8	Un-supported DSI Packets This bit is asserted when receiving Un-supported DSI Packets after application layer decodes Packet ID. The unsupported packet ID is reported in the ERRID field in this register.
Reserved	7:6	
I2CERR	5	I2C NACK error status 0: No error 1: Error – NACK received I2CBERR indicates the first byte position of the NACK byte.
I2CBUSY	4	I2C Port Busy 0: I2C port is done/idle 1: I2C port is in busy
Reserved	3	
CQOVF	2	Command Queue Overflow flag Note: Reading this register will clear this flag
VBOVF	1	Video Buffer Overflow flag Note: Reading this register will clear this flag
VBUNF	0	Video Buffer Underflow flag Note: Reading this register will clear this flag

Notes:

- Use DSI command to clear the flag:
  1. Issues Read command to this register – status return and then flag status will be clear after read cycle is completed.
- Use I2C command to clear the flag:
  1. Set all DSIERRCNT[31:16] to “1”
  2. Issues I2C Read command to this register – status return and then flag status will be clear after read cycle is completed.
  3. Re-Program all DSIERRCNT[31:16] back to its original value.

6.9.2 SYS Reset Register

Mnemonic	SYSRST (Adrs = 0x0504)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Access	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Access	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Access	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		RSTREG	RSTDSIRX	RSTBM	RSTLCD	RSTI2CM	RSTI2CS
Access	RO		W1C	W1C	W1C	W1C	W1C	W1C
Default	0x0		0x0	0x0	0x0	0x0	0x0	0x0

Field Name	Bit	Description
Reserved	31:6	
RSTREG	5	Software reset for Register (REG) module which includes all registers excluding DSI D-PHY, DSI PPI Layer, and DSI Protocol Layer registers
RSTDSIRX	4	Software reset for DSI-RX and Application controller
RSTBM	3	Software reset for Bus Management (BM) controller
RSTLCD	2	Software reset for LCD controller Notes: This will also reset LVDS-PHY and Video Line Buffer (VB)
RSTI2CM	1	Software reset I2C-Master controller and Data Queue (DQ) module
RSTI2CS	0	Software reset I2C-Slave controller 0: Normal (default) 1: Reset This bit is meaningful only when written to from DSI link, and is useful only as a chip debugging aide.

Note: All software reset bits are “W1C” type. Host only needs to write “1” to issue the reset command. Reading this register always returns 0.

6.10 GPIO Registers

6.10.1 GPIO Control Register

Mnemonic	GPIOC (Adrs = 0x0520)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				GPC[3:0]			
Access	RO				R/W			
Default	0x0				0x0			

Field Name	Bit	Description
Reserved	31:4	
GPC[3:0]	3:0	GPIO direction mode control 0: Input mode 1: Output mode

6.10.2 GPIO Output Register

Mnemonic	GPIOO (Adrs = 0x0524)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				GPO[3:0]			
Access	RO				R/W			
Default	0x0				0x0			

Field Name	Bit	Description
Reserved	31:4	
GPO[3:0]	3:0	GPIO Output data Value of this register will output to the GPIOx pins if the GPIOx select to be in OUTPUT mode

6.10.3 GPIO Input Register

Mnemonic	GPIOI (Adrs = 0x0 528)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				GPI[3:0]			
Access	RO				RO			
Default	0x0				0X			

Field Name	Bit	Description
Reserved	31:4	
GPI[3:0]	3:0	GPIO Input data Value of this register reflects the state of GPIOx pins (after a couple of synchronization clock delays.)

6.11 I2C Registers

6.11.1 I2C Timing Control and Enable Register

Mnemonic	I2CTIMCTRL (Adrs = 0x0540)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							I2CMEN
Access	RO							R/W
Default	0x0							0x0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	SCLTIME							
Access	RW							
Default	0x80							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved						SCL_Str	SDA_Str
Access	RO						R/W	R/W
Default	0x00						0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	I2CSCCTL[7:0]							
Access	R/W							
Default	0x80							

Field Name	Bit	Description
Reserved	31:25	
I2CMEN	24	I2C Master Enable 0: Disable 1: Enable
SCLTIME[7:0]	23:16	I2C Master interface SCL clock pulse control. Set SCLTIME such that, SCLTIME = $\frac{\text{DSI CLOCK frquency}}{20 \text{ x SCL frequency}}$ -1
Reserved	15:10	
SCL_Str	9	I2C SCL Output Signal Strength 1'b0: 4mA IO strength (Default) 1'b1: 8mA IO strength
SDA_Str	8	I2C SDA Output Signal Strength 1'b0: 4mA IO strength (Default) 1'b1: 8mA IO strength
I2CSCCTL[7:0]	7:0	I2C Slave interface SCL clock low control This field is used to define the period between the first valid read data bit on SDA and SCL low to high transition. SCL low period = I2CCLKCTL * i2c_clk. Value 0 is invalid and will result in undefined behaviour.

6.11.2 I2C Master Address Register

Mnemonic	I2CMADDR (Adrs = 0x0544)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved						I2CSB	I2CASEL
Access	RO						R/W	R/W
Default	0x0						0x0	0x0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved						I2CADD[9:8]	
Access	RO						R/W	
Default	0x0						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	I2CADD [7:0]							
Access	R/W							
Default	0x00							

Field Name	Bit	Description
Reserved	31:18	
I2CSB	17	I2C Start Byte Transfer 0: No Start Byte send at beginning of I2C transfer 1: Start Byte (8'b0000_0001) at beginning of I2C transfer
I2CASEL	16	I2C Master addressing mode Select 0: 7 bit addressing 1: 10 bit addressing
Reserved	15:10	Reserved
I2CADD[9:0]	9:0	I2C Master Address Parameter - I2CADD[6:0] used for 7-bit Addressing - I2CADD[9:0] used for 10-bit Addressing

6.11.3 WDATAQ Register

Mnemonic	WDATAQ (Adrs = 0x0548)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	WDATAQ[31:24]							
Access	WO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	WDATAQ[23:16]							
Access	WO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	WDATAQ[15:8]							
Access	WO							
Default								
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	WDATAQ[7:0]							
Access	WO							
Default								

Field Name	Bit	Description
WDATAQ	31:0	Write Data Queue Register This register is the Write data queue address Write to this register, the data goes to data queue

6.11.4 RDATAQ Register

Mnemonic	RDATAQ (Adrs = 0x054A)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	RDATAQ[31:24]							
Access	WO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	RDATAQ[23:16]							
Access	WO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	RDATAQ[15:8]							
Access	WO							
Default								
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	RDATAQ[7:0]							
Access	WO							
Default								

Field Name	Bit	Description
RDATAQ	31:0	Read Data Queue Register This register is the Read data queue address /offset Write to this register, the data goes to data queue

6.12 Chip ID/Revision Registers

6.12.1 Chip ID and Revision Register

Mnemonic	IDREG (Adrs = 0x0580)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	CHIPID[7:0]							
Access	RO							
Default	0x75							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	REVID							
Access	RO							
Default	0x00							

Field Name	Bit	Description
Reserved	31:16	
ChipID[7:0]	15:8	Chip ID 8'h75 (775XBG)
REVID[7:0]	7:0	Revision ID 8'h00

6.13 Debug Registers

These registers are for internal use only, for debug purpose.

6.13.1 Debug00 Register

Mnemonic	DEBUG00 (Adrs = 0x05A0)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved				LPRx_TM[1:0]		HSRx_TM[1:0]	
Access	RO				R/W		R/W	
Default	0x00				0x0		0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				ENI2CFILTER	Resvd	CLK_MON	Resvd
Access	RO				R/W	RO	R/W	R/W
Default	0x00				0x1	0x0	0x0	0x0

Field Name	Bit	Description
Reserved	31:12	
LPRx_TM	11:10	Production Test Mode : Select DSI Rx LP outputs to GPIO[1:0] 2'b00: D0P_out/D0M_out to GPIO1/GPIO0 2'b01: D1P_out/D1M_out to GPIO1/GPIO0 2'b10: D2P_out/D2M_out to GPIO1/GPIO0 2'b11: D3P_out/D3M_out to GPIO1/GPIO0
HSRx_TM	9:8	Production Test Mode : Select DSI Rx HS outputs to GPIO0 2'b00: Lane 3 Parity 2'b01: HSCKBY2 2'b10: HSCKBY4 2'b11: don't care
Reserved	7:4	
ENI2CFILTER	3	Enable I2C Filter 0: Disable 1: Enable
Reserved	2	
CLK_MON	1	Monitor clock (Debug only) 0: Normal 1: DSI byte clock and External clock are brought out to GPIO0 and GPIO1 respectively.
Reserved	0	

6.13.2 DEBUG01 Register

Mnemonic	DEBUG01 (Adrs = 0x05A4)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Access	RO							
Default	0x0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved		clk_c_sel	tm_lvds_ch_en				
Access	RO		R/W	R/W				
Default	0x0		0x0	0x1F				
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Shiften	LVDS_Data						
Access	R/W	R/W						
Default	0	0x63						

Field Name	Bit	Description
Reserved	31:14	
clk_c_sel	13	Clock on Channel C This bit selects if clock is to be output on channel C instead of the default channel D 1: output clock to physical channel C and data to physical channel D 0: output clock to physical channel D and data to physical channel C
tm_lvds_ch_en	[12:8]	Select channel enable This bus may only be used in LVDS test mode and controls the channel enable to LVDSPHY
Shiften	7	Shiften This bit enables the data register to behave as a shift register where LVDS_Data[6] is shifted into LVDS_Data[0]
LVDS_Data	6:0	LVDS Test data Data in this register is clocked to LVDS PHY during LVDS PHY Testmode for all links.

6.13.3 Debug02 Register

Mnemonic	DEBUG02 (Adrs = 0x05A8)							
Bit	**B31**	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
Name	WC[15:8]							
Access	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	WC[7:0]							
Access	RO							
Default	0x00							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	DataID[7:0]							
Access	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						ErrHD	LatchHD
Access	RO						RW	RW
Default	0x0						0	0

Field Name	Bit	Description
WC	[31:16]	**Word Count Field of DSI Packet** This Field is updated for each packet received. It stops updating when ErrHD or LatchHD is asserted as described below
DataID	[15:8]	**Packet Data Typ** This Field is updated for each packet received. It stops updating when ErrHD or LatchHD is asserted as described below
Reserved	[7:2]	
ErrHD	1	**Packet Error** When asserted HW latches the first erroneous Packet (as shown in register DSI_INTSTATUS) Data ID and WC in the bits [31:8]
LatchHD	0	**Latch Header Bytes** When asserted, HW stop latch packet Data ID and WC in the bits [31:8] for debugging purpose

Note:

1. When LatchHD is 1 (regardless what ErrHD is), hardware stops updating the packet header info.
2. When LatchHD is 0 and ErrHD is 1, hardware stops updating the packet header info when the INTSTATUS generates an interrupt internally.
   In order for an interrupt to be generated internally, the interrupt mask register DSI_INTMASK (addr 0x0224) must be programmed to unmask the event one would want to watch for.
3. When LatchHD is 0 and ErrHD is 0, hardware keeps updating the packet header info without stopping.
   Please note that because of synchronization issue, the stored packet header info cannot reflect every single packet header that is received on the fly if the incoming packets are faster than the synchronization scheme. But hardware guarantees that what is read from this register reflects accurately one of the packet headers that is received by D2LLP.

7 Package

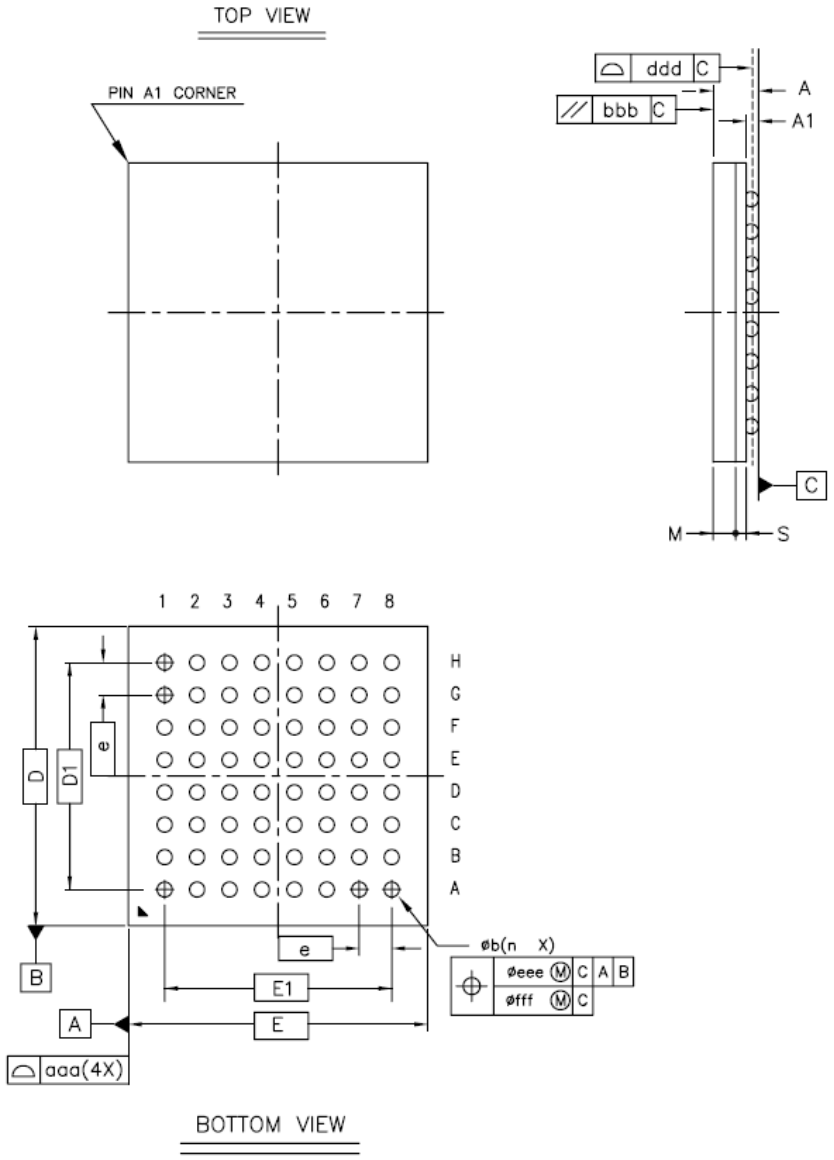

Figure 7-1 P-TFBGA64-0606-0.65AZ (TC358775XBG) Package Drawing

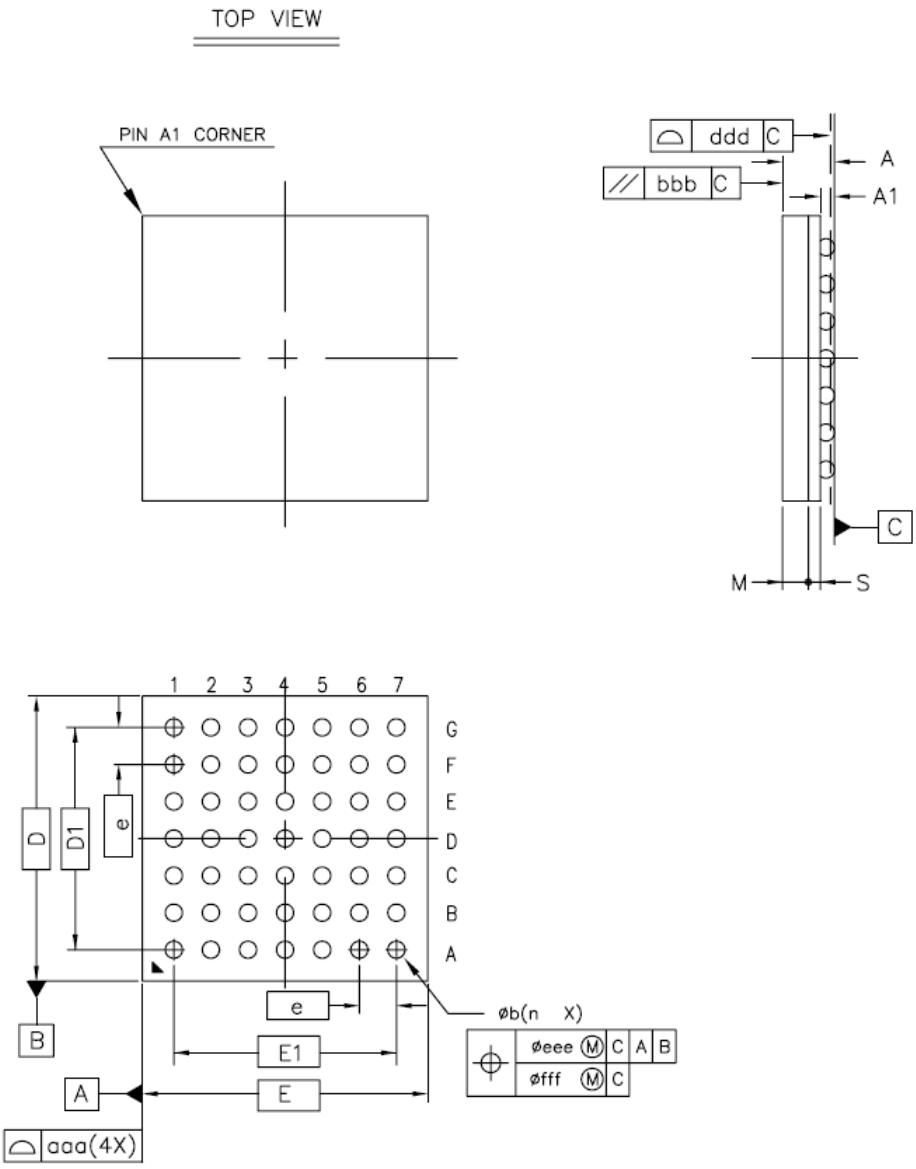

Figure 7-2 P-TFBGA49-0505-0.65AZ (774XBG) Package Drawing

Table 7-1 Information Summary

	775VBG Package	774 XBG Package
Package Type	VFBGA	VFBGA
Ball Diameter	0.3 mm	0.3mm
Ball Pitch (e)	0.65 mm	0.65 mm
Edge Ball center to center (E1 x D1)	4.55 mm x 4.55 mm	3.90 mm x 3.90 mm
Body Size (E x D)	6 mm x 6 mm	5 mm x 5 mm
Thickness (A)	1 mm	1 mm

8 Electrical characteristics

8.1 Absolute Maximum Ratings

Operating ambient Temperature range: Ta = -30**°C** - +85**°C**

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Table 8-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	-0.3 ~ +3.9 (??)	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 ~ +1.8	V
Supply voltage (1.2V – MIPI DSI PHY)	VDD_MIPI	-0.3 ~ +1.8	V
Supply voltage (1.8V – LVDS PHY)	VDD_LVDS1_18, VDD_LVDS2_18	-0.3 ~ +LVDS_18+0.3 (??)	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS1_12 VDD_LVDS2_12	-0.3 ~ +1.8	V
Input voltage (DSI I/O)	V_{IN_DSI}	-0.3 ~ VDD_MIPI+0.3	V
Output voltage (DSI I/O)	V_{OUT_DSI}	-0.3 ~ VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 ~ VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 ~ VDDIO+0.3	V
Output voltage (LVDS Driver)	V_{OUT_LVDS}	-0.3 ~ VDD_LVDS_18+0.3	V
Junction temperature	T_j	105	°C
Storage temperature	T_{stg}	-40 ~ +85	°C

8.2 Recommended Operating Conditions

Table 8-2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.7	1.8	1.9	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS_12	1.1	1.2	1.3	V
Supply voltage (1.8V – LVDS PHY)	VDD_LVDS_18	1.7	1.8	1.9	V
Supply voltage (1.2V – MIPI-DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T_a	-30	+25	+85	°C
Supply Noise Voltage	V_{SN}			100	mV_{pp}

8.3 DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

8.3.1 Normal CMOS I/Os DC Specifications

Table 8-3 Normal CMOS IOs DC Specifications

Parameter – CMOS I/Os	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage, High level Input Note1	V_{IH}		0.7 VDDIO	-	VDDIO	V
Input voltage, Low level Input Note1	V_{IL}		0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note 1,2	V_{IHS}		0.7 VDDIO		VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note 1,2	V_{ILS}		0		0.3 VDDIO	V
Output voltage, Low level Note1, 2	V_{OL}	I_{OL} = 2mA	0	-	0.2 VDDIO	V
Input leakage current, High level on Normal pin or Pull-up I/O pin	I_{ILH1} (Note4)	V_{IN} = +VDDIO, VDDIO = 3.6V	-10	-	10	µA
Input leakage current, High level on Pull-down I/O pin	I_{ILH2} (Note4)	V_{IN} = +VDDIO, VDDIO = 3.6V	-	-	100	µA
Input leakage current, Low level On Normal pin or Pull-down I/O pin	I_{ILL1} (Note5)	V_{IN} = 0V, VDDIO = 3.6V	-10	-	10	µA
Input leakage current, Low level On Pull-up I/O pin	I_{ILL2} (Note5)	V_{IN} = 0V, VDDIO = 3.6V	-	-	-200	µA

- Note1: Each power source is operating within recommended operating condition.
- Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.
- Note4: Normal pin or Pull-up I/O pin applied VDDIO supply voltage to Vin（input voltage）
- Note5: Normal pin, or Pull-down I/O pin applied VSSIO (0V) to Vin（input voltage）

8.3.2 DSI Differential I/Os DC Specifications

8.3.2.1 LP Transmitter

The low power transmitter is used for driving the lines in all low-power operating modes. The DC characteristics of the LP transmitter are given below.

Table 8-4 DSI LP Transmitter DC Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thevenin output low level	V_{OL}	-50	-	50	mV
Output impedance of the LP transmitter	Z_{OLP}	110			Ohm

8.3.2.2 HS Receiver

The high-speed receiver is a differential line receiver with a switch able parallel input termination. It is used to receive data during high speed transmission from the host. The DC characteristics of the HS receiver are given below.

Table 8-5 DSI HS Receiver DC Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70		330	mV
Differential input high threshold	V_{IDTH}			70	mV
Differential input low threshold	V_{IDTL}	-70			mV
Single-ended input high voltage	V_{IHHS}			460	mV
Single-ended input low voltage	V_{ILHS}	-40			mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$			450	mV
Differential input impedance	Z_{ID}	80	100	125	Ohm

8.3.2.3 LP Receiver

The low-power receiver is used to detect the Low-Power state on each pin. It is used to receive data during low speed transmission from the host. The DC characteristics of the LP receiver are given below.

Table 8-6 DSI LP Receiver DC Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic 1 input voltage	V_{IH}	880			mV
Logic 0 input voltage	V_{IL}			550	mV

8.3.3 LVDS Transmitter DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit

$\|V_{OD}\|$	Output differential voltageNormal	RLOAD = 100Ω±1%	150	300	450	mV
$\|V_{OD}\|$	Output differential voltage Reduced	RLOAD = 100Ω±1%	115	180	300	mV
ΔV_{OD}	Change in |VOD| between “0”and “1”	RLOAD = 100Ω±1%	-	-	30	mV
V_{OS}	Output offset voltage	RLOAD = 100Ω±1%	800	900	1000	mV
ΔV_{OS}	Change in VOS between “0”and “1”	RLOAD = 100Ω±1%	-	-	25	mV
I_{sab}	Output current	Driver shorted together	-	-	12	mA
I_{sab}, I_{sb}	Output current	Driver shorted to ground	-	-	30	mA

8.4 AC Characteristics

All typical values are at normal recommended operating conditions unless otherwise specified.

8.4.1 DSI Differential I/Os AC Specifications

8.4.1.1 DSI LP Transmitter

Table 8-7 DSI LP Transmitter AC Specifications

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
15%-85% rise time and fall time	T_{RLP} / T_{FLP}				25	ns
Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRaiL}$ period to start of LP-11 state	T_{EOT}				105 ns + n*12*UI	
Minimum LP pulse width of the EXOR clock	T_{MIN-TX}		20			ns
Slew rate, C_{LOAD} = 0-5 pF	dV/dt_{SR}				500	mV/ns
Slew rate, C_{LOAD} = 5-20 pF					200	mV/ns
Load Capacitance	CLOAD		0		70	pF

8.4.1.2 DSI HS Receiver

Table 8-8 DSI HS Receiver AC Specifications

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$				100	mV
Common-mode interference beyond 450MHz	$\Delta V_{CMR(LF)}$		-50		50	mV
Common-mode termination	CCM				60	pF

Notes:

1) $T_{HS-EXIT}$ is min 100ns in MIPI DSI spec, but in DSI2LVDS it is required to be greater than (8 x DSICLK + 10ns).

If DSICLK >= 88MHz, DSI2LVDS is working properl

If DSICLK < 88MHz, DSI-TX need to extend the $T_{HS-EXIT}$ timing to meet DSI2LVDS requirement.

2) MIPI Spec: Required $T_{HS-TRAIL}$ > max (8xUI, 60 ns + 4xUI)

DSI2LVDS: Required $T_{HS-TRAIL}$ > max (12xUI, 60 ns + 4xUI)

If DSICLK >= 67 MHz, DSI2LVDS is working properly

If DSICLK > 67 MHz, DSI-TX need to extend $T_{HS-TRAIL}$ to meet DSI2LVDS requirement.

3) When DSICLK used as Pixel clock source, Maximum Phase jitter (peak-to-peak) allowed is 40ps.

8.4.1.3 DSI LP Receiver

Table 8-9 DSI LP Receiver AC Specifications

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Input pulse rejection	e_{SPIKE}				300	V*ps
Minimum pulse width response	T_{MIN_RX}		20			ns
Peak interference amplitude	V_{INT}				200	mV
Interference frequency	f_{INT}		450			MHz

8.4.2 LVDS Transmitter AC Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low to High transition time	T_r	100	0	500	ps
High to Low transition time CLKIN(Input Clock) High Time	T_f T_{ch}	100 0.4 T_C	- 0.5 T_C	500 0..6 T_C	ps ns
CLKIN(Input Clock) Low Time	T_{cl}	0.4 T_C	0.5 T_C	0.6 T_C	ns

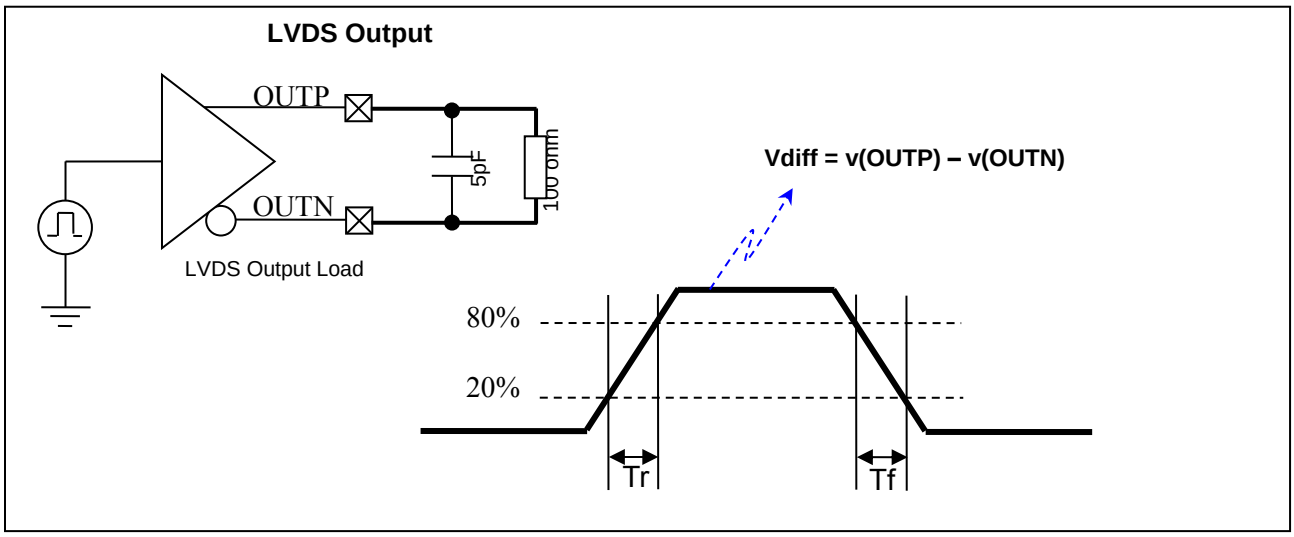

Figure 8-1 Transmitter Output Transition Timing Diagram

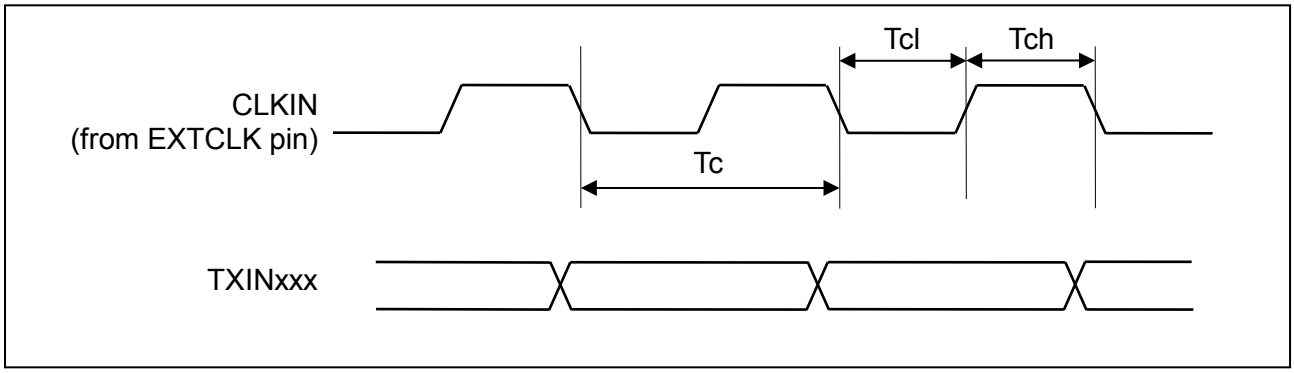

Figure 8-2 Input Clock AC Timing Diagram

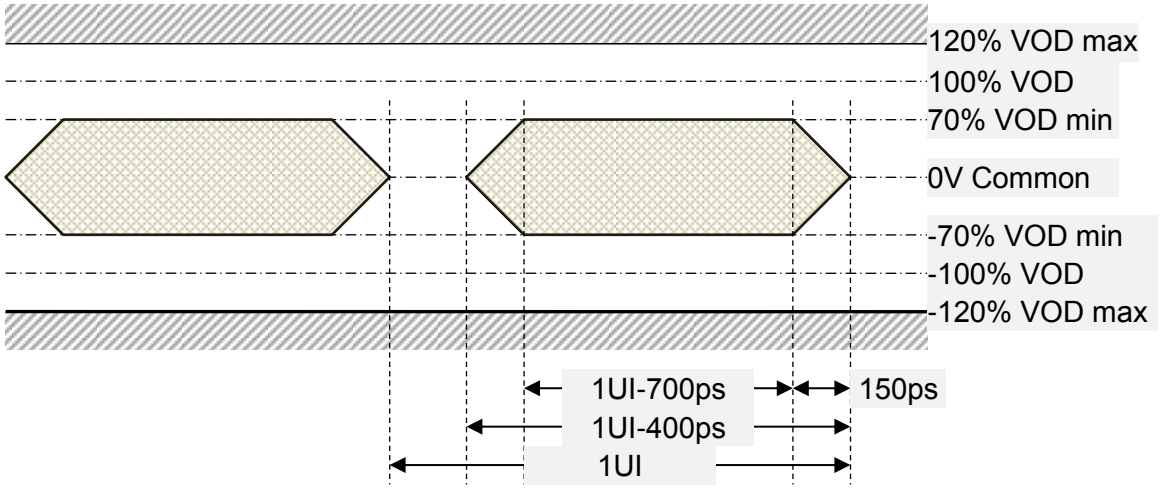

Figure 8-3 LVDS Output AC Characteristics (Output Eye)

Table 8-10 LVDS Switching Characteristics (Clock Frequency ≧ 50 MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T0 *1	Delay time, TCLK rising edge to serial bit position 0.	–0.20	0	+0.20	ns
T1 *1	Delay time, TCLK rising edge to serial bit position 1.	1/7*TC – 0.20	1/7*TC	1/7*TC + 0.20	ns
T2 *1	Delay time, TCLK rising edge to serial bit position 2.	2/7*TC – 0.20	2/7*TC	2/7*TC + 0.20	ns
T3 *1	Delay time, TCLK rising edge to serial bit position 3.	3/7*TC – 0.20	3/7*TC	3/7*TC + 0.20	ns
T4 *1	Delay time, TCLK rising edge to serial bit position 4.	4/7*TC – 0.20	4/7*TC	4/7*TC + 0.20	ns
T5 *1	Delay time, TCLK rising edge to serial bit position 5.	5/7*TC – 0.20	5/7*TC	5/7*TC + 0.20	ns

T6 *1	Delay time, TCLK rising edge to serial bit position 6.	6/7*TC – 0.20	6/7*TC	6/7*TC + 0.20	ns
TC *2	TCLK clock period.	9.52		20	ns

Notes: *1: without Input clock jitter *2: without Output Clock jitter

Table 8-11 LVDS Switching Characteristics (Clock Frequency < 50 MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T0 *1	Delay time, TCLK rising edge to serial bit position 0.	–0.2*UI	0	+0.2*UI	ns
T1 *1	Delay time, TCLK rising edge to serial bit position 1.	1/7*TC – 0.2*UI	1/7*TC	1/7*TC + 0.2*UI	ns
T2 *1	Delay time, TCLK rising edge to serial bit position 2.	2/7*TC – 0.2*UI	2/7*TC	2/7*TC + 0.2*UI	ns
T3 *1	Delay time, TCLK rising edge to serial bit position 3.	3/7*TC – 0.2*UI	3/7*TC	3/7*TC + 0.2*UI	ns
T4 *1	Delay time, TCLK rising edge to serial bit position 4.	4/7*TC – 0.2*UI	4/7*TC	4/7*TC + 0.2*UI	ns
T5 *1	Delay time, TCLK rising edge to serial bit position 5.	5/7*TC – 0.2*UI	5/7*TC	5/7*TC + 0.2*UI	ns
T6 *1	Delay time, TCLK rising edge to serial bit position 6.	6/7*TC – 0.2*UI	6/7*TC	6/7*TC + 0.2*UI	ns
TC *2	TCLK clock period.	20		40	ns

Notes: *1: without Input clock jitter *2: without Output Clock jitter

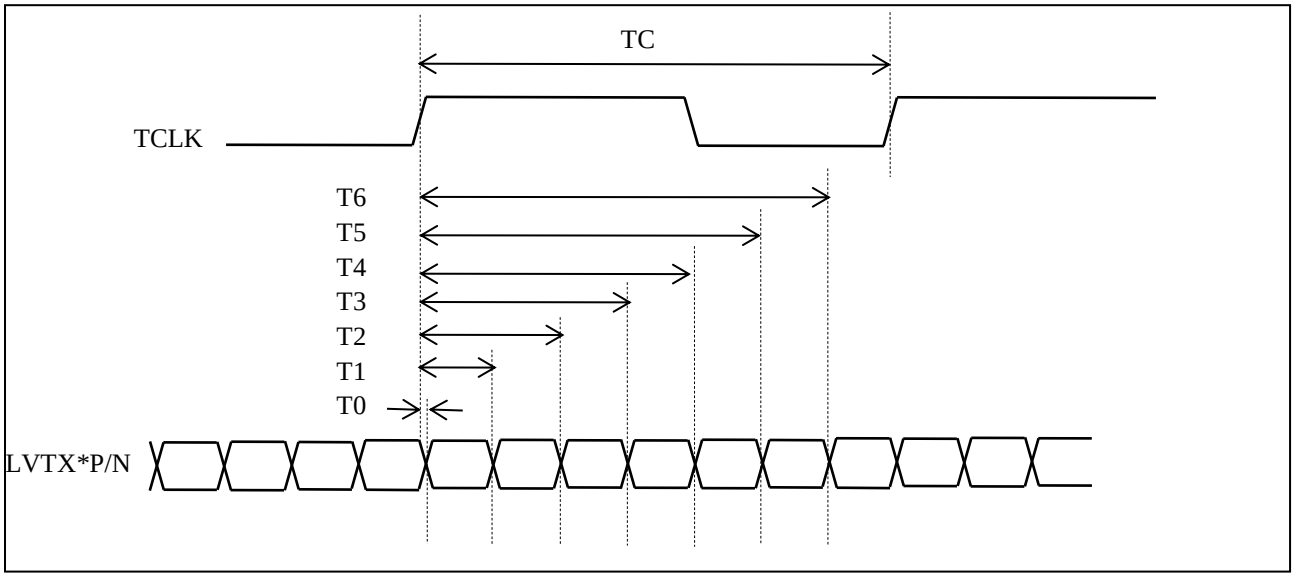

Figure 8-4 LVDS Switching Timing Definition

8.4.3 EXTCLK Clock Input Requirements

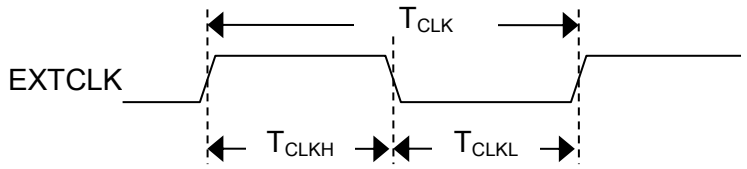

Figure 8-5 EXTCLK Clock Input Timing

Table 8-12 EXTCLK Clock Input Requirements

Description	Parameter	Min.	Typ.	Max.	Units
EXTCLK clock frequency	f_{CLK}	25	-	135	MHz
EXTCLK High level period	t_{CLKH}	40		60	%
EXTCLK Low level period	t_{CLKL}	40		60	%
EXTCLK phase jitter, peak-to-peak	$t_{Jitter-pp}$			40	ps

Note1: Clock amplitude should satisfy input voltage level requirement defined by 8.3.1 Normal CMOS I/Os DC Specifications

8.4.4 Reset Timing

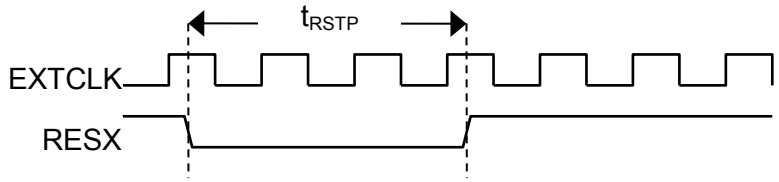

Figure 8-6 RESET input timing

Description	Parameter	Min.	Typ.	Max.	Units
Period of Reset signal	t_{RSTP}	50	-	-	nsec

8.4.5 Power Supply On and Off Sequence

STBY pin exhibits IO gated control, which controls the desired power on sequence and reset to TC358775. This internal power on sequence gives the system designer the flexibility to power on either 1.2V or 1.8V first as shown in Figure 8-7.

It is recommended to assert STBY before turning of the power source to TC358775.

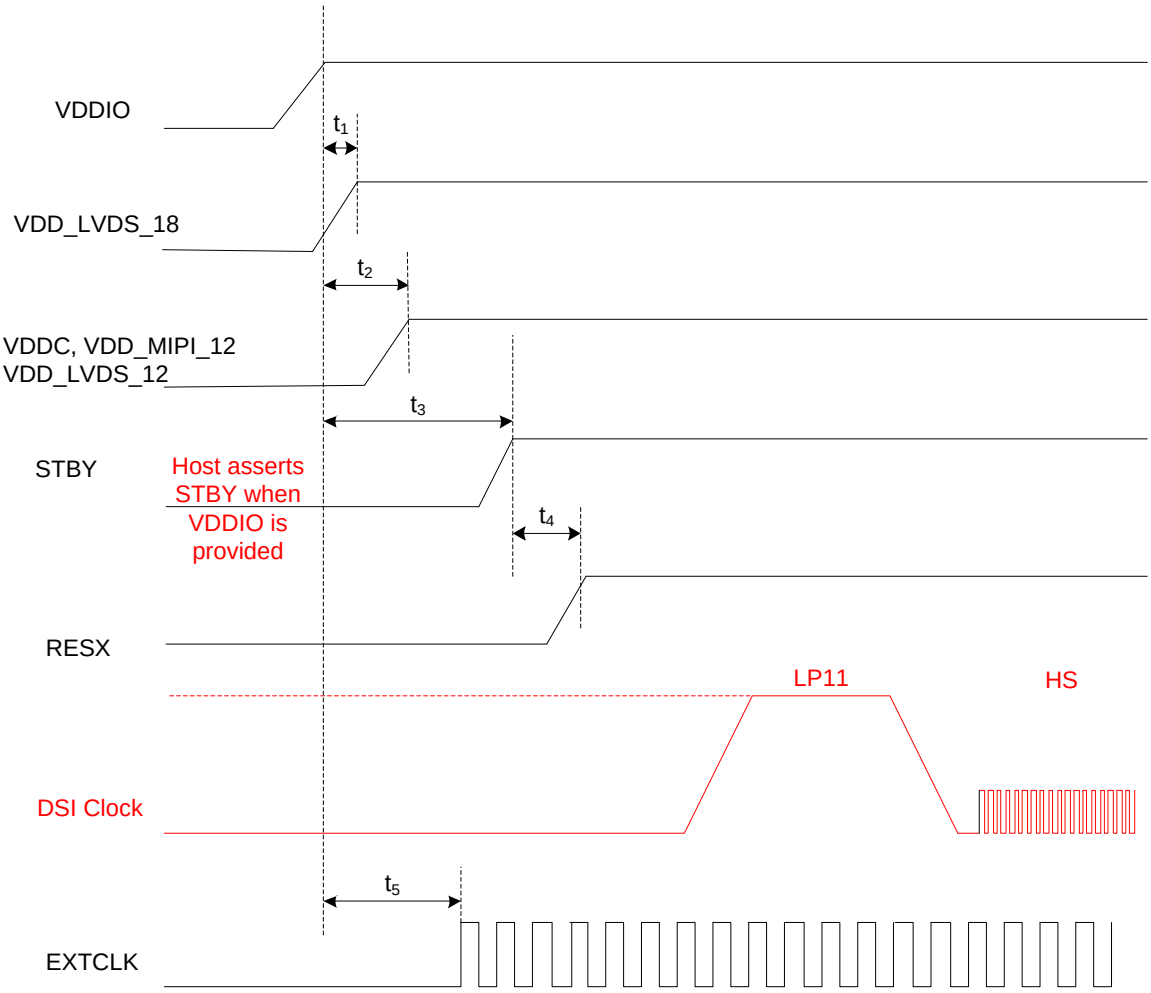

Figure 8-7 Power-On Sequence Timing

Table 8-14 Power-On Sequence Timing

Parameter	Description	Min.	Typ.	Max.	Units
t_1	VDD_LVDS*_18 on delay from VDDIO on	0	-	10	msec
t_2	VDD *_12 on delay from VDDIO on	0	-	10	msec
t_3	STBY “H” delay from VDDIO on	t_1	-	-	msec
t_4	RESX release from STBY rise edge	10	-	-	usec
t_5	ExtClk Delay from VDDIO on	0	-	t_2	msec

Please keep all the input signals at either “Hi-z” or “logic low” state before powering on VDDIO

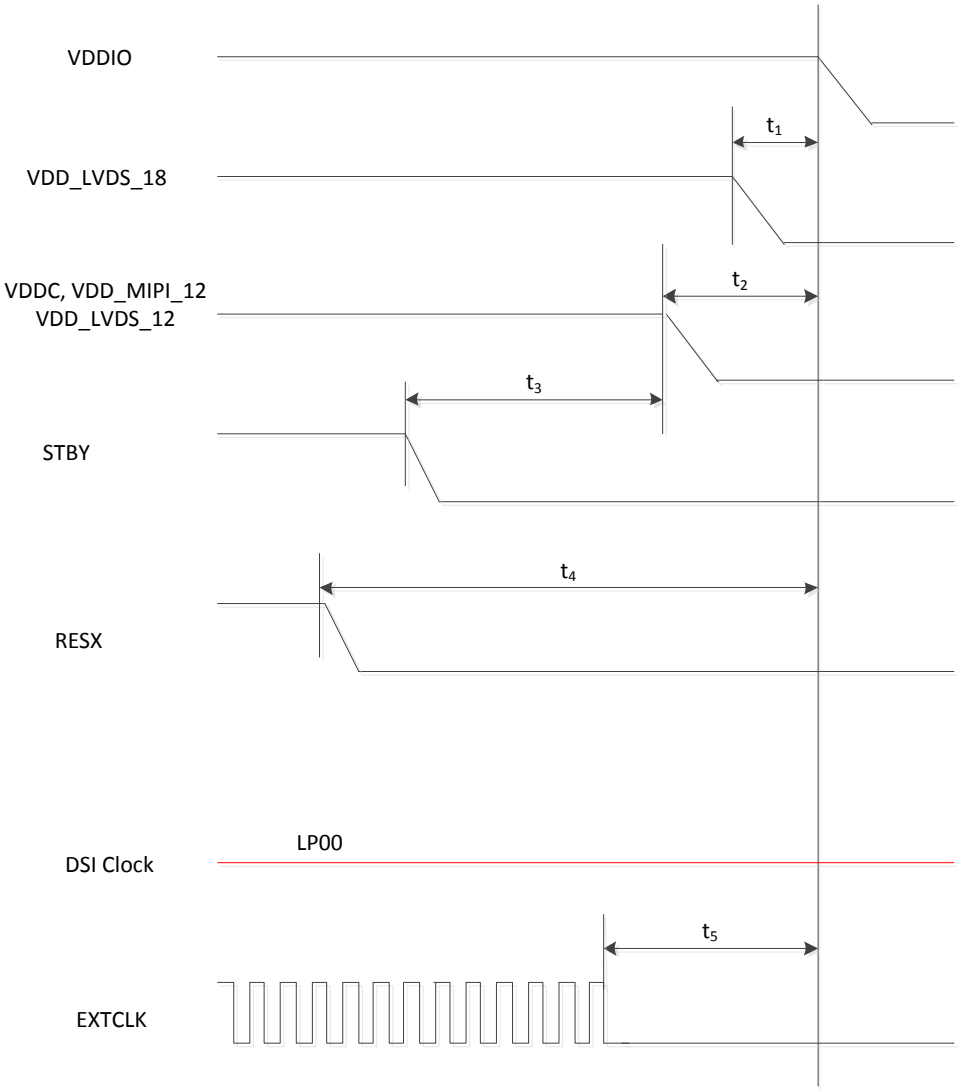

Figure 8-8 Power-Off Sequence Timing

Table 8-15 Power-Off Sequence Timing

Parameter	Description	Min.	Typ.	Max.	Units
t_1	VDD_LVDS*_18 off delay from VDDIO off	0	-	-	msec
t_2	VDD *_12 off delay from VDDIO off	0	-	10	msec
t_3	VDD *_12 off delay from STBY “L”	t_1	-	-	msec
t_4	RESX assertion delay to VDDIO off	10	-	-	usec
t_5	ExtClk Delay delay to VDDIO off	0	-	t_2	msec

Please keep all the input signals at either “Hi-z” or “logic low” state before cutting of VDDIO

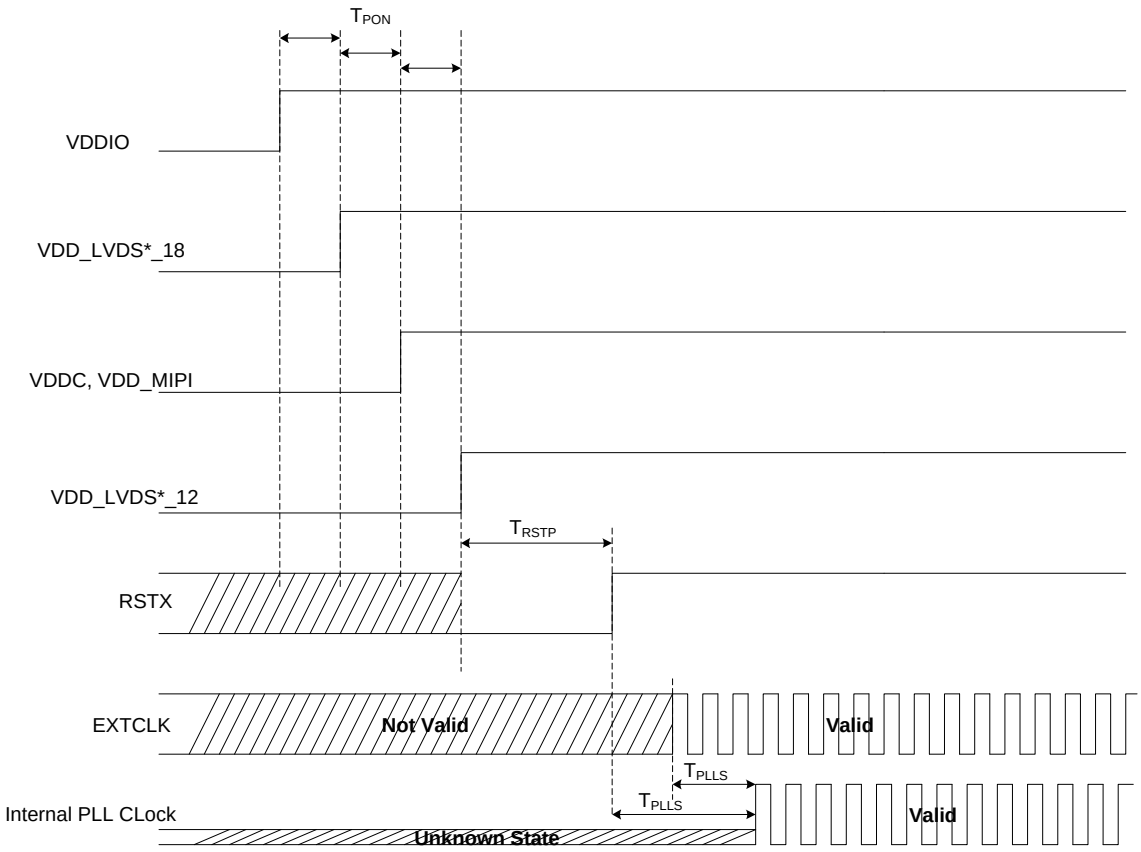

Figure 8-9 LVDS PLL Set Time (EXTCLK ON)

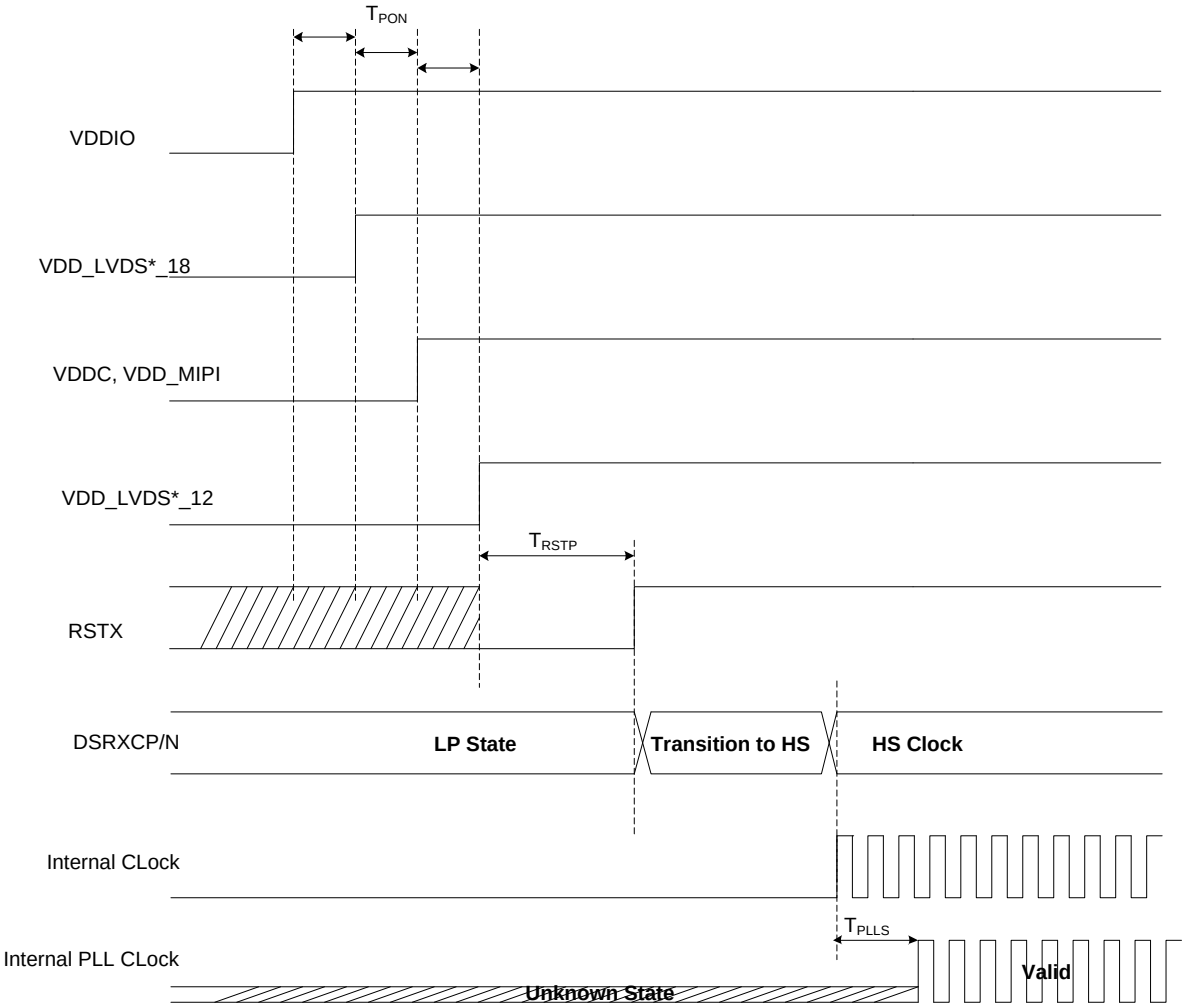

Figure 8-10 LVDS PLL Set Time (EXTCLK OFF)

Table 8-16 LVDS PLL Phase locked loop set time

Description	Parameter	Min.	Typ.	Max.	Units
PLL Lock/Stable Time	T_{PLLS}	200	-	-	us

8.4.6 I2C Interface Timing

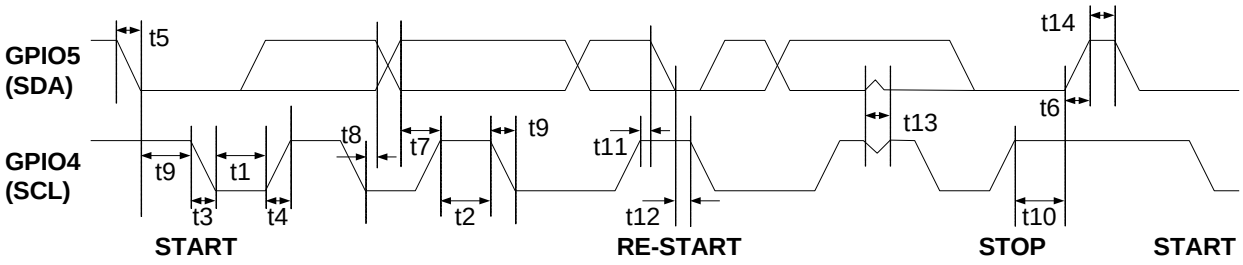

Figure 8-11 I2C Interface timing

Table 8-17 I2C Interface Timing

Parameter	Description	Min.	Typ.	Max.	Units
F_{CLK}	SCL CLK frequency			400	kHz
t_1	SCL low time	1.3			µsec
t_2	SCL high time	0.6			µsec
t_3	SCL fall time NOTE1			0.3	µsec
t_4	SCL rise time NOTE1			0.3	µsec
t_5	SDA fall time NOTE1			0.3	µsec
t_6	SDA rise time NOT1			0.3	µsec
t_7	Data setup time	0.1			µsec
t_8	Data hold time	0.0			µsec
t_9	Hold time start condition	0.6			µsec
t_{10}	Setup time stop condition	0.6			µsec
t_{11}	Setup time re-start condition	0.6			µsec
t_{12}	Hold time for re-start	0.6			µsec
t_{13}	Spike length			20	nsec
t_{14}	Guard time for start condition	1.3			µsec
t_{15}	DSICLK setup time before active I2C transaction	1			µsec
t_{16}	DSICLK hold time after last active I2C transaction	1			µsec

NOTE1: Rise/Fall time of SCL and SDA depends on the external pull-up resistor used and the load capacitance on the PCB. Input rise is measured from 0.3 VDDIO to 0.7 VDDIO and fall time is measured from 0.7 VDDIO to 0.3 VDDIO.

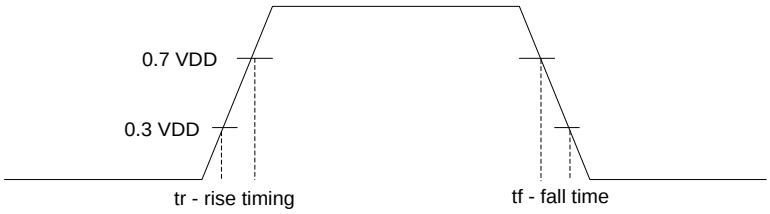

Figure 8-12 Rise and Fall Time of SCL/SDA

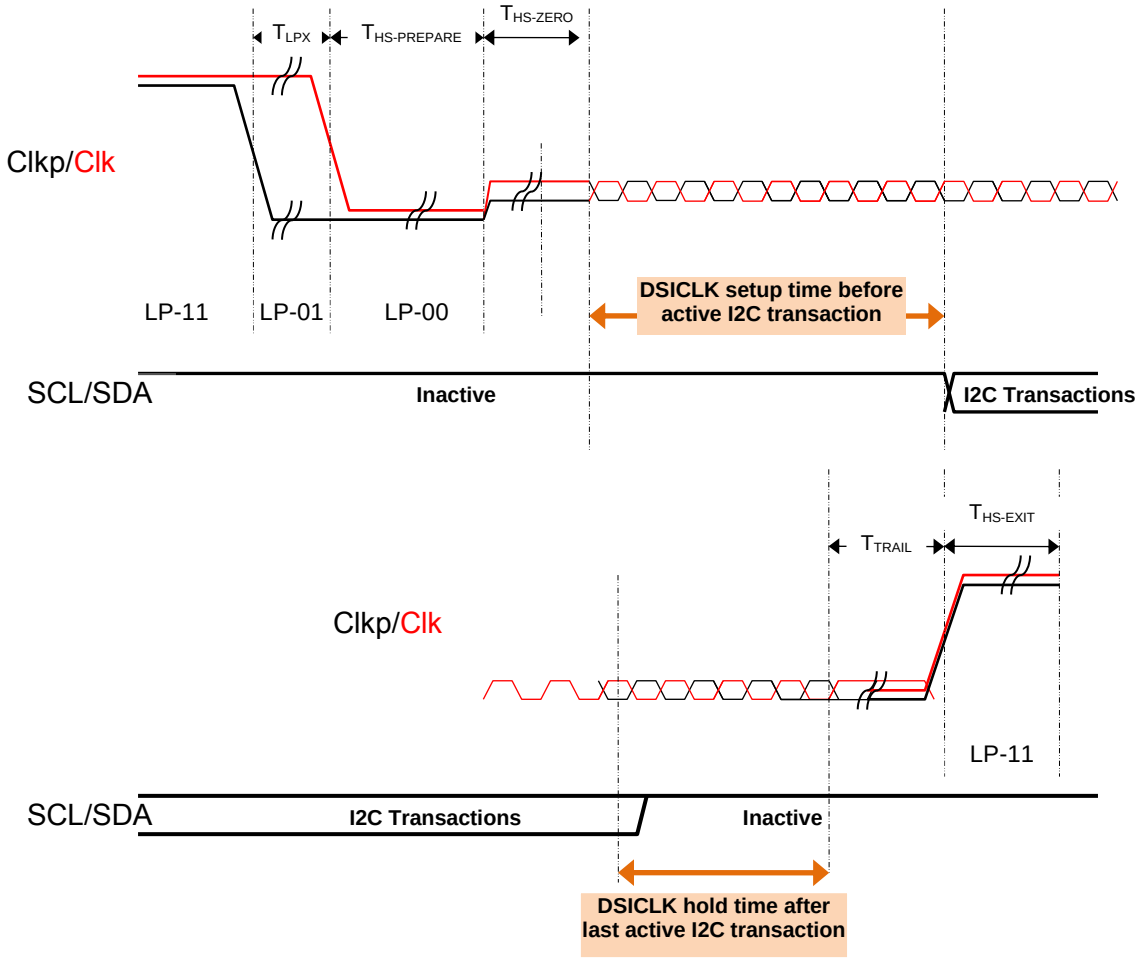

Figure 8-13 DSICLK Active Before and After I2C Slave Transactions

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