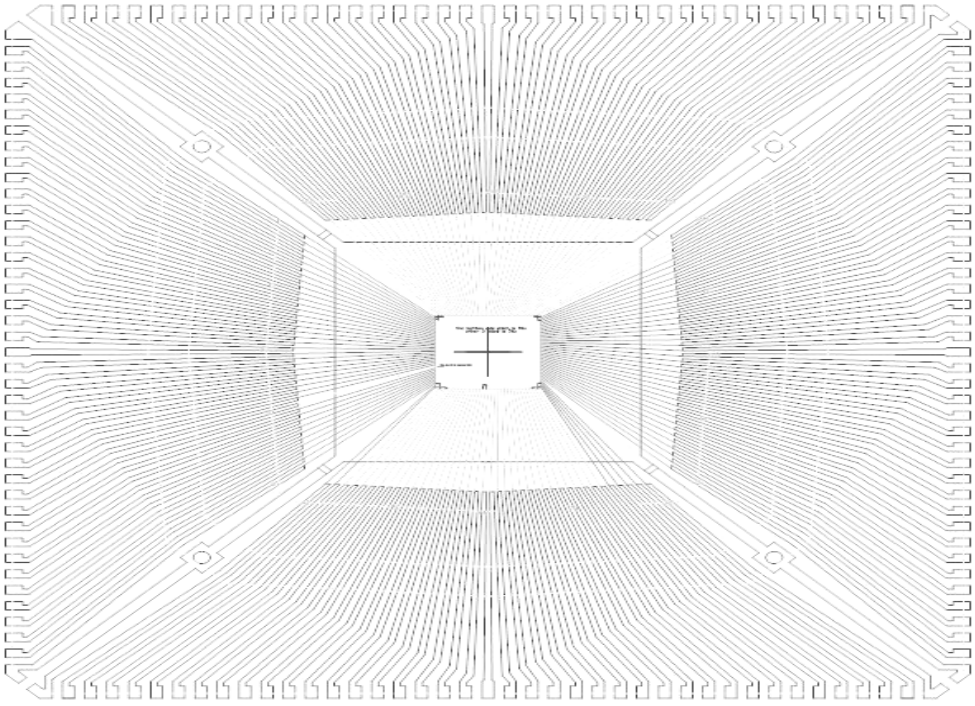
LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

LT8912

Single-Channel MIPI® DSI Bridge to LVDS/HDMI/MHL

DataSheet



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1. REVISION HISTORY

Version	Owner	Content	Date
R1.0	C.Tao	1. Initial Release	2015/03/01
R1.1	C.Tao	1. Change MHL feature from 30Hz 1080p to 60Hz 720p 2. Update Pin description	2015/03/15
R1.2	C.Tao	1. Add 7.5mm x 7.5mm QFN64 package type 2. Update product code: LT8912 for LQFP80, LT8912B for QFN64	2015/03/31
R1.3	N.Wang	1.Check package information	2015/03/31
R1.4	N.Wang	1.Add PCB footprint	2015/04/14
R1.5	C.Tao	1. Update feature list. Add “No DDC and HDCP support” 2. Add power consumption 3. Fix pin63 and pin64 definition error	2016/03/08
R1.6	C.Tao	1. Add power consumption information (Section4.5)	2016/03/18
R1.7	C.Tao	1. Add Tape and Reel Information and MSL Level	2016/04/06

2. GENERAL DESCRIPTION

The Lontium LT8912 MIPI® DSI to LVDS and HDMI/MHL bridge features a single-channel MIPI® D-PHY receiver front-end configuration with 4 data lanes per channel operating at 1.5Gbps per data lane and a maximum input bandwidth of 6Gbps.

For screen application, the bridge decodes MIPI® DSI 18bpp RGB666 and 24bpp RGB888 packets and converts the formatted video data stream to a compatible LVDS output operating at pixel clock operating from 25MHz to 154MHz, offering a single-link LVDS with 4 data lanes per link.

For TV application, the bridge provides a HDMI/MHL data output with optional S/PDIF or 2-channel I2S serial audio input. Its high fidelity 2-channel I2S can transmit stereo up to a 192kHz sampling rate. The S/PDIF can carry stereo LPCM audio or compressed audio, including Dolby® Digital and DTS®.

The LT8912 is fabricated in advanced CMOS process and implemented in both 12mm x 12mm LQFP at 0.5mm pitch package and 7.5mm x 7.5mm QFN at 0.4mm pitch package. These packages are RoHS compliant and specified to operate from −40°C to +85°C.

2.1 Application

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Personal media players
- Gaming

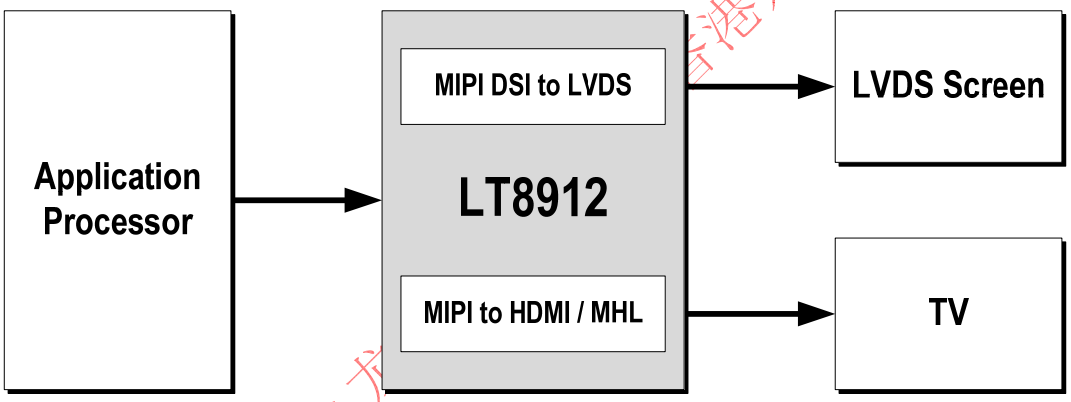


Figure 2.1 Typical Application and System Diagrams

2.2 Features

- **One-Channel MIPI® DSI Receiver**
  - Compaliant with D-PHY1.1 and DSI1.02
  - 1 clock lane and 1~4 configurable data lanes
  - 80Mb/s~1.5Gb/s per data lane
  - Data lane swappable and polarity swappable
  - Internal Rterm calibration w/i less than 5% error
  - 2-bit programmable equalization
  - Only Non-Burst Mode supported
- **One-Channel LVDS Transmitter**
  - 1 clock lane and 4 data lanes
  - Maximum 1.0Gb/s per data lane
  - Reduced output swing for low EMI
- **HDMI/MHL Transmitter**
  - Compaliant with HDMI1.4 and MHL2.0 standard
  - Up to 60Hz 1080p 8-bit HDMI output
  - Up to 60Hz 720p 8-bit MHL output
  - 7-bit automatic or manual output swing calibration
  - 3-bit programmable de-emphasis
  - Support Hot-Plug Detect
  - No DDC and HDCP support for LT8912
- **Miscellaneous**
  - Support scaler function for MIPI to LVDS bridge
  - Single 1.8V supply power
  - Temperature range: -40^{0}C ~ +85^{0}C
  - Packaged in both 12x12mm LQFP80 and 7.5mm x 7.5mm QFN64

2.3 Functional Diagram

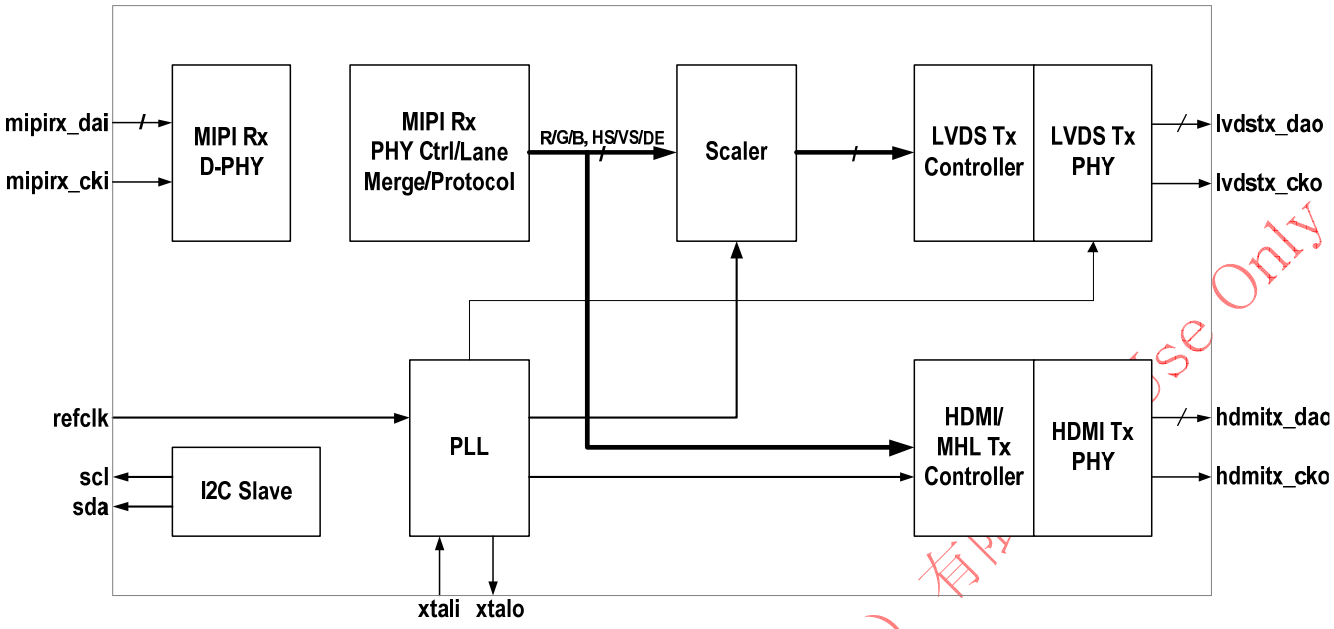


Fig 2.2 LT8912 Functional Diagram

3. PINNING INFORMATION

3.1 Pin Diagram

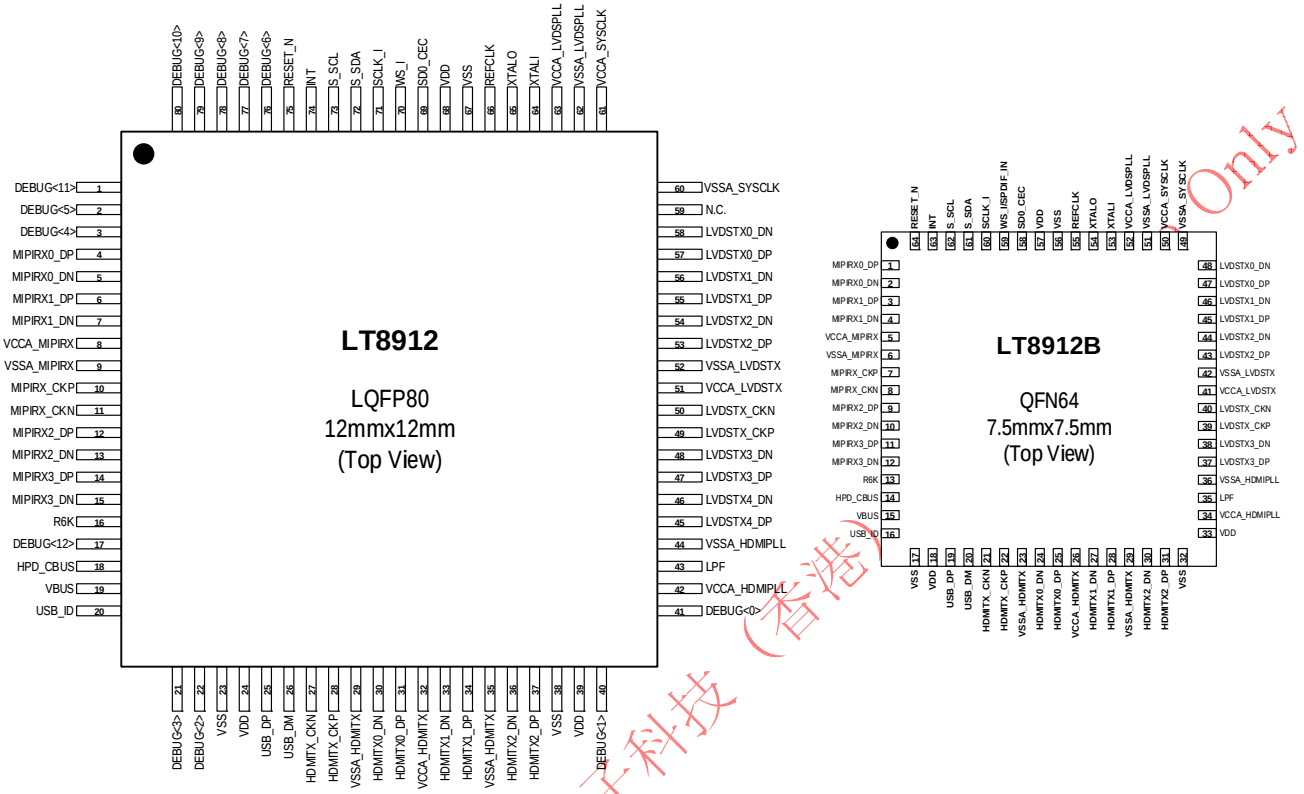


Figure 3.1 LQFP80 (LT8912) and QFN64 (LT8912B) Pin Assignment (Top View)

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance. Maximum trace length mismatch should be less than 5mil and keep total trace length to a minimum for all differential traces. Routing differential pairs on the top or bottom layer with no vias as on signal path is highly recommended.

For crystal oscillator, keep XTALI/XTALO as short as possible and away from noisy signal source. Minimize parasitic capacitances on these two pins and shield them with clean ground lines.

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitor is recommended to be installed near all the LT8912 power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized.

3.2 Pin Function

3.2.1 LQFP80 (LT8912)

PIN#	PIN NAME	I/O	DESCRIPTION
1	DEBUG<11>	IO	**Bit-11 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
2	DEBUG<5>	IO	**Bit-5 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
3	DEBUG<4>	IO	**Bit-4 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
4	MIPIRX0_DP	I	**MIPI® D-PHY Channel-0 Data Lane-0 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX0_DN.
5	MIPIRX0_DN	I	**MIPI® D-PHY Channel-0 Data Lane-0 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX0_DP.
6	MIPIRX1_DP	I	**MIPI® D-PHY Channel-0 Data Lane-1 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX1_DN.
7	MIPIRX1_DN	I	**MIPI® D-PHY Channel-0 Data Lane-1 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX0_DP.
8	VCCA_MIPIRX	IO	**MIPI® D-PHY Channel-0 Power** 1.8V power supply for MIPIRX input. Should be filtered and noiseless.
9	VSSA_MIPIRX	IO	**MIPI® D-PHY Channel-0 Ground** 1.8V ground for MIPIRX input.
10	MIPIRX_CKP	I	**MIPI® D-PHY Channel-0 Data Clock Lane Positive Input** Positive input of DDR clock differential pairs up to 750Mb/s in quadrature phase with data signals. There is an internal 100Ω terminator between this pin and MIPIRX_CKN.
11	MIPIRX_CKN	I	**MIPI® D-PHY Channel-0 Data Clock Lane Negative Input** Negative input of DDR clock differential pairs up to 750Mb/s in quadrature phase with data signals. There is an internal 100Ω terminator between this pin and MIPIRX_CKP.
12	MIPIRX2_DP	I	**MIPI® D-PHY Channel-0 Data Lane-2 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX2_DN.
13	MIPIRX2_DN	I	**MIPI® D-PHY Channel-0 Data Lane-2 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX2_DP.
14	MIPIRX3_DP	I	**MIPI® D-PHY Channel-0 Data Lane-3 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX3_DN.
15	MIPIRX3_DN	I	**MIPI® D-PHY Channel-0 Data Lane-3 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX3_DP.
16	R6K	IO	**BandGap External Resistor** External 6K resistor between this pin and VSSA_MIPIRX for setting internal reference current.
17	DEBUG<12>	IO	**Bit-12 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
18	HPD_CBUS	IO	**MHL TX CBUS Control** In default, this pin is configured as MHL transmitter CBUS signal. **HDMI TX HPD Control** This pin can also be configured through I2C as HDMI TX Hot-Plug Detect Control. In this case, there is a 100K pull-down resistor. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
19	VBUS	I	**+5V Power for Bus-Powered USB link**
20	USB_ID	I	**USB_ID for OTG application**
21	DEBUG<3>	IO	**Bit-3 debug data output**

PIN#	PIN NAME	I/O	DESCRIPTION
			In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
22	DEBUG<2>	IO	**Bit-2 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
23	VSS	IO	**Digital Ground** 1.8V ground for digital logic.
24	VDD	IO	**Digital Power Supply** 1.8V power supply for digital logic. Should be filtered and noiseless.
25	USB_DP	I	**USB Data Positive Input** Positive input of USB2.0 diffferential signal up to 480Mb/s.
26	USB_DM	I	**USB Data Negative Input** Negative input of USB2.0 diffferential signal up to 480Mb/s.
27	HDMITX_CKN	O	**HDMI TxPHY Channel-0 Clock Lane Negative Output** Negative HDMI TxPHY output TMDS clock up to 1.5GHz. This pin with HDMITX_CKP can also be used as internal clock signal output test pins.
28	HDMITX_CKP	O	**HDMI TxPHY Channel-0 Clock Lane Positive Output** Positive of HDMI TxPHY output TMDS clock up to 1.5GHz. This pin with HDMITX_CKN can also be used as internal clock signal output test pins.
29	VSSA_HDMITX	IO	**HDMI/MHL TxPHY Ground** 1.8V ground for HDMI TxPHY output.
30	HDMITX0_DN	O	**HDMI/MHL TxPHY Channel-0 Data Lane-0 Negative Output** HDMI output TMDS data up to 3.0Gb/s. In default, this pin with HDMITX0_DP is configured to MHL output data pins which operates at .
31	HDMITX0_DP	O	**HDMI/MHL TxPHY Channel-0 Data Lane-0 Positive Output** HDMI output TMDS data up to 3.0Gb/s. In default, this pin with HDMITX0_DN is configured to MHL output data pins which operates at .
32	VCCA_HDMITX	IO	**HDMI TxPHY Power** 1.8V power supply for HDMI TxPHY output. Should be filtered and noiseless.
33	HDMITX1_DN	O	**HDMI/MHL TxPHY Channel-0 Data Lane-1 Negative Output** HDMI output TMDS data up to 3.0Gb/s.
34	HDMITX1_DP	O	**HDMI/MHL TxPHY Channel-0 Data Lane-1 Positive Output** HDMI output TMDS data up to 3.0Gb/s.
35	VSSA_HDMITX	IO	**HDMI TxPHY Ground** 1.8V ground for HDMI TxPHY output.
36	HDMITX2_DN	O	**HDMI/MHL TxPHY Channel-0 Data Lane-2 Negative Output** HDMI output TMDS data up to 3.0Gb/s.
37	HDMITX2_DP	O	**HDMI/MHL TxPHY Channel-0 Data Lane-2 Positive Output** HDMI output TMDS data up to 3.0Gb/s.
38	VSS	IO	**Digital Ground** 1.8V ground for digital logic.
39	VDD	IO	**Digital Power Supply** 1.8V power supply for digital logic. Should be filtered and noiseless.
40	DEBUG<1>	IO	**Bit-1 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
41	DEBUG<0>	IO	**Bit-0 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
42	VCCA_HDMIPLL	IO	**HDMI TxPLL Power Supply** 1.8V power supply for HDMI TxPLL output.
43	LPF	IO	**HDMIPLL External Low-Pass Filter** Connect a 2nF capacitor to this pin. It serves as loop filter of internal HDMIPLL.
44	VSSA_HDMIPLL	IO	**HDMI TxPLL Ground** 1.8V ground for HDMI TxPLL output.
45	LVDSTX4_DP	O	**LVDS TxPHY Test Lane Positive Output** Positive output of differential pairs up to 1.0Gb/s.
46	LVDSTX4_DN	O	**LVDS TxPHY Test Lane Negative Output** Positive output of differential pairs up to 1.0Gb/s.

PIN#	PIN NAME	I/O	DESCRIPTION
47	LVDSTX3_DP	O	**LVDS Channel-0 Data Lane-3 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
48	LVDSTX3_DN	O	**LVDS Channel-0 Data Lane-3 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
49	LVDSTX_CKP	O	**LVDS Channel-0 Clock Lane Positive Output** Positive output of clock differential pairs up to 500Mb/s.
50	LVDSTX_CKN	O	**LVDS Channel-0 Clock Lane Positive Output** Negative output of clock differential pairs up to 500Mb/s.
51	VCCA_LVDSTX	IO	**LVDS TxPHY Power Supply** 1.8V power supply for LVDS TxPHY output.
52	VSSA_LVDSTX	IO	**LVDS TxPHY Ground** 1.8V ground for LVDS TxPHY output.
53	LVDSTX2_DP	O	**LVDS Channel-0 Data Lane-2 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
54	LVDSTX2_DN	O	**LVDS Channel-0 Data Lane-2 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
55	LVDSTX1_DP	O	**LVDS Channel-0 Data Lane-1 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
56	LVDSTX1_DN	O	**LVDS Channel-0 Data Lane-1 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
57	LVDSTX0_DP	O	**LVDS Channel-0 Data Lane-0 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
58	LVDSTX0_DN	O	**LVDS Channel-0 Data Lane-0 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
59	N.C.		No Connect.
60	VSSA_SYSCLK	IO	**System PLL Ground** 1.8V ground for system PLL.
61	VCCA_SYSCLK	IO	**System PLL Power Supply** 1.8V ground for system PLL.
62	VSSA_LVDSPLL	IO	**LVDS TxPLL Ground**1.8V ground for LVDS TxPLL
63	VCCA_LVDSPLL	IO	**LVDS TxPLL Power Supply** 1.8V power supply for LVDS TxPLL
64	XTALI	I	**Crystal Clock Input** A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8912
65	XTALO	O	**Crystal Clock Output** A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
66	REFCLK	IO	**External Pixel Clock Input** In default, this pin is configured as external reference (pixel) clock input for HDMIPLL. **Digital Test Signal Output (GPIO0)** When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
67	VSS	IO	**Digital Ground** 1.8V ground for digital logic.
68	VDD	IO	**Digital Power Supply** 1.8V power supply for digital logic. Should be filtered and noiseless.
69	SD0_CEC	IO	**I2S Serial Audio Data Input** In default, this pin is configured to I2S serial audio data input. **CEC** This pin can also be configured as MHLTx CEC IO with open-drain output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
70	WS_I	IO	**I2S Audio Word Select Input** In default, this pin is configured to I2S channel select input. **SPDIF Audio Signal Input** This pin can also be configured as SPDIF audio data input. **Digital Test Signal Output (GPIO2)** When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
71	SCLK_I	IO	**I2S Audio Data Clock Input** In default, this pin is configured as

PIN#	PIN NAME	I/O	DESCRIPTION
			Digital Test Signal Output (GPIO3) When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
72	S_SDA	IO	**I2C Data IO** It serves as the serial port data IO slave for register access with a 20K pull-up resistor. Supports 1.8V CMOS logic levels. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
73	S_SCL	I	**I2C Data Clock** **It s**erves as the serial port data clock slave for register access with a 20K pull-up resistor. Supports 1.8V CMOS logic levels. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
74	INT	IO	**Interrupt Request Output** In default, this pin is configured as interrupt request (IRQ) output. **Digital Test Signal Output (GPIO1)** When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V. **Analog Reference Voltage Test Signal Output** When INT and GPIO function are disabled, this pin can also be used as analog reference voltage test signal output.
75	RESET_N	I	**Hardware Reset Input** Chip reset signal. Active LOW. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
76	DEBUG<6>	IO	**Bit-6 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
77	DEBUG<7>	IO	**Bit-7 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
78	DEBUG<8>	IO	**Bit-8 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
79	DEBUG<9>	IO	**Bit-9 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
80	DEBUG<10>	IO	**Bit-10 debug data output** In debug mode, it serves as digital test output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.

3.2.2 QFN64 (LT8912B)

PIN#	PIN NAME	I/O	DESCRIPTION
1	MIPIRX0_DP	I	**MIPI® D-PHY Channel-0 Data Lane-0 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX0_DN.
2	MIPIRX0_DN	I	**MIPI® D-PHY Channel-0 Data Lane-0 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX0_DP.
3	MIPIRX1_DP	I	**MIPI® D-PHY Channel-0 Data Lane-1 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX1_DN.
4	MIPIRX1_DN	I	**MIPI® D-PHY Channel-0 Data Lane-1 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX0_DP.
5	VCCA_MIPIRX	IO	**MIPI® D-PHY Channel-0 Power** 1.8V power supply for MIPIRX input. Should be filtered and noiseless.
6	VSSA_MIPIRX	IO	**MIPI® D-PHY Channel-0 Ground** 1.8V ground for MIPIRX input.
7	MIPIRX_CKP	I	**MIPI® D-PHY Channel-0 Data Clock Lane Positive Input** Positive input of DDR clock differential pairs up to 750Mb/s in quadrature phase with data signals. There is an internal 100Ω terminator between this pin and MIPIRX_CKN.
8	MIPIRX_CKN	I	**MIPI® D-PHY Channel-0 Data Clock Lane Negative Input** Negative input of DDR clock differential pairs up to 750Mb/s in quadrature phase with

PIN#	PIN NAME	I/O	DESCRIPTION
			data signals. There is an internal 100Ω terminator between this pin and MIPIRX_CKP.
9	MIPIRX2_DP	I	**MIPI® D-PHY Channel-0 Data Lane-2 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX2_DN.
10	MIPIRX2_DN	I	**MIPI® D-PHY Channel-0 Data Lane-2 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX2_DP.
11	MIPIRX3_DP	I	**MIPI® D-PHY Channel-0 Data Lane-3 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX3_DN.
12	MIPIRX3_DN	I	**MIPI® D-PHY Channel-0 Data Lane-3 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. There is an internal 100Ω terminator between this pin and MIPIRX3_DP.
13	R6K	IO	**BandGap External Resistor** External 6K resistor between this pin and VSSA_MIPIRX for setting internal reference current.
14	HPD_CBUS	IO	**MHL TX CBUS Control** In default, this pin is configured as MHL transmitter CBUS signal. **HDMI TX HPD Control** This pin can also be configured through I2C as HDMI TX Hot-Plug Detect Control. In this case, there is a 100K pull-down resistor. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
15	VBUS	I	**+5V Power for Bus-Powered USB link**
16	USB_ID	I	**USB_ID for OTG application**
17	VSS	IO	**Digital Ground** 1.8V ground for digital logic.
18	VDD	IO	**Digital Power Supply** 1.8V power supply for digital logic. Should be filtered and noiseless.
19	USB_DP	I	**USB Data Positive Input** Positive input of USB2.0 diffferential signal up to 480Mb/s.
20	USB_DM	I	**USB Data Negative Input** Negative input of USB2.0 diffferential signal up to 480Mb/s.
21	HDMITX_CKN	O	**HDMI TxPHY Channel-0 Clock Lane Negative Output** Negative HDMI TxPHY output TMDS clock up to 1.5GHz. This pin with HDMITX_CKP can also be used as internal clock signal output test pins.
22	HDMITX_CKP	O	**HDMI TxPHY Channel-0 Clock Lane Positive Output** Positive of HDMI TxPHY output TMDS clock up to 1.5GHz. This pin with HDMITX_CKN can also be used as internal clock signal output test pins.
23	VSSA_HDMITX	IO	**HDMI TxPHY Ground** 1.8V ground for HDMI TxPHY output.
24	HDMITX0_DN	O	**HDMI/MHL TxPHY Channel-0 Data Lane-0 Negative Output** HDMI output TMDS data up to 3.0Gb/s. In default, this pin with HDMITX0_DP is configured to MHL output data pins which operates at .
25	HDMITX0_DP	O	**HDMI/MHL TxPHY Channel-0 Data Lane-0 Positive Output** HDMI output TMDS data up to 3.0Gb/s. In default, this pin with HDMITX0_DN is configured to MHL output data pins which operates at .
26	VCCA_HDMITX	IO	**HDMI TxPHY Power** 1.8V power supply for HDMI TxPHY output. Should be filtered and noiseless.
27	HDMITX1_DN	O	**HDMI/MHL TxPHY Channel-0 Data Lane-1 Negative Output** HDMI output TMDS data up to 3.0Gb/s.
28	HDMITX1_DP	O	**HDMI/MHL TxPHY Channel-0 Data Lane-1 Positive Output** HDMI output TMDS data up to 3.0Gb/s.
29	VSSA_HDMITX	IO	**HDMI TxPHY Ground** 1.8V ground for HDMI TxPHY output.
30	HDMITX2_DN	O	**HDMI/MHL TxPHY Channel-0 Data Lane-2 Negative Output** HDMI output TMDS data up to 3.0Gb/s.
31	HDMITX2_DP	O	**HDMI/MHL TxPHY Channel-0 Data Lane-2 Positive Output** HDMI output TMDS data up to 3.0Gb/s.
32	VSS	IO	**Digital Ground** 1.8V ground for digital logic.
33	VDD	IO	**Digital Power Supply**

PIN#	PIN NAME	I/O	DESCRIPTION
			1.8V power supply for digital logic. Should be filtered and noiseless.
34	VCCA_HDMIPLL	IO	**HDMI TxPLL Power Supply** 1.8V power supply for HDMI TxPLL output.
35	LPF	IO	**HDMIPLL External Low-Pass Filter** Connect a 2nF capacitor to this pin. It serves as loop filter of internal HDMIPLL.
36	VSSA_HDMIPLL	IO	**HDMI TxPLL Ground** 1.8V ground for HDMI TxPLL output.
37	LVDSTX3_DP	O	**LVDS Channel-0 Data Lane-3 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
38	LVDSTX3_DN		**LVDS Channel-0 Data Lane-3 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
39	LVDSTX_CKP	O	**LVDS Channel-0 Clock Lane Positive Output** Positive output of clock differential pairs up to Datarate/7 Mb/s.
40	LVDSTX_CKN	O	**LVDS Channel-0 Clock Lane Negative Output** Negative output of clock differential pairs up to Datarate/7 Mb/s.
41	VCCA_LVDSTX	IO	**LVDS TxPHY Power Supply** 1.8V power supply for LVDS TxPHY output.
42	VSSA_LVDSTX	IO	**LVDS TxPHY Ground** 1.8V ground for LVDS TxPHY output.
43	LVDSTX2_DP	O	**LVDS Channel-0 Data Lane-2 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
44	LVDSTX2_DN	O	**LVDS Channel-0 Data Lane-2 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
45	LVDSTX1_DP	O	**LVDS Channel-0 Data Lane-1 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
46	LVDSTX1_DN	O	**LVDS Channel-0 Data Lane-1 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
47	LVDSTX0_DP	O	**LVDS Channel-0 Data Lane-0 Positive Output** Positive output of differential pairs up to 1.0Gb/s.
48	LVDSTX0_DN	O	**LVDS Channel-0 Data Lane-0 Negative Output** Negative output of differential pairs up to 1.0Gb/s.
49	VSSA_SYSCLK	IO	**System PLL Ground** 1.8V ground for system PLL.
50	VCCA_SYSCLK	IO	**System PLL Power Supply** 1.8V ground for system PLL.
51	VSSA_LVDSPLL	IO	**LVDS TxPLL Ground**1.8V ground for LVDS TxPLL
52	VCCA_LVDSPLL	IO	**LVDS TxPLL Power Supply** 1.8V power supply for LVDS TxPLL
53	XTALI	I	**Crystal Clock Input** A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8912
54	XTALO	O	**Crystal Clock Output** A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
55	REFCLK	IO	**External Pixel Clock Input** In default, this pin is configured as external reference (pixel) clock input for HDMIPLL. **Digital Test Signal Output (GPIO0)** When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
56	VSS	IO	**Digital Ground** 1.8V ground for digital logic.
57	VDD	IO	**Digital Power Supply** 1.8V power supply for digital logic. Should be filtered and noiseless.
58	SD0_CEC	IO	**I2S Serial Audio Data Input** In default, this pin is configured to I2S serial audio data input. **CEC** This pin can also be configured as MHLTx CEC IO with open-drain output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
59	WS_I	IO	**I2S Audio Word Select Input** In default, this pin is configured to I2S channel select input. **SPDIF Audio Signal Input** This pin can also be configured as SPDIF audio data input.

PIN#	PIN NAME	I/O	DESCRIPTION
			Digital Test Signal Output (GPIO2) When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
60	SCLK_I	IO	**I2S Audio Data Clock Input** In default, this pin is configured as **Digital Test Signal Output (GPIO3)** When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
61	S_SDA	IO	**I2C Data IO** It serves as the serial port data IO slave for register access with a 20K pull-up resistor. Supports 1.8V CMOS logic levels. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
62	S_SCL	I	**I2C Data Clock** **It s**erves as the serial port data clock slave for register access with a 20K pull-up resistor. Supports 1.8V CMOS logic levels. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.
63	INT	IO	**Interrupt Request Output** In default, this pin is configured as interrupt request (IRQ) output. **Digital Test Signal Output (GPIO1)** When this pin is configured as GPIO, it serves as digital test signal output. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V. **Analog Reference Voltage Test Signal Output** When INT and GPIO function are disabled, this pin can also be used as analog reference voltage test signal output.
64	RESET_N	I	**Hardware Reset Input** Chip reset signal. Active LOW. The input schmitt trigger has a hysteresis window with VL=0.59V and VH=1.2V.

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCCA_MIPIRX VCCA_LVDSTX VCCA_HDMITX VCCA_HDMIPLL VCCA_LVDSPLL VCCA_SYSCLK VDD	1.8V Power Supplay Voltage	-0.3		2.2	V
V_I	CMOS Terminal Input Voltage Range	-0.3		2.2	V
V_O	CMOS Terminal Output Voltage Range	-0.3		2.2	V
T_S	Storage Temperature	-55		125	℃
ESD	HBM Elastrostatic Discharge Level			**TBD**	V

Notes:
1.Permanent device damage may occur if absolute maximum conditions are exceeded.
2.Function operation should be restricted to the conditions described under Normal Operating Conditions.

4.2 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCCA_MIPIRX VCCA_LVDSTX VCCA_HDMITX VCCA_HDMIPLL VCCA_LVDSPLL VCCA_SYSCLK VDD	1.8V Power Supplay Voltage	1.65	1.8	1.95	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

4.3 DC Characteristics

MIPIRX HS Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			70	mV
VIDTL	Differential input low voltage threshold	-70			mV
VIHHS	Single ended input high voltage			460	mV
VILHS	Single ended input low voltage	-40			mV
VCMRXDC	Input common mode voltage	70		330	mV
	Differential input impedance	80		125	Ω
MIPIRX LP Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIL-ULPS	Logic 0 input voltage, in ULP State			300	mV
VIL	Logic 0 input voltage, not in ULP State			550	mV
VIH	Input high voltage	880			mV
VHYST	Input hysteresis	25			mV
MIPIRX Contention Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**

VILF	Input low fault threshold	200		450	mV
LVDS Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			50	mV
VIDTL	Differential input low voltage threshold	-50			mV
VCMRXDC	Input common mode voltage	0	1200	1800	mV
HDMI/MHL Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
V_{SWING_HDMI}	HDMI TMDS output swing	400	500	600	mV
V_{SWING_MHL}	MHL TMDS output swing	300	500	600	mV
$V_{SWING\_MHL\_CLK}$	MHL Clock swing	360	540	720	mV

4.4 AC Characteristics

MIPIRX HS Line Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
ΔVCMRX(HF)	Common mode interference beyond 450MHz			200	mVpp
ΔVCMRX(LF)	Common mode interference between 50M and 450M.	-50		50	mVpp
Ccm	Common mode termination			60	pF
Rterm	Termination Resister	80	100	125	Ω
MIPIRX LP Line Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
LVDS Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
CLK	Ouput clk cycle	6.25	Tc	37.0	ns
t_{rise}	VOD rise time, 20% to 80%	250	350	500	ps
t_{fall}	VOD fall time, 20% to 80%	250	350	500	ps
T_0	Input data position0	-0.15	0	0.15	ns
T_1	Input data position1	Tc/7-0.15		Tc/7+0.15	ns
T_2	Input data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T_3	Input data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T_4	Inputdata position4	4Tc/7-0.15		4Tc/7+0.15	ns
T_5	Input data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T_6	Input data position6	6Tc/7-0.15		6Tc/7+0.15	ns
Rterm	Termination Resister	80	100	125	Ω
HDMI/MHL Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
f_{CLK_HDMI}	HDMI Clock frequency			150M	Hz
T_{D_HDMI}	HDMI Clock duty cycle	40	50	60	%
Tr/Tf	TMDS signal rise/fall time (20%~80%)	75			ps
f_{CLK_MHL}	MHL Clock frequency			150M	Hz
$T_{R\text{-}CM}/T_{F\text{-}CM}$	Common signal rise/fall time (20%80%)	600		2500	ps
T_{D_MHL}	MHL Clock duty cycle	35	50	65	%

4.5 Power Consumption

Function	Power Consumption (mA)		
MIPI-to-HDMI	149mA @ 1080P 60Hz	110mA @ 720P 60Hz	78mA @ 480P 60Hz
MIPI-to-MHL	—	118mA @ 720P 60Hz	78mA @ 480P 60Hz
MIPI-to-LVDS	—	144mA @ 720P 60Hz	115mA @ 480P 60Hz

5.DETAILED DESCRIPTION

5.1 MIPI DSI Controller

LT8912 implements one clock lane and four DSI data lanes with polarity swappable, and may be configured to support one, two, three or four DSI datalanes per channel. Unused DSI input pins should be left unconnected or driven to LP11 state.The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream. DSIdata lanes are bit and byte aligned.LT8912 supports only Non-Burst mode video operation with Sync Events and continuous clock on clock lane.

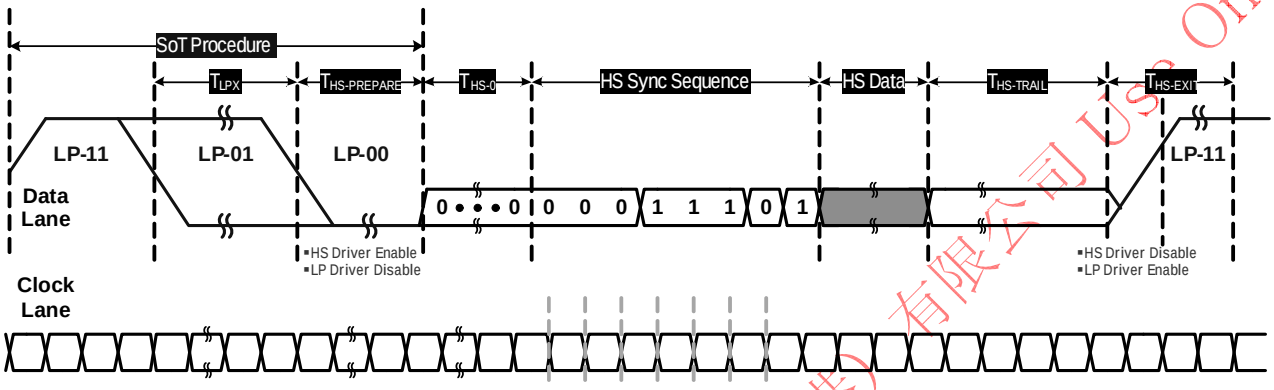


Fig 5.1.1 Switching Timing Between Low Power Mode and High SpeedMode in Video Mode

The DSI ControllerreceivesRx D-PHY signals, including LP mode data, 4 data-lane 8bit HS mode data and HS byte clock. Itthen merge 4-lane 8bit data into 32bit,decode MIPI packets and stores the video RGB data into the memory. The DSI controller can also rebuild display timing and put the video RGB data which are stored in the memory out to the display devices through the LVDS TX or HDMI TX.

The controller supports RGB666,RGB888,RGB666 loosely format data input from MIPI TX source. It supports 480P, 720P and 1080P VESA standard display format resolution output to LVDS or HDMI.The controller can also support dynamic adjusting PLL in order to send a stable video data and timing format to display device.

Fig5.1.1 shows the timing relation when MIPI receiver switches between Low-Power (LP) Mode and High-Speed Data Transmission (HSDP) Mode. LT8912 only supports video mode data transmission.

5.2 MIPI Rx D-PHY

MIPI Rx D-PHY has 4 data lanes and 1 clock lane, with each lane combiningHS-RX and LP-RX. Each HS-RX supports 80M to 1.5Gbps data rate, and the maximum data rate of LP-RX is 10 Mbps according to specification.

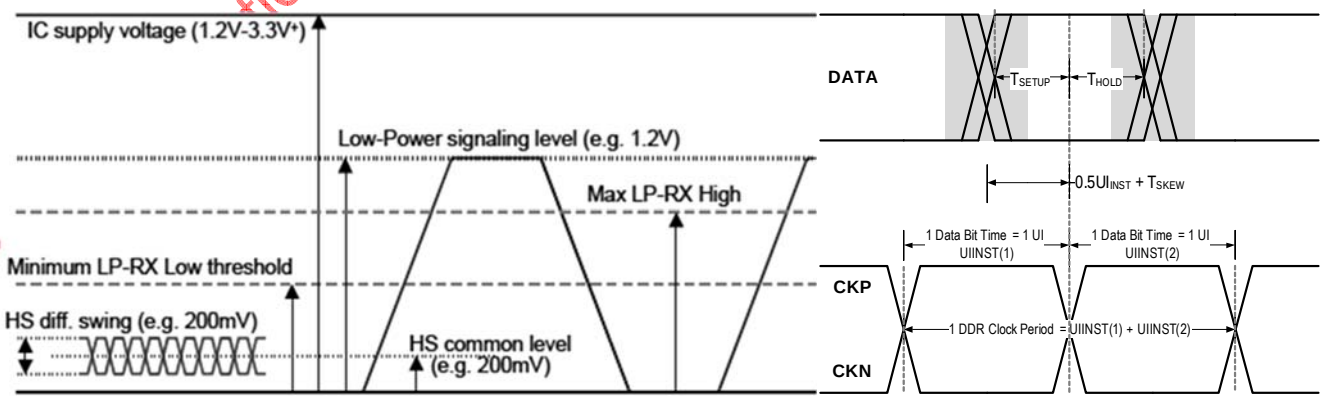


Fig 5.2.1 MIPI Rx D-PHY Electrical Parameter and Timing Definitions: (Left) Line Levels; (Right)DDR Clock and Data-to-Clock Timing

In High-Speed mode, each Lane is terminated on both sides and received a low-swing, differential signal. HS-RX will

convert the input serial data into 8-bit parallel data.RxEQ can compensate maximum 9dB attenuation introduced by PCB or cable.There is also internalpath to compensate the skew between data lane and clock lane toguarantee enough setup time and hold time.

In Low-Power mode, all wires are operated single-ended and non-terminated mode with a large swing, e.g. 1.2V. LP-RX shall be always working and monitoring line levels for working mode changing.

There is also on-chip Rterm Calibration scheme toensure differential input impedance between 80~125 Ω.

Table 5.2.1 MIPI DSI Rx PHY Clock and Data-Clock Timing Specifications

Clock Parameter	Symbol	Min	Tup	Max	Units	Notes
UI Instantaneous	UIINST			12.5	Ns	1,2
UI Variation	∆UI	-10%		10%	UI	3
		-5%		5%	UI	4
Data-Clock Skew @ Transmitter	$T_{SKEW[TX]}$	-0.15		0.15	UI_{INST}	5
		-0.20		0.20	UI_{INST}	6
Data-Clock Setup @ Receiver	$T_{SETUP[RX]}$	0.15			UI_{INST}	7
		0.20			UI_{INST}	8
Data-Clock Hold @ Receiver	$T_{HOLD[RX]}$	0.15			UI_{INST}	7
		0.20			UI_{INST}	8

1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst. The allowed instantaneous UI variation can cause instantaneous data rate variations.Therefore, devices should either accommodate these instantaneous variations with appropriateFIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminatethese instantaneous variations
3. When UI ≥ 1ns, within a single burst
4. When UI < 1ns, within a single burst
*5. Total silicon and package skew delay budget of 0.3*UI_{INST} *when D-PHY is supporting maximumdata rate = 1 Gbps.*
*6. Total silicon and package skew delay budget of 0.4*UI_{INST} *when D-PHY is supporting maximumdata rate > 1 Gbps.*
*7. Total setup and hold window for receiver of 0.3*UI_{INST} *when D-PHY is supporting maximum datarate = 1 Gbps.*
*8. Total setup and hold window for receiver of 0.4*UI_{INST} *when D-PHY is supporting maximum datarate > 1 Gbps.*

5.3 LVDS Controller

5.3.1 Display Interface

The display interface supports single (24-bit) pixel out format, and supports the 6-bit/color or 8-bit/color LCD panel. Built in internal PLL locking to the reference clock generates all of the display timing to various LCD panels.

5.3.2 Single Pixel LVDS Transmitter

The LVDS transmitter is designed to support single pixel data transmission between Scaler and Flat Panel Display. For single pixel mode, thetransmitter converts 24 bits (single Pixel 24-bit color) data into 4 LVDS (Low Voltage Differential Signaling) data streams. Control signals (VSYNC, HSYNC, DE and one user-defined signals) are sent during blanking intervals. LVDS transmitter can support the following mode:

1. Single pixel mode
2. 24-bit panel mapping to the LVDS channels
3. 18-bit panel mapping to the LVDS channels

5.3.3Panel Data Mappings

Table 5.3.1 Bit-Mapping 6 bit(5~0)+2 bit(7~6)

TCLK+

LVDS	Bit1	Bit0	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit6	Bit5
TX0	R1	R0	G0	R5	R4	R3	R2	R1	R0	G0	R5
TX1	G2	G1	B1	B0	G5	G4	G3	G2	G1	B1	B0
TX2	B3	B2	DE	VS	HS	B5	B4	B3	B2	DE	VS
TX3	R7	R6	RSV	B7	B6	G7	G6	R7	R6	RSV	B7

Table 5.3.2 Bit-Mapping 6 bit(7~2)+2 bit(1~0)

TCLK+

LVDS	Bit1	Bit0	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit6	Bit5
TX0	R3	R2	G2	R7	R6	R5	R4	R3	R2	G2	R7
TX1	G4	G3	B3	B2	G7	G6	G5	G4	G3	B3	B2
TX2	B4	B3	DE	VS	HS	B7	B6	B5	B4	DE	VS
TX3	R1	R0	RSV	B1	B0	G1	G0	R1	R0	RSV	B1

5.4 LVDS TxPHY

LVDSTx PHY has 4 data lanes and 1 clock lane. It receives video data and timing from lvds controller to construct lvds data format for transmission. The highest data rate on every single data lane is 1.12Gbps depending on the setting of lane number and video data rate.The LVDS clock frequency is up to 160MHz. The LVDS signal swing can be set from 150mV to 500mV for different application environment and lower EMI.The common mode voltage of LVDS signal can be set from 0.8V to 1.4V to cover the requirement of different LVDS Rx. For detailed information please refer to LVDS DC and AC specification.

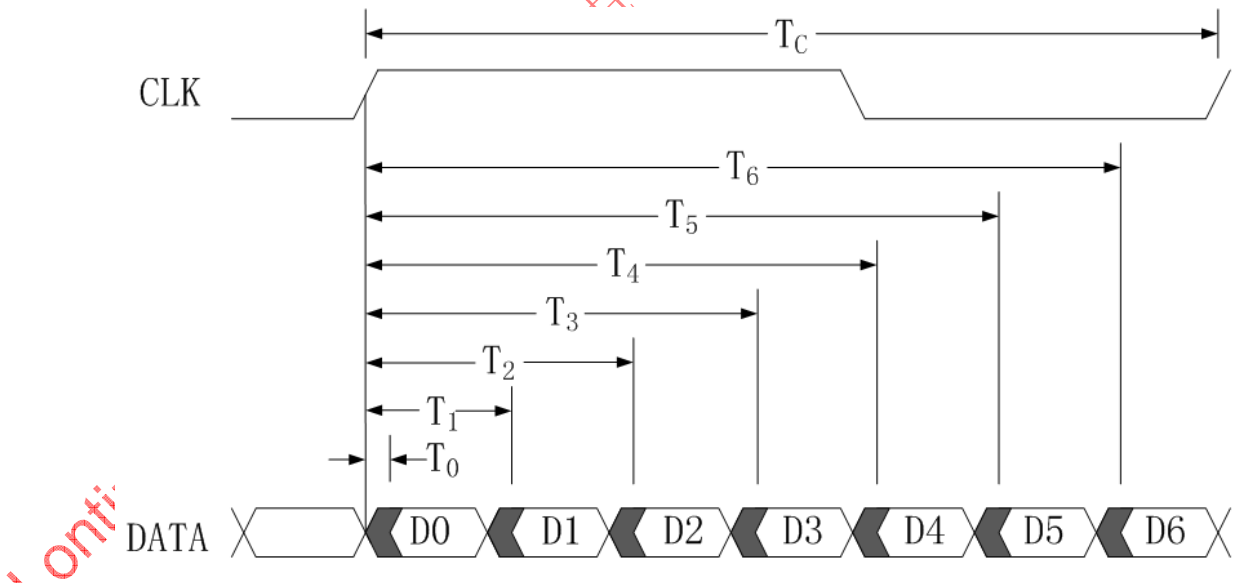


Fig 5.4.1 LVDS TxPHY Output Clock and Data Timing Diagram

5.5 HDMI/MHL Controller

5.5.1 Audio Data Capture Logic Block

The LT8912 device supports S/PDIF, 2 channel I2S audio interface as audio input. One I2S serial data input allows transmission of DVD-Audio and decoded Dolby Digital to A/V receivers and high-end displays. The interface supports 2-channel audio from 32 kHz to 192 kHz. The input clock (SCK) latches the incoming data.

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The S/PDIF input supports audio sampling rates from 32 to 192 kHz. No clock input is required for S/PDIF; the chip logic extracts the clock from the incoming S/PDIF data stream. Stream frequency information is automatically extracted from incoming stream headers.

5.5.2 HDMI Process Block

The HDMI processor block takes the video data from the video capture block and the audio data from the audio FIFO. Packet generator block and merges with the video data to form the HDMI link frame. The TMDS encoder performs 8 to10 bit TMDS encoding on the audio/video data. This data is output to three TMDS differential data lines along with a TMDS differential clock. The link data is encoded with the TMDS encoder and traverses an output FIFO to perform clock domain conversion. The output of the FIFO is synchronized with the 'tx_read_clk' from the transmitter analog core.

5.5.3MHL Transmitter Block

The LT8912 MHL transmitter digital core multiplexes video and audio data into the MHL stream and performs TMDS encoding. Multiple logical channels are multiplexed onto one physical channel, where the bit stream is then modulated by a clock signal running at a fixed ratio to the video pixel rate, and then transmitted to the MHL receiver. The video modes are supported up to 75 MHz MHL clock.

In addition, the MHL transmitter carries a single-wire control bus called CBUS, which replaces the DDC bus used in a standard DVI connection. It also supports the MHL Sideband Channel (MSC) that provides high-level control functions between the MHL transmitter and the receiver.

Finally, the MHL transmitter has a dedicated VBUS pin and associated ground pin to provide power to the MHL receiver or to receive power from the receiver.

5.6 HDMI/MHL TxPHY

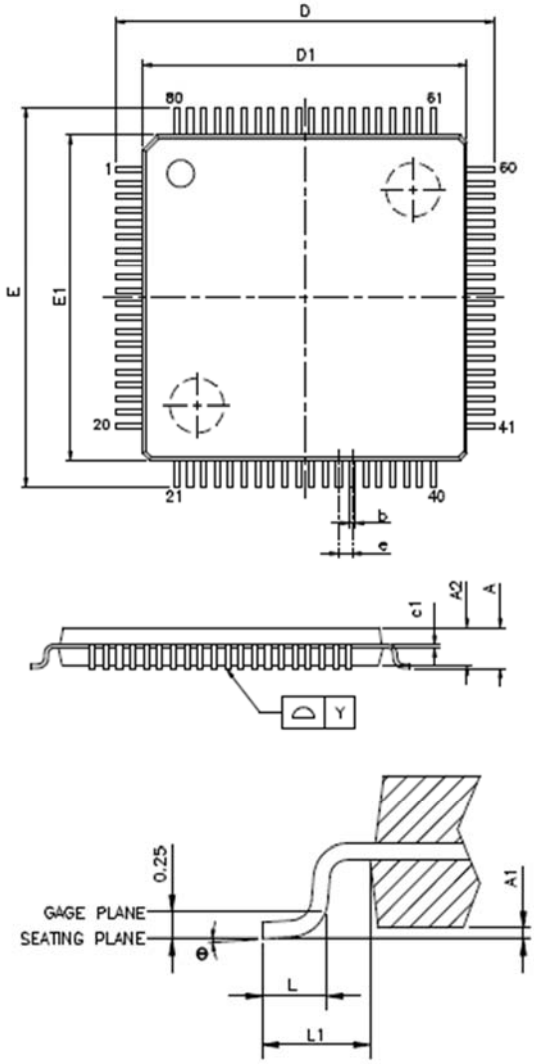
HDMI TxPHY is compliant with HDMI1.4 standard .It can support up to 60Hz 1080p 8-bit HDMI output. The swing of TMDS signal can be set from 400mV to 600mV. There is a pre-emphasis function in the PHY which could help to compensate the attenuation of signal caused by a long cable. With the inner HPD circuit , the PHY can detect the attendance or absence of RX terminal instantly.

MHL is compliant with MHL2.0 standard. It can support up to 60Hz 720p 8-bit MHL output. As same as HDMI Tx PHY, the swing of data and clock signal can be set by registers. There are also pre-emphasis and HPD functions in the MHL Tx PHY. For detailed information, please refer to the HDMI and MHL DC and AC specification.

6. PACKAGE INFORMATION

6.1 Package

The LT8912 is available in both LQFP80 12x 12x1.4mm package and QFN64 7.5x 7.5x0.75mm.

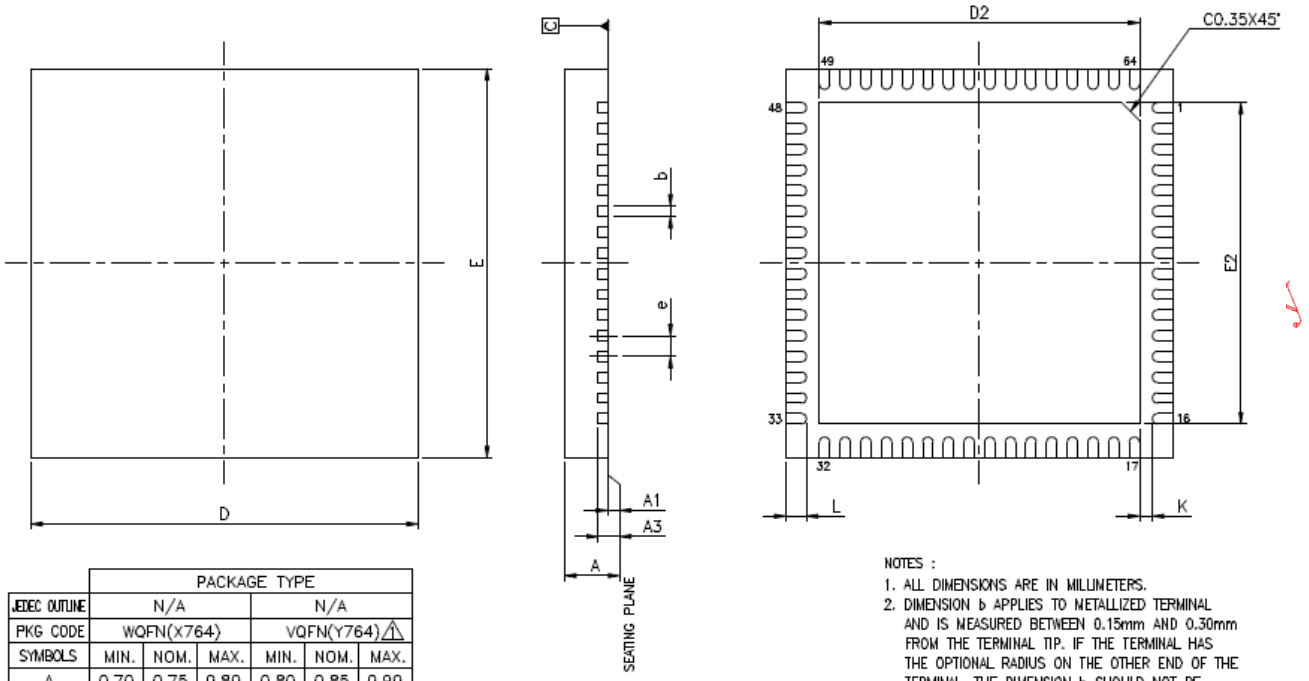


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	14 BSC	
D1	12 BSC	
E	14 BSC	
E1	12 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	
Y	—	0.08
θ	0°	7°

NOTES:
1.JEDEC OUTLINE:MS-026 BDD
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Fig6.1 LT8912 LQFP80 12mmx12mm Package



	PACKAGE TYPE					
JEDEC OUTLINE	N/A			N/A		
PKG CODE	WQFN(X764)			VQFN(Y764)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	7.50 BSC			7.50 BSC		
E	7.50 BSC			7.50 BSC		
e	0.40 BSC			0.40 BSC		
L	0.30	0.40	0.50	0.30	0.40	0.50
K	0.20	—	—	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X252 MIL	6.10	6.20	6.25	6.10	6.20	6.25	X	V	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Fig6.2 LT8912B QFN64 7.5mmx7.5mm Package

6.2 Recommended footprint

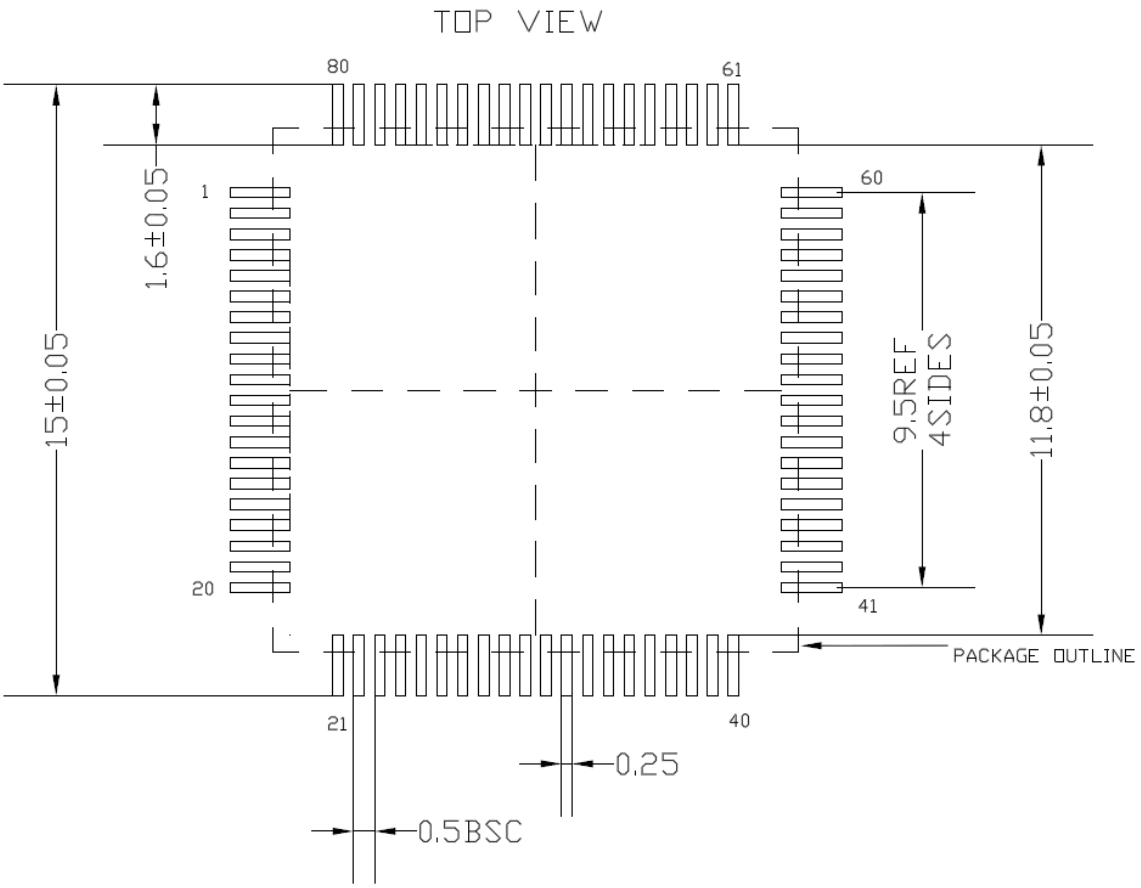


Fig6.3 LT8912 LQPF80 12mmx12mm recommended footprint

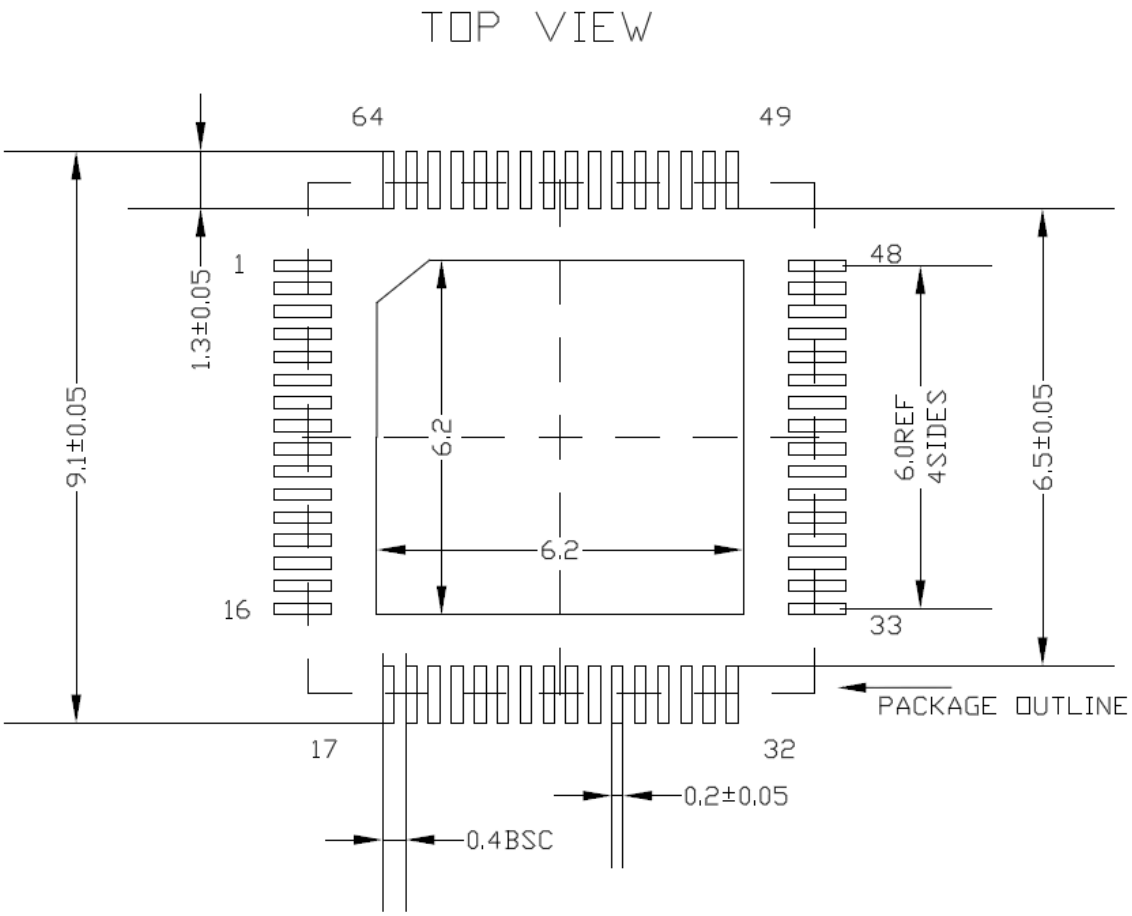
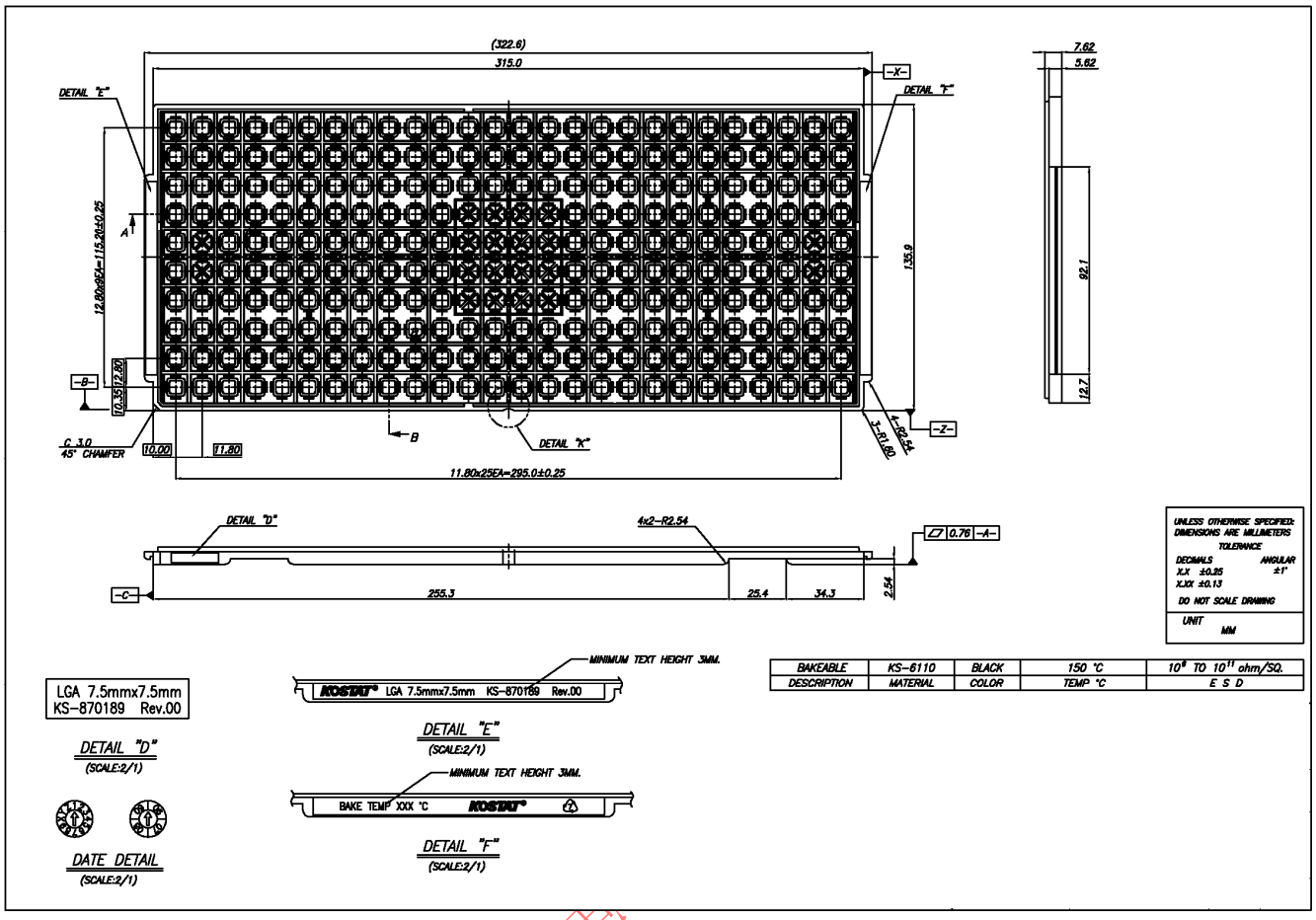
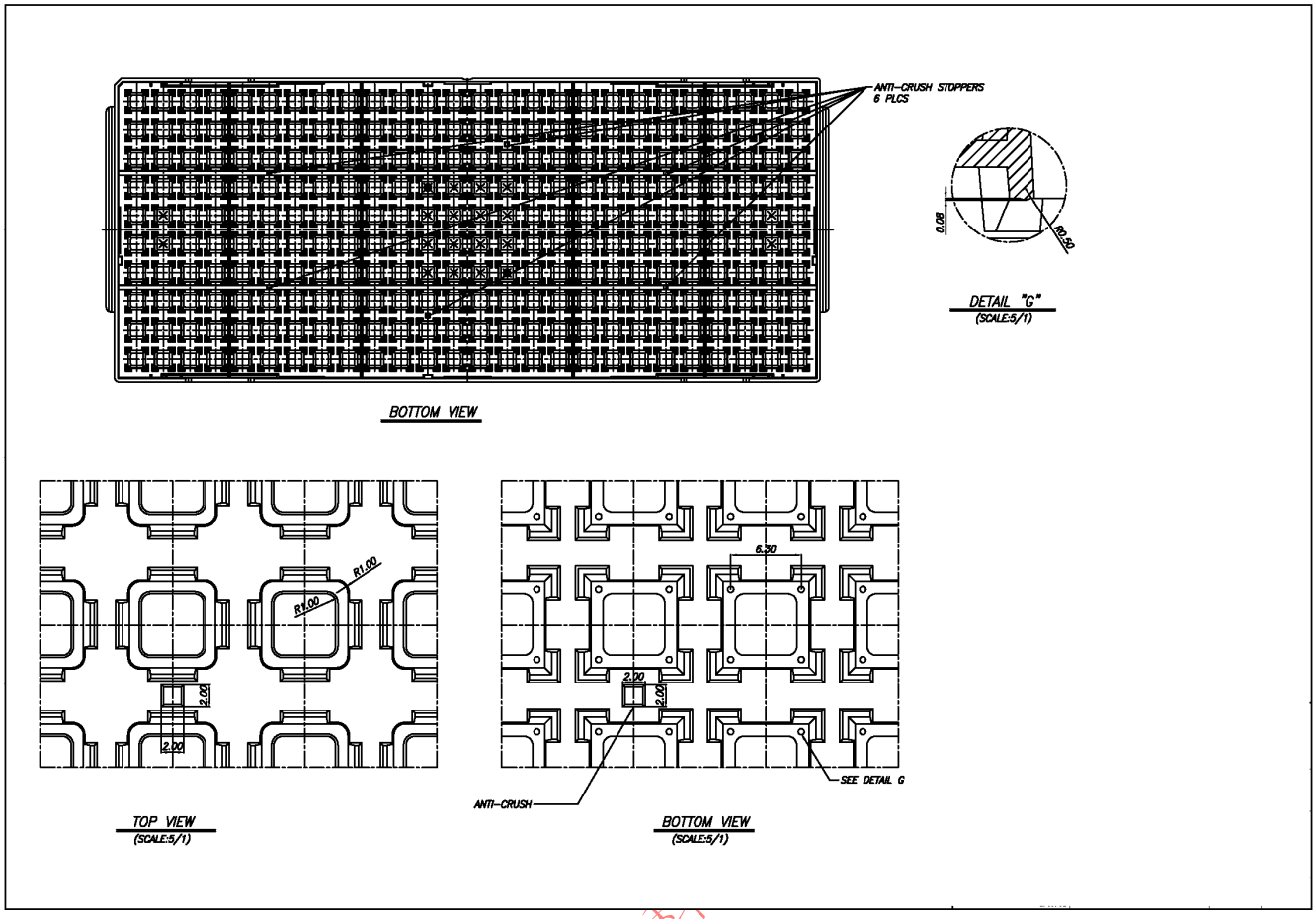


Fig6.4 LT8912B QFN64 7.5mmx7.5mm recommended footprint

6.3 Tape and Reel Information





MSL: Level-3

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