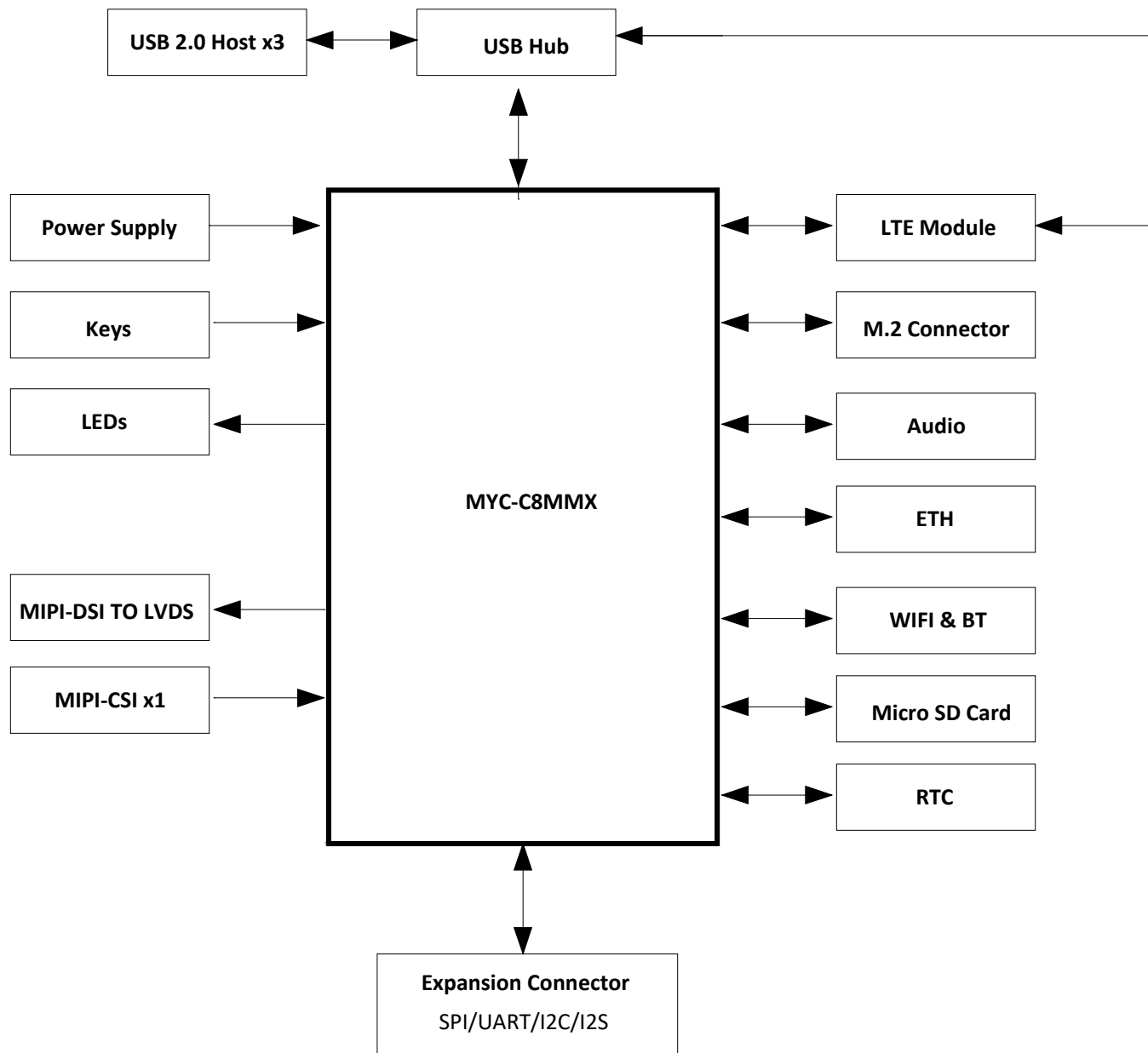
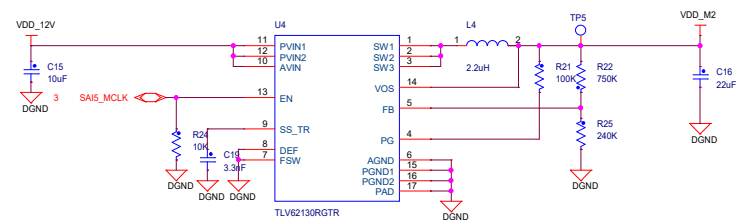
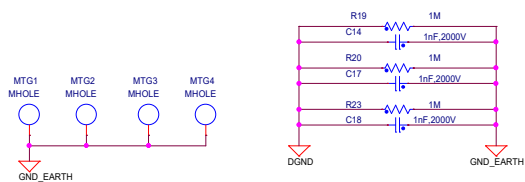
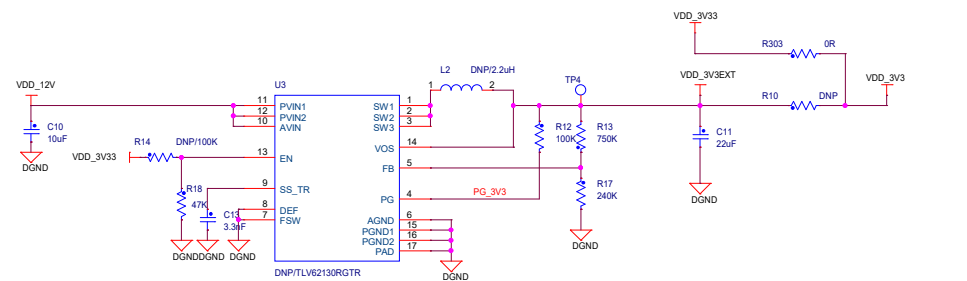
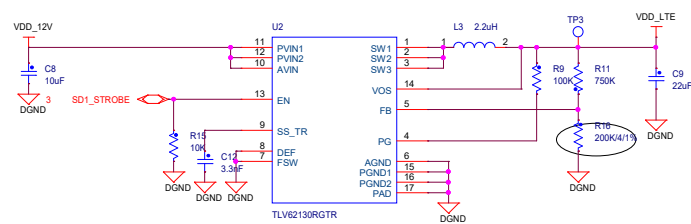
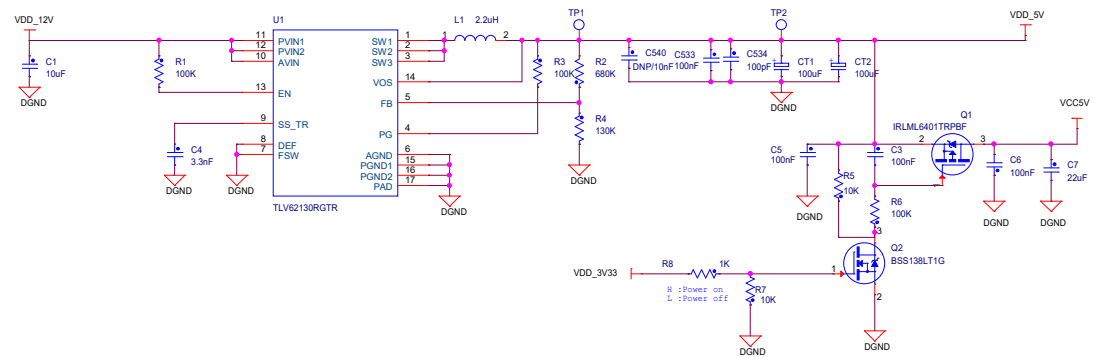


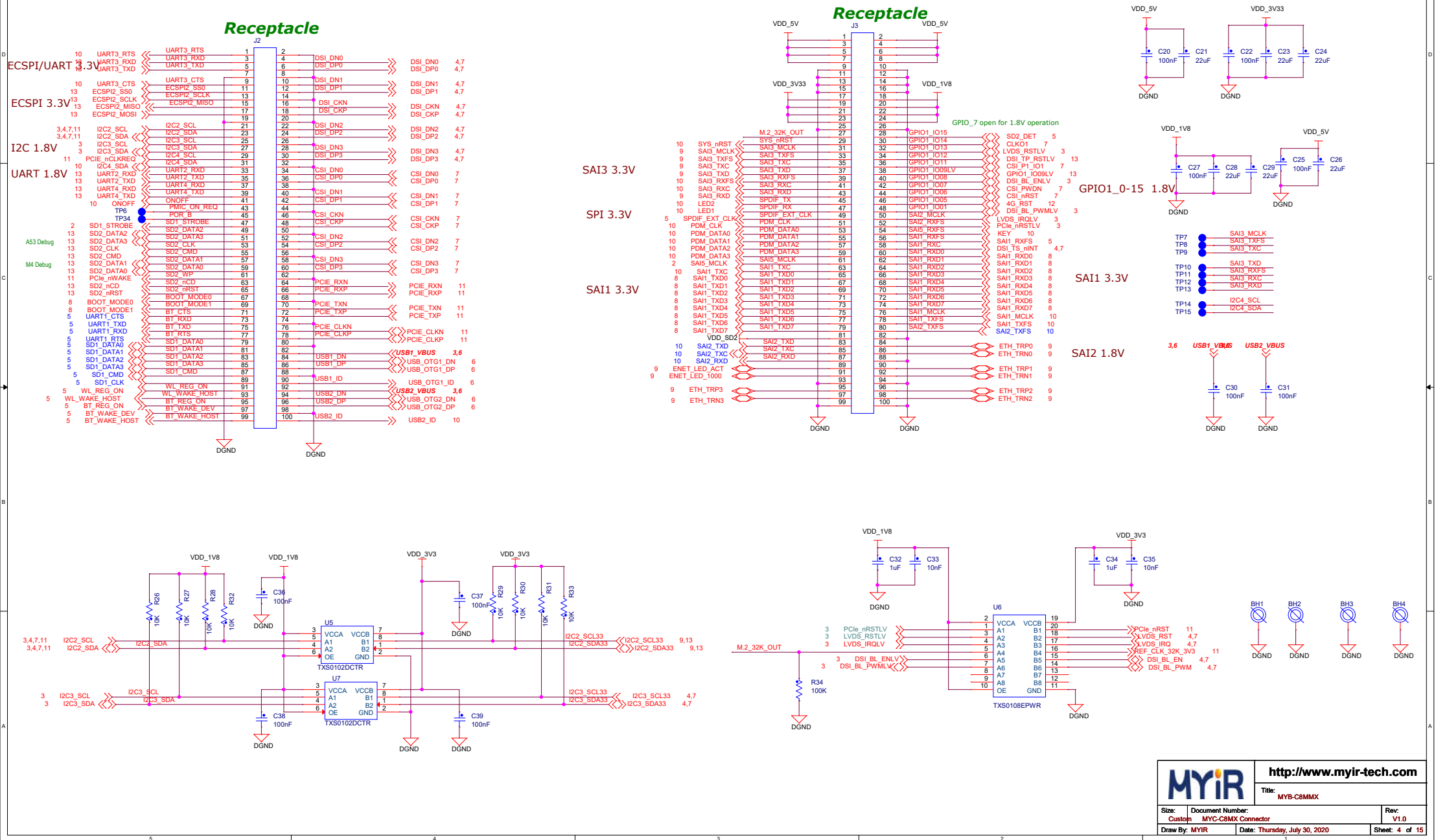
# MYB-C8MMX\_V1.0 修改说明

项目	修改内容	修改原因	处理结果
1	减少编码开关	编码太多	OK
2	触摸中断脚更换IO（GPIO1_09改为SAI1_RXC）	GPIO1_09电平是1.8V经过电平转换3.3V还不是做中断脚用。	OK
3	J2 J3位置不对	修改设计	OK
4	把R47 R43 R44电阻10K改为NC	修改设计	OK
5	把R144 1K改为0R R145去掉 C90 47nF改为15pF	修改设计	OK
6			
修改人：霍军其		审核人：	

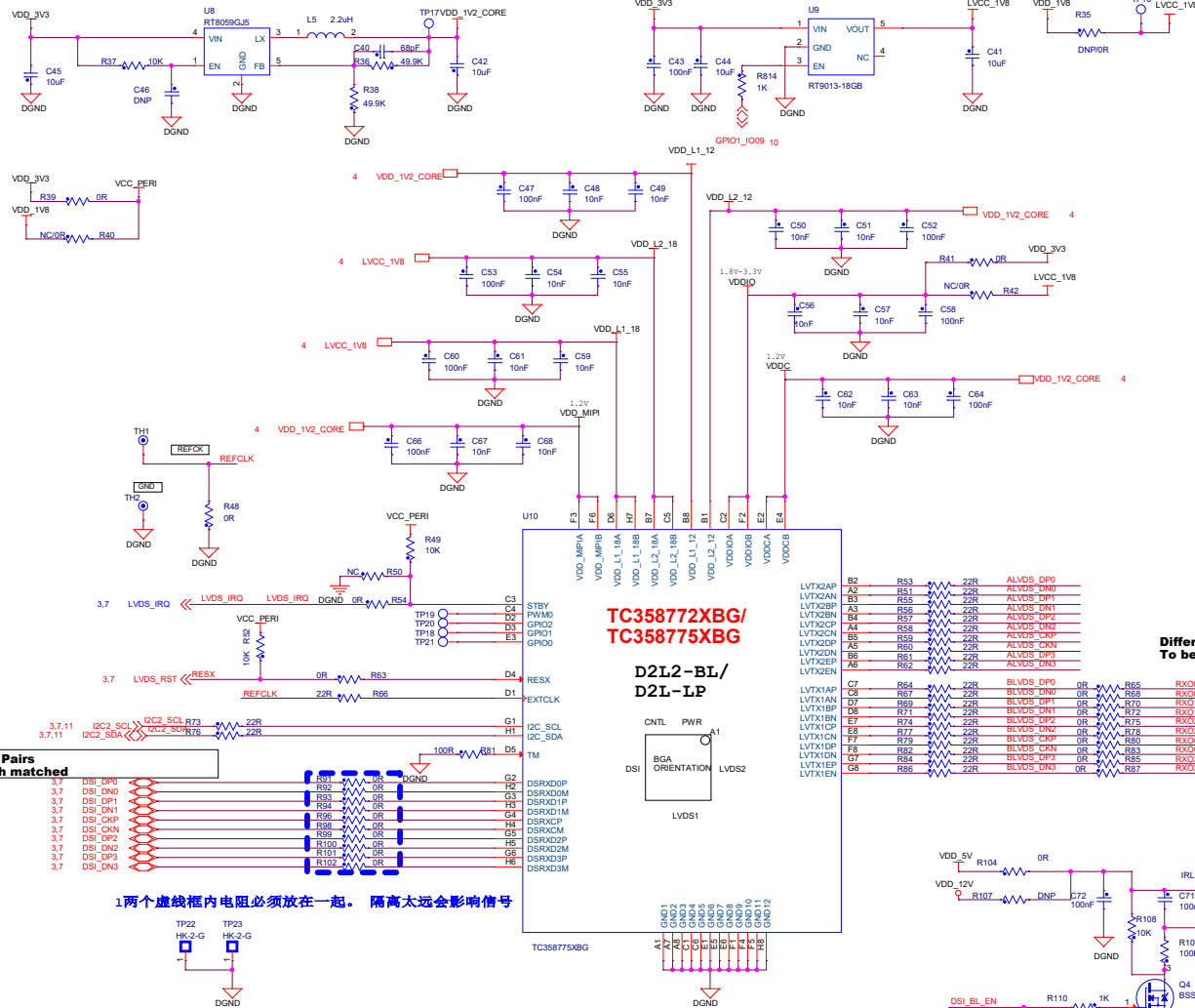




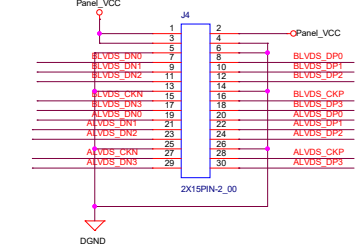
## IO connector



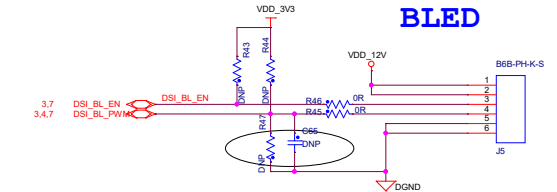
# DSI TO LVDS



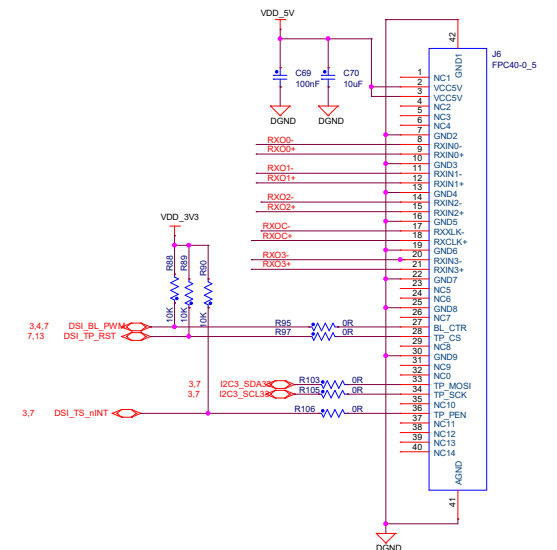
## LVDS Connector



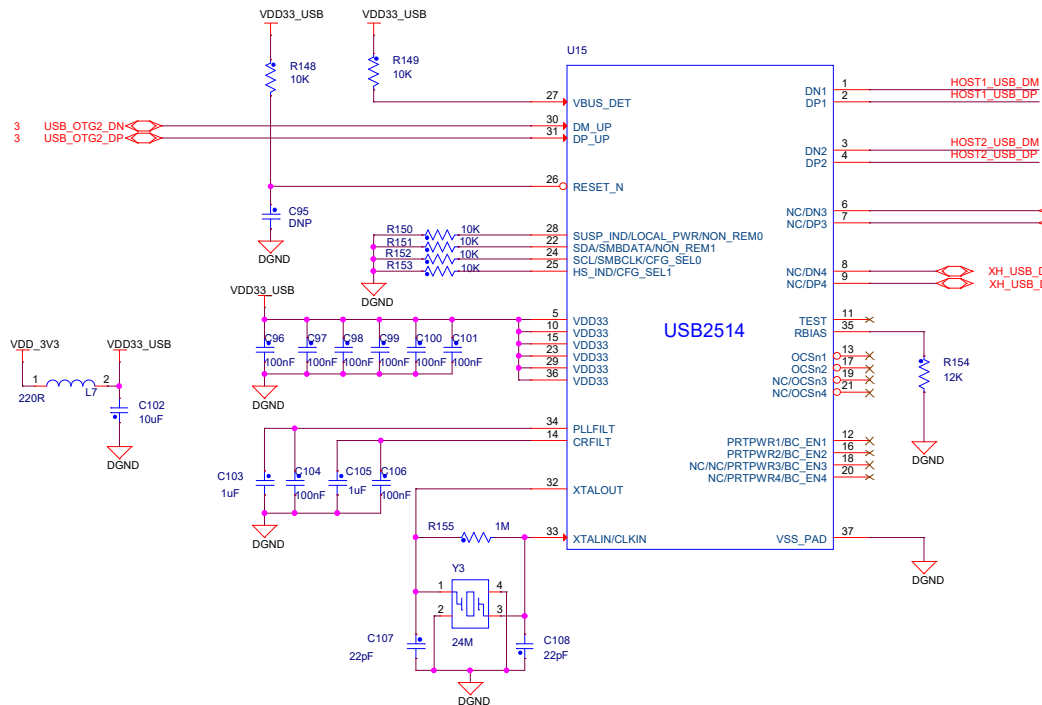
**BLED**



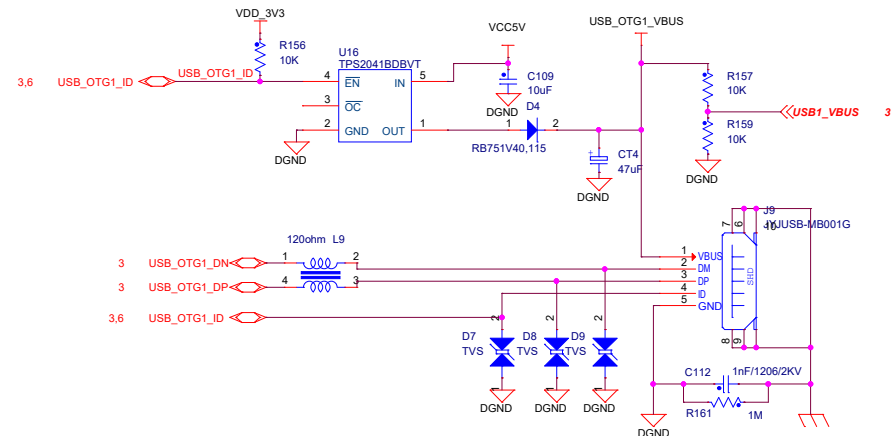
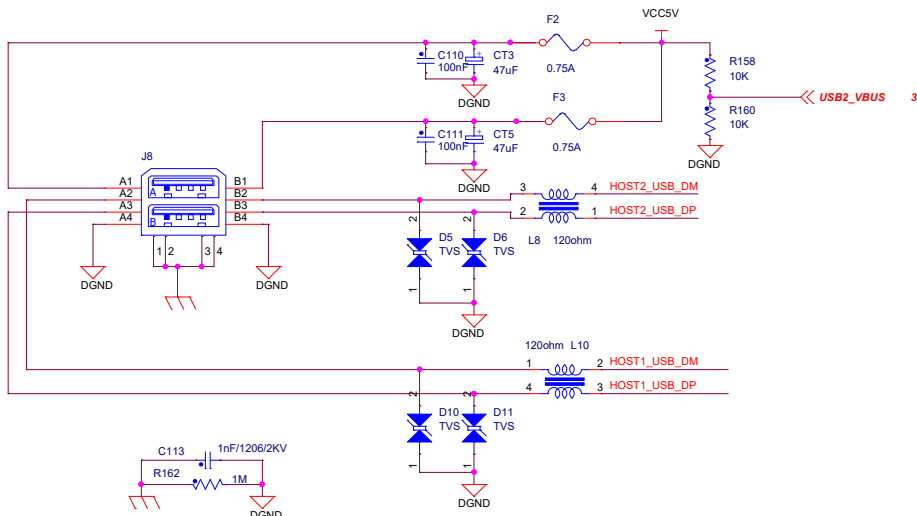
## 10.1' LVDS LCD



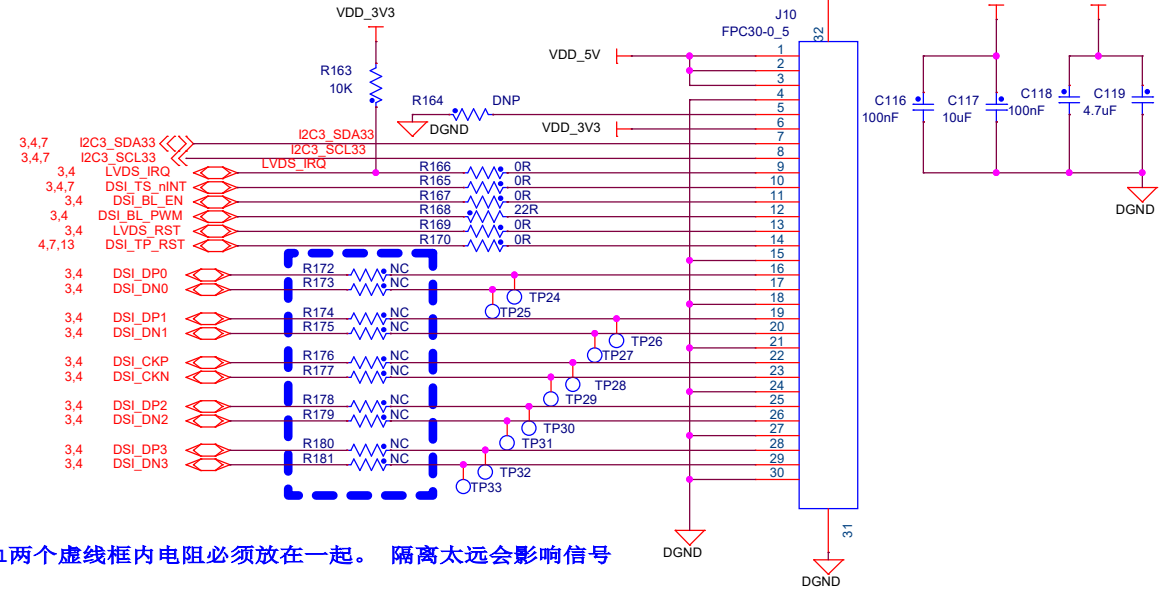




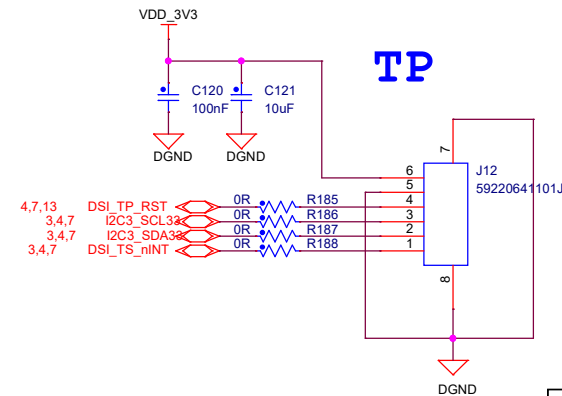
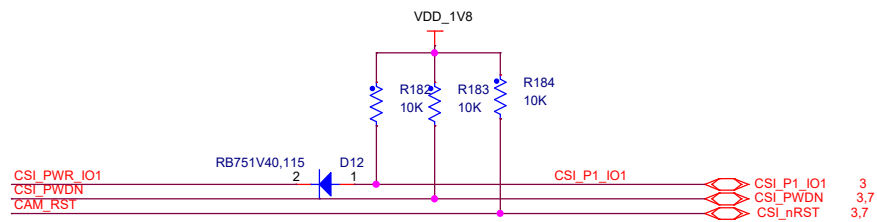
## USB HOST



## MIPI LCD



1两个虚线框内电阻必须放在一起。 隔离太远会影响信号

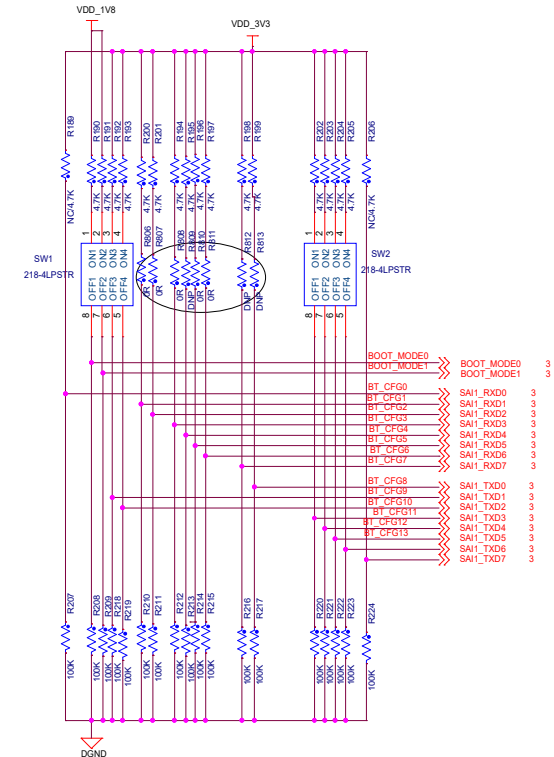




# Boot Mode and CFG Switch

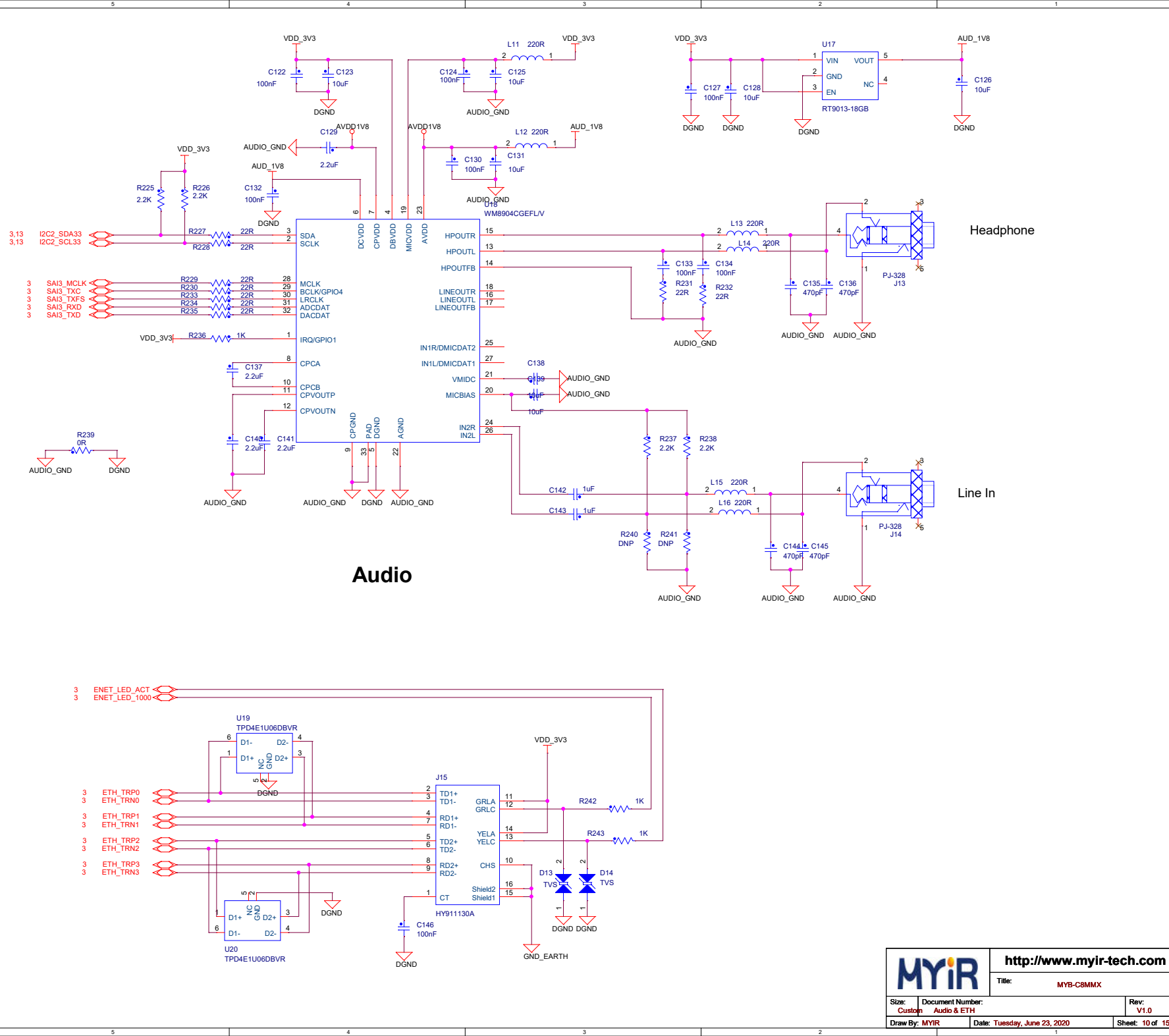
## i.MX8M Mini ROM Fuse

Address		7	6	5	4	3	2	1	0	
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	
	0x470[15:8]	Infiniit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR5 and SDR104 only) '0' - through SD pad '1' - direct	
	0x470[15:8]		010 - MMC/eMMC							
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5		
	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSP1 001 - eCSP2 010 - eCSP3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	
	0x470[15:8]	Others - Reserved for future use								
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]	
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved		Reserved		
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V	
	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.				Reserved	
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle				
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	



## BMODE

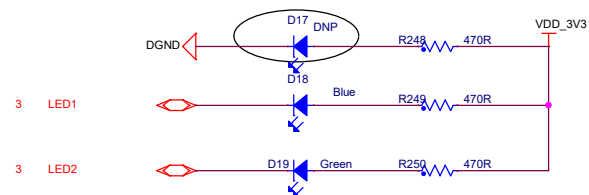
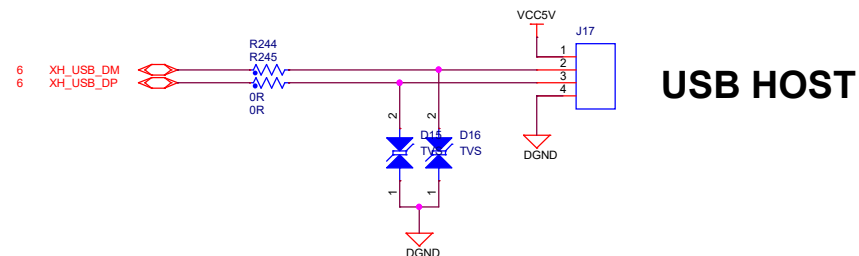
BOOT_MODE1	BOOT_MODE0
<b>BOOT TYPE:</b>	
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

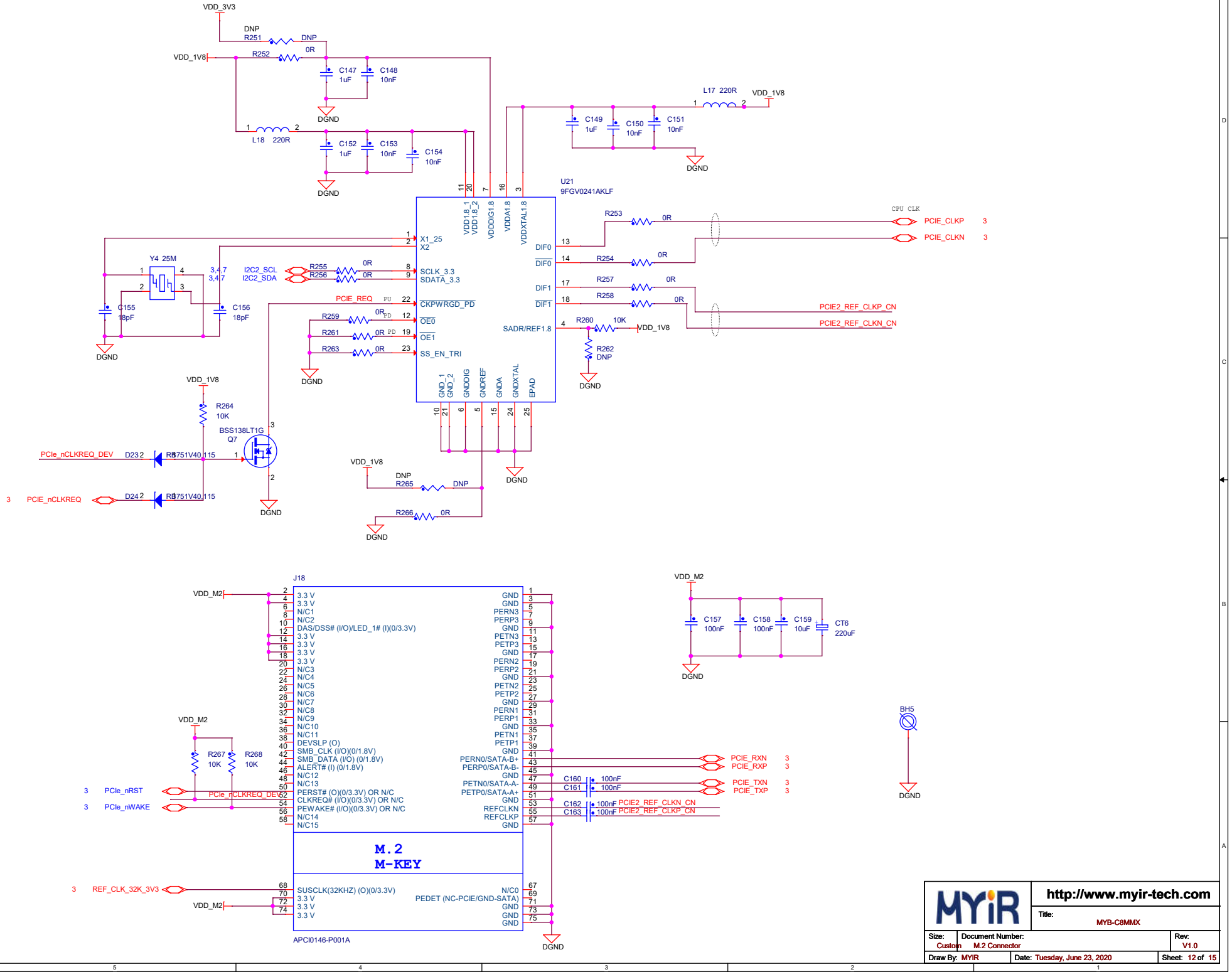


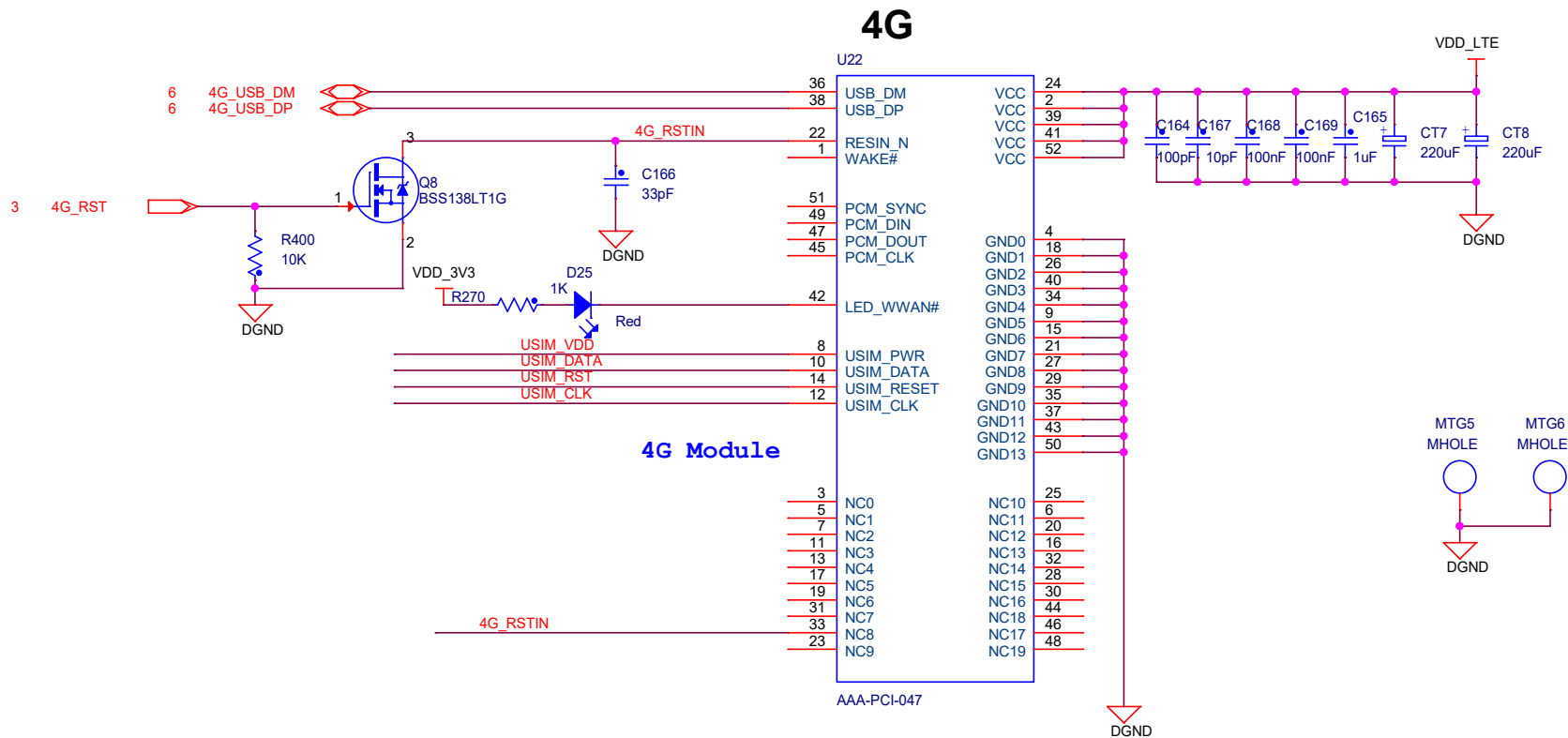
Audio

Headphone

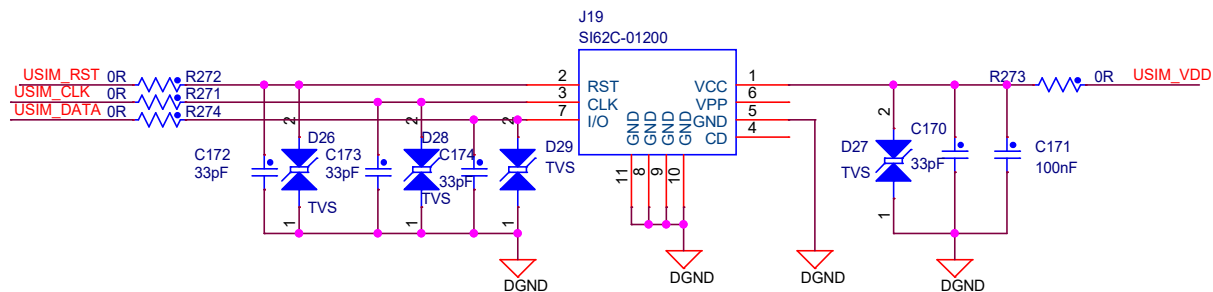
Line In







## Micro SIM Card



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Title: MYB-C8MMX

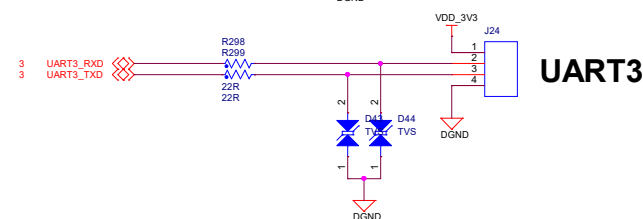
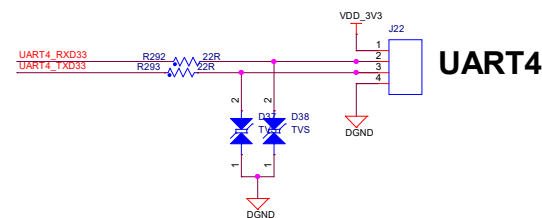
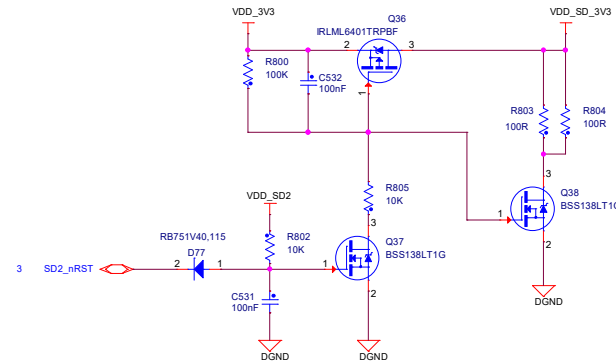
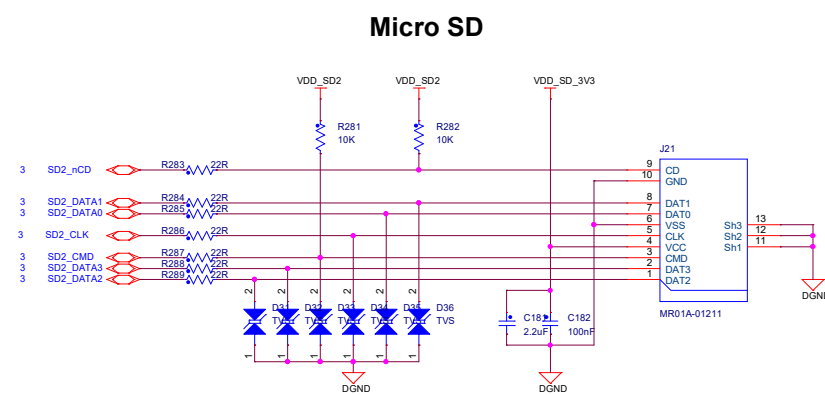
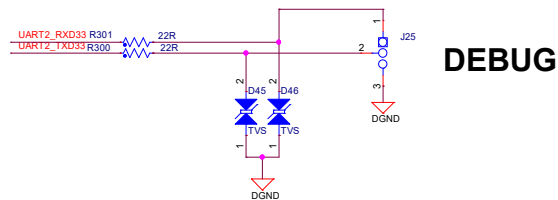
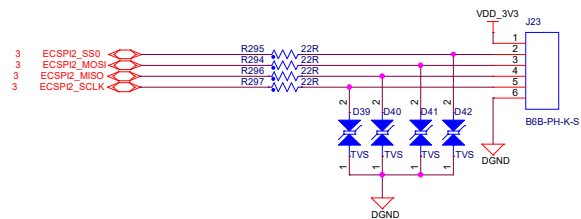
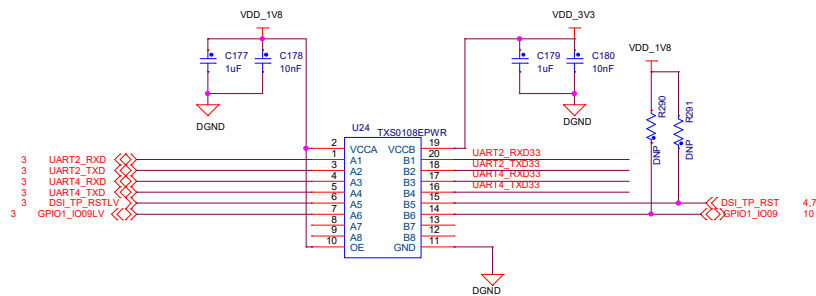
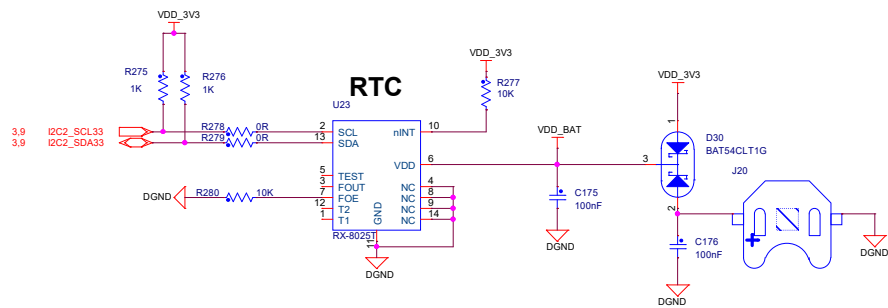
Size: Custom  
Document Number: Mini PCIe Connector

Rev: V1.0

Draw By: MYIR


Date: Tuesday, June 23, 2020

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## i.MX 8M MINI IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
TEST_MODE	test_mode	test_mode	test_mode						
BOOT_MODE0	comcarcopdmix BOOT_MODE0[0]	comcarcopdmix BOOT_MODE0[0]	comcarcopdmix BOOT_MODE0[0]						
BOOT_MODE1	comcarcopdmix BOOT_MODE0[1]	comcarcopdmix BOOT_MODE0[1]	comcarcopdmix BOOT_MODE0[1]						
UTAG_MODE	<tag_wrapper.MODE	<tag_wrapper.MODE	<tag_wrapper.MODE						
UTAG_READY_B	<tag_wrapper.READY_B	<tag_wrapper.READY_B	<tag_wrapper.READY_B						
UTAG_T01	<tag_wrapper.T01	<tag_wrapper.T01	<tag_wrapper.T01						
UTAG_T02	<tag_wrapper.T02	<tag_wrapper.T02	<tag_wrapper.T02						
UTAG_T03	<tag_wrapper.T03	<tag_wrapper.T03	<tag_wrapper.T03						
UTAG_T04	<tag_wrapper.T04	<tag_wrapper.T04	<tag_wrapper.T04						
UTAG_T05	<tag_wrapper.T05	<tag_wrapper.T05	<tag_wrapper.T05						
UTAG_T06	<tag_wrapper.T06	<tag_wrapper.T06	<tag_wrapper.T06						
UTAG_T07	<tag_wrapper.T07	<tag_wrapper.T07	<tag_wrapper.T07						
UTAG_T08	<tag_wrapper.T08	<tag_wrapper.T08	<tag_wrapper.T08						
UTAG_T09	<tag_wrapper.T09	<tag_wrapper.T09	<tag_wrapper.T09						
UTAG_T10	<tag_wrapper.T10	<tag_wrapper.T10	<tag_wrapper.T10						
UTAG_T11	<tag_wrapper.T11	<tag_wrapper.T11	<tag_wrapper.T11						
UTAG_T12	<tag_wrapper.T12	<tag_wrapper.T12	<tag_wrapper.T12						
UTAG_T13	<tag_wrapper.T13	<tag_wrapper.T13	<tag_wrapper.T13						
UTAG_T14	<tag_wrapper.T14	<tag_wrapper.T14	<tag_wrapper.T14						
UTAG_T15	<tag_wrapper.T15	<tag_wrapper.T15	<tag_wrapper.T15						
ENET_MODE	enet1.MODE	enet1.MODE	enet1.MODE						
ENET_T01	enet1.T01	enet1.T01	enet1.T01						
ENET_T02	enet1.T02	enet1.T02	enet1.T02						
ENET_T03	enet1.T03	enet1.T03	enet1.T03						
ENET_T04	enet1.T04	enet1.T04	enet1.T04						
ENET_T05	enet1.T05	enet1.T05	enet1.T05						
ENET_T06	enet1.T06	enet1.T06	enet1.T06						
ENET_T07	enet1.T07	enet1.T07	enet1.T07						
ENET_T08	enet1.T08	enet1.T08	enet1.T08						
ENET_T09	enet1.T09	enet1.T09	enet1.T09						
ENET_T10	enet1.T10	enet1.T10	enet1.T10						
ENET_T11	enet1.T11	enet1.T11	enet1.T11						
ENET_T12	enet1.T12	enet1.T12	enet1.T12						
ENET_T13	enet1.T13	enet1.T13	enet1.T13						
ENET_T14	enet1.T14	enet1.T14	enet1.T14						
ENET_T15	enet1.T15	enet1.T15	enet1.T15						
SDI_CLK	usdh01.CLK	usdh01.CLK	usdh01.CLK						
SDI_DATA0	usdh01.DATA0	usdh01.DATA0	usdh01.DATA0						
SDI_DATA1	usdh01.DATA1	usdh01.DATA1	usdh01.DATA1						
SDI_DATA2	usdh01.DATA2	usdh01.DATA2	usdh01.DATA2						
SDI_DATA3	usdh01.DATA3	usdh01.DATA3	usdh01.DATA3						
SDI_DATA4	usdh01.DATA4	usdh01.DATA4	usdh01.DATA4						
SDI_DATA5	usdh01.DATA5	usdh01.DATA5	usdh01.DATA5						
SDI_DATA6	usdh01.DATA6	usdh01.DATA6	usdh01.DATA6						
SDI_DATA7	usdh01.DATA7	usdh01.DATA7	usdh01.DATA7						
SDI_RESET_B	usdh01.RESET_B	usdh01.RESET_B	usdh01.RESET_B						
SDI_STROBE	usdh01.STROBE	usdh01.STROBE	usdh01.STROBE						
SD2_CS_B	usdh02.CS_B	usdh02.CS_B	usdh02.CS_B						
SD2_CMD	usdh02.CMD	usdh02.CMD	usdh02.CMD						
SD2_DATA0	usdh02.DATA0	usdh02.DATA0	usdh02.DATA0						
SD2_DATA1	usdh02.DATA1	usdh02.DATA1	usdh02.DATA1						
SD2_DATA2	usdh02.DATA2	usdh02.DATA2	usdh02.DATA2						
SD2_DATA3	usdh02.DATA3	usdh02.DATA3	usdh02.DATA3						
SD2_DATA4	usdh02.DATA4	usdh02.DATA4	usdh02.DATA4						
SD2_DATA5	usdh02.DATA5	usdh02.DATA5	usdh02.DATA5						
SD2_DATA6	usdh02.DATA6	usdh02.DATA6	usdh02.DATA6						
SD2_DATA7	usdh02.DATA7	usdh02.DATA7	usdh02.DATA7						

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	Title: <b>MYB-C8MMX</b>	
Size: <b>C</b>	Document Number: <b>IOMULX</b>	Rev: <b>V1.0</b>
Draw By: <b>MYIR</b>	Date: <b>Tuesday, June 23, 2020</b>	Sheet: <b>15 of 15</b>