MYC-C8MMX-V2

Product Manual

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History

Version	Author	Participants	Date	Description
V1.0	Dana		20211223	Initial Version

Contents

1. Overview

In response to industry applications and meet customers' demand for high-performance boards,MYIR launched the NXP company i.MX 8M Mini series processor development platform:MYD-C8MMX.

The development board adopts the form of a core board (MYC-C8MMX-V2) carrier board(MYB-C8MMX), which supports common communication and multimedia interfaces,such as Gigabit Ethernet, MIPI-DSI, MIPI-CSI, USB2.0, I2C, SPI, UART etc.We will provide Linux and Android 9 full package and supporting documentation to help guests reduce development difficulty to accelerate product development and shorten time to market.In the development stage, it is recommended to match the core board supporting evaluation suite MYD-C8MMX to accelerate the development.

Product resources download address: http://d.myirtech.com/MYD-C8MMX/

Evaluation suite, please visit: MYD-C8MMX Development Board | NXP i.MX 8M Mini ARM Board, Cortex-A53, Linux-Welcome to MYIR (myirtech.com)

The MYC-C8MMX-V2 series core board is based on the MYC-C8MMX-V1.4 core board, and the hardware interface is fully compatible.The appearance of MYC-C8MMX-V2 core board after this product upgrade is different from the previous version of the product, mainly reflected in the PCB silk screen update, as well as EMMC chip, PHY chip, SPI chip and crystal oscillator.

This is because some chips used on the old products are no longer suitable for continued use due to supply reasons, so these chips are replaced in the model upgrade.The replaced components and new products have been fully tested, Customers do not need to worry about the impact of the replacement.

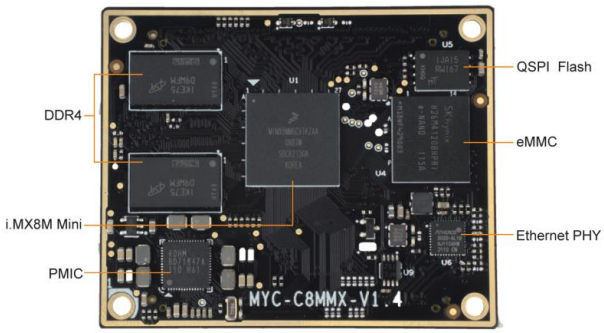

Figure 1-1 MYC-C8MMX-V1.4 Core board

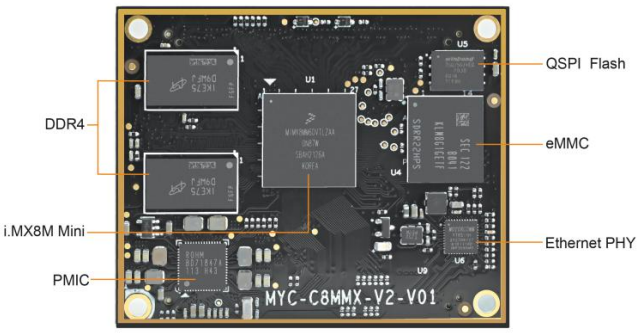

Figure 1-2 MYC-C8MMX-V2 Core board

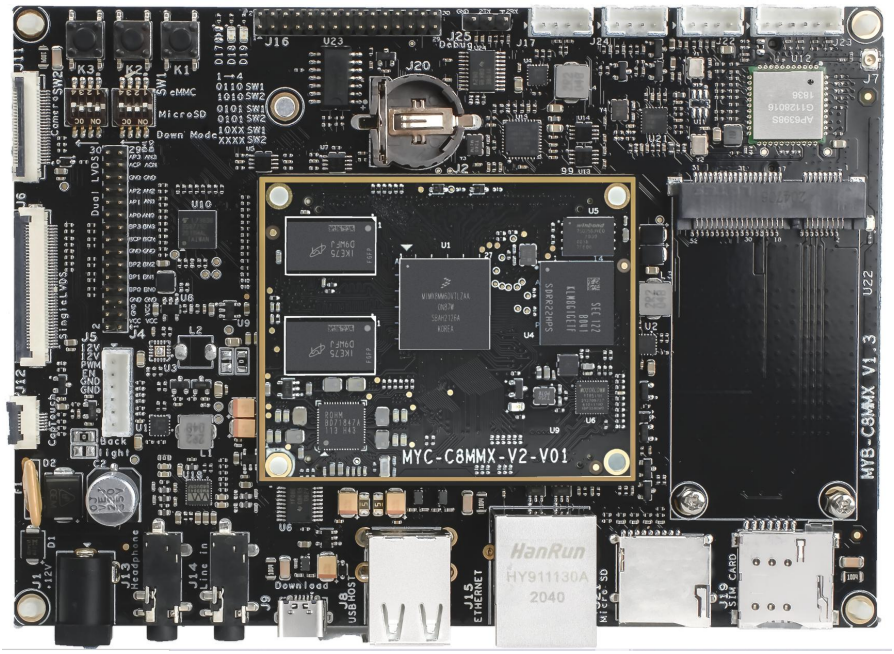

Figure 1-3 MYD-C8MMX Kit

2. Product Presentation

The MYC-C8MMX-V2 core board is designed with a high-density high speed circuit board, which integrates a processor, DDR4, EMMC, Ethernet, QSPI, PMIC power management circuit on a board with a size of 49x60mm.The processor supports the model of i.MX 8M Mini Dual / 8M mini Quad Lite / 8M Mini Quad Series.

The MYC-C8MMX-V2 series core board contains two standard product models: They have some differences in storage configuration, primary CPU specifications, etc., customers can choose the appropriate model based on demand.Differences between product models, see section 2.4.

2.1. CPU Introduction

The i.MX 8M Mini series integrates a high-performance Cortex-A53 + Cortex-M4 processor, the processor runs up to 1.8GHz, supports 16/32-bit LPDDR4 / DDR4 / DDR3L.The interior integrates power management, security units and rich interconnection interfaces with high performance, low power consumption, flexible memory options and high-speed interfaces as well as industry-leading audio and video capabilities. It provides a safe and high-performance solution for Internet of Things applications.

2.1.1. The i.MX8M Mini family

The i.MX 8M Mini family mainly includes Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite six processors.Quad, Dual, Solo represents the number of Cortex-A53 cores 4, 2, 1, Lite does not include VPU.Table 2-1, the Solo series processor is not listed in the table.

Family	Part Number	Configuration	Temperature
i.MX 8M Mini Quad	MIMX8MM6DVTLZAA	4x A53 (1.8Ghz), M4, GPU, VPU	0℃ - +95℃
i.MX 8M Mini Quad Lite	MIMX8MM5DVTLZAA	4x A53 (1.8Ghz), M4, GPU	0℃ - +95℃
i.MX 8M Mini Dual	MIMX8MM4DVTLZAA	2x A53 (1.8Ghz), M4, GPU	0℃ - +95℃
i.MX 8M Mini Quad	MIMX8MM6CVTKZAA	4x A53 (1.6Ghz), M4, GPU, VPU	-40℃ - +105℃
i.MX 8M Mini Quad Lite	MIMX8MM5CVTKZAA	4x A53((1.6Ghz)), M4, GPU	-40℃ - +105℃
i.MX 8M Mini Dual	MIMX8MM4CVTKZAA	2x A53((1.6Ghz)), M4, GPU	-40℃ - +105℃

Table 2-1 i.MX8M Mini family

i.MX8M Mini CPU features

● ARM Cortex-A53，Max frequency 1.8Ghz，ARM Cortex-M4 400Mhz
● 32/16 bit DRAM interface，support LP-DDR4, DDR4-2400,DDR3L-1600
● x1,8-bit NAND Flash
● x3,SPI NOR FLASH
● x1, PCIe Gen2
● X2 USB2.0 OTG controllers with integrated PHY Interfaces
● x3 uSDHC interface with MMC5.1 compliance
● x1 Gigabit Ethernet controller
● x4 UART, x4 I2C, x3 ECSPI
● Video Processing Unit 1080p60 VP9 Profile0,2 (10 bit) 1080p60 HEVC/H2.65 Decoder
● Graphic Processing Unit GCNanoUltra for 3D acceleration GC320 for 2D acceleration
● LCDIF Display Controller Support up to 2 layers of overlay Support up to 1080p60 display through MIPI DSI
● MIPI Interface 4 lane MIPI CSI interface 4 lane MIPI DSI interface
● Audio S/PDIF，x5 SAI
● FCBGA486, 0.5mm pitch, 14x14mm；

Table 2-2 i.MX8M Mini main features

For more information about the processor,please refer to NXP’s official documents:
https://www.nxp.com.cn/docs/en/data-sheet/IMX8MMIEC.pdf

2.2. Core Board Features

Item	features
Master chip series	i.MX 8M Mini Quad
Main control chip model	MIMX8MM6CVTKZAA (standard layout) MIMX8MM6DVTLZAA (standard layout)
Processor Specifications	x4 Cortex-A53、Cortex-M4、GPU、VPU
internal storage	DDR4 2GB
eMMC	eMMC 8GB
Core board size	60x49x1.2mm
interface type	B2B Connector
PCB board specifications	8-layer board design, gold immersion process
operating system	Linux 5.4.3/Linux 4.14.98

Table 2-3 Core board features

2.3. Block Diagram

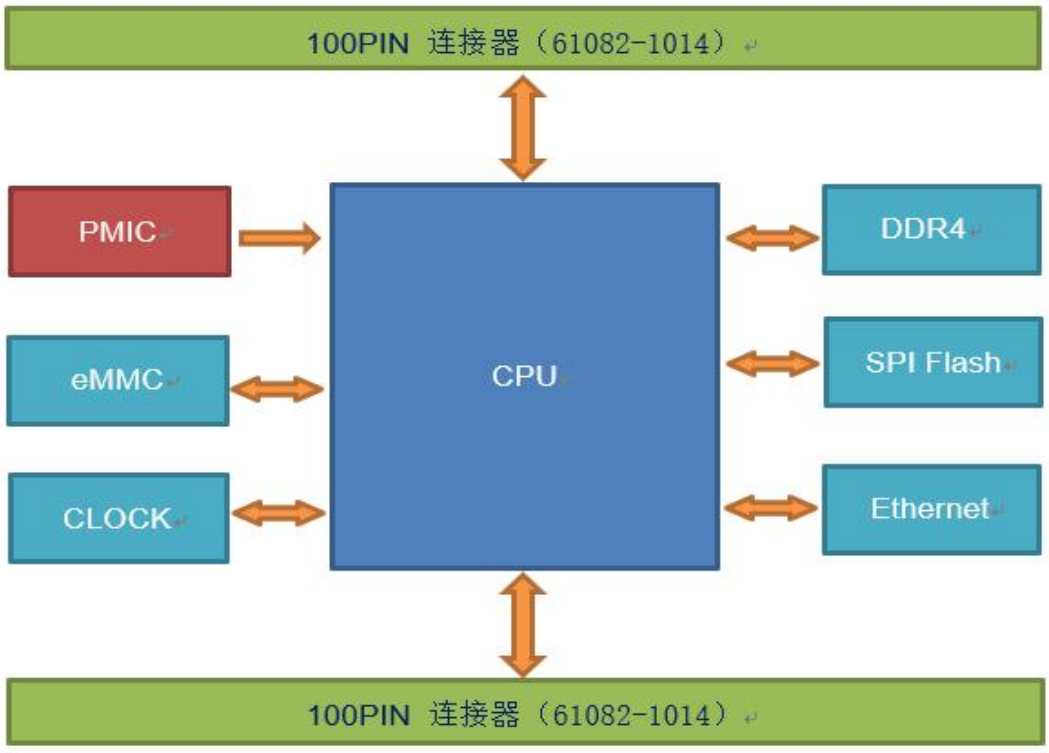

Figure 2-1 Core board block diagram

2.4. Core Board Ordering Information

According to the CPU model, operating temperature and other parameters, MYC-C8MMX-V2 core board standard products have two models, please select the most suitable model for you from the following list.For batch requirements, MYIR provides customized services, optional core board parameters.

Part No. / Item	MYC-C8MMQ6-V2-8E2D-160-I	MYC-C8MMQ6-V2-8E2D-180-C
CPU	MIMX8MM6CVTKZAA	MIMX8MM6DVTLZAA
CPU series	i.MX 8M Mini Quad	i.MX 8M Mini Quad
Core	4xCortex-A53 + Cortex-M4	4xCortex-A53 + Cortex-M4
Frequency	A53 1.6GHz, M4 200Mhz	A53 1.8GHz, M4 200Mhz
System	Linux 5.4.3/Linux 4.14.98	Linux 5.4.3/Linux 4.14.98
DDR	2GB	2GB
eMMC	8GB	8GB
Display Resolution	1920x1080p60 (MIPI DSI)	1920x1080p60 (MIPI DSI)
MIPI DSI	One interface with 4 lane	One interface with 4 lane
MIPI CSI	One interface with 4 lane	One interface with 4 lane
UART	4 (Max)	4 (Max)
USB OTG	2	2
Ethernet	1 RGMII / RMII	1 RGMII / RMII
I2C	4 (Max)	4 (Max)
SPI	3 (Max)	3 (Max)
GPIO	99	99
Power Supply	+5V	+5V
Mechanical size	60x49mm	60x49mm
Operating temperature	-40℃ - +75℃	0℃ - +70℃
Connector	200	200
Certification	CE ROHS	CE ROHS

Table 2-4 MYC-C8MMX-V2 core board ordering information

3. Pin Description

3.1. Pinout

The MYC-C8MMX-V2 core board and the carrier board are connected with the B2B connector.The part number of the connectors used on the core board is 61082-101400LF,and the corresponding model used on carrier board is 61083-101400LF

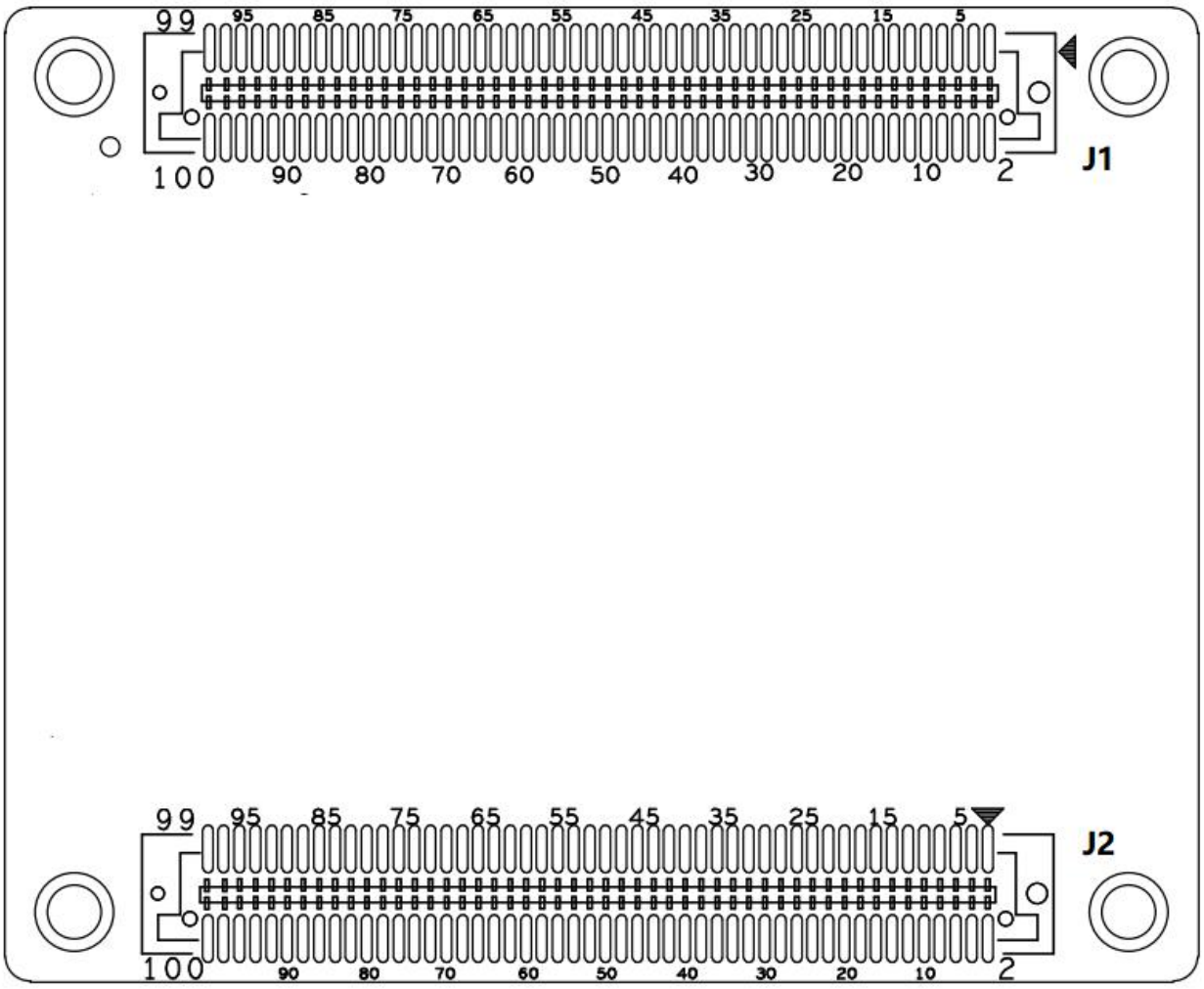

Figure 3-1 Module pin map (bottom side)

3.2. Pinlist

The MYC-C8MMX-V2 core board interface pin is defined as shown in the following table, and the pin function of the BSP development package is configured as the "default function" of the following table.If you need to change the Pin default function, modify the relevant driver configuration code, otherwise it will have an unsure abnormality such as device driver collision.

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J2	1	VDD_5V	POWER	5.0V power supply	5V	I		If VDD_3V33 and VDD_1V8 are used to supply the carrier board, the maximum output current of 5V power supply is recommended: 3A; If not used, maximum output current 2A
	2	VDD_5V	POWER	5.0V power supply	5V	I		
	3	VDD_5V	POWER	5.0V power supply	5V	I		
	4	VDD_5V	POWER	5.0V power supply	5V	I		
	5	VDD_5V	POWER	5.0V power supply	5V	I		
	6	VDD_5V	POWER	5.0V power supply	5V	I		
	7	VDD_5V	POWER	5.0V power supply	5V	I		
	8	VDD_5V	POWER	5.0V power supply	5V	I		
	9	DGND	DGND	GND	0V			
	10	DGND	DGND	GND	0V			
	11	DGND	DGND	GND	0V			
	12	DGND	DGND	GND	0V			
	13	DGND	DGND	GND	0V			
	14	DGND	DGND	GND	0V			
	15	DGND	DGND	GND	0V			
	16	DGND	DGND	GND	0V			
	17	VDD_3V33	VDD_3V33	3.3V output of SOC	3.3V	O		Can be used to supply power to the carrier board, and when used to supply power to the carrier board, VDD_3V33 Maximum output current: 2.5A VDD_1V8 Maximum output current: 1.5A
	18	VDD_1V8	VDD_1V8	1.8V output of SOC	1.8V	O		
	19	VDD_3V33	VDD_3V33	3.3V output of SOC	3.3V	O		
	20	VDD_1V8	VDD_1V8	1.8V output of SOC	1.8V	O		
	21	VDD_3V33	VDD_3V33	3.3V output of SOC	3.3V	O		
	22	VDD_1V8	VDD_1V8	1.8V output of SOC	1.8V	O		
	23	VDD_3V33	VDD_3V33	3.3V output of SOC	3.3V	O		
	24	VDD_1V8	VDD_1V8	1.8V output of SOC	1.8V	O		
	25	DGND	DGND	GND	0V			
	26	DGND	DGND	GND	0V			
	27	M.2_32K_OUT	M.2_32K_OUT	ANAMIX_REF_CLK_32K	1.8V	O	AG14	100K pull down

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	28	SD2_DET	GPIO	General GPIO1_IO15	1.8V	I/O	AB9	The default configuration is the output, Internal pull down
	29	SYS_nRST	SYS_nRST	Core board reset input	1.8V	I		Internal pull up
	30	CLKO1	CAM_P1_MCLK	CSI Master Clock	1.8V	O	AC9	
	31	SAI3_MCLK	SAI3	SAI3 Master Clock	3.3V	O	AD6	
	32	LVDS_RSTLV	GPIO	General GPIO1_IO1	1.8V	I/O	AD9	The default configuration is the output, Internal pull down
	33	SAI3_TXFS	SAI3	SAI3 frame clock	3.3V	O	AC6	
	34	DSI_TP_RSTLV	GPIO	General GPIO1_IO12	1.8V	I/O	AB10	The default configuration is the output, Internal pull down
	35	SAI3_TXC	SAI3	SAI3 bit clock	3.3V	O	AG6	
	36	CSI_P1_IO1	CSI_P1_IO1	CSI power control	1.8V	I/O	AC10	
	37	SAI3_TXD	SAI3	SAI3 data transmit	3.3V	O	AF6	
	38	GPIO1_09LV	GPIO	General GPIO1_IO09	1.8V	I/O	AF10	The default configuration is the input, Internal pull down
	39	SAI3_RXFS	GPIO	General GPIO4_IO28	3.3V	I/O	AG8	The default configuration is the input, Internal pull down
	40	DSI_BL_ENLV	GPIO	General GPIO1_IO08	1.8V	I/O	AG10	The default configuration is the input, Internal pull down
	41	SAI3_RXC	GPIO	General GPIO4_IO29	3.3V	I/O	AG7	The default configuration is the input, Internal pull down
	42	CSI_PWDN	CSI_PWDN	CSI Enable Control	1.8V	I/O	AF11	
	43	SAI3_RXD	GPIO	SAI3 data receive	3.3V	I/O	AF7	The default configuration is the input, Internal pull down
	44	CSI_Nrst	CSI_Nrst	CSI Reset	1.8V	I/O	AG11	
	45	LED2	GPIO	General GPIO5_IO03	3.3V	I/O	AF9	The default configuration is the output, Internal pull down
	46	4G_RST	GPIO	General GPIO1_IO05	1.8V	I/O	AF12	The default configuration is the output, Internal pull down
	47	LED1	GPIO	General GPIO5_IO04	3.3V	I/O	AG9	The default configuration is the output, Internal pull down
	48	DSI_BL_PWML	DSI_BL_PWM	LCD Backlight	1.8V	O	AF14	

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
		V		adjustment				
	49	SPDIF_EXT_CLK	CLK_REQ	WIFI Clock Request	3.3V	I	AF8	
	50	LVDS_IRQLV	LVDS_IRQLV	LVDS IRQ	1.8V	O	AD19	
	51	PDM_CLK	GPIO	General GPIO3_IO20	3.3V	I/O	AC15	The default configuration is the input, Internal pull down
	52	PCIe_nRSTLV	PCIe_nRSTLV	PCIE Interface Reset	1.8V	O	AC19	
	53	PDM_DATA0	GPIO	General GPIO3_IO21	3.3V	I/O	AD18	The default configuration is the input, Internal pull down
	54	KEY	GPIO	General GPIO3_IO19	3.3V	I/O	AB15	The default configuration is the input, 10K pull up to 3.3V
	55	PDM_DATA1	GPIO	General GPIO3_IO22	3.3V	I/O	AC14	The default configuration is the input, Internal pull down
	56	SAI1_RXFS	SAI1_RXFS	WIFI power control	3.3V	I/O	AG16	
	57	PDM_DATA2	GPIO	General GPIO3_IO23	3.3V	I/O	AD13	The default configuration is the input, Internal pull down
	58	DSI_TS_nINT	DSI_TS_nINT	Disruption of the touch screen	3.3V	I	AF16	The default configuration is the input, 10K pull up to 3.3V
	59	PDM_DATA3	GPIO	General GPIO3_IO24	3.3V	I/O	AC13	The default configuration is the input, Internal pull down
	60	SAI1_RXD0	BOOT CFG0	Boot mode configuration pin	1.8V	I	AG15	
	61	SAI5_MCLK	GPIO	General GPIO3_IO25	3,.3V	I/O	AD15	The default configuration is the input, Internal pull down
	62	SAI1_RXD1	BOOT CFG1	Boot mode configuration pin	1.8V	I	AF15	
	63	SAI1_TXC	GPIO	General GPIO4_IO11	3.3V	I/O	AC18	The default configuration is the input, Internal pull down
	64	SAI1_RXD2	BOOT CFG2	Boot mode configuration pin	3.3V	I	AG17	
	65	SAI1_TXD0	BOOT CFG8	Boot mode configuration pin	3.3V	I	AG20	
	66	SAI1_RXD3	BOOT CFG3	Boot mode configuration pin	3.3V	I	AF17	
	67	SAI1_TXD1	BOOT CFG9	Boot mode	3.3V	I	AF20	

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
				configuration pin				
	68	SAI1_RXD4	BOOT CFG4	Boot mode configuration pin	3.3V	I	AG18	
	69	SAI1_TXD2	BOOT CFG10	Boot mode configuration pin	3.3V	I	AG21	
	70	SAI1_RXD5	BOOT CFG5	Boot mode configuration pin	3.3V	I	AF18	
	71	SAI1_TXD3	BOOT CFG11	Boot mode configuration pin	3.3V	I	AF21	
	72	SAI1_RXD6	BOOT CFG6	Boot mode configuration pin	3.3V	I	AG19	
	73	SAI1_TXD4	BOOT CFG12	Boot mode configuration pin	3.3V	I	AG22	
	74	SAI1_RXD7	BOOT CFG7	Boot mode configuration pin	3.3V	I	AF19	
	75	SAI1_TXD5	BOOT CFG13	Boot mode configuration pin	3.3V	I	AF22	
	76	SAI1_MCLK	GPIO	General GPIO4_IO20	3.3V	I/O	AB18	The default configuration is the input, Internal pull down
	77	SAI1_TXD6	BOOT CFG14	Boot mode configuration pin	3.3V	I	AG23	
	78	SAI1_TXFS	GPIO	General GPIO4_IO10	3.3V	I/O	AB19	The default configuration is the input, Internal pull down
	79	SAI1_TXD7	BOOT CFG15	Boot mode configuration pin	3.3V	I	AF23	
	80	SAI2_TXFS	GPIO	General GPIO4_IO24	1.8V	I/O	AD23	The default configuration is the input, Internal pull down
	81	NVCC_SD2	NVCC_SD2	SD card power supply	3.3V/1.8V	O		Default 3.3V, available with 1.8V
	82	DGND	DGND	GND	0V			
	83	SAI2_TXD	GPIO	General GPIO4_IO26	1.8V	I/O	AC22	The default configuration is the input, Internal pull down
	84	ETH_TRP0	ENET1	ENET1 Data 0+				Built in Ethernet chip(YT8511) pin
	85	SAI2_TXC	GPIO	General GPIO4_IO25	1.8V	I/O	AD22	
	86	ETH_TRN0	ENET1	ENET1 Data 0-				Built in Ethernet chip(YT8511) pin

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	87	SAI2_RXD	GPIO	General GPIO4_IO23	1.8V	I/O	AC24	The default configuration is the input, Internal pull down
	88	DGND	DGND	GND	0V			
	89	ENET_LED_ACT	ENET_LED_ACT	ENET1 Activity LED				Built in Ethernet chip(YT8511) pin
	90	ETH_TRP1	ETH_TRP1	ENET1 Data 1+				
	91	ENET_LED_1000	ENET_LED_1000	ENET1 LINK LED				Built in Ethernet chip(YT8511) pin
	92	ETH_TRN1	ETH_TRN1	ENET1 Data 1-				Built in Ethernet chip(YT8511) pin
	93	DGND	DGND	GND	0V			
	94	DGND	DGND	GND	0V			
	95	ETH_TRP3	ENET1	ENET1 Data 3+				Built in Ethernet chip(YT8511) pin
	96	ETH_TRP2	ENET1	ENET1 Data 2+				Built in Ethernet chip(YT8511) pin
	97	ETH_TRN3	ENET1	ENET1 Data 3-				Built in Ethernet chip(YT8511) pin
	98	ETH_TRN2	ENET1	ENET1 Data 2-				Built in Ethernet chip(YT8511) pin
	99	DGND	DGND	GND	0V			
	100	DGND	DGND	GND	0V			
J1	1	UART3_RTS	GPIO	General GPIO5_IO09	3.3V	I/O	B6	The default configuration is the input, Internal pull down
	2	DGND	DGND	GND	0V			
	3	UART3_RXD	UART3	Uart3 data receive	3.3V	I	D6	
	4	DSI_DN0	LCD	MIPI-DSI lane 0-	1.8V	O	A9	
	5	UART3_TXD	UART3	Uart3 data transmit	3.3V	O	B7	
	6	DSI_DP0	LCD	MIPI-DSI lane 0+	1.8V	O	B9	
	7	DGND	DGND	GND	0V			
	8	DGND	DGND	GND	0V			
	9	UART3_CTS	GPIO	GPIO5_IO08	3.3V	I/O	A7	The default configuration is the input, Internal pull down
	10	DSI_DN1	LCD	MIPI-DSI lane 1-	1.8V	O	A10	
	11	ECSPI2_SS0	ECSPI2	SPI2 Chip Selection	3.3V	O	A6	

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	12	DSI_DP1	LCD	MIPI-DSI lane1+	1.8V	O	B10	
	13	ECSPI2_SCLK	ECSPI2	SPI2 clock	3.3V	O	E6	
	14	DGND	DGND	GND	0V			
	15	ECSPI2_MISO	ECSPI2	SPI2 data in	3.3V	I	A8	
	16	DSI_CKN	LCD	MIPI-DSI clock-	1.8V	O	A11	
	17	ECSPI2_MOSI	ECSPI2	SPI2 data out	3.3V	O	B8	
	18	DSI_CKP	LCD	MIPI-DSI clock+	1.8V	O	B11	
	19	DGND	DGND	GND	0V			
	20	DGND	DGND	GND	0V			
	21	I2C2_SCL	I2C2	I2C2 bus clock	1.8V	O	D10	2.2K pull up to 1.8V
	22	DSI_DN2	LCD	MIPI-DSI lane 2-	1.8V	O	A12	
	23	I2C2_SDA	I2C2	I2C2 bus data	1.8V	I/O	D9	2.2K pull up to 1.8V
	24	DSI_DP2	LCD	MIPI-DSI lane 2+	1.8V	O	B12	
	25	I2C3_SCL	I2C3	I2C3 bus clock	1.8V	O	E10	2.2K pull up to 1.8V
	26	DGND	DGND	GND	0V			
	27	I2C3_SDA	I2C3	I2C3 bus data	1.8V	I/O	F10	2.2K pull up to 1.8V
	28	DSI_DN3	LCD	MIPI-DSI lane 3-	1.8V	O	A13	
	29	I2C4_SCL	I2C4	I2C4 bus clock	1.8V	O	D13	2.2K pull up to 1.8V
	30	DSI_DP3	LCD	MIPI-DSI lane 3+	1.8V	O	B13	
	31	I2C4_SDA	I2C4	I2C4 bus data	1.8V	I/O	E13	2.2K pull up to 1.8V
	32	DGND	DGND	GND	0V			
	33	UART2_RXD	UART2	UART2 Data receive	1.8V	I	F15	
	34	CSI_DN0	CSI	MIPI-CSI lane 0-	1.8V	O	A14	
	35	UART2_TXD	UART2	UART2 Data transmit	1.8V	O	E15	
	36	CSI_DP0	CSI	MIPI-CSI lane 0+	1.8V	O	B14	
	37	UART4_RXD	UART4	UART4 Data receive	1.8V	I	F19	
	38	DGND	DGND	GND	0V			
	39	UART4_TXD	UART4	UART4 Data transmit	1.8V	O	F18	
	40	CSI_DN1	CSI	MIPI-CSI lane 1-	1.8V	O	A15	
	41	ONOFF	ONOFF	ONOFF signal	3.3V	I	A25	
	42	CSI_DP1	CSI	MIPI-CSI lane 1+	1.8V	O	B15	
	43	ENET_LED_100	ENET1	ENET1 LED 100M control	3.3V/1.8V		A24	Built in Ethernet chip(YT8511) pin

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	44	DGND	DGND	GND	0V			
	45	POR_B		PMIC Reset output	1.8V	O	B24	Internal pull up The PMIC can reset the output signal, which can be used to reset the carrier board peripheral
	46	CSI_CKN	CSI	MIPI-CSI clock-	1.8V	O	A16	
	47	SD1_STROBE	GPIO	General GPIO2_IO11	3.3V	I/O	R24	The default configuration is the input, Internal pull down
	48	CSI_CKP	CSI	MIPI-CSI clock+	1.8V	O	B16	
	49	SD2_DATA2	uSDHC2	uSDHC2 data 2	3.3V/1.8V	I/O	V24	
	50	DGND	DGND	GND	0V			
	51	SD2_DATA3	uSDHC2	uSDHC2 data 3	3.3V/1.8V	I/O	V23	
	52	CSI_DN2	CSI	MIPI-CSI lane 2-	1.8V	I	A17	
	53	SD2_CLK	uSDHC2	uSDHC2 clock	3.3V/1.8V	O	W23	
	54	CSI_DP2	CSI	MIPI-CSI lane 2+	1.8V	I	B17	
	55	SD2_CMD	uSDHC2	uSDHC2 command	3.3V/1.8V	I	W24	
	56	DGND	DGND	GND	0V			
	57	SD2_DATA1	uSDHC2	uSDHC2 data 1	3.3V/1.8V	I/O	AB24	
	58	CSI_DN3	CSI	MIPI-CSI lane 3-	1.8V	I	A18	
	59	SD2_DATA0	uSDHC2	uSDHC2 data 0	3.3V/1.8V	I/O	AB23	
	60	CSI_DP3	CSI	MIPI-CSI lane 3+	1.8V	I	B18	
	61	SD2_WP	PCIe_nWAKE	PCIE Interface wake up	3.3V/1.8V	I	AA27	
	62	DGND	DGND	GND	0V			
	63	SD2_nCD	uSDHC2	uSDHC2 check	3.3V/1.8V	I	AA26	
	64	PCIE_RXN	PCIE	PCIE data receive -		I	A19	
	65	SD2_nRST	GPIO	General GPIO2_IO19	3.3V/1.8V	I/O	AB26	The default configuration is the input, Internal pull down
	66	PCIE_RXP	PCIE	PCIE data receive+		I	B19	

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	67	BOOT_MODE0	BOOT_MODE0	Start and Download mode control	1.8V	I	G26	Internal pull down
	68	DGND	DGND	GND	0V			
	69	BOOT_MODE1	BOOT_MODE1	Start and Download mode control	1.8V	I	G27	Internal pull down
	70	PCIE_TXN	PCIE	PCIE data transmit-		O	A20	
	71	UART1_CTS	UART1	Uart1 flow control	1.8V	I/O	E18	
	72	PCIE_TXP	PCIE	PCIE data transmit+		O	B20	
	73	UART1_TXD	UART1	Uart1 data transmit	1.8V	O	F13	
	74	DGND	DGND	GND	0V			
	75	UART1_RXD	UART1	Uart1 data receive	1.8V	I	E14	
	76	PCIE_CLKN	PCIE	PCIE Reference clock-	1.8V	I/O	A21	
	77	UART1_RTS	UART1	Uart1 flow control	1.8V	I/O	D18	
	78	PCIE_CLKP	PCIE	PCIE Reference clock+	1.8V	I/O	B21	
	79	SD1_DATA0	uSDHC1	uSDHC1 data 0	3.3V	I/O	Y27	
	80	DGND	DGND	GND	0V			
	81	SD1_DATA1	uSDHC1	uSDHC1 data 1	3.3V	I/O	Y26	
	82	USB1_VBUS	USB1_VBUS	USB1 Bus power monitoring	3.3V	I/O	F22	
	83	SD1_DATA2	uSDHC1	uSDHC1 data 2	3.3V	I/O	T27	
	84	USB_OTG1_DN	USB1	USB1 data-	3.3V	I/O	A22	
	85	SD1_DATA3	uSDHC1	uSDHC1 data 3	3.3V	I/O	T26	
	86	USB_OTG1_DP	USB1	USB1 data+	3.3V	I/O	B22	
	87	SD1_CMD	uSDHC1	uSDHC1 command	3.3V	O	V27	
	88	DGND	DGND	GND	0V			
	89	SD1_CLK	uSDHC1	uSDHC1 clock	3.3V	O	V26	
	90	USB1_ID	USB1	USB1 ID	3.3V	I	D22	
	91	WL_REG_ON	WL_REG_ON	WIFI Module Internal power enable	3.3V	O	R23	
	92	USB2_VBUS	USB2_VBUS	USB2 Bus power monitoring	3.3V	I	F23	
	93	WL_WAKE_HOST	WL_WAKE_HOST	WIFI module the HOST wake-up	3.3V	I	W26	
	94	USB_OTG2_DN	USB_OTG2_DN	USB2 data-	3.3V	I/O	A23	

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	95	BT_REG_ON	BT	BT Module Internal power enable	3.3V	O	U27	
	96	USB_OTG2_DP	USB_OTG2_DP	USB2 data+	3.3V	I/O	B23	
	97	BT_WAKE_DEV	BT	BT Module wake up	3.3V	O	U26	
	98	DGND	DGND	GND	0V			
	99	BT_WAKE_HOST	BT	BT module the HOST wake-up	3.3V	I	W27	
	100	USB2_ID	USB2_ID	USB2 ID	3.3V	I	D23	

Table 3-1 MYC-C8MMX-V2 Core board PIN LIST

4. Electrical Characteristics

4.1. Primary System Power (VDD_5V)

The main power supply of the MYC-C8MMX-V2 core board is VDD_5V, corresponding to J2 connector 1 to 10 pins.To ensure proper operation, the carrier board must provide a voltage of 5V ± 5% and ensure that the output capacity of the power supply circuit can meet the power consumption of the core board. The 4.4 chapter lists the power consumption and current of the core board under each condition, and the appropriate margin is reserved when designing the power supply circuit.

4.2. Power Domain

The external power supply voltage requires the carrier board to provide the corresponding voltage, the internal generating voltage is the voltage generated by the core board, and does not require additional power supply.

The core board is powered by VDD_5V, generating different voltages by a PMIC power management chip to meet the power of MPU, DDR4, Flash, etc.The complete PMIC model is BD71847MWV.

Name	Description	Recommended Voltage
VDD_5V	Main supply voltage, 5V input	5V
VDD_3V33	3.33V output	-
VDD_1V8	1.8V output	-
USB1_VBUS USB2_VBUS	USB power supply, 5V input	5V
NVCC_SD2	Support 1.8V/3.3V output, software controllable	3.3V/1.8V

Table 4-1 External input / output voltage

Name	Description	Voltage
NVCC_3V3	NVCC_SAI1,NVCC_SAI3,NVCC_SAI5,NVCC_ECSPI, NVCC_SD1,NVCC_CLK	3.3V @3A
VDD_SOC_0V8	Power supply for SOC	0.8V@1A
VDD_ARM_0V9 VDD_DRAM VDD_VPU_0V9	Power supply for ARM core	0.9V@3A
NVCC_DRAM_1V2	Power supply for DRAM	1.2V@3A
VDD_1V8	NVCC_JTAG, NVCC_NAND, NVCC_SAI2, NVCC_GPIO1, NVCC_I2C, NVCC_UART	1.8V@1.5A

Table 4-2 Internally generated voltages

4.3. Power Consumption

Conditon	Voltage (V)	Average Current (mA)	Peak Current (mA)	Power Consumption (mW)
During boot	5	110	130	550
Full-load stage	5	420	-	2100
Mem low-power mode	5	10	-	50
Freeze Low-power mode	5	90	-	450

Table 4-3 Power consumption parameters

4.4. GPIO DC Parameters

Parameter	Symbol	Min	Typical	Max	Units
High-lever DC output voltage	$V_{OH\ (1.8V)}$	1.35	—	—	V
	$V_{OH\ (3.3V)}$	2.4	—	—	V
Low-lever DC output voltage	$V_{OL\ (1.8V)}$	—	—	0.36	V
	$V_{OL\ (3.3V)}$	—	—	0.4	V
High-lever DC input voltage	$V_{IL(1.8V)}$	1.26	—	1.8	V
	$V_{IH(3.3V)}$	2	—	3.3	V
Low-lever DC input voltage	$V_{IL(1.8V)}$	0	—	0.36	V
	$V_{IH(3.3V)}$	0	—	0.8	V

Table 4-4 GPIO DC Parameters

5. System Start-up Configuration

5.1. BOOT MODE

The I.MX8M Mini series processor starts first executes the program in the Boot ROM within the chip.Boot ROM enters the boot mode by reading the Boot Mode pin. The specific correspondence is as follows:

Boot Mode [1:0]	function	Description
00	Boot from Fuse	Internal Fuses reads the startup information, which NXP recommends shipping in mass production
01	Serial Downloader	Support to download programs from the USB_OTG1 port.It should be noted that UART1 in this mode, UART1 and UART2 have higher priority than USB_OTG port. If the data will not enter USB firing mode, the computer cannot detect the device and the Mfgtools cannot be used.
10	Internal Boot	Start configuration bit from the GPIO read, NXP is recommended for development mode.However, in this mode, use Fuse without writing (one-time programming, not erasable), modify the startup mode is convenient, and many users are directly used for mass production.
11	Reserved	

Table 5-1 CPU Start mode configuration

The Boot Mode pin does not add pull-up or pull-down resistors in the core board.But the chip has a Internal pull-down resistor by default.

5.2. BOOT Device

The I.MX8M Mini series processor supports many launching equipment, and you need to configure the pin of the boot device. There are 16 pins.Boot_cfg [7: 0] corresponds to the pin SAI1_RXD [7: 0], boot_cfg [15: 8] corresponds pin SAI1_TXD [7: 0].

Before setting up BOOT_CFG, make sure that boot mode is set correctly.Here the internal boot mode is chosen as an example to set the boot device.

BOOT_CFG[15:0] has no pull-up or pull-down resistors designed on the core board.The states of all these pins during chip reset and when the reset is complete are:input type, chip internal design with 95K pull-down resistance.

BOOT_CFG[15:0]	Boot device	description
X001 00XX XXX1 000X	SD/eSD (uSDHC1	
X001 01XX XXX1 000X	SD/eSD (uSDHC2)	
X010 10XX X010 0011	eMMC (uSDHC3)	
X110 X010 XXXX XXXX	QSPI	

Table 5-2 CPU Boot device description

5.3. Reset

The MYC-C8MMX-V2 core board provides two dedicated pins, NRST reset and ONOFF, with different functions and are suggested to be connected for different purposes.

Pin	Description
SYS_nRST (Core board J2.29 Pin)	System reset for core board: RC reset circuit or hardware watchdog reset chip can be used on carrier board.
ONOFF (Core board J1.41 Pin)	If you press ONOFF key for the first time, the system shuts do wn automatically, press the button again,then the system will start up. When the system is in sleep mode, press this key to wake up the system.

Table 5-3 Reset and ONOFF pin function description

6. Interfaces

6.1. uSDHC

The MYC-C8MMX-V2 core board has a 3 lane uSDHC interface.And leads to 2 lane MMC interfaces, uSDHC1 and uSDHC2. Both the two uSDHC interfaces support interfaces canbe used as the launch device.USDHC2 is typically used to design a Micro SD card, and uSDHC1 can be used to design a communication interface between modules having an SDIO interface.

6.1.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	49	SD2_DATA2	uSDHC2	uSDHC2 data 2	3.3V/1.8V	I/O	V24	
	51	SD2_DATA3	uSDHC2	uSDHC2 data 3	3.3V/1.8V	I/O	V23	
	53	SD2_CLK	uSDHC2	uSDHC2 clock	3.3V/1.8V	O	W23	
	55	SD2_CMD	uSDHC2	uSDHC2 command	3.3V/1.8V	O	W24	
	57	SD2_DATA1	uSDHC2	uSDHC2 data 1	3.3V/1.8V	I/O	AB24	
	59	SD2_DATA0	uSDHC2	uSDHC2 data 0	3.3V/1.8V	I/O	AB23	

Table 6-1 uSDHC2 pin description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	79	SD1_DATA0	uSDHC1	uSDHC1 data 0	3.3V	I/O	Y27	
	81	SD1_DATA1	uSDHC1	uSDHC1 data 1	3.3V	I/O	Y26	
	83	SD1_DATA2	uSDHC1	uSDHC1 data 2	3.3V	I/O	T27	
	85	SD1_DATA3	uSDHC1	uSDHC1 data 3	3.3V	I/O	T26	
	87	SD1_CMD	uSDHC1	uSDHC1 command	3.3V	O	V27	
	89	SD1_CLK	uSDHC1	uSDHC1 clock	3.3V	O	V26	

Table 6-2 uSDHC1 pin description

6.2. UART

The MYC-C8MMX-V2 core board has asynchronous serial ports of up to 4 channels.The core board is configured with 4 serial port by default, where the UART1 has a stream control (RTS and CTS signal) function.

6.2.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	3	UART3_RXD	UART3	UART3 Data receive	3.3V	I	D6	
	5	UART3_TXD	UART3	UART3 Data transmit	3.3V	O	B7	
	33	UART2_RXD	UART2	UART2 Data receive	1.8V	I	F15	
	35	UART2_TXD	UART2	UART2 Data transmit	1.8V	O	E15	
	37	UART4_RXD	UART4	UART4 Data receive	1.8V	I	F19	
	39	UART4_TXD	UART4	UART4 Data transmit	1.8V	O	F18	
	71	UART1_CTS	UART1	UART1 flow control	1.8V	I/O	E18	
	73	UART1_TXD	UART1	UART1 Data transmit	1.8V	O	F13	
	75	UART1_RXD	UART1	UART1 Data receive	1.8V	I	E14	
	77	UART1_RTS	UART1	UART1 flow control	1.8V	I/O	D18	

Table 6-3 UART pin description

6.3. USB

The MYC-C8MMX-V2 core board provides two high-speed USB2.0 OTG controllers, supporting Host, Device mode.Where USB1 can be used as a port of the download program.

6.3.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	82	USB1_VBUS	USB1_VBUS	USB1 Bus power monitoring	3.3V	I/O	F22	
	84	USB_OTG1_DN	USB1	USB1 Data -	3.3V	I/O	A22	
	86	USB_OTG1_DP	USB1	USB1 Data+	3.3V	I/O	B22	
	90	USB1_ID	USB1	USB1 ID	3.3V	I	D22	
	92	USB2_VBUS	USB2_VBUS	USB2 Bus power monitoring	3.3V	I	F23	
	94	USB_OTG2_DN	USB_OTG2_DN	USB2 Data -	3.3V	I/O	A23	
	96	USB_OTG2_DP	USB_OTG2_DP	USB2 Data+	3.3V	I/O	B23	
	100	USB2_ID	USB2_ID	USB2 ID	3.3V	I	D23	

Table 6-4 USB pin description

6.4. Ethernet

The MYC-C8MMX-V2 core board has an Ethernet PHY circuit designed to support 10/100/1000M adaptive mode.When the user designs the carrier board circuit, only needs to design the transformer isolation circuit and the RJ45 part of the circuit.

6.4.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J2	84	ETH_TRP0	ENET1	ENET1 data 0 signal+		I/O		
	86	ETH_TRN0	ENET1	ENET1 data 0 signal-		I/O		
	89	ENET_LED_ACT	ENET_LED_ACT	ENET1 Activity LED		I/O		
	90	ETH_TRP1	ETH_TRP1	ENET1 data 1 signal+		I/O		
	91	ENET_LED_1000	ENET_LED_1000	ENET1 LINK LED		I/O		
	92	ETH_TRN1	ETH_TRN1	ENET1 data 1 signal-		I/O		
	95	ETH_TRP3	ENET1	ENET1 data 3 signal+		I/O		
	96	ETH_TRP2	ENET1	ENET1 data 2 signal+		I/O		
	97	ETH_TRN3	ENET1	ENET1 data 3 signal-		I/O		
	98	ETH_TRN2	ENET1	ENET1 data 2 signal-		I/O		
J1	43	ENET_LED_100	ENET1	ENET1 LED 100M control	3.3V/ 1.8V		A24	

Table 6-5 Ethernet pin description

6.5. CSI

The MYC-C8MMX-V2 core board supports one CSI interface. For external camera input signal, 4 lane MIPI interface.Users can purchase the camera module MY-CAM003M to evaluate the CSI Functions from MYIR.

6.5.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	34	CSI_DN0	CSI	MIPI-CSI lane 0-	1.8V	O	A14	
	36	CSI_DP0	CSI	MIPI-CSI lane 0+	1.8V	O	B14	
	40	CSI_DN1	CSI	MIPI-CSI lane 1-	1.8V	O	A15	
	42	CSI_DP1	CSI	MIPI-CSI lane 1+	1.8V	O	B15	
	46	CSI_CKN	CSI	MIPI-CSI clock-	1.8V	O	A16	
	48	CSI_CKP	CSI	MIPI-CSI clock+	1.8V	O	B16	
	52	CSI_DN2	CSI	MIPI-CSI lane 2-	1.8V	I	A17	
	54	CSI_DP2	CSI	MIPI-CSI lane 2+	1.8V	I	B17	
	58	CSI_DN3	CSI	MIPI-CSI lane 3-	1.8V	I	A18	
	60	CSI_DP3	CSI	MIPI-CSI lane 3+	1.8V	I	B18	

Table 6-6 CSI pin description

6.6. I2C

The i.MX8M Mini supports a maximum 4 I2C bus, where the I2C1 is used to connect the core board PMIC power management chip, and the I2C1 does not lead to the core board interface.Therefore, the MYC-C8MMX-V2 core board supports a maximum 3 I2C bus.

6.6.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	21	I2C2_SCL	I2C2	I2C2 bus clock	1.8V	O	D10	
	23	I2C2_SDA	I2C2	I2C2 bus data	1.8V	I/O	D9	
	25	I2C3_SCL	I2C3	I2C3 bus clock	1.8V	O	E10	
	27	I2C3_SDA	I2C3	I2C3 bus data	1.8V	I/O	F10	
	29	I2C4_SCL	I2C4	I2C4 bus clock	1.8V	O	D13	
	31	I2C4_SDA	I2C4	I2C4 bus clock	1.8V	I/O	E13	

Table 6-7 I2C pin description

6.7. SPI

The MYC-C8MMX-V2 core board supports a maximum 3 SPI controller and supports master/ slave mode.SPI signals include SPI_CLK, SPI_MOSI and SPI_MISO,During design, the relationship between master and slave devices should be confirmed first, and then the direction of MOSI and MISO signals should be confirmed.Due to the pin multiplexing relationship, the core board is configured with the ECSPI2 interface. If you want to use more SPI interfaces, check the chip manual or use the Config Tools for I.mx software to configure, and modify the pin configuration in the driver.

6.7.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	11	ECSPI2_SS0	ECSPI2	SPI2 chip selection	3.3V	O	A6	
	13	ECSPI2_SCLK	ECSPI2	SPI2 clock	3.3V	O	E6	
	15	ECSPI2_MISO	ECSPI2	SPI2 data in	3.3V	I	A8	
	17	ECSPI2_MOSI	ECSPI2	SPI2 data out	3.3V	O	B8	

Table 6-8 SPI2 pin description

6.8. DSI

The MYC-C8MMX-V2 core board supports a 4-lane MIPI DSI display interface with the highest resolution of 1080p60.

6.8.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	4	DSI_DN0	LCD	MIPI-DSI lane 0-	1.8V	O	A9	
	6	DSI_DP0	LCD	MIPI-DSI lane 0+	1.8V	O	B9	
	10	DSI_DN1	LCD	MIPI-DSI lane 1-	1.8V	O	A10	
	12	DSI_DP1	LCD	MIPI-DSI lane 1+	1.8V	O	B10	
	16	DSI_CKN	LCD	MIPI-DSI clock-	1.8V	O	A11	
	18	DSI_CKP	LCD	MIPI-DSI clock+	1.8V	O	B11	
	22	DSI_DN2	LCD	MIPI-DSI lane 2-	1.8V	O	A12	
	24	DSI_DP2	LCD	MIPI-DSI lane 2+	1.8V	O	B12	
	28	DSI_DN3	LCD	MIPI-DSI lane 3-	1.8V	O	A13	
	30	DSI_DP3	LCD	MIPI-DSI lane 3+	1.8V	O	B13	
J2	30	CLKO1	CAM_P1_MCLK	CSI master clock	1.8V	O	AC9	

Table 6-9 DSI pin description

6.9. PCIE

The MYC-C8MMX-V2 core board supports a 1-lane PCIE 2.0 interface.

6.9.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J1	61	SD2_WP	PCIe_nWAKE	PCIE wake up	3.3V/1.8V	I	AA27	
	64	PCIE_RXN	PCIE	PCIE data receive -		I	A19	
	66	PCIE_RXP	PCIE	PCIE data receive +		I	B19	
	70	PCIE_TXN	PCIE	PCIE data transmit-		O	A20	
	72	PCIE_TXP	PCIE	PCIE data transmit+		O	B20	
	76	PCIE_CLKN	PCIE	PCIE Reference clock-	1.8V	I/O	A21	
	78	PCIE_CLKP	PCIE	PCIE Reference clock+	1.8V	I/O	B21	

Table 6-10 PCIE pin description

6.10. AUDIO

The MYC-C8MMX-V2 core board provides five SAI interfaces for synchronous audio. By default, only one SAI interface is configured. SAI interface supports all kinds of full-duplex and serial communication audio interfaces with frame synchronization function, such as I2S, AC97, TDM, CODEC and other common audio interfaces.

When using it, you need to connect the interface to the external audio codec, and then plug in the headphones and microphone.

6.10.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J2	31	SAI3_MCLK	SAI3_MCLK	I2S3 master clock	3.3V	O	AD6	
	33	SAI3_TXFS	SAI3	SAI3 frame clock	3.3V	O	AC6	
	35	SAI3_TXC	SAI3	SAI3 bit clock	3.3V	O	AG6	
	37	SAI3_TXD	SAI3	SAI3 data transmit	3.3V	O	AF6	

Table 6-11 AUDIO pin description

6.11. GPIO

MYC-C8MMX-V2 core board supports GPIO's pin, these pins are used as some functions.Table 6-13 lists the default pins used as GPIOs.Customers can flexibly configure GPIO according to the specific needs of their own products. It is recommended to use Config Tools for I.mx to assign pin resources.

6.11.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
J2	28	SD2_DET	GPIO	General GPIO1_IO15	1.8V	I/O	AB9	The default configuration is output, Internal pull down
	32	LVDS_RSTLV	GPIO	General GPIO1_IO1	1.8V	I/O	AD9	The default configuration is output, Internal pull down
	34	DSI_TP_RSTLV	GPIO	General GPIO1_IO12	1.8V	I/O	AB10	The default configuration is output, Internal pull down
	36	CSI_P1_IO1	CSI_P1_IO1	CSI power control	1.8V	I/O	AC10	Input with PD
	38	GPIO1_09LV	GPIO	General GPIO1_IO09	1.8V	I/O	AF10	The default configuration is input, Internal pull down
	39	SAI3_RXFS	GPIO	General GPIO4_IO28	3.3V	I/O	AG8	The default configuration is input, Internal pull down
	40	DSI_BL_ENLV	GPIO	General GPIO1_IO08	1.8V	I/O	AG10	The default configuration is input, Internal pull down
	41	SAI3_RXC	GPIO	General GPIO4_IO29	3.3V	I/O	AG7	The default configuration is input, Internal pull down
	42	CSI_PWDN	CSI_PWDN	CSI Enable control	1.8V	I/O	AF11	The default configuration is output
	43	SAI3_RXD	GPIO	General GPIO4_IO30	3.3V	I/O	AF7	The default configuration is input, Internal pull down
	44	CSI_Nrst	CSI_Nrst	CSI reset signal	1.8V	I/O	AG11	The default configuration is output, Internal pull down
	45	LED2	GPIO	General GPIO5_IO03	3.3V	I/O	AF9	The default configuration is output
	46	4G_RST	GPIO	General GPIO1_IO05	1.8V	I/O	AF12	The default configuration is output
	47	LED1	GPIO	General GPIO5_IO04	3.3V	I/O	AG9	The default configuration is output, Internal pull down
	48	DSI_BL_PWMLV	DSI_BL_PWM	LCD Backlight regulation	1.8V	O	AF14	
	49	SPDIF_EXT_CLK	CLK_REQ	WIFI Clock request	3.3V	I	AF8	
	50	LVDS_IRQLV	LVDS_IRQLV	TC358775 chip STBY	1.8V	O	AD19	
	51	PDM_CLK	GPIO	General GPIO3_IO20	3.3V	I/O	AC15	The default configuration is input, Internal pull down
	52	PCIe_nRSTLV	PCIe_nRSTLV	PCIE Interface reset	1.8V	O	AC19	The default configuration is input, Internal pull down
	53	PDM_DATA0	GPIO	General GPIO3_IO21	3.3V	I/O	AD18	The default configuration is input, Internal pull down

	Pin	Signal	Default Function	Description	Voltage	IO	MPU Pin	Comments
	54	KEY	GPIO	General GPIO3_IO19	3.3V	I/O	AB15	The default configuration is input, 10K pull up to 3.3V
	55	PDM_DATA1	GPIO	General GPIO3_IO22	3.3V	I/O	AC14	The default configuration is input, Internal pull down
	57	PDM_DATA2	GPIO	General GPIO3_IO23	3.3V	I/O	AD13	The default configuration is input, Internal pull down
	58	DSI_TS_nINT	DSI_TS_nINT	Touch screen interruption	3.3V	I	AF16	The default configuration is input, 10K pull up to 3.3V
	59	PDM_DATA3	GPIO	General GPIO3_IO24	3.3V	I/O	AC13	The default configuration is input, Internal pull down
	61	SAI5_MCLK	GPIO	General GPIO3_IO25	3,.3V	I/O	AD15	The default configuration is input, Internal pull down
	63	SAI1_TXC	GPIO	General GPIO4_IO11	3.3V	I/O	AC18	The default configuration is input, Internal pull down
	76	SAI1_MCLK	GPIO	General GPIO4_IO20	3.3V	I/O	AB18	The default configuration is input, Internal pull down
	78	SAI1_TXFS	GPIO	General GPIO4_IO10	3.3V	I/O	AB19	The default configuration is input, Internal pull down
	80	SAI2_TXFS	GPIO	General GPIO4_IO24	1.8V	I/O	AD23	The default configuration is input, Internal pull down
	83	SAI2_TXD	GPIO	General GPIO4_IO26	1.8V	I/O	AC22	The default configuration is input, Internal pull down
	85	SAI2_TXC	GPIO	General GPIO4_IO25	1.8V	I/O	AD22	
	87	SAI2_RXD	GPIO	General GPIO4_IO23	1.8V	I/O	AC24	The default configuration is input, Internal pull down
J1	1	UART3_RTS	GPIO	General GPIO5_IO09	3.3V	I/O	B6	The default configuration is input, Internal pull down
	9	UART3_CTS	GPIO	GPIO5_IO08	3.3V	I/O	A7	The default configuration is input, Internal pull down
	47	SD1_STROBE	GPIO	General GPIO2_IO11	3.3V	I/O	R24	The default configuration is input, Internal pull down
	65	SD2_nRST	GPIO	General GPIO2_IO19	3.3V/ 1.8V	I/O	AB26	The default configuration is input, Internal pull down
	91	WL_REG_ON	WL_REG_ON	WIFI Module Internal control power	3.3V	O	R23	
	93	WL_WAKE_HOST	WL_WAKE_HOST	WIFI module the HOST wake-up	3.3V	I	W26	
	95	BT_REG_ON	BT	BT Internal power control	3.3V	O	U27	
	97	BT_WAKE_DEV	BT	BT Module wake up	3.3V	O	U26	
	99	BT_WAKE_HOST	BT	BT module the HOST wake-up	3.3V	I	W27	

Table 6-12 GPIO pin description

7. Package Information

7.1. Package Dimensions

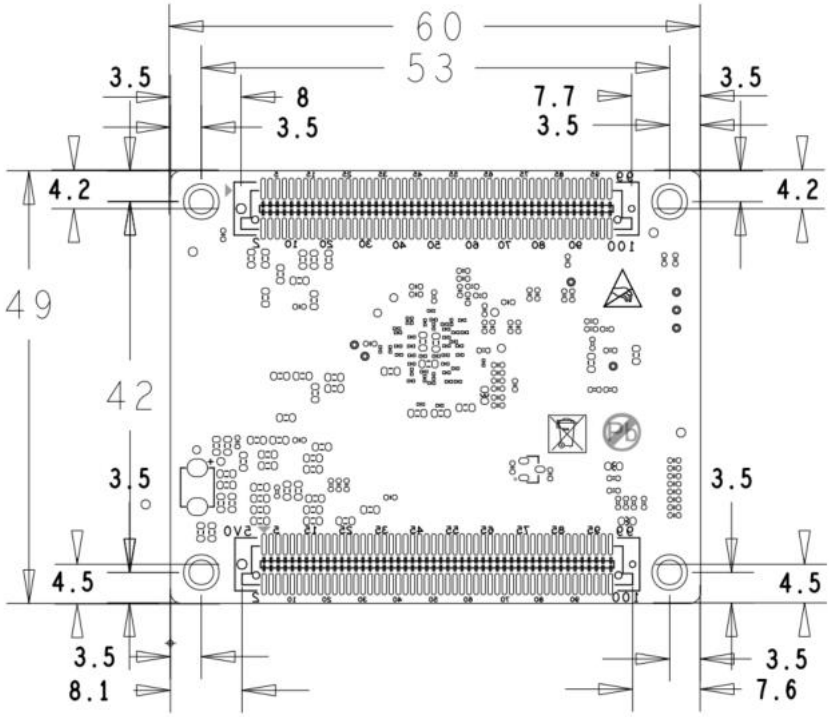

Figure 7-1 MYC-C8MMX-V2 Core board Bottom view

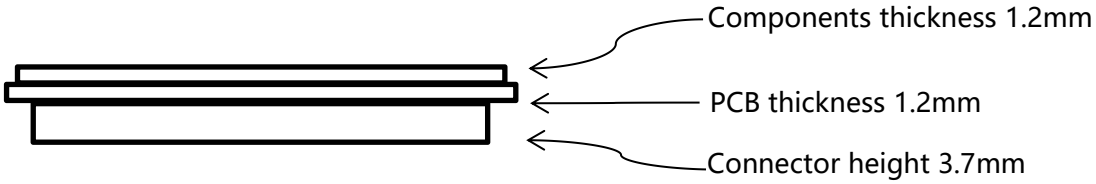

Figure 7-2 MYC-C8MMX-V2 Core board side view

7.2. Carrier Board PCB Requirements

- Recommended PCB thickness is 1.6mm, pay attention to the balance of copper coating, if the PCB deformation of the furnace, it is recommended to use the cure device to fix the furnace.
- To ensure the mounting and upper tin quality, ensure that the distance between the PCB upper module and the other components is at least 3mm.
- Please design the package of the core board module as per section 7, or use the PCB package provided by Mill Electronics.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;

- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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