MYC-C8MMX-V2

Hardware Design Guide

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History

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1. Overview

This document is intended to assist hardware engineers in designing board-level circuits based on the MYC-C8MMX-V2 core module. Please be fully aware of the document before you begin your design.The document contains common information such as design references, layout suggestions, and design checklists to assist hardware engineers.

Resources referenced in this document is from the MYIR Electronics website, included in the MYC-C8MMX-V2 product information download page, you can download them in the following website: http://d.myirtech.com/MYD-C8MMX/

In addition, MYIR Electronics the following resources to speed up your design:

- Core board / evaluation board product manual;
- Evaluation board principle graphical source file;
- Related device manuals.

1.1. Supported products

This document is suitable for all models of MYC-C8MMX series core boards.

1.2. Disclaimer

- Some of reference designs in the document are based on MYIR electronic evaluation boards and cannot be guaranteed to be suitable for all application scenarios. If your product has special requirements for application scenarios or technical specifications, please adjust the design according to the actual situation.
- Reference design and layout in the document are recommended for reference only and do not necessarily contain all the matters needing attention. Please make adjustments according to the actual situation.
- MYIR shall not be liable for any form of technical endorsement or joint liability for any proposal contained in any document.

2. Power supply design

The design of the power supply system is of vital importance in the design of embedded products, engineers need to consider not only the basic electrical parameters of power itself, but also the stability of the power supply design, such as electromagnetic compatibility, temperature range, safety design, etc. Any neglect of these factors may lead to the entire system cannot work normally. Before starting to design a power supply system for a new product, the engineer should thoroughly understand the actual needs of the whole system, and comprehensively demonstrate a feasible design scheme based on cost and efficiency, so as to select an appropriate power supply method for the system.

2.1. Reference Design

The core board needs to provide voltage of 5V for normal operation. The average current under full load is about 0.24A, and the peak current can reach 0.29A. Although the power consumption of the core board is not high,considering the performance of the circuit itself under the condition of high temperature will be reduced, if the power is not enough can lead to system to start, so the power supply design should have a certain margin to ensure system stable and reliable work, it is recommended to use more than 1A power supply chip separately to the core board power supply. It is not recommended to use this power chip to drive loads except the core board, especially some high-power load devices.

The power supply chip can be LDO or DCDC. LDO has the advantages of simple use, low cost, small electromagnetic interference, but high calorific value. DCDC has the advantages of strong current output capacity, high conversion efficiency and low calorific value, but high electromagnetic interference. If the input voltage is close to 5V, use the LDO power chip. If the input voltage is different from 5V, use the DCDC power chip.

Among them, the evaluation board uses DCDC chip, because the input voltage 12V and 5V gap is large, the model is TLV62130RGTR. In order to ensure the accuracy of the output voltage, it is recommended to use more than 1% accuracy for R2 and R4.

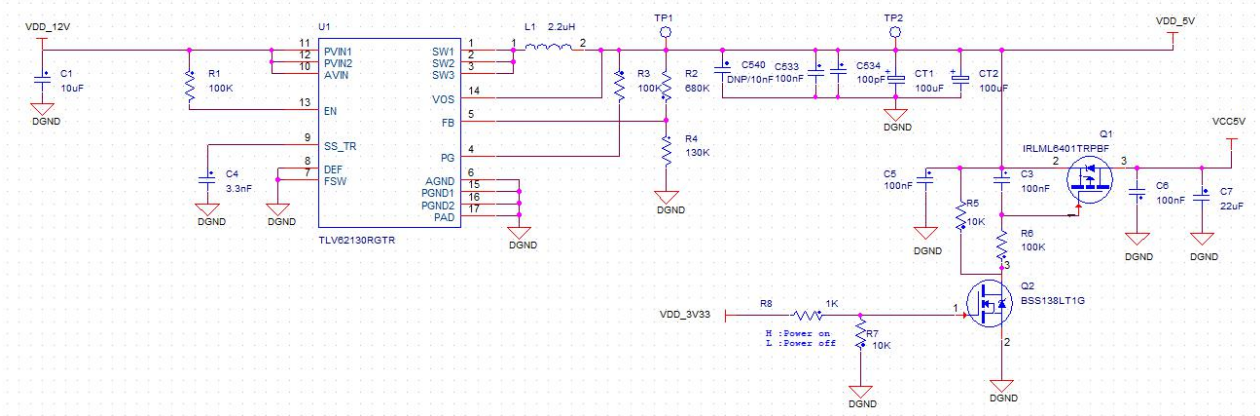


Figure 2-1 Core board 5V power supply

2.2. Power Protection

In order to ensure the reliability of the power supply system, it is not recommended to directly supply the external unopened input voltage directly to the input of the power supply chip, and the power supply can be processed after processing the power supply to improve the reliability of the input power supply. Safety and reduce electromagnetic interference. The bottom board input power supply in the design is 12V, only as an example, the value of the input power should be determined according to your actual needs.

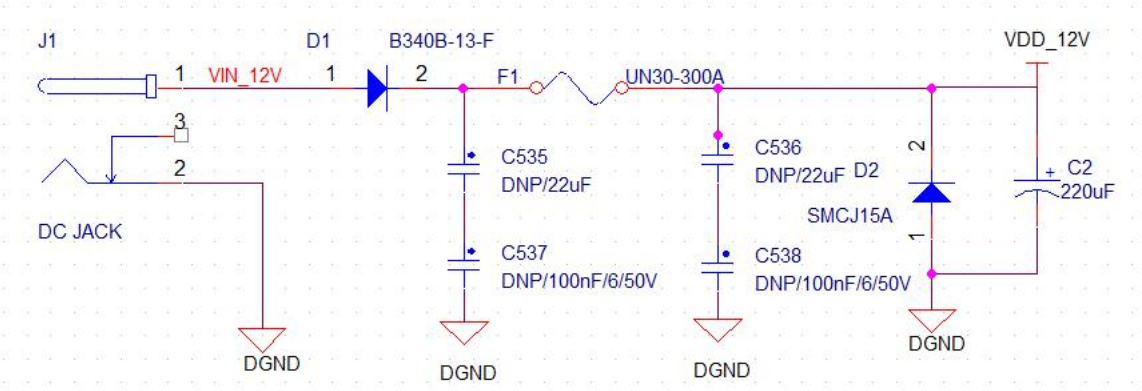


Figure 2-2 General power input circuit

2.3. Power Sequence

In the design, it is suggested that MYC-C8MMX-V2 core board should be powered on first, whereafter the other peripheral devices of the carrier board should be powered on. Failure to meet the power sequence may lead to the following situation:

- The carrier board peripheral`s I / O current is filled to the processor, and the processor cannot start normally;
- The carrier board peripheral`s I / O current is filled to the processor, and the bad situation causes irreversible damage to the processor (the most);

Therefore, it is highly recommended that the core panel is powered on the other peripheral of the bottom plate.

2.4. Layout Guidelines

- The distance between different power supply planes should be at least 20mil;
- Widen the width of the power line and ground wire as far as possible, to meet the required rated current value, the width of the feedback signal should not be too narrow, it is recommended to be more than 10mil;
- If DCDC is used, the signal line is not recommended in the area below the inductance;

- If DCDC is used, the current loop path should be as short as possible, and the inductor and capacitor should be placed as close to the chip as possible, i.e. the red and green paths in the figure below

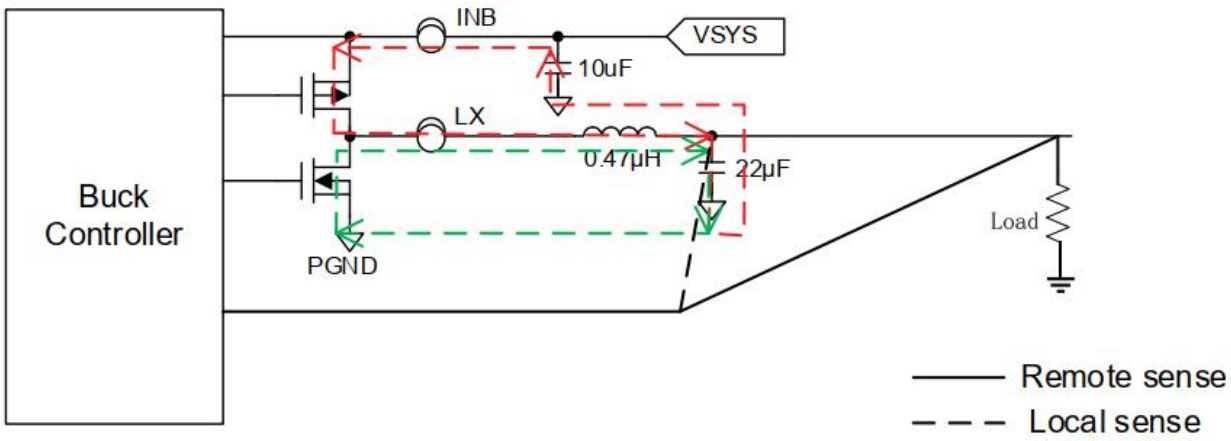


Figure 2-3 DCDC current backflow path

- If LDO is used, it is necessary to pay attention to the thermal resistance of the LDO chip, because the thermal resistance of the LDO chip is relatively high. It is recommended to add the grounding pad and make more ground vias on the grounding pad.
- Choose the capacitance of small ESR as far as possible
- The power chip with digital ground and analog ground shall be separated from each other and only connected at a single point at the input of the main power supply. The analog ground shall not be connected to the grounding pad.

3. Boot config

3.1. Boot Mode

The i.MX 8M Mini series processor starts by executing the program in the internal boot ROM of the chip.Boot ROM determines the boot mode by reading the boot mode register and configuring pins.The specific correspondence is as follows:

Boot Mode [1:0]	function	Description
00	Boot from Fuse	Internal Fuses reads the startup information, which NXP recommends shipping in mass production
01	Serial Downloader	Support to download programs from the USB_OTG1 port.It should be noted that UART1 in this mode, UART1 and UART2 have higher priority than USB_OTG port. If the data will not enter USB firing mode, the computer cannot detect the device and the Mfgtools cannot be used.
10	Internal Boot	Start configuration bit from the GPIO read, NXP is recommended for development mode.However, in this mode, use Fuse without writing (one-time programming, not erasable), modify the startup mode is convenient, and many users are directly used for mass production.
11	Reserved	

Table 3-1 Boot configuration

switch	Signal name	Voltage level
SW1-Bit1	BOOT_MODE0	0
SW1-Bit2	BOOT_MODE1	1
SW1-Bit3	SAI1_TXD1	1
SW1-Bit4	SAI1_TXD2	0
SW2-Bit1	SAI1_TXD3	1
SW2-Bit2	SAI1_TXD4	0
SW2-Bit3	SAI1_TXD5	1
SW2-Bit4	SAI1_TXD6	0

Table 3 - 2 Boot from EMMC

switch	Signal name	Voltage level
SW1-Bit1	BOOT_MODE0	0
SW1-Bit2	BOOT_MODE1	1
SW1-Bit3	SAI1_TXD1	0
SW1-Bit4	SAI1_TXD2	1
SW2-Bit1	SAI1_TXD3	0
SW2-Bit2	SAI1_TXD4	1
SW2-Bit3	SAI1_TXD5	0
SW2-Bit4	SAI1_TXD6	1

Table 3 - 3 Boot from SD

3.2. Reference Design

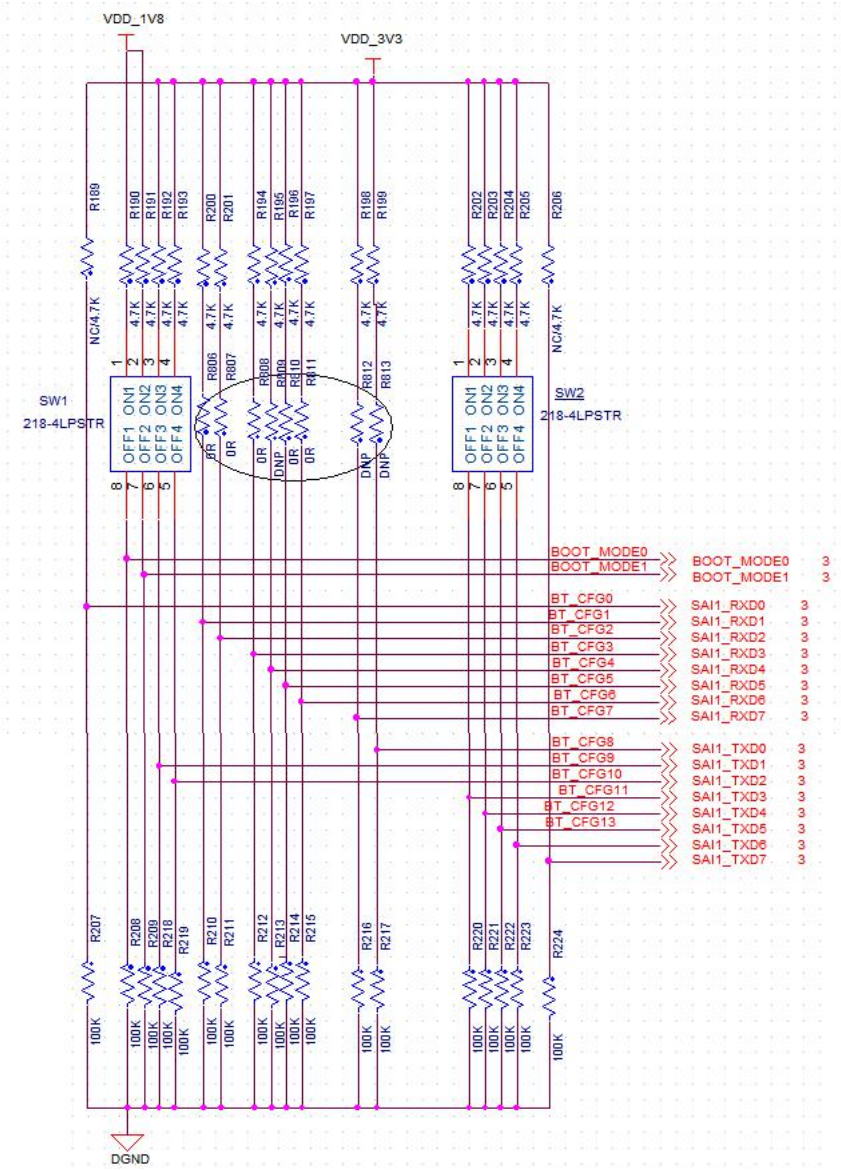


Figure 3-1 Boot mode reference design

4. Reset and key circuit design

MYC-C8MMX-V2 core board provides two special reset pins, respectively nRST reset and ONOFF reset, the two functions are different, it is suggested to connect them for different purposes. An additional pin is reserved in the reference circuit as the user - defined key pin. The resistors and capacitors in the reference circuit form a simple RC filter to filter out the jitter interference when the key is pressed, while avoiding the interference introduced from the key to affect the reset signal.In the harsh electromagnetic environment, in order to eliminate the electrostatic interference from the key to ensure more reliable operation of the system, another ESD device can be connected in parallel. If there are more stringent requirements for chattering elimination, logic circuits such as RS flip-flops can be considered to build reset circuits.

Pin	Description
SYS_nRST (Core board J2.29 Pin)	System reset for core board: RC reset circuit or hardware watchdog reset chip can be used on carrier board.
ONOFF (Core board J1.41 Pin)	If you press ONOFF key for the first time, the system shuts down automatically, press the button again,then the system will start up. When the system is in sleep mode, press this key to wake up the system.

Figure 4-1 Reset and ONOFF pin function description

4.1. Reference Design

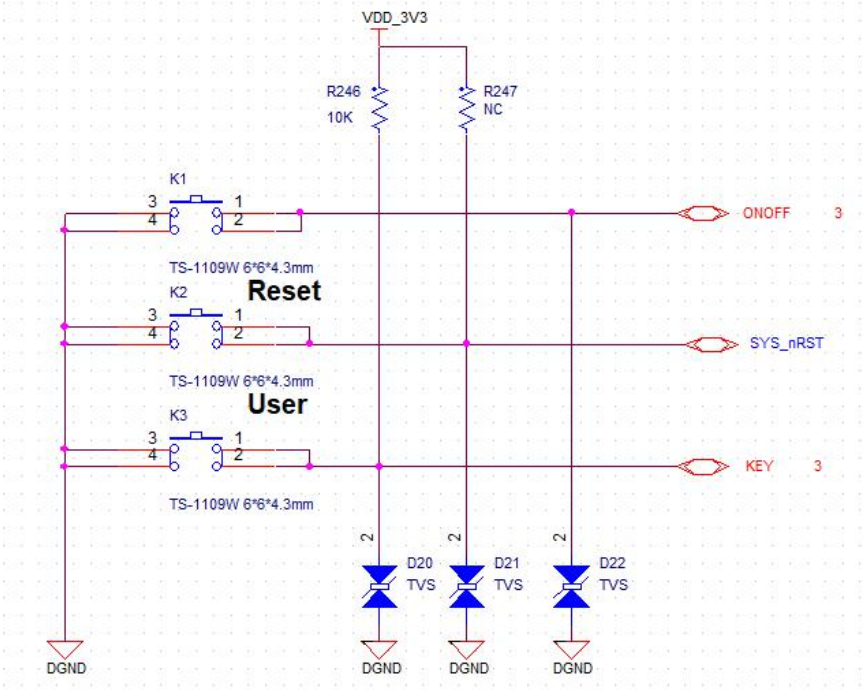


Figure 4-2 reset Reference design

4.2. Layout Guidelines

- The width of reset signal line should not be too narrow, it is recommended not less than 8mil;
- Reset signal is sensitive signal, which is recommended to be surrounded by ground;
- Place TVS as close to the button as possible.

5. Interface circuit design

5.1. uSDHC

The uSDHC interface (Ultra Secured Digital Host Controller) is a proprietary secure Digital Host interface of NXP that provides secure communication between the CPU and external SD/SDIO/MMC cards. The MYC-C8MMX-V2 core board is equipped with three uSDHC interfaces. Two MMC interfaces, uSDHC1 and uSDHC2, are introduced. Both uSDHC interfaces can be used as interfaces corresponding to boot devices. USDHC2 is commonly used to design microSD cards, uSDHC1 can be used to design communication interfaces between modules with SDIO interfaces.

When designing the SD/SDIO/MMC card interface circuit, you only need to connect these interfaces to the SD/MMC card accordingly.

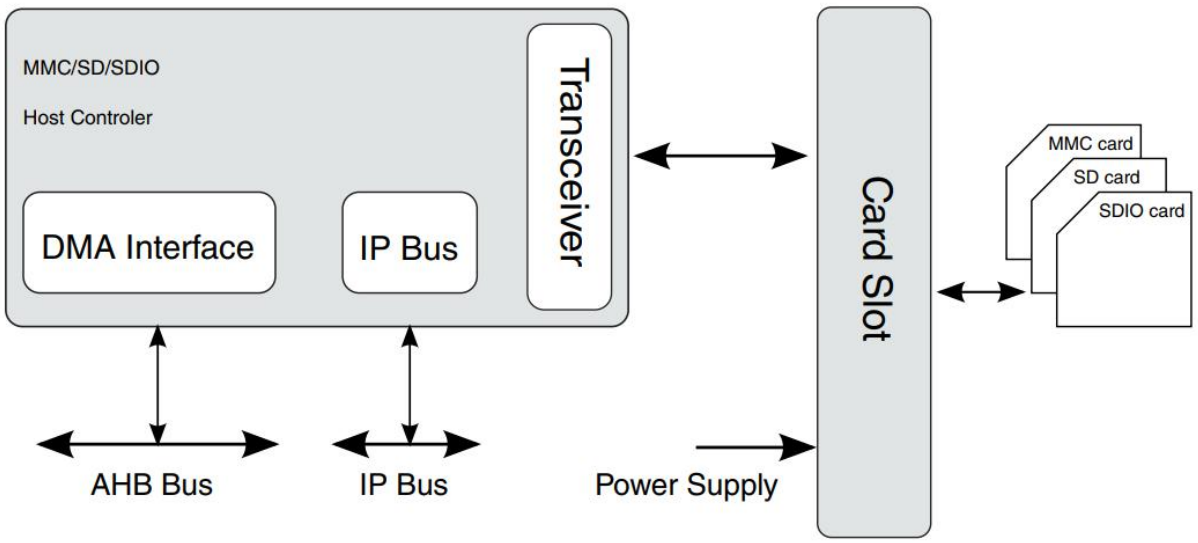


Figure 5-1 uSDHC interface

5.1.1. Reference design

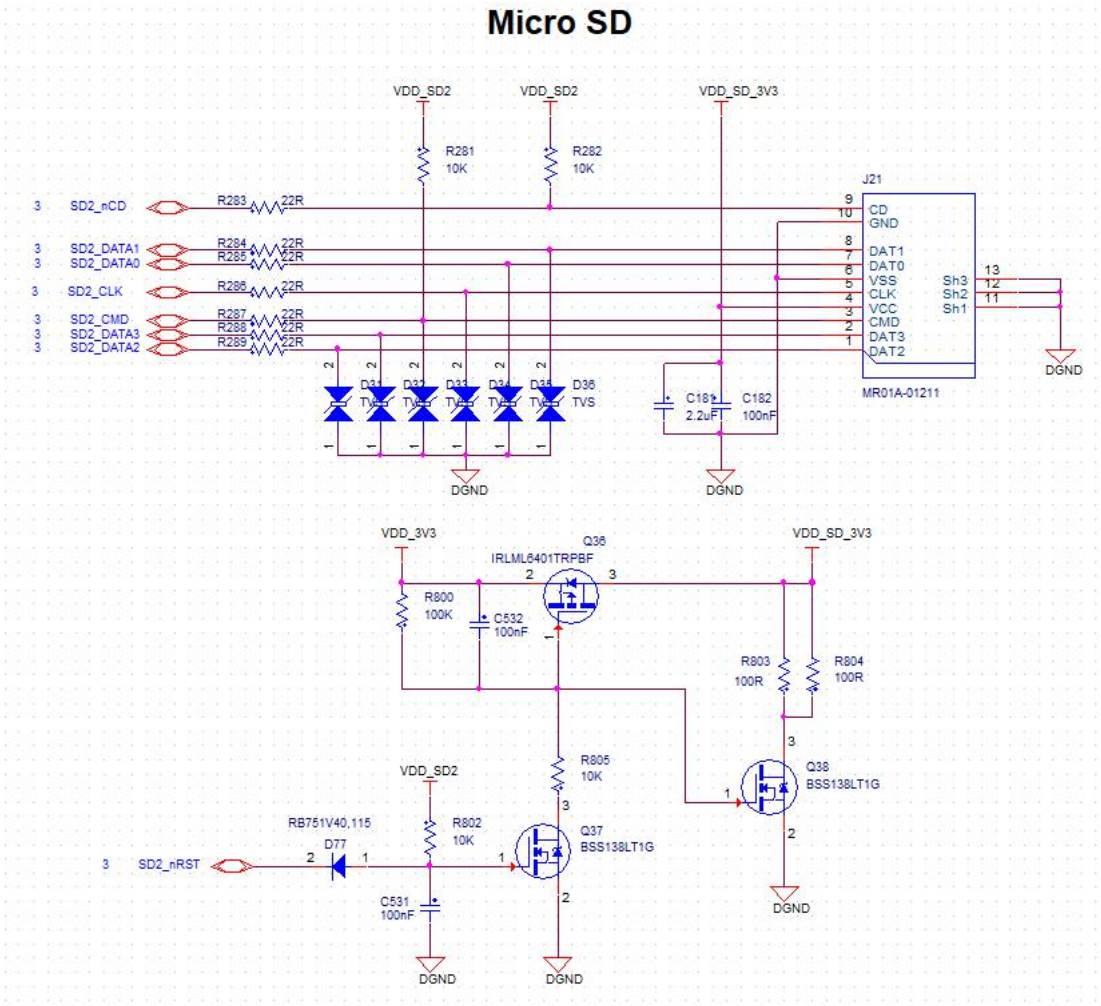


Figure 5-2 SD card Reference design

5.1.2. Layout guidelines

- Single-ended signal 50 Ω impedance;
- Trace match the data line and control line to be within 100 mils;
- SD1_CLK is recommended to be surrounded with ground. If not, ensure the distance between the clock signal and other signals follow 3W rule.

5.2. UART

MYC-C8MMX-V2 core board has up to 4 channels of asynchronous serial port. The core board is configured with four serial ports by default, among which UART1 has the function of flow control (RTS and CTS signals) for the baseboard WIFI/BT module.

In addition, as the voltage level of UART2 and UART4 led from the core board is 1.8V, so the voltage conversion chip TXS0108EPWR used in the carrier board can be directly output after being converted into 3.3V level,while the level of UART3 led from the core board is 3.3V and can be directly output. UART2 is used as the debugging serial port, and UART3 and UART4 are used as external extension serial ports.

5.2.1. Reference Design

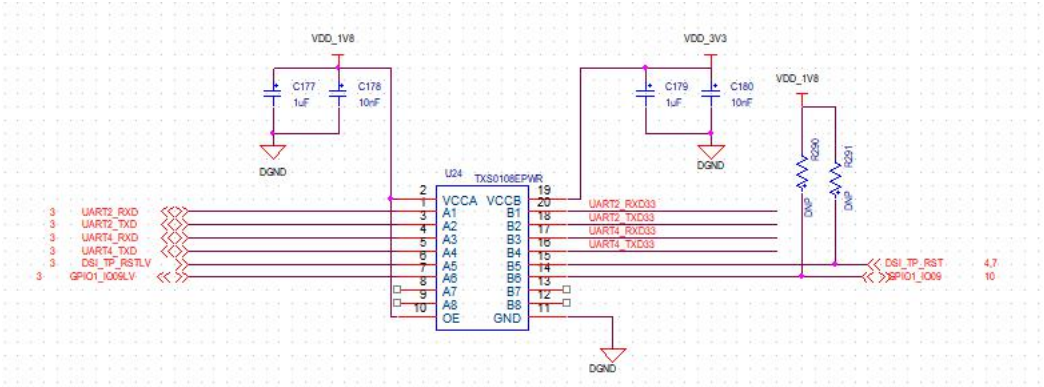


Figure 5-3 Voltage Conversion Circuit

Figure 5-4 debug and external serial reference circuit

5.2.2. Layout Guidelines

- TVS tightening connector placement;
- 22Ω resistors are located close to the connector;

5.3. USB

MYC-C8MMX-V2 core board has two built-in USB2.0 controllers.

One USB1 is directly connected to Micro USB, supports OTG mode, and can also be used as an interface for downloading software. The other USB2 supports only HOST mode and uses the SMSC USB2514BI-AEZ chip to expand four USB HOST ports. Two channels are directly led out through double-layer USB Type A connection socket , the third channel is used to connect LTE module, and the fourth channel is connected to a 4 pin 2.0 mm pitch connector.

USB signal is recommended to add a TVS tube, a common mode inductor.

5.3.1. Reference Design

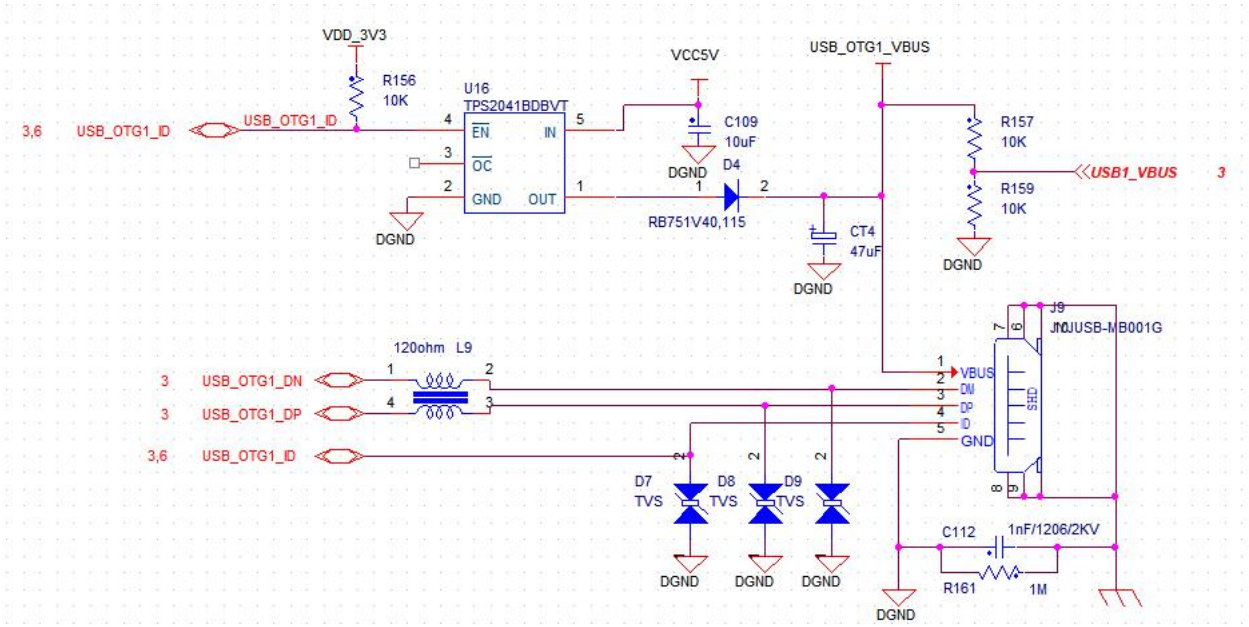


Figure 5-5 Micro USB Reference Circuit

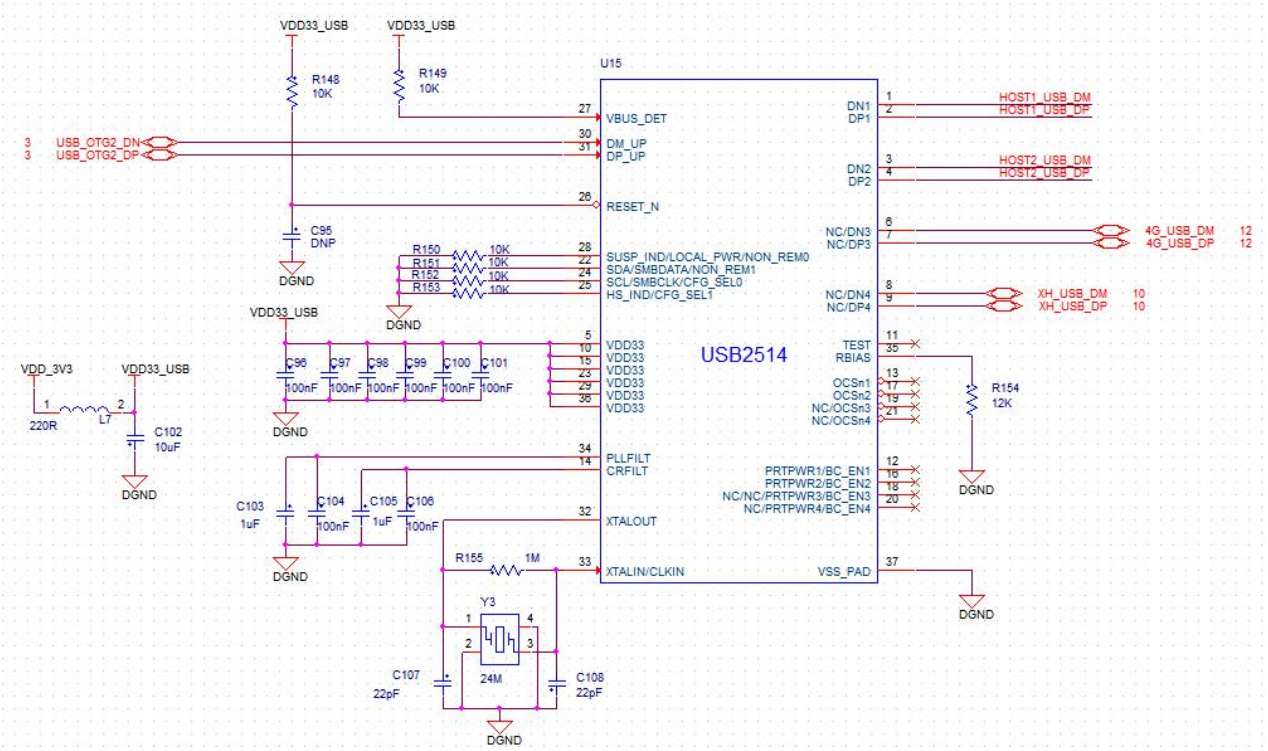
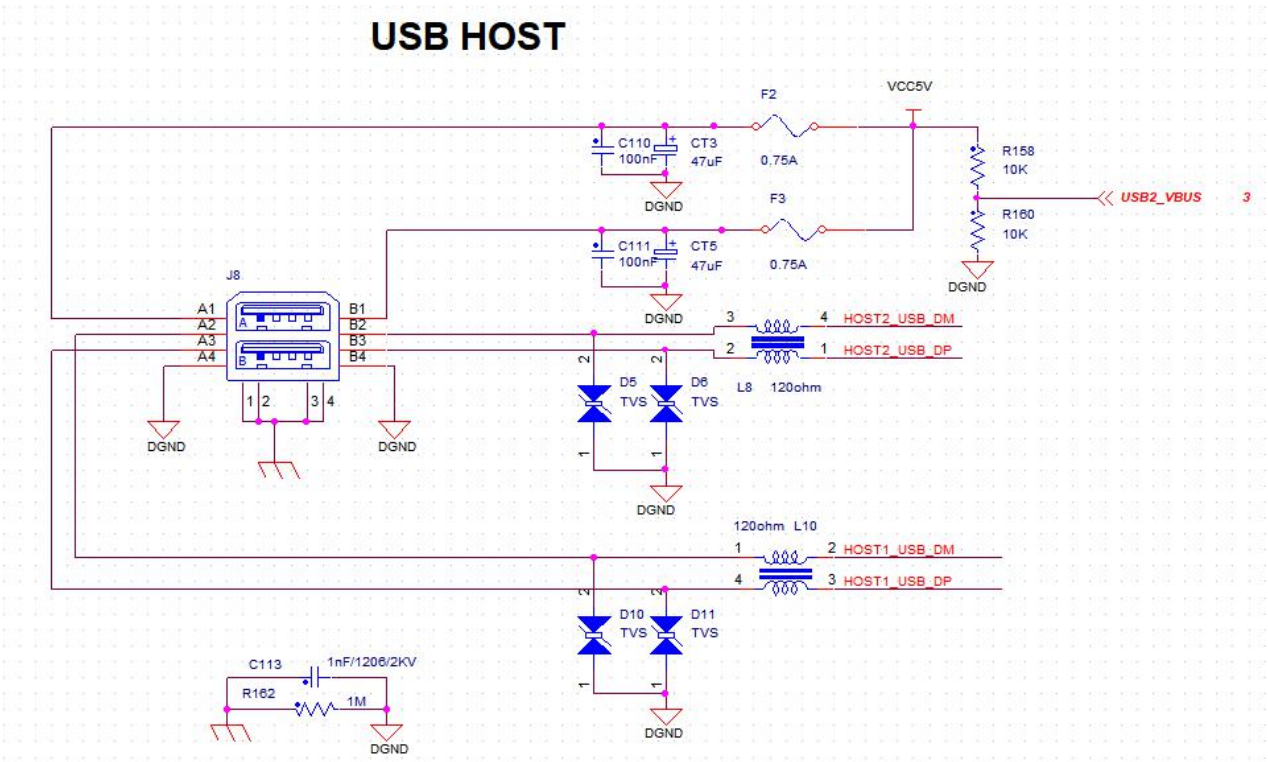


Figure 5-6 USB HUB Reference Circuit



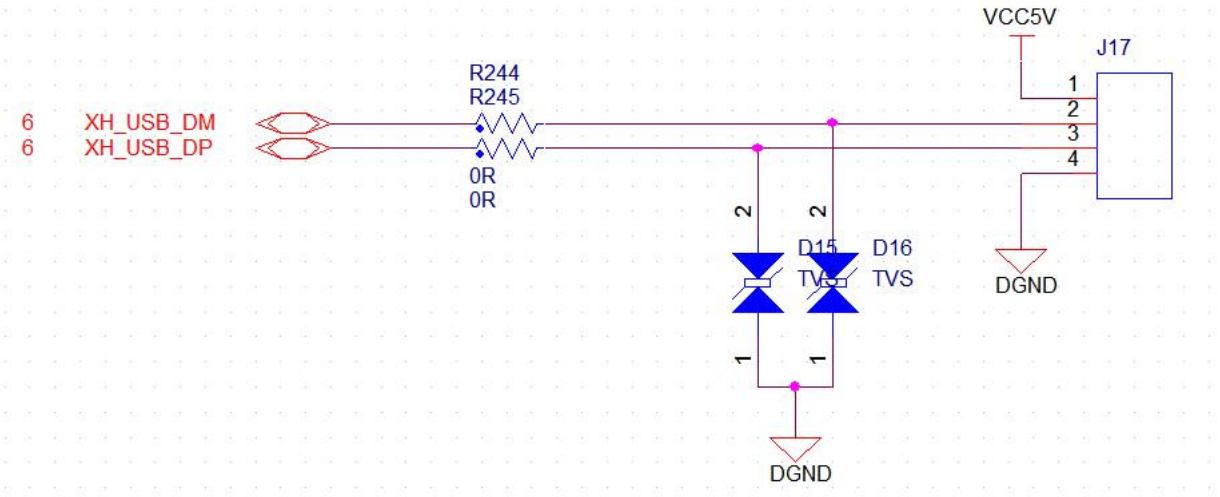


Figure 5-7 USB HOST circuit reference circuit

5.3.2. Layout Guidelines

- USB signal line does the equal length control, error range ± 10mil;
- Differential impedance of the USB signal is controlled by 90Ω;
- USB signal line as short as possible;
- USB signals as soon as possible, if the substation is changed, it is necessary to place the GND reflow via in the range of 200 mils from the changing layer.
- Ensure that the reference plane is continuous, the USB signal should not split;
- USB signal is recommended in TOP / BOTTOM layer;
- The USB signal is remote from other clocks and digital signals.

5.4. Ethernet

MYC-C8MMX-V2 core board is designed with Ethernet PHY circuit, support 10/100/1000M adaptive mode; Users only need to design the transformer isolation circuit and the RJ45 part of the circuit.

5.4.1. Reference Design

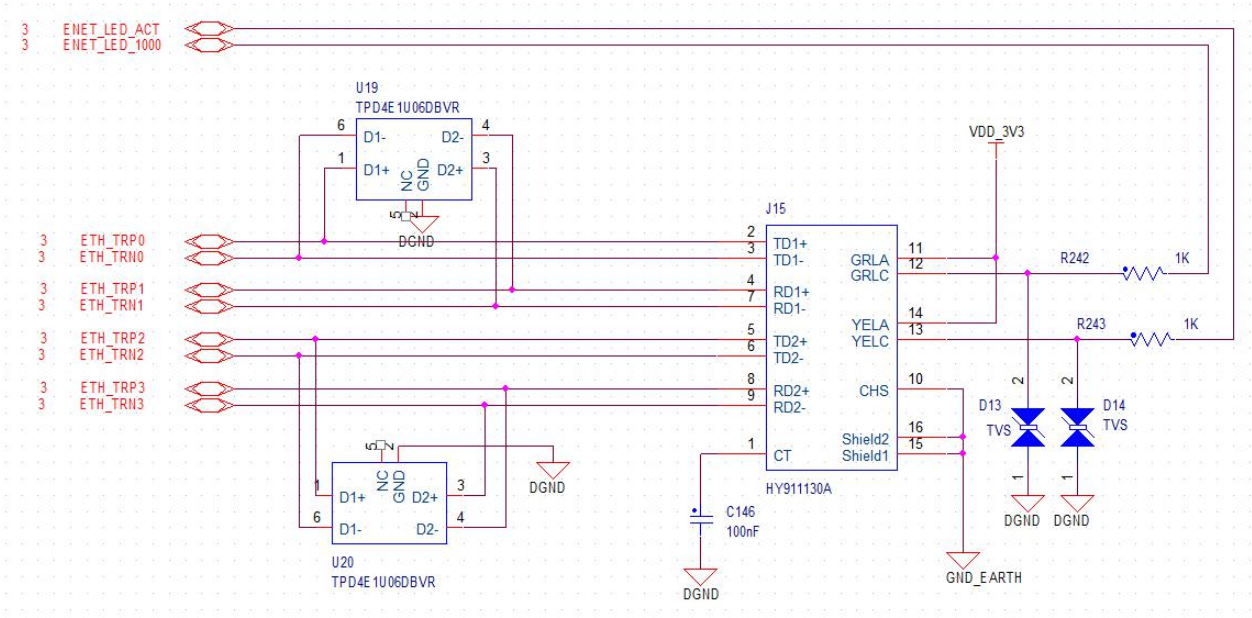


Figure 5-8 Ethernet reference circuit

5.4.2. Layout Guidelines

- Network differential signal is equal long control, differential pair error ± 5 mil, adjacent differential pitch is 3W;
- The 15 \ 16 pin recommended by J15 is directly connected to the metal shell;

5.5. I2C

The I.MX 8M Mini supports a maximum of four I2C buses. The I2C1 is used to connect the PMIC power management chip of the core board, and it is not connected to the core board interface. Therefore, MYC-C8MMX-V2 core board supports up to 3 I2C buses.

Several devices can be mounted on the same I2C main line. The following points should be paid attention to in schematic design:

- Check whether the device address under the same bus is in conflict;
- Ensure that each I2C bus has a pair of pull-up resistors, the resistance value is recommended to be 2.2K~10K, but do not repeatedly add;
- Check whether the level of I2C interface of the device is 3.3V. If not, add the level shift circuit.
- The number of devices under the same bus should not be too large, otherwise it is possible to exceed the load capacitance limit of 400 pF required by the I2C specification and affect the signal waveform.

5.5.1. Reference design

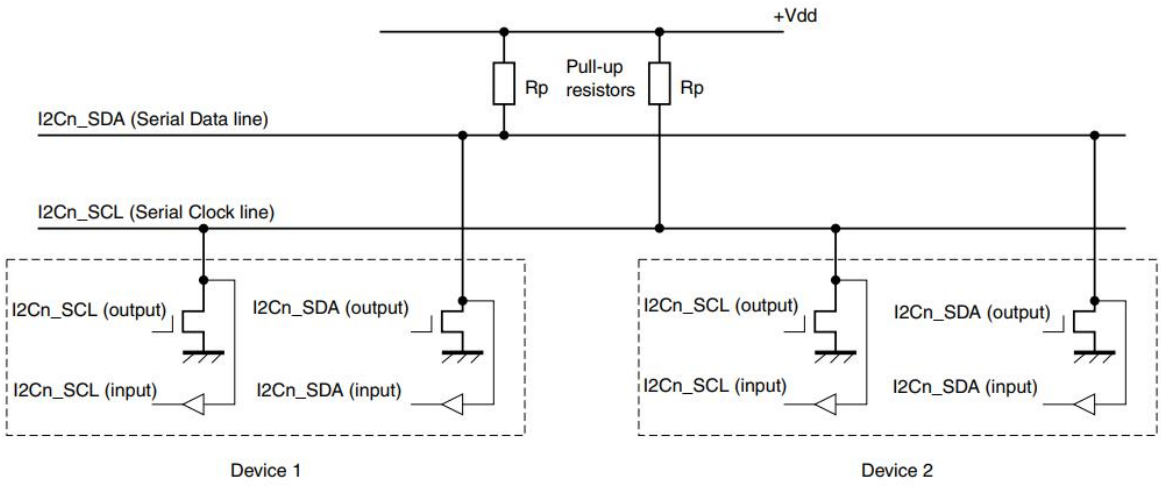


Figure 5-9 I2C reference design

5.5.2. Layout guidelines

- I2C signal line width should not be too narrow, it is recommended to be 6mil or above;
- The location of each I2C device should be planned before layout, if the length of I2C bus is too long will also cause the increase of the bus load capacitance;
- avoid the interference source line, adjacent the pitch of 10 mils.

5.6. SPI

MYC-C8MMX-V2 core board supports a maximum of 3 SPI controllers, supporting master/slave mode. SPI signals include SPI_CLK, SPI_MOSI and SPI_MISO. During design, the relationship between master and slave devices should be confirmed first, and then the direction of MOSI and MISO signals should be confirmed. Due to pin reuse, one ECSPI2 interface is configured on the core board by default. If you want to use more SPI interfaces, please consult the chip manual or use Config Tools for I. MX software for configuration, and modify the pin configuration in the driver.

Access the link for more information:

https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-mini-arm-cortex-a53-cortex-m4-audio-voice-video:i.MX8MMINI

5.6.1. Reference design

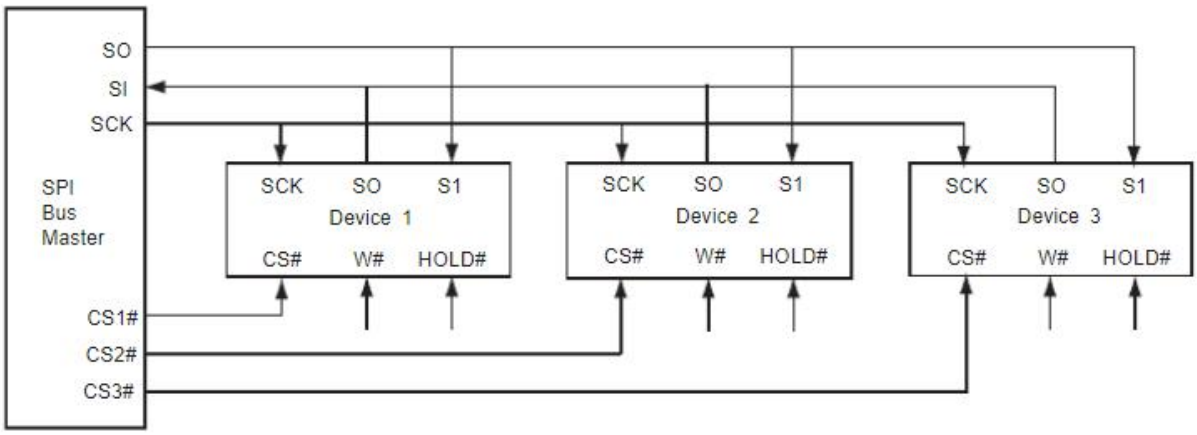


Figure 5-10 SPI reference circuit

5.6.2. Layout guidelines

- Route all SPI signals with 50 Ω single-ended impedance;
- Keep no less than 3 times trace width spacing from other signals;
- Ensure that the reference layer of the signal is continuous.

5.7. CSI

MYC-C8MMX-V2 core board supports one MIPI-CSI interface for external camera input signal. It is recommended that users can purchase the camera module MY-CAM003M in the official flagship store of Taobao To evaluate the CSI function.

Please visit: http://www.myir-tech.com/product/my_cam003m.htmTake more information on the module.

» Key Specifications (typical)

Item		Paramenters
图像分辨率		2592 x 1944
电源供电	核心	1.5VDC ± 5% (with embedded 1.5V regulator)
	模拟电压	2.6 ~ 3.0VDC
	I/O电压	1.8V to 2.8V
功耗	Active	140 mA
	Standby	20 µA
温度范围	工作温度	-30°C to 70°C junction temperature
	稳定图像	0°C to 50°C junction temperature
输出格式		8-/10-bit RGB RAW data
透镜尺寸		1/4"
透镜主射线角		24°
时钟频率		6~27 MHz
Max S/N比率		36 dB (maximum)
动态范围		68 dB @ 8x gain
最大图像传输速率	QSXGA (2592x1944)	15 fps
	1080P	30 FPS
	1280x960	45 fps
	720p	60 fps
	VGA (640x480)	90 fps
	QVGA (320x240)	120 fps
灵敏度		600 mV/Lux-sec
快门		Solling shutter / frame exposure
最大曝光间隔		1964 x tROW
像素大小		1.4 µm x 1.4 µm
暗流		8 mV/s at 60°C junction temperature
图像区域		3673.6µm x 2738.4µm
封装尺寸		5985µm x 5835µm

Figure 5-11 MY-CAM003M camera module specification

5.7.1. Reference design

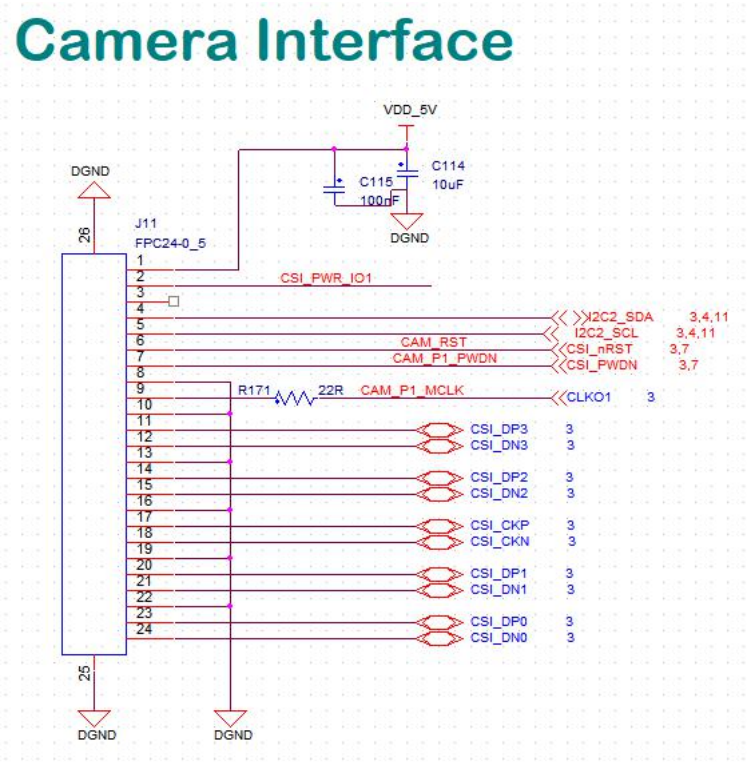


Figure 5-12 CSI Interface Reference Circuit

5.7.2. Layout guidelines

- 22Ω resistor is located close to the FPC connector;
- CSI signal lines do equal long control, differential pairs of ± 5mil, group equal length ± 20mil; CSI signal line spacing at least 2W.

5.8. LCD

The original display interface of i.MX 8M Mini processor is DSI interface, but LVDS interface is not supported. In order to facilitate the use of customers, we use Toshiba's TC358775XBG chip in the design of MYB-C8MMX baseboard to convert the MIPI-DSI signal of the core board into LVDS signal. To support LVDS interface display.

The main function of the chip is to convert DSI signal into LVDS signal to drive LVDS compatible display panel.It supports single-channel LVDS up to 1600x1200 24-bit pixel resolution, dual-channel LVDS up to 1920x1200 24-bit pixel resolution, and supports an I2C master controlled by DSI signals.

The carrier board has two LVDS ports, J4 and J6; 4 port is used to connect to dual LVDS large screen, J6 port is used to connect to single LVDS small screen. J4 and J6 cannot be used at the same time. Customers can choose according to their own requirements.

In addition, when we use J4 interface, also should use J5 interface, J5 is the backlight in terface of the external screen, using 6pin 2.0mm spacing public Socket ; If the J6 port is connected to the touchscreen, the J12 port should also be used. The J12 port is a touchs creen signal port and adopts a 6pin 0.5mm spacing FPC socket .

5.8.1. Reference Design

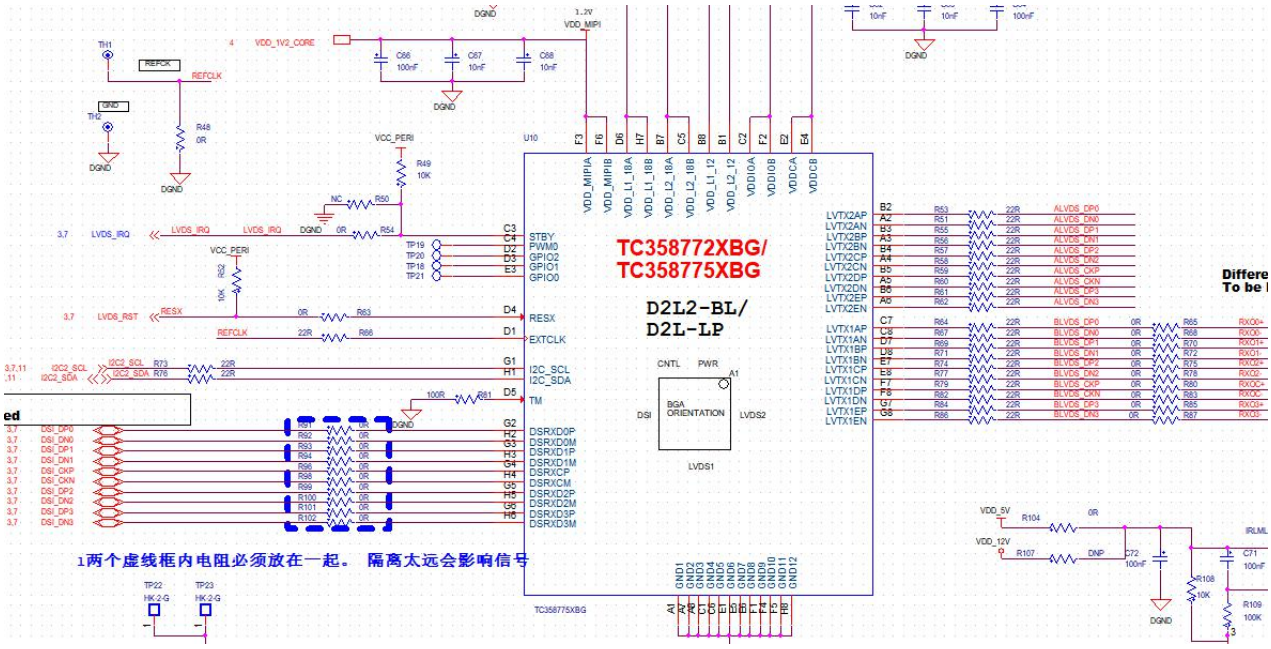


Figure 5-13 DSI-LVDS Interface Reference Circuit

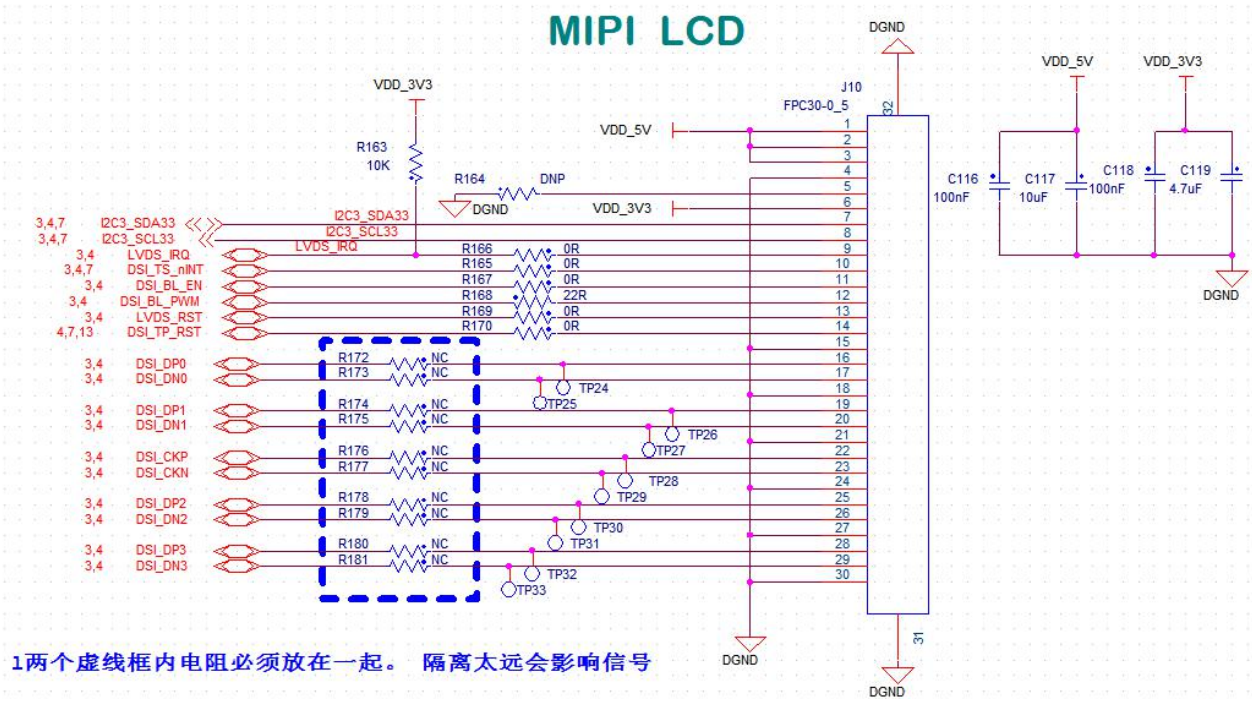


Figure 5-14 DSI Interface Reference Circuit

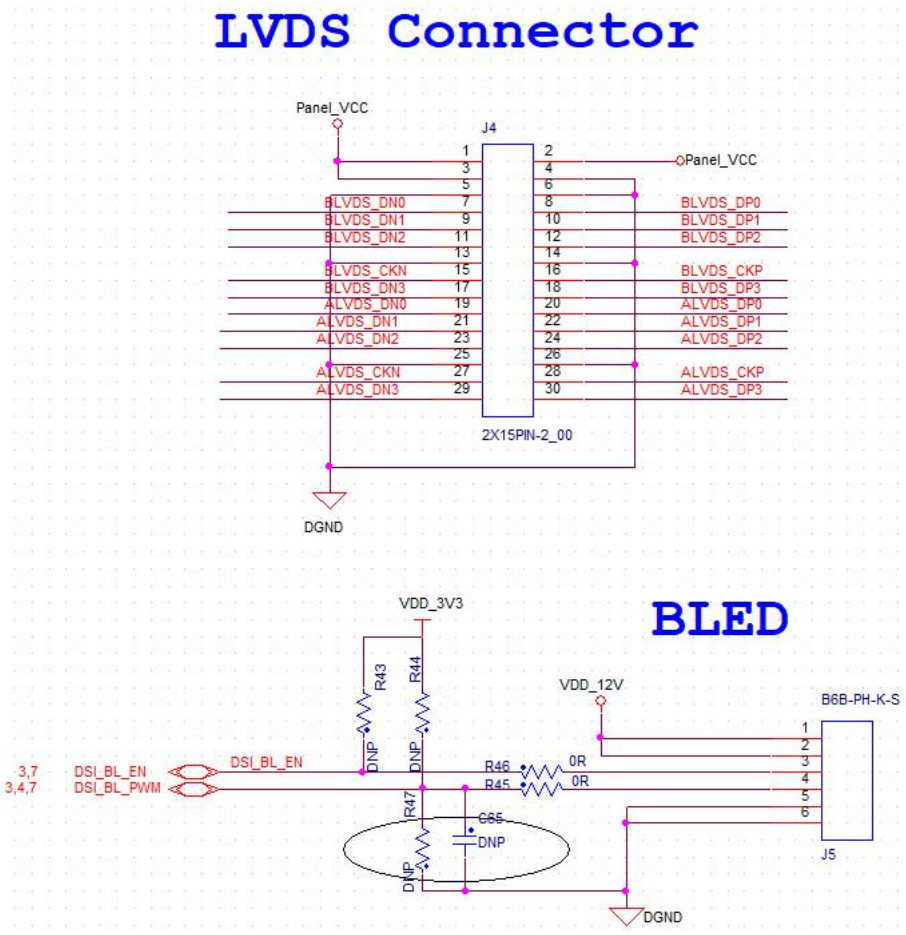


Figure 5-15 Dual LVDS Interface Interface

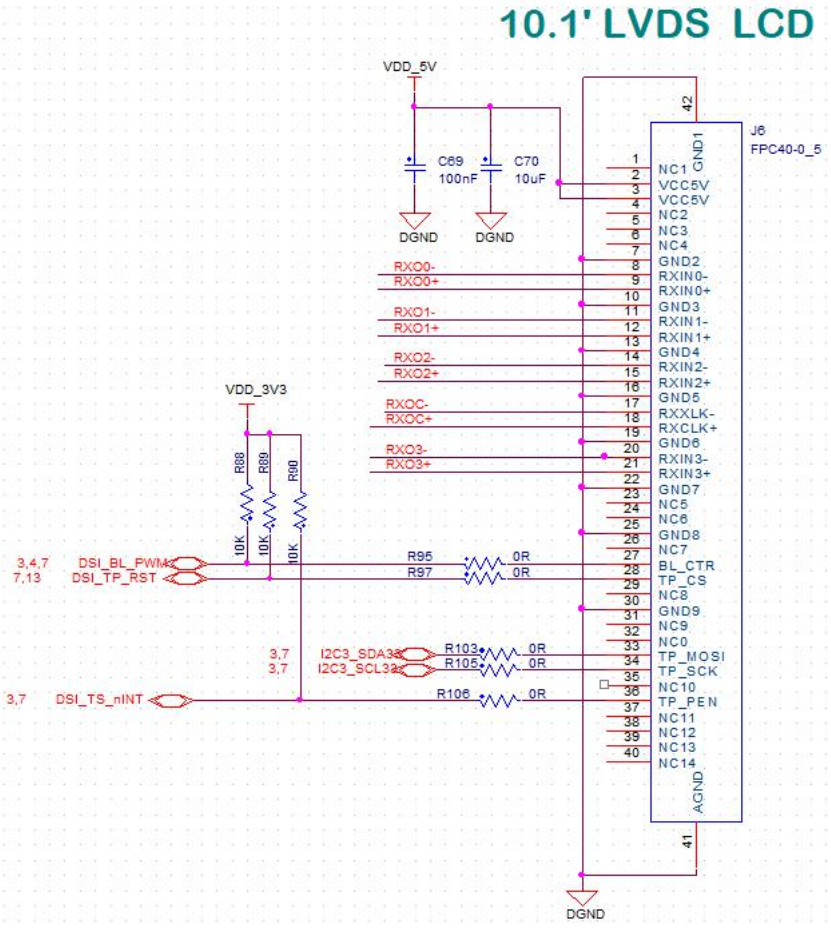


Figure 5-16 Single LVDS Interface Reference Circuit

5.8.2. Layout Guidelines

- 22Ω resistance is located close to the chip stamp hole;
- The resistance in the dashed line must be placed, and the isolation will affect the signal;
- DSI signal lines do equal long control, differential pairs of ± 5 mils, group equal length ± 20mil;
- LVDS signal trace is equal long control, differential pairs of ± 5mil, group equal length ± 20mil;

5.9. AUDIO

The MYC-C8MMX-V2 core board provides five SAI interfaces for synchronous audio. By default, only one SAI interface is configured. SAI interface supports all kinds of full-duplex and serial communication audio interfaces with frame synchronization function, such as I2S, AC97, TDM, CODEC and other common audio interfaces.

The AUDIO_GND of the audio circuit is isolated from the DGND of the digital circuit by a 0 ω resistor. The capacitor of the power supply pin and the filter capacitor of the audio signal should also be connected to the AUDIO_GND.

5.9.1. Reference Design

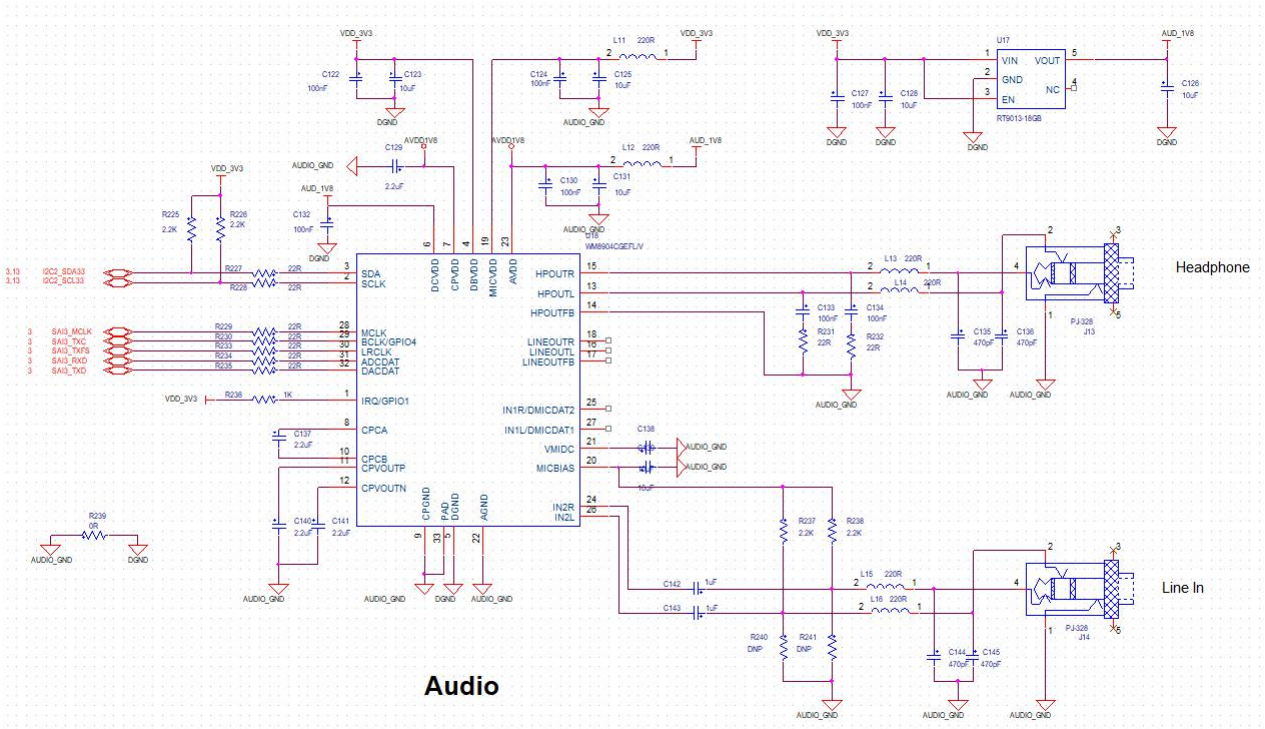


Figure 5-17 Audio Interface Reference Circuit

5.9.2. Layout Guidelines

- The isolation point (R239) of AUDIO_GND and GND uses a star ground to close to the carrier board power input;
- The layout position of the audio circuit is remote from the source of interference, it is recommended to apply a region in the PCB to place analog circuitry separately;
- The audio chip is as close as possible to the headset and microphone jack, and the audio signal is as short as possible.

5.10. Backup battery interface

The evaluation board is equipped with a back-up battery holder that can connect to the CR1225 button battery. When the system is powered off, it can be used to maintain the operation of RTC. Its circuit structure is shown in the figure below:

5.10.1. Reference Design

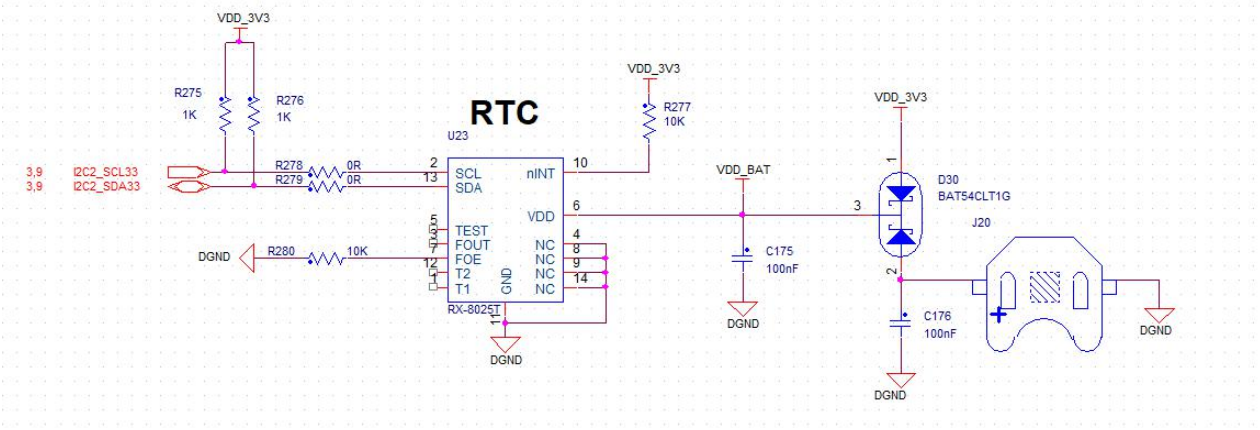


Figure 5-18 Backup Battery Interface

5.10.2. Layout Guidelines

- C176 is located close to J20;
- The I2C signal line width cannot be too narrow, it is recommended to 6MIL or more;
- The location of each device should be planned before the I2C wiring, and the trace should not be too wound;

5.11. WIFI/BT

The MYB-C8MMX incorporates the AP6212 WiFi+Bluetooth 4.1 module from AMPAK. The communication and data interface of the module are UART and SDIO, support 802.11b/ G/N. The standard SMA antenna interface is reserved on the board, which can be used with the complimentary WIFI antenna. Please refer to the design below for details:

5.11.1. Reference Design

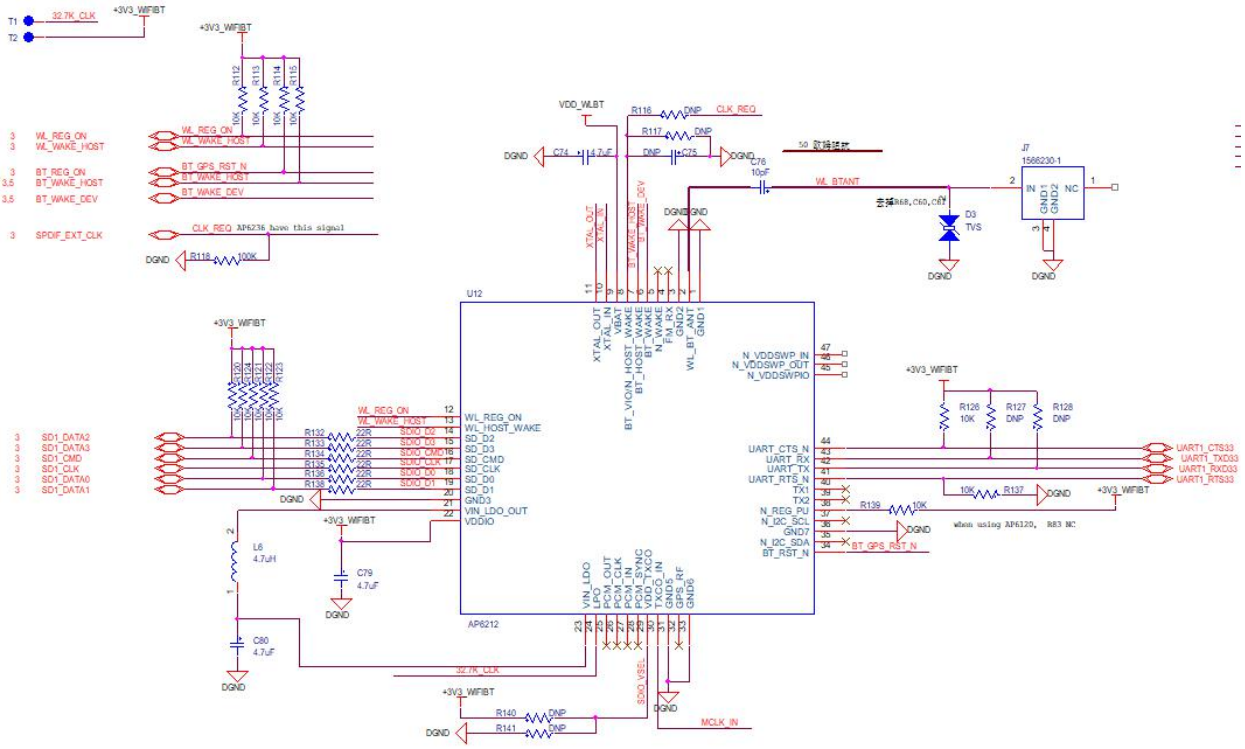


Figure 5-19 WiFi / BT Antenna Interface

5.11.2. Layout Guidelines

- In the package area (including a Bottom layer) to avoid placing other irrelevant devices and traces;
- Single-end impedance of SDIO signals 50Ω, group equal length is less than ± 100mil;
- If there is enough space, the SD1_CLK clock proposes to handle it;

5.12. 4G LTE

MYB-C8MMX development board provides Linux driver support and code samples based on Shanghai Mobile Communication EC20 LTE module. The module adopts 3.8V power supply, and the USB end of LTE module on the board is connected to the third port of USB Hub.

To be used with LTE module, MYB-C8MMX is equipped with a popable SIM card, and 4G antenna users can connect to the ANTENNA interface of LTE module through I-PEX.

5.12.1. Reference Design

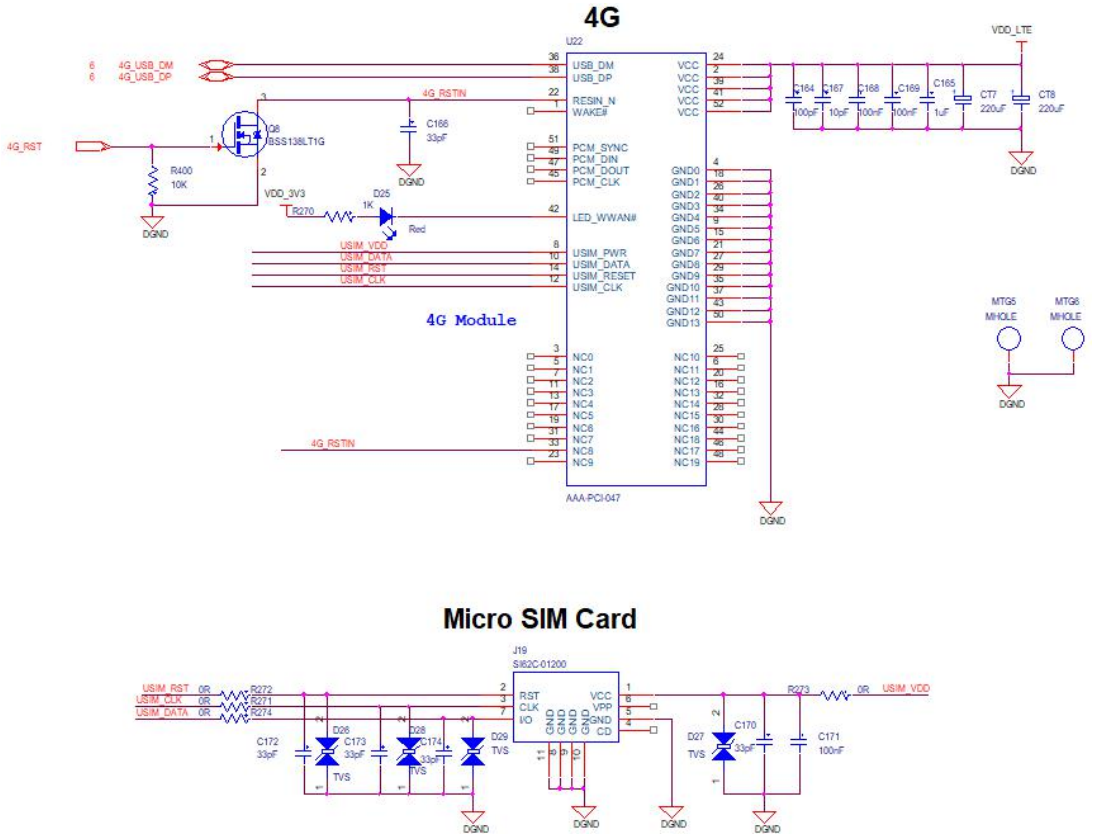


Figure 5-20 4G LTE module reference circuit

5.12.2. Layout Guidelines

- 4G module remote from sensitive circuits and other interference sources, SIM cards are close to 4G modules;
- USB signal differential impedance 90Ω, equal length control error ± 10mil;
- To prevent USIM_DATA signals from crosstalk with the USIM_CLK signal, the wiring is not too close, and the blockade is needed between the two traces;
- The parasitic capacitance of the selected TVS tube is not more than 10pF, and the value of the C172 \ C173 \ C174 is recommended 33pF.

6. Design checklist

6.1. Power supply design

Check box	Proposal
1. core module supply voltage	The recommended value is 5V and the absolute value is 4.5V-5.5V
2. Decoupling capacitance	Use capacitors with 47uF and above value for core module power supply
4. IO level of carrier board peripherals	The IO voltage level of the peripheral should match the corresponding interface level of the core module
5. core module power sequence	It is recommended that the core module power start before the peripheral power
6. Power chip temperature rise	Confirm the thermal resistance of the power chip, and calculate the maximum temperature rise of the power chip based on the power consumption of the core module to ensure that the final temperature is within the specified range of the power chip

Table 6-1 Power supply checklist

6.2. System startup circuit design

Check box	Proposal
1. Configuration of BOOT_MODE pins	Choose the right BOOT MODE according to the needs of the product
2. Reset pins	POR and ONOFF pins are both recommended to be used

Table 6-2 System startup checklist

6.3. Peripheral circuits design

Category	Check box	Proposal
USB	Capacitance value of USB D+/D- signal ESD device	The capacitance value of ESD devices is recommended to be less than 2pF
	Whether the capacitor of the supply pin is added series resistance	The interface 5V capacitor requires a 1-ohm resistor in series to limit the voltage surge at the USB port
I2C	The value of pull up resistor of I2C	The more devices on the bus, the smaller the resistance value should be, otherwise the larger; Recommended resistance is 1.5K/ 2.2k /4.7K;
	How many pull-up resistors are required for each I2C bus	Just one pair
	The voltage value of the pulled up resistor	The pulled up resistor must be connected to the voltage that matches the I/O level
uSDHC	Whether the DATA and CMD signals are pulled up	Need to be pull up, i.e 47K resistor pulled up to 3.3V
CAN	Whetther the CAN-BUS should be isolated	In the cases of complex electrical environment, high reliability requirement or long CAN-BUS cable, CAN transceiver and its power supply circuit should be isolated

Table 6-3 Check list of peripheral circuits

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;

- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

MYIR Electronics Limited

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