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MYC-Y6ULX Product Manual

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Shenzhen MYIR Electronic Co. LTD

History

Version	Author	Participants	Date	Description
V1.0	Leoric	Jacob	20211221	The version is updated to V2
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1. Overview

As the increasingly advanced technology, a variety of industry applications with embedded processors appear continually. ARM processors with its rich features and excellent cost-effectiveness has become the most indispensable component of embedded products. Therefore, Myirtech has launched the embedded core module MYC-Y6ULX-V2 based on NXP's i.MX 6UL/6ULL series processors. MYC-Y6ULX-V2 core module has the advantages of low cost , rich interfaces and high performance ,which can be used in many applications such as IOT, image processing, electric power industry, etc.

The MYC-Y6ULX-V2 core module integrates all core elements of a micro controller system on a subminiature board and is designed in a manner that ensures its easy expansion and embedding in peripheral hardware developments.

In order to accelerate your design, Myirtech will offer relate materials such as SDK, desi gn documents, development tools, etc. All of above can be found in the following websit e:http://down.myir-tech.com/MYD-Y6ULX-V2.

During development phase, you can select the matched EVK to assist your development. The MYD-Y6ULX-V2 EVK is an entry level development board for industrial and commercial application, which helps developers get familiar with the processor before investing a large amount of resources in more specific designs. Visit the following link to get more information:

http://www.myir-tech.com/product/myc_y6ulx.htm

Figure 1-1 MYC-Y6ULX-V2 Core Board

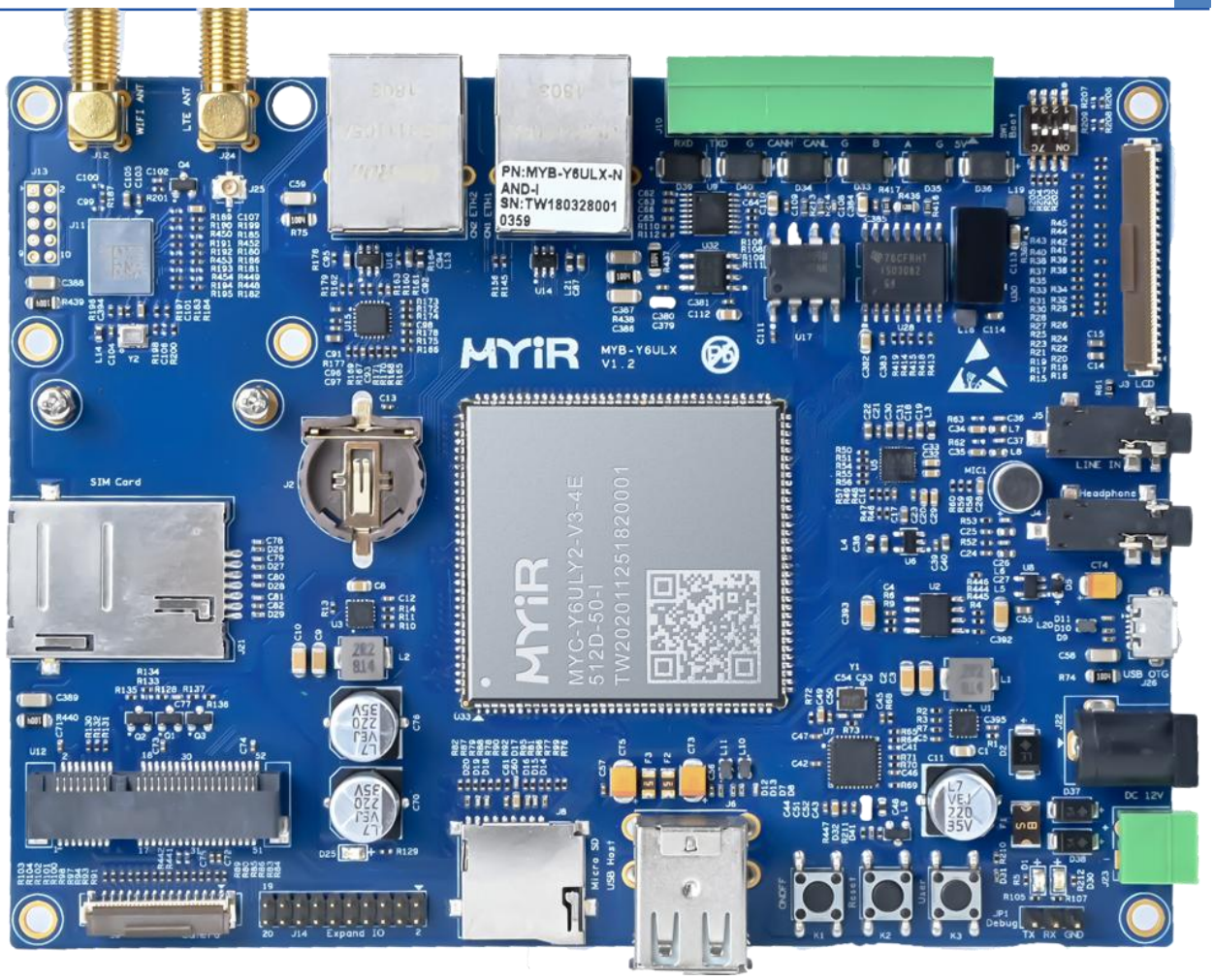

Figure 1-2 MYD-Y6ULX-V2 EVK

2. Product Introduction

MYC-Y6ULX-V2 series core module is a well-designed embedded core module with low cost, low power consumption and high performance using stamp hole interface. It adopts NXP Cortex-A7 kernel i.MX6UL/ULL processor, and the main frequency is as high as 528 MHz, with plenty of commonly used industrial control communication interfaces.

The core modules of the MYC-Y6ULX-V2 series contain five specific product models: they differ in storage configuration, main CPU specifications, etc., and customers can choose the right model according to their needs. See the instructions in section 2.4 for differences between product models.

2.1. i.MX.6UL/6ULL

i.MX 6UL and i.MX 6ULL are two different processor series introduced by NXP, but they are basically different in terms of chip architecture and functional interfaces, but some differences in encryption capabilities.

2.1.1. 6UL

The i. MX6UL series is based on a high-performance, ultra-low power ARM Cortex-A7 core processor that runs at up to 528 MHz and includes 128 KB L2 caches and 16-bit DDR3 /LPDDR2 support. Power management is integrated internally, simplifying the power-on timing design. It also integrates security units and a rich interconnect interface for next-generation consumer electronics, industrial control and automotive applications.

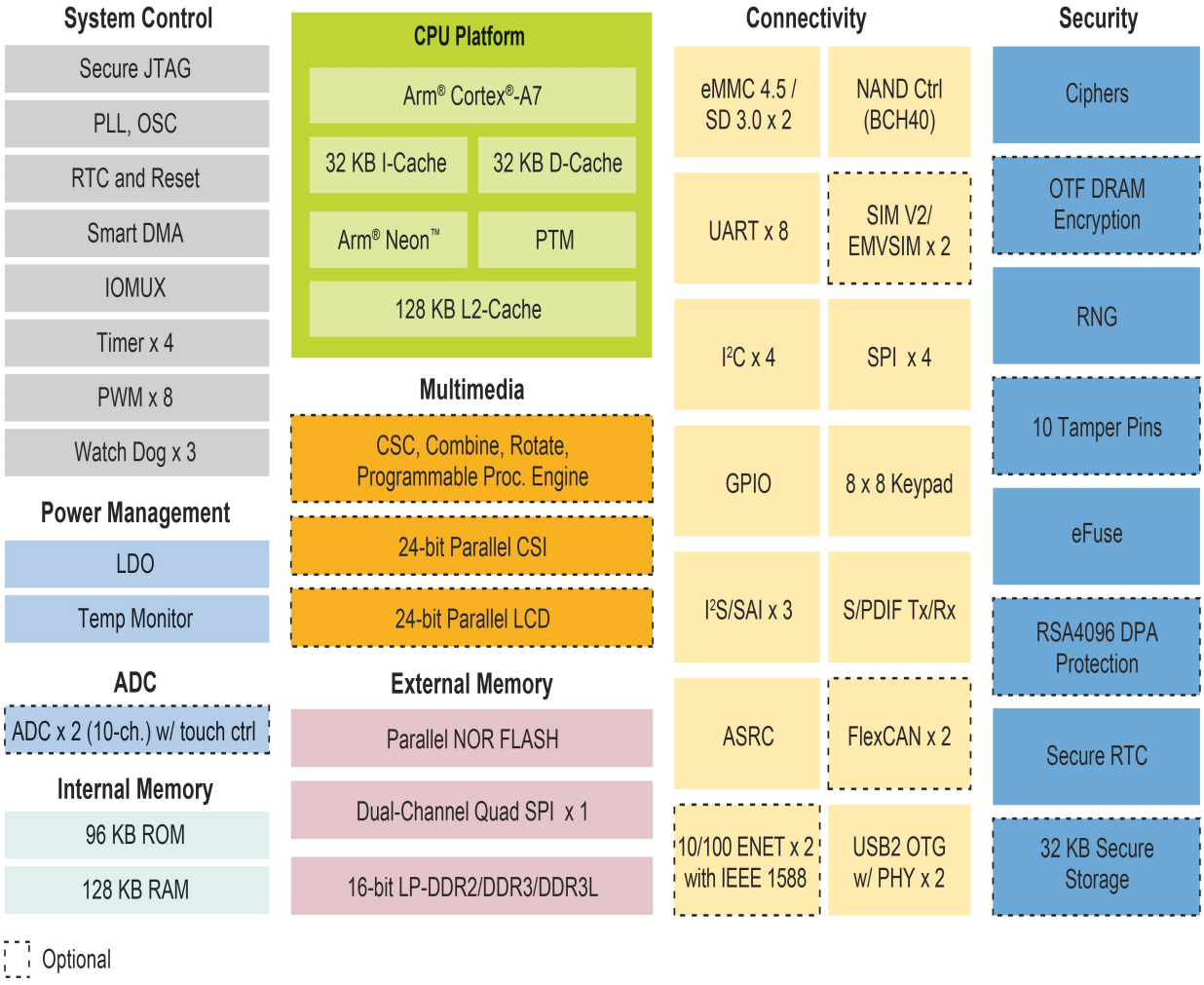

Figure 2-1 i.MX6UL Block Diagram

● Arm Cortex-A7 up to 696 MHz, 128 KB L2 cache
● Parallel LCD Display up to WXGA (1366x768)
● 8/10/16/24-bit Parallel Camera Sensor Interface
● 16-bit LP-DDR2, DDR3/DDR3L
● 8/16-bit Parallel NOR FLASH / PSRAM
● 8-bit Raw NAND FLASH with 40-bit ECC
● Dual-channel Quad-SPI NOR FLASH
● 2x MMC 4.5/SD 3.0/SDIO Port
● 2x USB 2.0 OTG, HS/FS, Device or Host with PHY
● Audio Interfaces include 3x I2S/SAI, S/PDIF Tx/Rx
● 2x 10/100 Ethernet with IEEE 1588
● 2x 12-bit ADC, up to 10 input channel total, with resistive touch controller (4-wire/5-wire)
● Partial PMU Integration
● Encryption, PCI4.0 pre-certification
● Security Block: TRNG, Crypto Engine (AES with DPA, TDES/SHA/RSA), Tamper Monitor, Secure Boot, SIMV2/EVMSIM X 2, OTF DRAM
● 14x14 289 MAPBGA 0.8mm pitch

Figure 2-1 i.MX6UL CPU Features

For more information, please refer to the website link:https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?&tab=Documentation_Tab&linkline=Data-Sheet

2.1.2. 6ULL

Compared to The i.MX6UL series, i.MX6ULL series processor streamlines some encryption functions while maintaining the original features (cost-effective and ultra-low power), which can be regarded as Cost-optimized version of the i.MX6UL series.

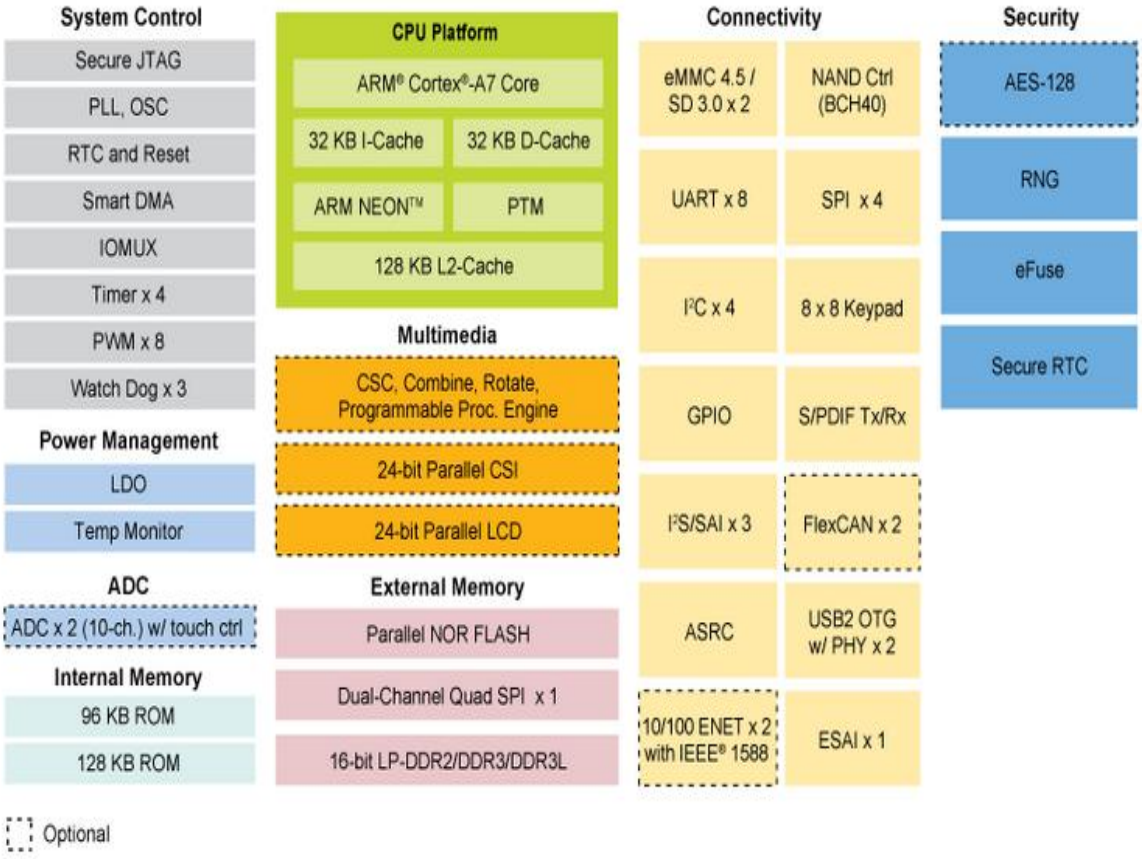

Figure 2-2 i.MX6ULL Block Diagram

● Cortex-A7 core up to 900 MHz, 128 KB L2 cache
● Parallel LCD Display up to WXGA (1366x768)
● 8/10/16/24-bit Parallel Camera Sensor Interface
● 16-bit LP-DDR2, DDR3/DDR3L
● 2x MMC 4.5/SD 3.0/SDIO Port
● 2x USB 2.0 OTG, HS/FS, Device or Host with PHY
● Audio Interfaces include 3x I2S/SAI, S/PDIF Tx/Rx
● 2x 10/100 Ethernet with IEEE 1588
● 2x 12-bit ADC, up to 10 input channel total, with resistive touch controller (4-wire/5-wire)
● Partial PMU Integration
● Security Block: TRNG, Crypto Engine (AES with DPA, TDES/SHA/RSA), Secure Boot
● 14x14 289 MAPBGA 0.8mm pitch

Figure 2-2 i.MX6ULL CPU Features

For more information, please refer to the website link:https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ull-single-core-processor-with-arm-cortex-a7-core:i.MX6ULL?&tab=Documentation_Tab&linkline=Data-Sheet

2.2. Key Features

Item	Parameter
MPU Series	i.MX6UL/6ULL
MPU Part Number	MCIMX6G2CVM05AB (i.MX6UL) MCIMX6Y2CVM05AB (i.MX6ULL)
MPU ARCH	ARM Cortex-A7
Frequency	528Mhz
Support DRAM	DDR3L，optional 256MB / 512MB
Support Flash	optional Nand Flash / eMMC
Mechanical Size	37 x 39 x 3.5 mm (PCB 1.6mm thickness, Shielding case is 1.8mm)
Half stamp hole connector	Pin pitch is 1.0mm
PCB technology	10 layers, immersion gold on surface of PCB
Operation System	Linux 5.4
Security	TRNG, Crypto Engine (AES with DPA, TDES/SHA/RSA), Secure Boot

Figure 2-3 Key Features

2.3. Block Diagram

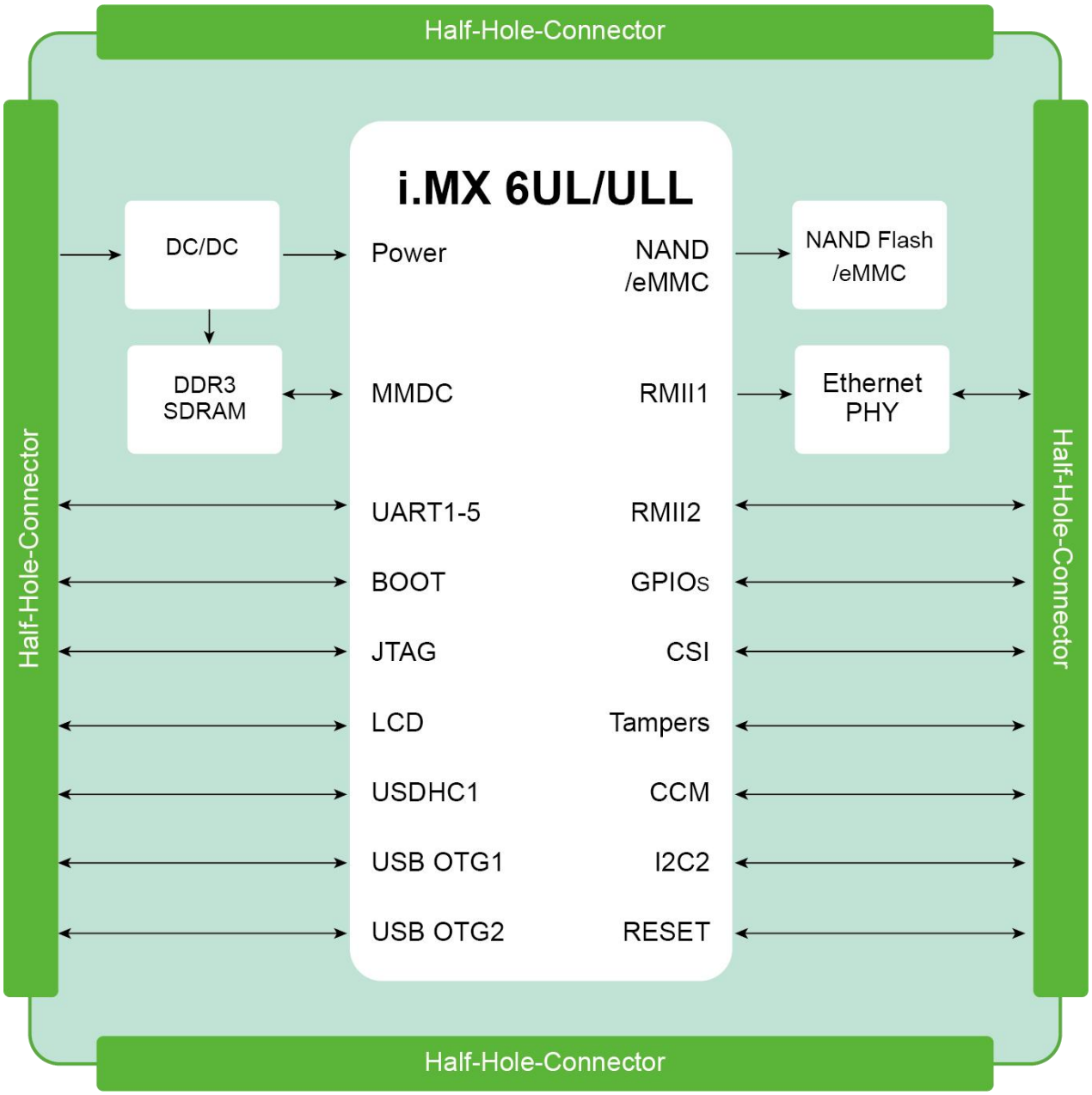

Figure 2-3 MYC-Y6ULX-V2 Block Diagram

2.4. Ordering Information

Depending on cpu model, storage device, operating temperature and other parameters, MYC-Y6ULX-V2 core module is broken down into 5 different models, please choose the best model for you from the lists below.

Models / Item	MYC-Y6ULY2-V2-256N256D-50-C	MYC-Y6ULY2-V2-256N256D-50-I
MPU	MCIMX6Y2CVM05AB	MCIMX6Y2CVM05AB
i.MX6	i.MX 6ULL	i.MX 6ULL
Cortex Arch	Cortex-A7	Cortex-A7
Core clock	528MHz	528MHz
Linux version	Linux 5.4	Linux 5.4
DDR3/DDR3L	256MB DDR3	256MB DDR3
Flash	256MB Nand Flash	256MB Nand Flash
Display resolution	1366*768@60 Hz	1366*768@60 Hz
Displays RGB Mode	8/16/18/24bit	8/16/18/24bit
TSC	support capacitive touch screen support resistive touch screen	support capacitive touch screen support resistive touch screen
UART	x8	x8
CAN-bus	x2	x2
USB OTG	x2	x2
ENET	x2, RMII	x2, RMII
I2C	x4	x4
SPI	x4	x4
GPIO	97	97
PWM	x8	x8
AD	x2 ADC PHY (10 channels) 10bit	x2 ADC PHY (10 channels) 10bit
Power Supply	+3.3V	+3.3V
Mechanical Size	37mm*39mm	37mm*39mm
Work Temp	0℃ - +70℃	-40℃ - +85℃
Footprint PIN	140	140
Certification	CE ROHS	CE ROHS

Figure2-5 MYC-Y6ULX-V2 Part Number List1

Note: 1. Amount of interfaces listed above is the max parameter. Due to the pin multiplexing, some interfaces haven`t been set as their max ports by default, such as the amount of UARTS is up to 8, but only 5 of them are used by default.

2. If you want to use more ports then that configured by default, please use the pinmux tool offered by us to assist you to accomplish the pin multiplexing config.

Models / Item	MYC-Y6ULY2-V2-4E512D-50-C	MYC-Y6ULY2-V2-4E512D-50-I
MPU	MCIMX6Y2CVM05AB	MCIMX6Y2CVM05AB
i.MX6	i.MX 6ULL	i.MX 6ULL
Cortex Arch	Cortex-A7	Cortex-A7
Core clock	528MHz	528MHz
Linux version	Linux 5.4	Linux 5.4
DDR3/DDR3L	512MB DDR3	512MB DDR3
Flash	4GB eMMC Flash	4GB eMMC Flash
Display resolution	1366*768@60 Hz	1366*768@60 Hz
Displays RGB Mode	8/16/18/24bit	8/16/18/24bit
TSC	support capacitive touch screen support resistive touch screen	support capacitive touch screen support resistive touch screen
UART	x8	x8
CAN-bus	x2	x2
USB OTG	x2	x2
ENET	x2, RMII	x2, RMII
I2C	x4	x4
SPI	x4	x4
GPIO	97	97
PWM	x8	x8
AD	x2 ADC PHY (10 channels) 10bit	x2 ADC PHY (10 channels) 10bit
Power Supply	+3.3V	+3.3V
Mechanical Size	37mm*39mm	37mm*39mm
Work Temp	0℃ - +70℃	-40℃ - +85℃
Footprint PIN	140	140
Certification	CE ROHS	CE ROHS

Figure2-6 MYC-Y6ULX-V2 Part Number List2

Note: 1. Amount of interfaces listed above is the max parameter. Due to the pin multiplexing, some interfaces haven`t been set as their max ports by default, such as the amount of UARTS is up to 8, but only 5 of them are used by default.

2. If you want to use more ports then that configured by default, please use the pinmux tool offered by us to assist you to accomplish the pin multiplexing config.

Models / Item	MYC-Y6ULG2-V2-256N256D-50-I
MPU	MCIMX6G2CVM05AB
i.MX6	i.MX 6UL
Cortex Arch	Cortex-A7
Core clock	528MHz
Linux Version	Linux 5.4
DDR3/DDR3L	256MB DDR3
Flash	256MB Nand Flash
Display resolution	1366*768@60 Hz
Displays RGB Mode	8/16/18/24bit
TSC	support capacitive touch screen support resistive touch screen
UART	x8
CAN-bus	x2
USB OTG	x2
ENET	x2, RMII
I2C	x4
SPI	x4
GPIO	97
PWM	x8
AD	x2 ADC PHY (10 channels) 10bit
Power Supply	+3.3V
Mechanical Size	37mm*39mm
Work Temp	0℃ - +70℃
Footprint PIN	140
Certification	CE ROHS

Figure2-7 MYC-Y6ULX-V2 Part Number List3

Note: 1. Amount of interfaces listed above is the max parameter. Due to the pin multiplexing, some interfaces haven`t been set as their max ports by default, such as the amount of UARTS is up to 8, but only 5 of them are used by default.

2. If you want to use more ports then that configured by default, please use the pinmux tool offered by us to assist you to accomplish the pin multiplexing config.

3. Pin Description

3.1. Pinout

The MYC-Y6ULX-V2 core module and baseboard are connected by 1.0mm pitch stamp holes, which can be directly soldered onto your carrier board.

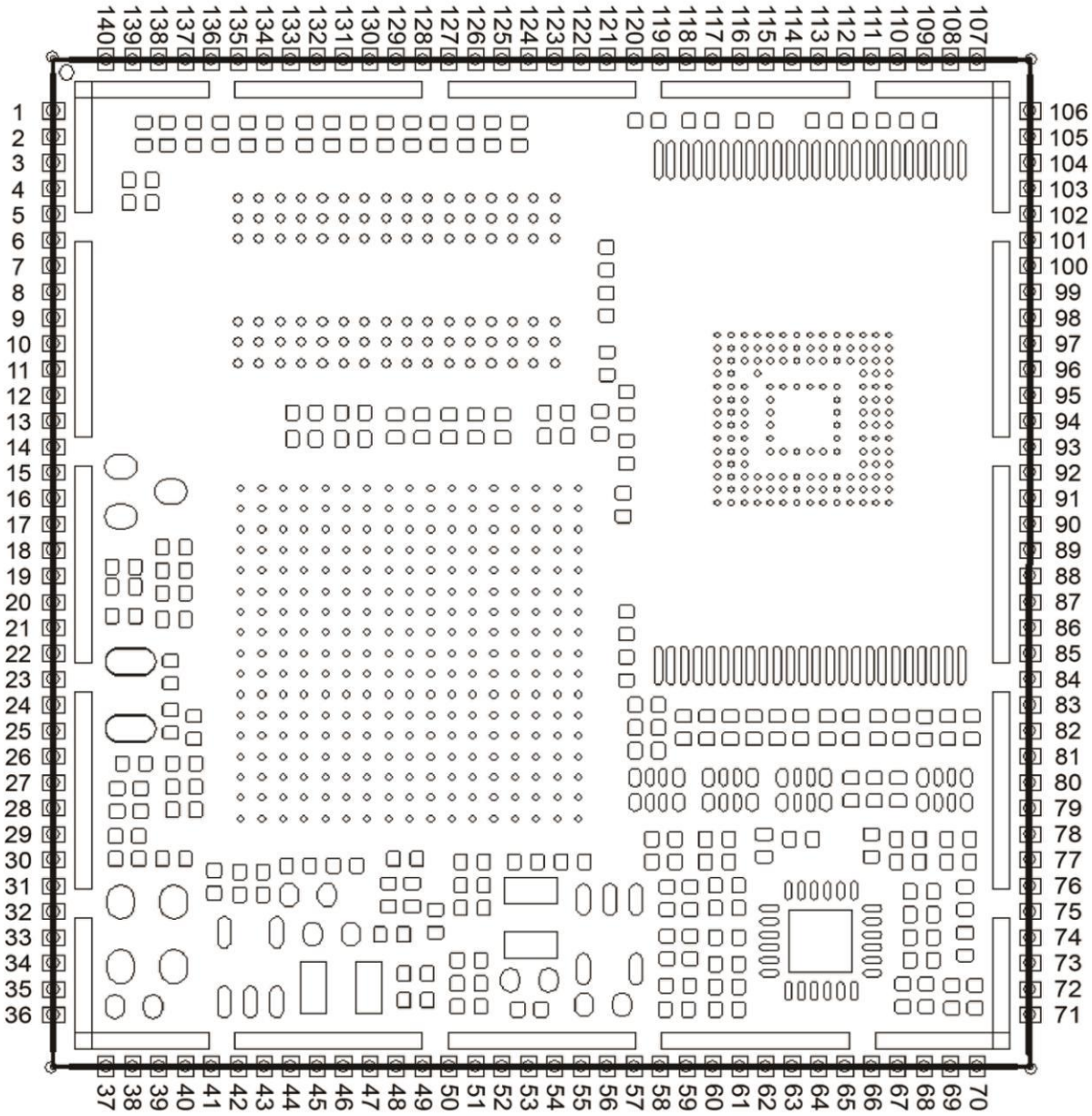

Figure 3-1 Top View of MYC-Y6ULX-V2

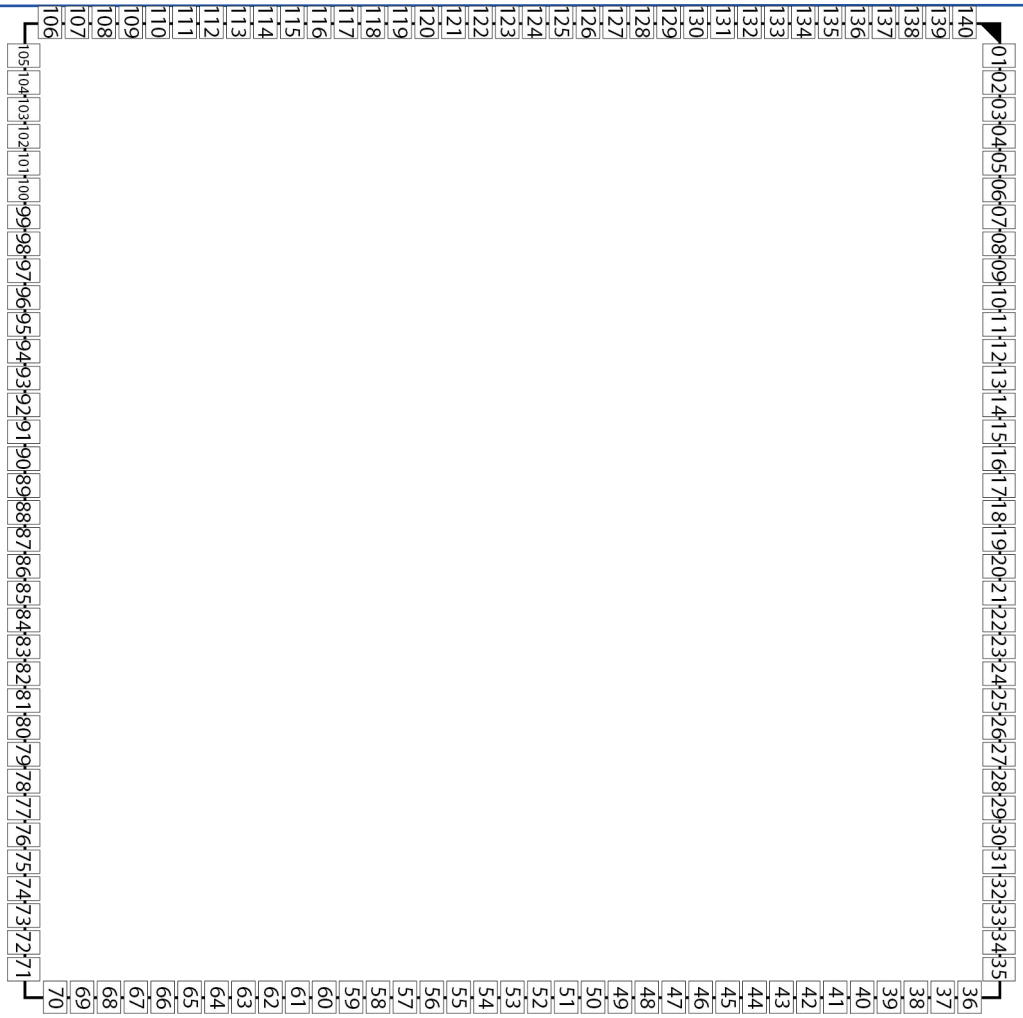

Figure 3-2 Bottom View of MYC-Y6ULX-V2

3.2. Pinlist

MYC-Y6ULX-V2 core module interface pins definition is shown in table below, BSP development package pin functions are configured according to the column "default function", if you need to change the pin default function, please modify the relevant driver configuration code, otherwise it will cause conflicts or other uncertain anomalies.

Pin	Label	Function	Description	Voltage	I/O	BGA Pin	Note
1	ONOFF	On or OFF	i.MX 6UL/6ULL ONOFF (Button) input	3.3V	In	R8	if not use,let it floating
2	POR_B	nRST_IN	Reset input (low active)	3.3V	In	P8	10K pull up to 3.3V on SOM
3	PMIC_ON_REQ	PMIC_ON_REQ	PMIC on request	3.3V	In	T9	if not use,let it floating
4	BOOT_MODE0	BOOT	Boot mode 0	3.3V	In	T10	10K pull up to 3.3V on SOM
5	BOOT_MODE1	BOOT	Boot mode 1	3.3V	In	U10	10K pull up to 3.3V on SOM
6	GND	GND	Power GND	0V	—	—	
7	GPIO5_8	GPIO	GPIO5_8	3.3V	In/Out	N9	
8	GPIO5_7	GPIO	GPIO5_7	3.3V	In/Out	N10	
9	GPIO5_6	ENET_RST	Reset LAN8720 (low active)	3.3V	In	N11	10K pull down to GND on SOM
10	GPIO5_5	GPIO	GPIO5_5	3.3V	In/Out	N8	
11	GPIO5_4	GPIO	GPIO5_4	3.3V	In/Out	P9	
12	GPIO5_3	GPIO	GPIO5_3	3.3V	In/Out	P10	
13	GPIO5_2	GPIO	GPIO5_2	3.3V	In/Out	P11	
14	GPIO5_1	GPIO	GPIO5_1	3.3V	In/Out	R9	
15	GPIO5_0	GPIO	GPIO5_0	3.3V	In/Out	R10	
16	GND	GND	Power GND	0V	—	—	
17	SAI2_RXD	SAI2	SAI2 data receive	3.3V	In	M14	10K pull down to GND on SOM
18	SAI2_BCLK	SAI2	SAI2 transmit bit clock	3.3V	In/Out	N16	
19	SAI2_TXD	SAI2	SAI2 data transmit	3.3V	Out	N14	
20	SAI2_MCLK	SAI2	SAI2 master clock	3.3V	In/Out	P14	
21	SAI2_SYNC	SAI2	SAI2 transmit frame synchronization	3.3V	In/Out	N15	
22	GPIO1_5	GPIO	GPIO1_5	3.3V	In/Out	P15	10K pull down to GND on SOM
23	GND	GND	Power GND	0V	—	—	
24	USB_OTG2_VBUS	USB2	USB2 VBUS Power In	5V	In	U12	
25	USB_OTG1_VBUS	USB1	USB2 VBUS Power In	5V	In	T12	
26	GND	GND	Power GND	0V	—	—	
27	USB_OTG2_DP	USB2	USB2 data+	3.3V	In/Out	U13	
28	USB_OTG2_DN	USB2	USB2 data-	3.3V	In/Out	T13	
29	GND	GND	Power GND	0V	—	—	

Pin	Label	Function	Description	Voltage	I/O	BGA Pin	Note
30	USB_OTG1_DN	USB1	USB1 data-	3.3V	In/Out	T15	
31	USB_OTG1_DP	USB1	USB1 data+	3.3V	In/Out	U15	
32	GND	GND	Power GND	0V	—	—	
33	CLK1_N	CLK1	No used	3.3V	In/Out	P16	let it floating if no use or please reference toi. MX6UL/i.MX6ULL datasheet
34	CLK1_P	CLK1	No used	3.3V	In/Out	P17	
35	GND	GND	Power GND	0V	—	—	
36	GND	GND	Power GND	0V	—	—	
37	VDD_3V3	POWER	3.3V power supply input	3.3V	In	—	3.3V input
38	VDD_3V3	POWER	3.3V power supply input	3.3V	In	—	3.3V input
39	VDD_BAT	POWER	Power supply for backup region of i.MX6UL/6ULL	3V	In	—	if not use,let it floating
40	GPIO1_00	USB_OTG1_ID	USB ID pin	3.3V	In/Out	K13	Can be used as analog input,refer to i.mx6ul/6ull user manual for detail.
41	ADC1_IN1	ADC	Resistive TSC Y-	3.3V	In/Out	L15	
42	ADC1_IN2	ADC	Resistive TSC Y+	3.3V	In/Out	L14	
43	ADC1_IN3	ADC	Resistive TSC X-	3.3V	In/Out	L17	
44	ADC1_IN4	ADC	Resistive TSC X+	3.3V	In/Out	M16	
45	GPIO1_05	GPIO	GPIO1_05	3.3V	In/Out	M17	
46	MDIO	ENET1& ENET2	MDIO data	3.3V	In/Out	K17	Can only be used for ENET
47	MDC	ENET1& ENET2	MDIO clock	3.3V	In	L16	Can only be used for ENET
48	GPIO1_IO08	LCD_PWM	Backlight for LCD screen	3.3V	Out	N17	Can be used as analog input, refer to i.mx6ul/6ull user manual for detail.
49	GPIO1_IO09	LCD_DISP	Reserved	3.3V	In	M15	
50	GND	GND	Power GND	0V	—	—	
51	UART1_TXD	UART1	UART1 data send	3.3V	Out	K14	Debug UART
52	UART1_RXD	UART1	UART1 data receive	3.3V	In	K16	Debug UART
53	SD1_CD	SD1_CD	SD1 command	3.3V	In	J14	
54	GPIO1_18	GPIO	GPIO1_18	3.3V	In/Out	K15	
55	UART2_TXD	UART2	UART2 data send	3.3V	Out	J17	
56	UART2_RXD	UART2	UART2 data receive	3.3V	In	J16	
57	CAN1_RX	CAN1	CAN bus data receive	3.3V	In	H14	
58	CAN1_TX	CAN1	CAN bus data send	3.3V	Out	J15	
59	GND	GND	Power GND	0V	—	—	
60	UART3_TXD	UART3	UART3 data send	3.3V	Out	H17	
61	UART3_RXD	UART3	UART3 data receive	3.3V	In	H16	
62	UART3_RTS	UART3	UART3 RTS signal	3.3V	Out	G14	
63	UART3_CTS	UART3	UART3 CTS signal	3.3V	In	H15	
64	UART4_TXD	UART4	UART4 data send	3.3V	Out	G17	
65	UART4_RXD	UART4	UART4 data receive	3.3V	In	G16	
66	I2C2_SCL	I2C2	I2C2 clock	3.3V	Out	F17	
67	I2C2_SDA	I2C2	I2C2 data	3.3V	In/Out	G13	
68	GND	GND	Power GND	0V	—	—	

Pin	Label	Function	Description	Voltage	I/O	BGA Pin	Note
69	ETH1_LED1	ETH1	ENET1 Link Activity LED	3.3V	Out	—	Built in Ethernet PHY chip (LAN8720A)
70	ETH1_LED2	ETH1	As a indicator of transmission data	3.3V	Out	—	Built in Ethernet PHY chip (LAN8720A)
71	GND	GND	Power GND	0V	—	—	
72	ETH1_TXN	ETH1	ENET1 data transmit-	A	Out	—	Built in Ethernet PHY chip (LAN8720A)
73	ETH1_TXP	ETH1	ENET1 data transmit+	A	Out	—	Built in Ethernet PHY chip (LAN8720A)
74	GND	GND	Power GND	0V	—	—	
75	ETH1_RXN	ETH1	ENET1 data receive-	A	In	—	Built in Ethernet PHY chip (LAN8720A)
76	ETH1_RXP	ETH1	ENET1 data receive+	A	In	—	Built in Ethernet PHY chip (LAN8720A)
77	GND	GND	Power GND	0V	—	—	
78	ENET2_TX_CLK	ENET2	ENET2 RMII reference clock	3.3V	Out	D17	
79	ENET2_RXD0	ENET2	ENET2 RMII receive data 0	3.3V	In	C17	
80	ENET2_CRS_DV	ENET2	ENET2 RMII receive enable	3.3V	Out	B17	
81	ENET2_RXER	ENET2	ENET2 RMII receive error	3.3V	Out	D16	
82	ENET2_RXD1	ENET2	ENET2 RMII receive data 1	3.3V	In	C16	
83	ENET2_TXEN	ENET2	ENET2 RMII transmit enable	3.3V	Out	B15	
84	ENET2_TXD1	ENET2	ENET2 RMII transmit data 1	3.3V	Out	A16	
85	ENET2_TXD0	ENET2	ENET2 RMII transmit data 0	3.3V	Out	A15	
86	GND	GND	Power GND	0V	—	—	
87	LCD_DATA0	LCD	LCD Data 0	3.3V	Out	B9	47K pull down to GND on SOM
88	LCD_DATA1	LCD	LCD Data 1	3.3V	Out	A9	47K pull down to GND on SOM
89	LCD_DATA2	LCD	LCD Data 2	3.3V	Out	E10	47K pull down to GND on SOM
90	LCD_DATA3	LCD	LCD Data 3	3.3V	Out	D10	47K pull down to GND on SOM
91	LCD_DATA4	LCD	LCD Data 4	3.3V	Out	C10	10K pull up to 3.3v on SOM
92	LCD_DATA5	LCD	LCD Data 5	3.3V	Out	B10	NAND:10K pull down to GND on SOM EMMC: 10K pull up to VCC on SOM
93	LCD_DATA6	LCD	LCD Data 6	3.3V	Out	A10	10K pull up to 3.3v on SOM

Pin	Label	Function	Description	Voltage	I/O	BGA Pin	Note
94	LCD_DATA7	LCD	LCD Data 7	3.3V	Out	D11	NAND: 10K pull up to VCC on SOM EMMC:10K pull down to GND on SOM
95	GND	GND	Power GND	0V	—	—	
96	LCD_DATA8	LCD	LCD Data 8	3.3V	Out	B11	10K pull down to GND on SOM
97	LCD_DATA9	LCD	LCD Data 9	3.3V	Out	A11	10K pull down to GND on SOM
98	LCD_DATA10	LCD	LCD Data 10	3.3V	Out	E12	10K pull down to GND on SOM
99	LCD_DATA11	LCD	LCD Data 11	3.3V	Out	D12	NAND:10K pull down to GND on SOM EMMC: 10K pull up to VCC on SOM
100	LCD_DATA12	LCD	LCD Data 12	3.3V	Out	C12	47K pull down to GND on SOM
101	LCD_DATA13	LCD	LCD Data 13	3.3V	Out	B12	47K pull down to GND on SOM
102	LCD_DATA14	LCD	LCD Data 14	3.3V	Out	A12	47K pull down to GND on SOM
103	LCD_DATA15	LCD	LCD Data 15	3.3V	Out	D13	47K pull down to GND on SOM
104	GND	GND	—	0V	—	—	
105	UART7_TXD	UART7	UART7 data send	3.3V	Out	C13	47K pull down to GND on SOM
106	UART7_RXD	UART7	UART7 data receive	3.3V	Out	B13	47K pull down to GND on SOM
107	SD2_CMD	uSDHC2	uSDHC2 CMD	3.3V	Out	A13	47K pull down to GND on SOM
108	SD2_CLK	uSDHC2	uSDHC2 clock	3.3V	Out	D14	47K pull down to GND on SOM
109	SD2_DATA0	uSDHC2	uSDHC2 Data 0	3.3V	Out	C14	47K pull down to GND on SOM
110	SD2_DATA1	uSDHC2	uSDHC2 Data 1	3.3V	Out	B14	47K pull down to GND on SOM
111	SD2_DATA2	uSDHC2	uSDHC2 Data 2	3.3V	Out	A14	47K pull down to GND on SOM
112	SD2_DATA3	uSDHC2	uSDHC2 Data 3	3.3V	Out	B16	47K pull down to GND on SOM
113	GND	GND	Power GND	0V	—	—	
114	LCD_RESET	LCD	Reset LCDC	3.3V	In	E9	
115	LCD_VSYNC	LCD	LCD vertical sync	3.3V	Out	C9	
116	LCD_HSYNC	LCD	LCD horizontal sync	3.3V	Out	D9	
117	LCD_DE	LCD	LCD data enable	3.3V	Out	B8	
118	LCD_PCLK	LCD	LCD pixel clock	3.3V	Out	A8	
119	GPIO4_16	GPIO	GPIO4_16	3.3V	In/Out	E6	
120	GPIO4_14	GPIO	GPIO4_14	3.3V	In/Out	B5	
121	GND	GND	Power GND	0V	—	—	
122	SD1_DATA3	uSDHC1	uSDHC1 data 3	3.3V	In/Out	A2	
123	SD1_DATA2	uSDHC1	uSDHC1 data 2	3.3V	In/Out	B1	
124	SD1_DATA1	uSDHC1	uSDHC1 data 1	3.3V	In/Out	B2	

Pin	Label	Function	Description	Voltage	I/O	BGA Pin	Note
125	SD1_DATA0	uSDHC1	uSDHC1 data 0	3.3V	In/Out	B3	
126	SD1_CMD	uSDHC1	uSDHC1 command	3.3V	Out	C2	
127	SD1_CLK	uSDHC1	uSDHC1 clock	3.3V	Out	C1	
128	GND	GND	Power GND	0V	—	—	
129	CSI_DATA7	CSI	CSI data 7	3.3V	In	D1	
130	CSI_DATA6	CSI	CSI data 6	3.3V	In	D2	
131	CSI_DATA5	CSI	CSI data 5	3.3V	In	D3	
132	CSI_DATA4	CSI	CSI data 4	3.3V	In	D4	
133	CSI_DATA3	CSI	CSI data 3	3.3V	In	E1	
134	CSI_DATA2	CSI	CSI data 2	3.3V	In	E2	
135	CSI_DATA1	CSI	CSI data 1	3.3V	In	E3	
136	CSI_DATA0	CSI	CSI data 0	3.3V	In	E4	
137	CSI_VSYNC	CSI	CSI vertical sync	3.3V	In	F2	
138	CSI_HSYNC	CSI	CSI horizontal sync	3.3V	In	F3	
139	CSI_PIXCLK	CSI	CSI pixel clock	3.3V	In	E5	
140	CSI_MCLK	CSI	CSI master clock	3.3V	Out	F5	

Figure 3-1 MYC-Y6ULX-V2 Pin List

4. Electrical Characteristics

4.1. Primary System Power

The primary power supply for the MYC-Y6ULX-V2 core module is VDD_3V3, corresponding to the connector's 37 and 38 pins. For proper operation, the carrier board must provide 3.3V±5% voltage and ensure that the output capacity of the power supply circuit meets the power consumption of the core module. Section 4.4 lists the power consumption and current of the core module under various conditions, ensure the appropriate amount of margin has been reserved for the design of the power supply circuit.

4.2. Backup Power

VBAT is a backup battery interface that corresponds to the connector's 39 pin and can be powered by an external battery. Its function is to remain the CPU internal RTC function by powering VBAT through the external battery when the main power is down. The VBAT has a voltage range of 2.6-3.3V.
However, because the RTCS inside the core board consume more power, you are advised to use an external real-time clock module (RX-8025T/UC).

4.3. Power Domain

External voltages need to be supplied from carrier board, while the internally generated voltages are provided by the core module itself.

Name	Description	Recommended Voltage
VDD_3V3:	Primary power supply of the core module	3.3V
USB_OTG1_VBUS	USB1 Bus voltage,must be supplied with 5Vif USB1 is used	5V
USB_OTG2_VBUS	USB1 Bus voltage,must be supplied with 5Vif USB1 is used	5V
VDD_BAT	Backup power supply of the core module	3.3V

Table 4-1 External voltages

Name	Description	Recommended Voltage
VDD_1V2	i.MX6UL/ULL core and soc voltage	1.2V
VDD_1V35	Voltage of i.MX6UL/ULL DDR interface	1.35v

Table 4-2 Internally generated voltages

4.4. Power Consumption

Conditions	Primary Voltage	Average Current	Peak Current	Power Consumption
During boot	3.3V	200mA	280mA	660mW
Full-load 阶段	3.3V	285mA	360mA	940.5mW

Table 4-3 Power Consumption

4.5. GPIO DC Parameters

Parameter	Symbol	Min	Typical	Max	Units
High-lever DC input voltage	VIH	2.3	3.3	3.6	V
Low-lever DC input voltage	VIL	-0.3	—	1.0	V
High-lever DC output voltage	VOH	2.64	3.3	—	V
Low-lever DC output voltage	VOL	—	—	0.66	V

Table 4-3 GPIO DC Parameters

5. System Start-up Configuration

5.1. Boot Mode

After power-on reset, i.MX.6UL/6ULL chip first runs the built-in program in ROM, which detects the configuration of BOOT MODE pin to determine the boot mode, and then detects the configuration of CFGx[7:0] pin to select and configure the boot device.

For more details on the boot configuration, go to the NXP website i.MX.6UL/6ULL product page and download Reference Manual:

https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ull-single-core-processor-with-arm-cortex-a7-core:i.MX6ULL?_TAB_=_Documentation_Tab.

Boot Mode (1:0)	Boot Mode	Description
00	Boot From Fuses	Read the start-up information from internal fuses, which is recommended by NXP for mass production.
01	Serial Downloader	Support for downloading program from serial port to flash.It should be noted that in this mode, UART1 and UART2 have a higher priority than the USB1_OTG port. If there is data being checked in UART1or UART2, the downloader can`t load the programme with USB1 port.
10	Internal Boot	Read the boot configuration from the boot pin. This mode is recommended for development phase, and many users alse use this mode directly for mass production
11	Reserved	

Table 5-1 Boot Mode

The BOOT_MODE0 and BOOT_MODE1 pins have been pulled up through 10K resistors on the core module, if it is necessary to set these two pins to low voltage level, please use 1K resistors to pull down to the ground.

5.2. Boot Device

Typically, setting the cpu to the internal boot mode during products development phase is recommended. Then the CPU will read the voltage level of LCD_DATA0-DATA23 pins during cpu reset to determine the boot device. The LCD_DATA0-DATA23 pins have been configured rightly on the MYC-Y6ULX-V2 core module, only the followling two pins should been configured in the baseboard design.

Depending on the selected core module storage device, the pins needed to be configured are also different, please refer to **Table5-2** and **Table 5-3** for details.

Device / Pin	eMMC(SDIO2)	SD Card(SDIO1)
LCD_DATA5	Floating	Pull down to gnd with 1K resistor
LCD_DATA11	Floating	Pull down to gnd with 1K resistor

Table 5-2 Boot Configuration of eMMC Version Core Voard

Device / Pin	NAND Flash	SD Card(SDIO1)
LCD_DATA6	Pull down to gnd with 1K resistor	Floating
LCD_DATA7	Floating	Pull down to gnd with 1K resistor

Table 5-3 Boot Configuration of Nandflash Version core module

5.3. Reset

The MYC-Y6ULX-V2 core module provides 2 dedicated reset pins, POR reset (pin 2) and ONOFF reset (pin 1), which have different functions and are recommended both used for different purposes.

POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.

Table 5-4 Descriptions of Reset Pins

6. Interfaces

MYC-Y6ULX-V2 core board leads all the IO pins of the i.MX6UL/i.MX6ULL chip. Except the pins occupied by the ENET1 and the Nand Flash/eMMC, the other pins can be allocated by the user freely based on the functions supported by the chip. Check section 6.12 for IO pins that can not be redistributed.

Users are recommended to allocate pins using NXP `s pinmux tool **Pins Tool for i.MX Processors ，** which will simplify the pin multiplex work. Open the software, select the MPU model, select the desired resources such as serial port you want, the software will automatically locate relevant pins and ensure these pins does not conflict. Visit NXP official website for instructions on the software and download:

https://www.nxp.com/design/designs/pins-tool-for-i-mx-application-processors:PINS-TOOL-IMX

6.1. uSDHC

uSDHC (Ultra Secured Digital Host Controller) is NXP's unique secure digital host interface that provides secure communication between the CPU and external SD/SDIO//MMC cards. The MYC-Y6ULX-V2 core module is equipped with 2 uSDHC interfaces, uSDHC1 and uSDHC2, which can be used as an SD card startup or SDIO communication. uSDHC1 can be used on all MYC-Y6ULX-V2 core module models,but uSDHC2 is only available on the core module of nandflash version, and on the core module of eMMC version, uSDHC2 can`t be used.

6.1.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
53	SD1_CD	SD1	SD1 detection signal	3.3V	I	J14	
122	SD1_DATA3	SD1	SD1 data3	3.3V	I/O	A2	
123	SD1_DATA2	SD1	SD1 data2	3.3V	I/O	B1	
124	SD1_DATA1	SD1	SD1 data1	3.3V	I/O	B2	
125	SD1_DATA0	SD1	SD1 data0	3.3V	I/O	B3	
126	SD1_CMD	SD1	SD1 cmd signal	3.3V	O	C2	
127	SD1_CLK	SD1	SD1clock	3.3V	O	C1	

Table 6-1 Pin Description of uSDHC1

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
107	SD2_CMD	SD2	SD2 cmd signal	3.3V	O	A13	47K pull down on SOM
108	SD2_CLK	SD2	SD2 clock	3.3V	O	D14	47K pull down on SOM
109	SD2_D0	SD2	SD2 data0	3.3V	O	C14	47K pull down on SOM
110	SD2_D1	SD2	SD2 data1	3.3V	O	B14	47K pull down on SOM
111	SD2_D2	SD2	SD2 data2	3.3V	O	A14	47K pull down on SOM
112	SD2_D3	SD2	SD2 data3	3.3V	O	B16	47K pull down on SOM

Table 6-2 Pin Description of uSDHC2

6.2. UART

The i.MX6UL/ULL series processors have up to 8 UART interfaces. Due to the pins multiplexing, the core module uses only 5 UART interfaces by default, of which UART3 has a flow control (RTS and CTS signal) function by default.

6.2.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
51	UART1_TXD	UART1	UART1 data transmit	3.3V	O	K14	
52	UART1_RXD	UART1	UART1 data receive	3.3V	I	K16	
55	UART2_TXD	UART2	UART2 data transmit	3.3V	O	J17	
56	UART2_RXD	UART2	UART2 data receive	3.3V	I	J16	
60	UART3_TXD	UART3	UART3 data transmit	3.3V	O	H17	
61	UART3_RXD	UART3	UART3 data receive	3.3V	I	H16	
62	UART3_RTS	UART3	UART3 RTS signal	3.3V	O	G14	
63	UART3_CTS	UART3	UART3 CTS signal	3.3V	I	H15	
64	UART4_TXD	UART4	UART4 data transmit	3.3V	O	G17	
65	UART4_RXD	UART4	UART4 data receive	3.3V	I	G16	
105	UART7_TXD	UART7	UART5 data transmit	3.3V	O	C13	
106	UART7_RXD	UART7	UART7 data receive	3.3V	I	B13	

Table 6-3 Pin Description of UART

6.3. USB

MYC-Y6ULX-V2 core module offers two high-speed USB 2.0 to support OTG functionality. If the user wants to use the OTG function of USB, the USB interface is recommended to use the Micro-USB interface, because Micro-USB is a 5-wire interface with a USB_ID signal, which can be used to identify HOST and DEVICE, so as to achieve OTG function. If the user only uses the USB as a HOST, either 4-wire or 5-wire USB interface can be selected.

6.3.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
24	USB_OTG2_VBUS	USB2	Power supply for USB2 Bus	5V	I	U12	
25	USB_OTG1_VBUS	USB1	Power supply for USB1 Bus	5V	I	T12	
26	GND	GND	GND	0V	—	—	
27	USB_OTG2_DP	USB2	USB2 Bus data+	3.3V	I/O	U13	
28	USB_OTG2_DN	USB2	USB2 Bus data-	3.3V	I/O	T13	
29	GND	GND	GND	0V	—	—	
30	USB_OTG1_DN	USB1	USB1 Bus data-	3.3V	I/O	T15	
31	USB_OTG1_DP	USB1	USB1 Bus data+	3.3V	I/O	U15	
32	GND	GND	GND	0V	—	—	

Table 6-4 Pin Description of USB

6.4. Ethernet

MYC-Y6ULX-V2 core module has two 10/100 ethernet controller that support the IEEE 1588 protocol. The first ethernet controller Eth1 on the MYC-Y6UL core module has placed ethernet PHY chip, can be used directly with external network transformer. Another ethernet controller Eth2, offer the RMII signals as a mac, the user needs to add their own PHY chip on baseboard.

6.4.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
69	ETH1_LED1	ETH1	ETH1 Link activity LED	3.3V	O	—	Built in Ethernet PHY chip(LAN8720A)
70	ETH1_LED2	ETH1	ETH1 Link speed LED	3.3V	O	—	Built in Ethernet PHY chip(LAN8720A)
72	ETH1_TXN	ETH1	ETH1 data transmit-	—	O	—	Built in Ethernet PHY chip(LAN8720A)
73	ETH1_TXP	ETH1	ETH1 data transmit+	—	O	—	Built in Ethernet PHY chip(LAN8720A)
75	ETH1_RXN	ETH1	ETH1 data receive-	—	I	—	Built in Ethernet PHY chip(LAN8720A)
76	ETH1_RXP	ETH1	ETH1 data receive+	—	I	—	Built in Ethernet PHY chip(LAN8720A)

Table 6-5 Pin Description of Ethernet1

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
46	MDIO	ETH1& ETH2	ETH management data	3.3V	I/O	K17	
47	MDC	ETH1& ETH2	ETH management clock	3.3V	I	L16	
78	ENET2_TX_CLK	ETH2	RMII reference clock	3.3V	O	D17	
79	ENET2_RXD0	ETH2	RMII data receive 0	3.3V	I	C17	
80	ENET2_CRS_DV	ETH2	RMII receive enable	3.3V	O	B17	
81	ENET2_RXER	ETH2	RMII receive error	3.3V	O	D16	
82	ENET2_RXD1	ETH2	RMII data receive 1	3.3V	I	C16	
83	ENET2_TXEN	ETH2	RMII transmit enable	3.3V	O	B15	
84	ENET2_TXD1	ETH2	RMII data transmit 1	3.3V	O	A16	
85	ENET2_TXD0	ETH2	RMII data transmit 0	3.3V	O	A15	

Table 6-6 Pin Description of Ethernet2

6.5. CAN

The MYC-Y6ULX-V2 core module offer two CAN controllers, which support the CAN protocol specification of 2.0b version.The built-in FLEXCAN module supports data frames in standard or extended formats, as well as 64 Message Buffers. Due to pin multiplexing, only CAN1 is used by default. Users should place CAN transceiver chip on the carrier board to achieve CAN communication.

6.5.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
57	CAN1_RX	CAN1	CAN Bus receive	3.3V	I	H14	
58	CAN1_TX	CAN1	CAN Bus transmit	3.3V	O	J15	

Table 6-7 Pin Description of CAN

6.6. I2C

The MYC-Y6ULX-V2 core module supports up to 4 I2C buses, of which only one I2C bus(I2C2) is used by default due to pinmux .If you need to use more I2C interfaces, please query instructions for pinmux in the official i. MX6UL/6ULL manual and modify the pin configuration in the driver.

Links to official manuals:

https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?&tab=Documentation_Tab&linkline=Data-Sheet

6.6.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
66	I2C2_SCL	I2C2	I2C2 clock	3.3V	O	F17	
67	I2C2_SDA	I2C2	I2C2 data	3.3V	I/O	G13	

Table 6-8 Pin Description of I2C

6.7. SPI

The MYC-Y6ULX-V2 core module supports up to 4 SPI controllers and supports master/from mode. Due to pinmux, the SPI signals on the core module are not used by default . IF you want to use the SPI function, please query the instructions of pinmux in the official i.MX6UL/6ULL manual and modify the pin configurations in the driver.

Links to official manuals:https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?&tab=Documentation_Tab&linkline=Data-Sheet

Table 6-9 illustrates the pinmux relationship of the SPI 1 interface.

6.7.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
131	CSI_DATA5	CSI	SPI1 chip select	3.3V	O	D3	
132	CSI_DATA4	CSI	SPI1 clock	3.3V	O	D4	
130	CSI_DATA6	CSI	SPI1 MOSI	3.3V	O	D2	
129	CSI_DATA7	CSI	SPI1 MISO	3.3V	I	D1	

Table 6-9 Pin Description of SPI

6.8. CSI

CSI interface supports 8-bit or 24-bit YCbCr, YUV, RGB format; 8-bit, 10-bit, or 16-bit Bayer format with a maximum pixel clock of 238 MHz. Due to pinmux, the CSI interface of the MYC-Y6ULX-V2 core module is configured to 8-bit data width by default,therefore the carrier board design is recommended to use 8-bit parallel camera interface.You can obtain the camera module MY-CAM011B from Myirtech Electronics, visit http://www.myir-tech.com/product/my_cam011b.htm for more information.

Figure 6-1 CSI Interface

6.8.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
129	CSI_DATA7	CSI	CSI data 7	3.3V	I	D1	
130	CSI_DATA6	CSI	CSI data 6	3.3V	I	D2	
131	CSI_DATA5	CSI	CSI data 5	3.3V	I	D3	
132	CSI_DATA4	CSI	CSI data 4	3.3V	I	D4	
133	CSI_DATA3	CSI	CSI data 3	3.3V	I	E1	
134	CSI_DATA2	CSI	CSI data 2	3.3V	I	E2	
135	CSI_DATA1	CSI	CSI data 1	3.3V	I	E3	
136	CSI_DATA0	CSI	CSI data 0	3.3V	I	E4	
137	CSI_VSYNC	CSI	CSI vertical sync	3.3V	I	F2	
138	CSI_HSYNC	CSI	CSI horizontal sync	3.3V	I	F3	
139	CSI_PIXCLK	CSI	CSI pixel clock	3.3V	I	E5	
140	CSI_MCLK	CSI	CSI master clock	3.3V	O	F5	

Table 6-10 Pin Description of SPI

6.9. LCD

The LCD interface of the MYC-Y6ULX-V2 core module supports 8/16/18/24bit data formats, allowing customers to choose the right data bit width according to their needs, the default configuration of the driver is 16Bit RGB data format, which can be connected externally to a 16 or 24bit TFT screen. The driver supports 480x272 resolution (4.3 inch screen) and 800x480 resolution (7 inch screen) by default.

Myirtech offer various models of TFT touch screen: MY-TFT043RV2, MY-TFT070RV2 or MY-TFT070CV2. you can visit http://www.myir-tech.com/product for more details.

6.9.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
87	LCD_DATA0	LCD	LCD data 0	3.3V	O	B9	
88	LCD_DATA1	LCD	LCD data 1	3.3V	O	A9	
89	LCD_DATA2	LCD	LCD data 2	3.3V	O	E10	
90	LCD_DATA3	LCD	LCD data 3	3.3V	O	D10	
91	LCD_DATA4	LCD	LCD data 4	3.3V	O	C10	
92	LCD_DATA5	LCD	LCD data 5	3.3V	O	B10	
93	LCD_DATA6	LCD	LCD data 6	3.3V	O	A10	
94	LCD_DATA7	LCD	LCD data 7	3.3V	O	D11	
96	LCD_DATA8	LCD	LCD data 8	3.3V	O	B11	
97	LCD_DATA9	LCD	LCD data 9	3.3V	O	A11	
98	LCD_DATA10	LCD	LCD data 10	3.3V	O	E12	
99	LCD_DATA11	LCD	LCD data 11	3.3V	O	D12	
100	LCD_DATA12	LCD	LCD data 12	3.3V	O	C12	
101	LCD_DATA13	LCD	LCD data 13	3.3V	O	B12	
102	LCD_DATA14	LCD	LCD data 14	3.3V	O	A12	
103	LCD_DATA15	LCD	LCD data 15	3.3V	O	D13	
105	LCD_DATA16	UART7_TXD	LCD data 16	3.3V	O	C13	
106	LCD_DATA17	UART7_RXD	LCD data 17	3.3V	O	B13	
107	LCD_DATA18	SD2_CMD	LCD data 18	3.3V	O	A13	
108	LCD_DATA19	SD2_CLK	LCD data 19	3.3V	O	D14	
109	LCD_DATA20	SD2_D0	LCD data 20	3.3V	O	C14	
110	LCD_DATA21	SD2_D1	LCD data 21	3.3V	O	B14	
111	LCD_DATA22	SD2_D2	LCD data 22	3.3V	O	A14	

112	LCD_DATA23	SD2_D3	LCD data 23	3.3V	O	B16	
114	LCD_RESET	LCD	LCD screen reset	3.3V	O	E9	
115	LCD_VSYNC	LCD	LCD vertical sync	3.3V	O	C9	
116	LCD_HSYNC	LCD	LCD horizontal sync	3.3V	O	D9	
117	LCD_DE	LCD	LCD data output enable	3.3V	O	B8	
118	LCD_PCLK	LCD	LCD pixel clock	3.3V	O	A8	
48	GPIO1_IO08	LCD_PWM	LCD brightness control	3.3V	O	N17	

Table 6-11 Pin Description of LCD

6.10. AUDIO

The MYC-Y6ULX-V2 core module provides 3-channel synchronous audio (SAI) interface, supporting all kinds of full-duplex, serial communication audio interfaces with frame synchronization function, such as I2S,AC97,TDM,CODEC and other common audio interfaces.

To use it, you need to connect the interface to an external audio codec chip, and then an external headset and microphone.

6.10.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
17	SAI2_RXD	SAI2	I2S data receive	3.3V	I	M14	
18	SAI2_BCLK	SAI2	I2S transmit bit clock	3.3V	O	N16	
19	SAI2_TXD	SAI2	I2S data transmit	3.3V	O	N14	
20	SAI2_MCLK	SAI2	I2S master clock	3.3V	O	P14	
21	SAI2_SYNC	SAI2	I2S transmit frame sync	3.3V	O	N15	

Table 6-12 Pin Description of SAI2

6.11. GPIO

Due to the pin multiplexing the GPIO pins of MYC-Y6ULX-V2 core module are mostly used as specific functional interfaces. Table 6-13 lists the pins that are used as GPIO by default. Using these pins as GPIO will not reduce the number of other main interfaces.

You can configure GPIO flexibly according to the specific requirements of your products. If you want to use more GPIO, please refer to the official 6UL/6ULL manual for detailed description of pinmux and use **Pins Tool for i.MX Processors** to allocate pin resources.

Link to official manual: https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?&tab=Documentation_Tab&linkline=Data-Sheet

6.11.1. Pin Description

Package Pin	Name	Default Function	Description	Voltage	I/O	CPU Pin	Comments
7	GPIO5_8	GPIO	GPIO5_8	3.3V	I/O	N9	
8	GPIO5_7	GPIO	GPIO5_7	3.3V	I/O	N10	
10	GPIO5_5	GPIO	GPIO5_5	3.3V	I/O	N8	
11	GPIO5_4	GPIO	GPIO5_4	3.3V	I/O	P9	
12	GPIO5_3	GPIO	GPIO5_3	3.3V	I/O	P10	
13	GPIO5_2	GPIO	GPIO5_2	3.3V	I/O	P11	
14	GPIO5_1	GPIO	GPIO5_1	3.3V	I/O	R9	
15	GPIO5_0	GPIO	GPIO5_0	3.3V	I/O	R10	
22	GPIO1_5	GPIO	GPIO1_5	3.3V	I/O	P15	10K pulled down to GND on SOM
45	GPIO1_05	GPIO	GPIO1_5	3.3V	I/O	M17	
54	GPIO1_18	GPIO	GPIO1_18	3.3V	I/O	K15	
119	GPIO4_16	GPIO	GPIO4_16	3.3V	I/O	E6	
120	GPIO4_14	GPIO	GPIO4_14	3.3V	I/O	B5	

Table 6-13 Pin Description of GPIO

6.12. Pins not suggested to be redistributed

MYC-Y6ULX-V2 core board integrated DDR3, Nand Flash /EMMC and Ethernet PHY chip. The DDR3 pins are special functional resources, while Nand Flash /EMMC and Ethernet will also occupy some IO resources. Users can not redistribute the pins in tables 6-14 and 6-15 to GPIO or other functions, otherwise the main function of the core board will be abnormal, maintain the default configuration of these pins.

Nand Flash Function	EMMC Function	CPU Pins
NAND_ALE	SD2_RST	B4
NAND_CE0		C5
NAND_CLE		A4
NAND_D0	SD2_D0	D7
NAND_D1	SD2_D1	B7
NAND_D2	SD2_D2	A7
NAND_D3	SD2_D3	D6
NAND_D4	SD2_D4	C6
NAND_D5	SD2_D5	B6
NAND_D6	SD2_D6	A6
NAND_D7	SD2_D7	A5
NAND_RE_B	SD2_CLK	D8
NAND_Ready_B		A3
NAND_WE_B	SD2_CMD	C8
NAND_WP_B		D5

Table 6-14 Pins used by Nand Flash /eMMC

Name	Default Function	Description	Voltage	I/O	CPU Pins
MDIO	ETH1& ETH2	ETH management data	3.3V	I/O	K17
MDC	ETH1& ETH2	ETH management clock	3.3V	I	L16
ENET1_TCLK	ETH1	RMII reference clock	3.3V	O	F14
ENET1_RXD0	ETH1	RMII data receive 0	3.3V	I	F16
ENET1_RX_EN	ETH1	RMII receive enable	3.3V	O	E16
ENET1_RXER	ETH1	RMII receive error	3.3V	O	D15
ENET1_RXD1	ETH1	RMII data receive 1	3.3V	I	E17
ENET1_TXEN	ETH1	RMII transmit enable	3.3V	O	F15
ENET1_TXD1	ETH1	RMII data transmit 1	3.3V	O	E14
ENET1_TXD0	ETH1	RMII data transmit 0	3.3V	O	E15

Table 6-15 Pins used by Ethernet1

7. Package Information

7.1. Package Dimensions

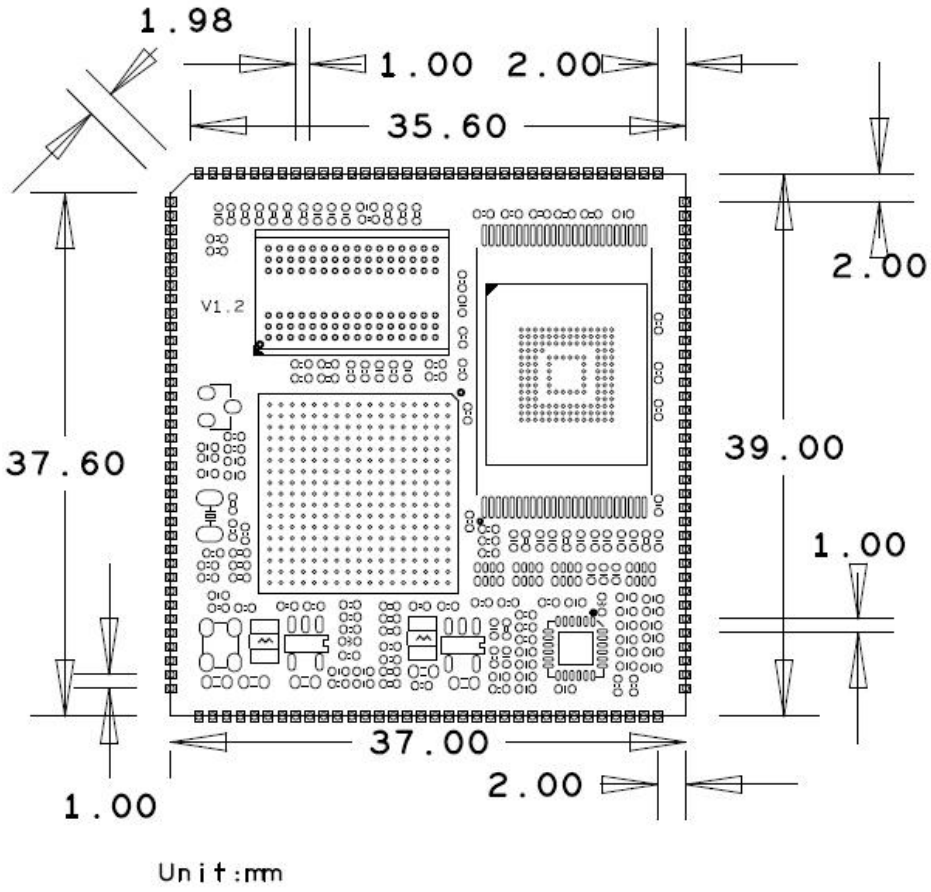

Figure7-1 Top View of MYC-Y6UL

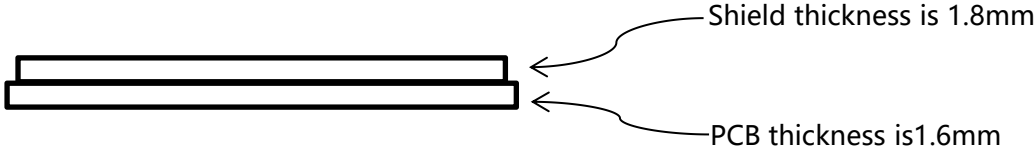

Figure7-2 Thickness of MYC-Y6ULX-V2

7.2. Recommended Land Pattern

Myirtech offers recommended PCB package, please visit http://down.myir-tech.com/MYD-Y6ULX-V2/ to get the source file.

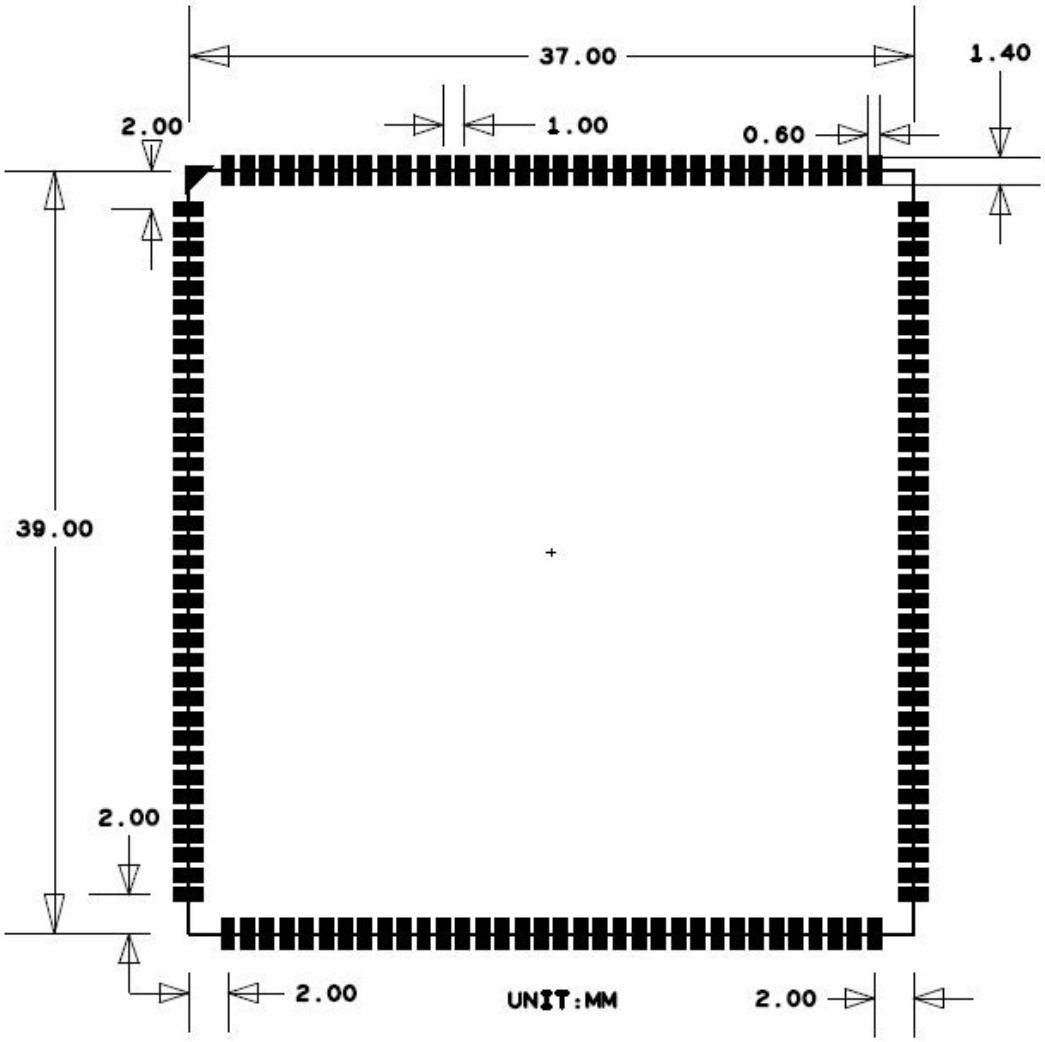

Figure 7-2 MYC-Y6ULX-V2 Land Pattern

7.3. Carrier Board PCB Design

- The thickness of carrier board is no less than 1.6mm to prevent board warpage.
- The spacing between the core module and other elements on carrier board is no less than 3mm.

8. SMT & Storage

8.1. SMT Stencil Requirements

- The recommended thickness of stencil for the core board pad is 0.18 - 0.2mm. Solder preforms need to be considered in the case that the stencil thickness is less than 0.18mm.
- The dimension of the stencil slot is suggested to be contracted by 10% compared to the land pattern.

8.2. Storage Requirements

The module is shipped in the form of vacuum seal, and can be stored in 12 months at most in the following environment:：

- Ambient temperature ≤ 40℃, air humidity ≤ 90%

8.3. PCB Baking

Once the vacuum seal bag is opened, if the ambient temperature is less than 30℃ and the air humidity is less than 10%, product can be reflow soldered directly within 72 hours,otherwise the product should be baked before SMT.

Because the product original packaging material can not withstand high temperature, if necessary, please bake according to the following way to avoid affecting SMT quality:

- Baking with original packaging :The baking temperature is 40~60℃ and the time is 5~7 days.
- Transfer the product to high temperature resistant tray: Baking temperature is 100~120, baking time is more than 48 hours

8.4. Welding Procedure

- In order to avoid repeated heating of the module, it is recommended to weld the module after finishing the first side welding of PCB.
- The time of Preheating Area is recommended 60~120s.
- The temperature of reflow soldering is recommended 235~245℃, no more than 250℃, reflow soldering should be completed in 40~60s.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;

- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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