MYiR 米尔电子
Make Your Idea Real

MYC-YT113i Product Manual

Version：V1.0

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MYIR Electronics Limited

History

Version	Author	Participants	Date	Description
V1.0	Sender		20230804	Official release

Contents

1. Overview

The Allwinner T113-i is an advanced application processor designed for the automotive and industrial control markets. The T113-i integrates a dual-core Cortex™-A7 CPU and a single-core HiFi4 DSP to provide efficient computing power. The T113-i supports H.265, H.264, H.263, MPEG-1/2/4, JPEG and other full-format decoding, and the encoder can encode in JPEG or MJPEG format, up to 1080@60fps. The T113-i processor has rich interfaces RGB*1, LVDS *2, MIPI DSI*1, Parallel CSI*1, DAC*2, ADC*3, I2S/PCM*2, USB*2, SDIO*3, Ethernet*1, TWI*4, UART*6, SPI*2, PWM*8, LRADC*1, GPADC*2, TPADC*4, CAN*2, etc.

Based on Allwinner T113-i chip as the main processor, MYIR Electronics launched a new series of core board: MYC-YT113i. MYC-YT113i has a good software development environment, the kernel supports the open source operating system Linux. The processor is a dual-core Cortex-A7 processor designed for intelligent control and human-machine interface in areas such as automotive and industrial applications. It offers a high cost performance ratio and is suitable for entry-level Linux embedded ARM applications. Meanwhile,can simplify hardware design and shorten research and development period.

Product introduction link: https://www.myir.cn/shows/118/66.html

Download link: https://d.myirtech.com/MYD-YT113/

Figure 1-1 MYC-YT113i Core board

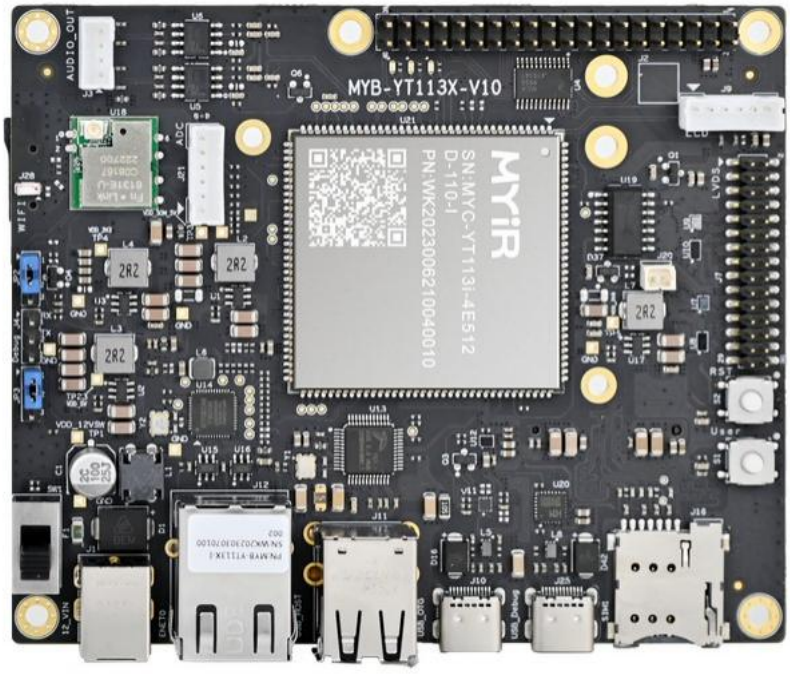

Figure 1-2 MYD-YT113i Kit

2. Product introduction

MYC-YT113i core board adopts high density and high speed circuit board design, and integrates T113-i, eMMC, E2PROM, discrete power supply and other circuits on the 37mm*39mm board card.

MYC-YT113i series core board includes two standard product models: they have some differences in storage configuration, customers can choose the appropriate model according to their needs. For details about the differences between product models, see Section 2.4.

2.1. CPU Introduction

The T113-i integrates a dual-core Cortex™-A7 CPU with a single-core HiFi4 DSP to provide efficient computing power and is designed for intelligent control and human-machine interface in areas such as automotive and industrial applications.

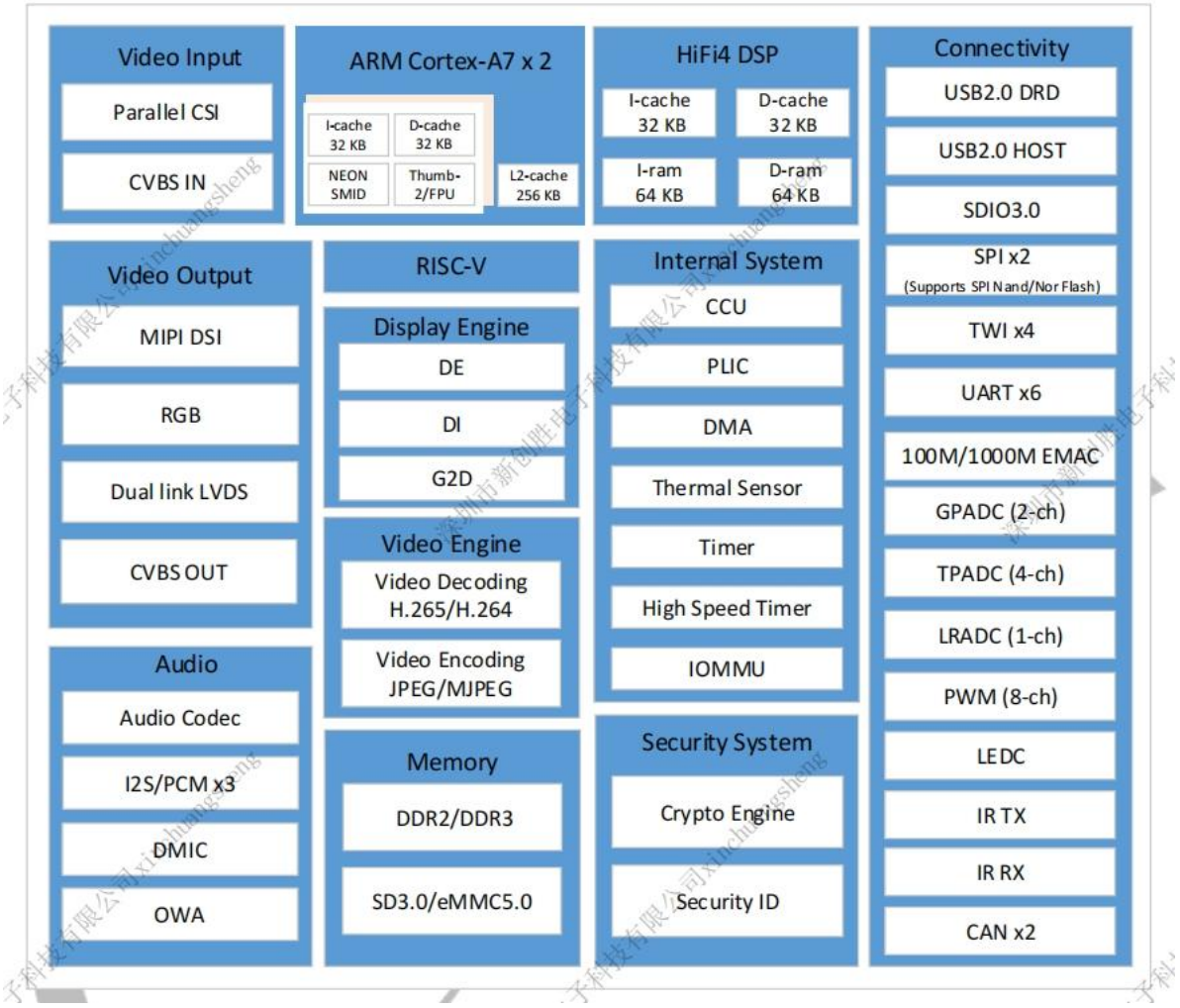

Figure 2-1 T113-i Resource block diagram

Resource	Parameter description
CPU	● Dual-Core ARM Cortex-A7 ● 32 KB L1 1-cache + 32 KB L1 D-cache per core, and 256 KB L2 cache
DSP	● HiFi4 ● 32 KB L1 1-cache and 32 KB L1 D-cache ● 64 KB I-ram and 64 KB D-ram
External storage	**Three SD/MMC host controller (SMHC) interfaces** ● The SMHCO controls the devices that comply with the protocol Secure Digital Memory (SD mem-version3.0) ● The SMHC1 controls the device that complies with the protocol Secure Digital I/0 (SDIO-version 3.0) ● The SMHC2 controls the device that complies with the protocol Multimedia Card (eMMC-version 5.0)
Video engine	**Video Encoder / Decoder support** ● H.265 MP@L4.1 up to 1080p@60fps ● H.264 BP/MP/HP@L4.2 up to 1080p@60fps ● H.263 BP up to 1080p@60fps ● MPEG-4 SP/ASP L5.0 up to 1080p@60fps ● MPEG-2 MP/HL up to 1080p@60fps ● MPEG-1 MP/HL up to 1080p@60fps ● JPEG/MJPEG up to 1080p@60fps ● Supports input picture scaler up/down
Video input	**Parallel CSI** ● Supports 8-bit digital camera interface (RAW8/YUV422/YUV420) ● Supports BT656,BT601 interface (YUV422) ● Supports ITU-R BT.656 time-multiplexed format up to 2*1080p@30fps in DDR sample mode ● Maximum pixel clock of 148.5 MHz ● Supports de-interlacing for interlace video input ● Supports conversion from YUV422 to YUV420, YUV422 to YUV400,YUV420 to YUV400 ● Supports horizontal and vertical flip **CVBS IN** ● 2-channel CVBS input and 1-channel CVBS decoder ● Supports NTSC and PAL format ● Supports YUV422/YUV420 format ● With 1 channel 3D comb filter

	● Detection for signal locked and 625 lines ● Programmable brightness, contrast, and saturation ● 10-bit video ADCs
Audio	● Two audio digital-to-analog converter (DAC) channels ● One audio output：One stereo headphone output: HPOUTL/R ● Three audio analog-to-digital converter (ADC) channels ● Three audio inputs: - One differential microphone input: MICIN3P3N, or one single-end microphone input: MICIN3 - One stereo LINEIN input: INEINL/R - One stereo FMIN input: FMINL/R
Display output	**RGB and LVDS LCD** ● Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@ 60fps ● Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps ● Supports LVDS interface with dual link, up to 1920 x 1080@60fps ● Supports LVDS interface with single link, up to 1366 x 768@60fps ● Supports i8080 interface, up to 800 x 480@60fps ● Supports BT656 interface for NTSC and PAL ● RGB666 and RGB565 with dither function ● Gamma correction with R/G/B channel independence **MIPI DSI** ● Compliance with MIPI DSI V1.01 ● Supports 4-lane MIPI DSI, up to 1920 x 1200@60fps ● Supports non-burst mode with sync pulse/sync event and burst mode ● Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565 ● Supports continuous and non-continuous lane clock modes ● Supports bidirectional communication of all generic commands in LP through data lane 0 ● Supports low power data transmission ● Supports ULPS and escape modes
Safety Engine	**Crypto Engine (CE)** ● Supports Symmetrical algorithm for encryption and decryption: AES, DES, TDES ● Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC ● Supports Asymmetrical algorithm for signature verification: RSA ● Supports 160-bit hardware PRNG with 175-bit seed

connection	● 2 x USB （USB2.0 OTG+USB2.0 HOST） ● 1 x Gigabit Ethernet Interface – 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces ● 2 x CAN Interface ● 4 x TWI（Two Wire Interface） ● 6 x UART ● 2 x SPI ● 3 x SD/MMC ● 8 x PWM ● 1 x LPADC ● 2 x GPADC ● 4 x TPADC
package	● LFBGA337, package ● 13 mm x 13 mm size

Table 2-1 T113-i resources

Refer to the chip manual for details.

2.2. Core Board Features

Item	features
CPU series	T113
CPU Chip type	T113-i
DDR storage	256M/512M/1024 MDDR3
eMMC	4/8GB eMMC
CPU Processor	Dual-Core A7@1.1GHz
Core board size	37mm x 39mm
interface type	Stamp hole+LGA:140 +50Pin
PCB board specifications	8 layer plate design, gold sinking process production

Table 2-2 Core board features

2.3. Block Diagram

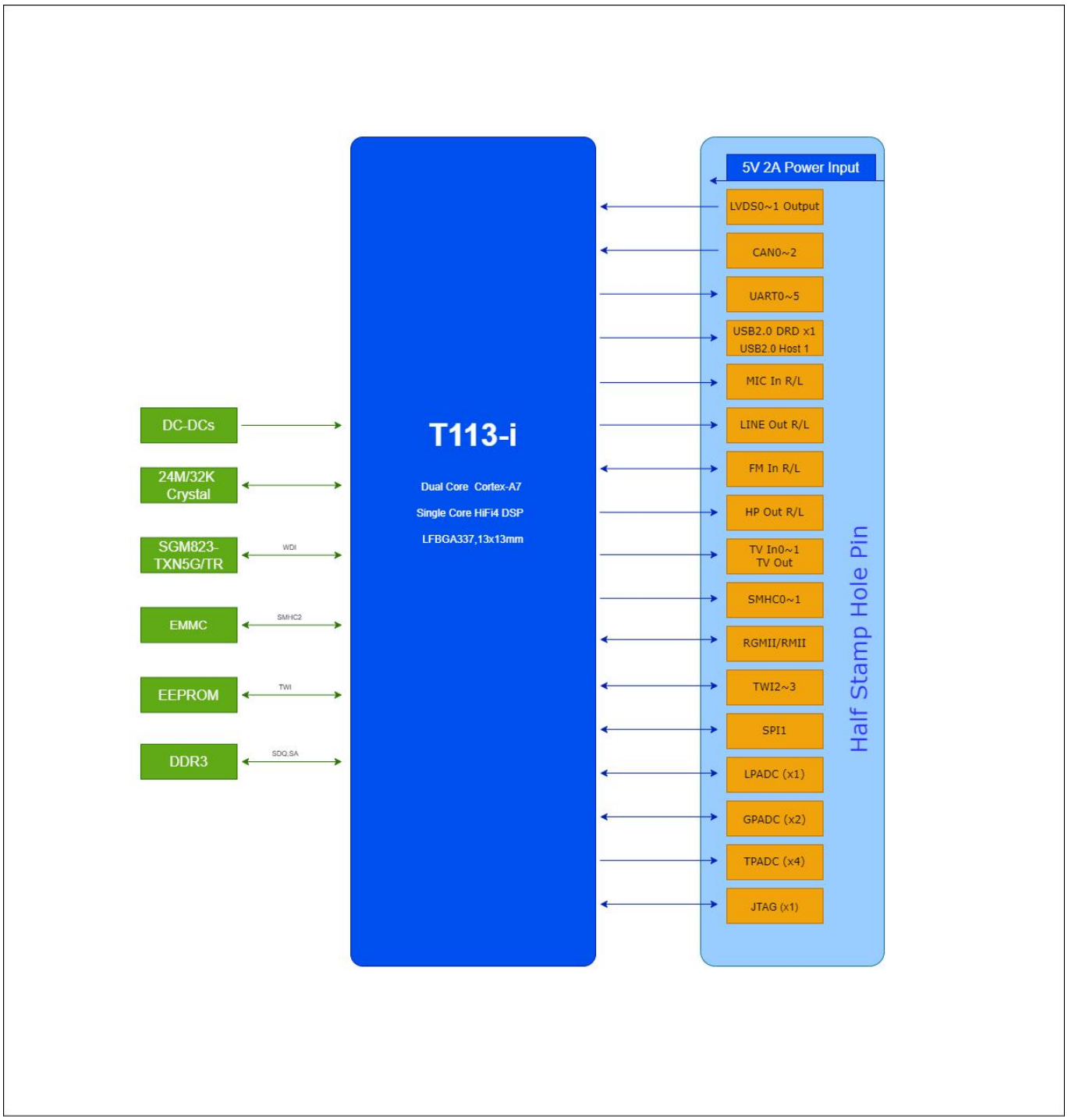

Figure 2-2 Core board block diagram

2.4. Core Board Ordering Information

MYC-YT113i series core board includes 4 standard product models: they have some differences in operating temperature parameters, customers can choose the appropriate model according to their needs. For batch requirements, MYIR provides customized services, you can choose the core board parameters.

Part No. / Item	MYC-YT113i-4E256/512D-110-I	MYC-YT113i-8E512/1D-110-I
CPU	T113-i	T113-i
CPU series	T113	T113
DDR	256/512MB DDR3	512/1024MB DDR3
eMMC	4GB EMMC	8GB EMMC
Core	2 x Cortex-A7	2 x Cortex-A7
Frequency	1.1GHz	1.1GHz
Video output	LVDS0 x 1 LVDS0 + LVDS1 x 1 LCD x1 MIPI DSI x1	LVDS0 x 1 LVDS0 + LVDS1 x 1 LCD x1 MIPI DSI x1
Audio	HPOUTL/R x1 MICIN3N/3P x1 LINEINL/R x1 FMINL/R x1	HPOUTL/R x1 MICIN3N/3P x1 LINEINL/R x1 FMINL/R x1
Parallel CSI	1	1
uSDHC	2	2
USB	USB2.0 OTG x 1 USB2.0 Host x 1	USB2.0 OTG x 1 USB2.0 Host x 1
Ethernet	RGMII x 1	RGMII x 1
UART	6	6
TWI	4	4
CAN	2	2
SPI	2	2
CVBS in	2	2
CVBS out	1	1
ADC	LRADC x1 GPADC x2 TPADC x4	LRADC x1 GPADC x2 TPADC x4

PWM	8	8
GPIO	88	88
System	Linux 5.4.61	Linux 5.4.61
Power Supply	+5V	+5V
Mechanical size	37mm x 39mm	37mm x 39mm
Operating temperature	-40℃ - +85℃	-40℃ - +85℃
Connector	Stamp Hole (total 190 pins)	Stamp Hole (total 190 pins)
Certification	CE ROHS	CE ROHS

Table 2-3 MYC-YT113i core board ordering information

***Note**: The blue background represents the interface type supported by the core board module; The gray background represents the others. The selection table is the maximum resource extracted from the core board, and there may be a reuse relationship.*

3. Pin Description

3.1. Pin Out

The MYC-YT113i core board is soldered to the bottom plate in the form of an SMD patch and the pins are stamp holes. For the package design of baseboard, refer to the instructions in Section 7.2.

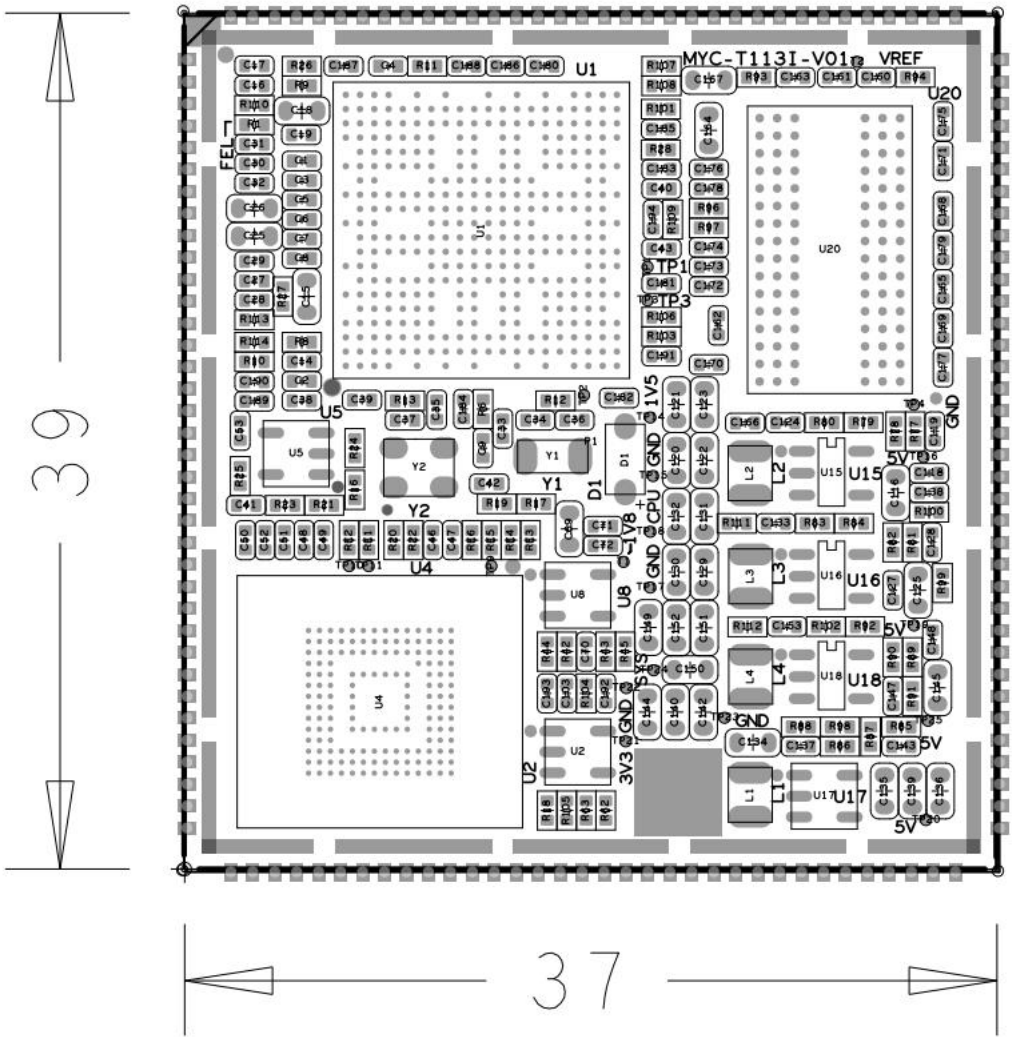

Figure 3-1 Module Pin map (Top side)

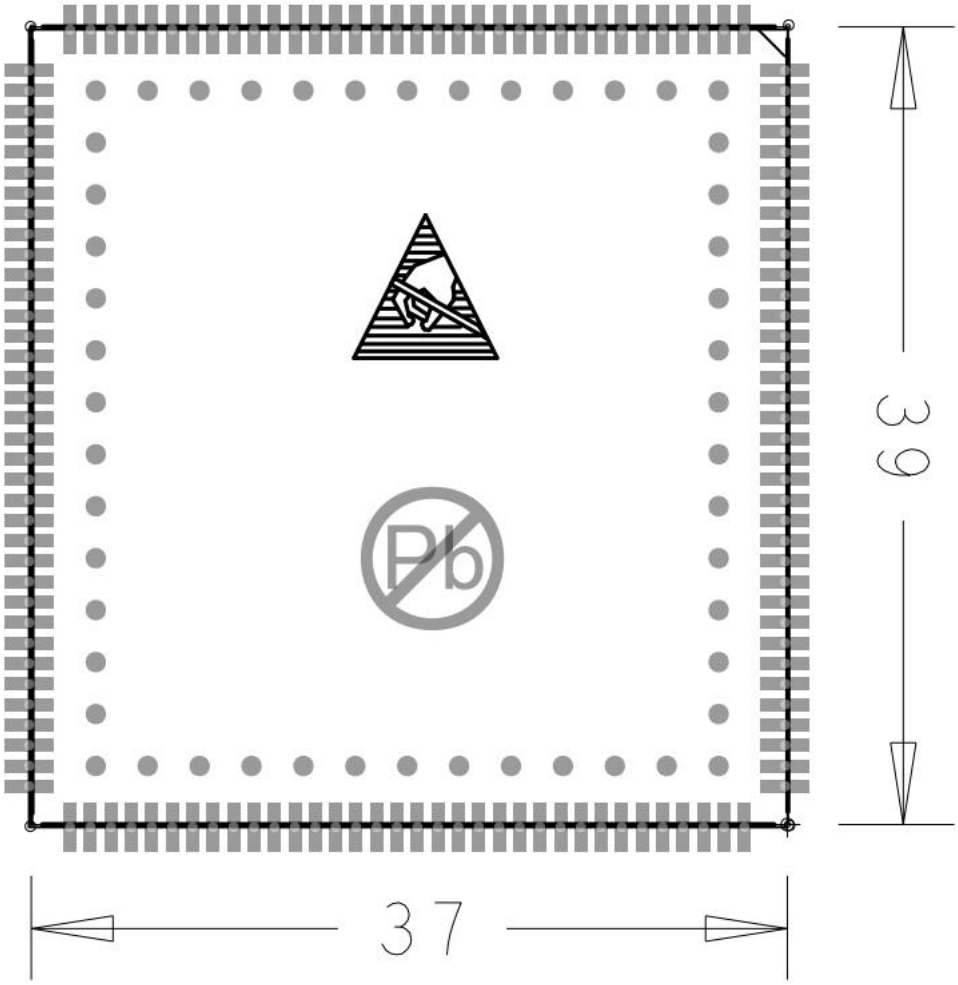

Figure 3-2 Module pin map（Bottom side）

3.2. Pin List

The following table shows the definition of the interface pins of the MYC-YT113i core board. The pin functions of the BSP development kit are configured according to "Default functions" in the following table. If you need to change the default pin functions, please modify the related driver configuration code.

-	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	1	GND	/		0V		
	2	PD14	PD14	GPIO	3.3V	I/O	
	3	PD15	PD15	GPIO	3.3V	I/O	
	4	GND	/		0V		
	5	PD16	PD16	GPIO	3.3V	I/O	
	6	PD17	PD17	GPIO	3.3V	I/O	
	7	GND	/		0V		
	8	PD18	PD18	GPIO	3.3V	I/O	
	9	PD19	PD19	GPIO	3.3V	I/O	
	10	GND	/		0V		
	11	TWI3_SCK	TWI3	TWI3 clock	3.3V	O	Pull Up
	12	TWI3_SDA	TWI3	TWI3 data	3.3V	I/O	Pull Up
	13	TWI1_SDA	CAN1	CAN1 data receive	3.3V	I/O	
	14	GND	/		0V		
	15	CAN0-TX	CAN0	CAN0 data transmit	3.3V	O	
	16	CAN0-RX	CAN0	CAN0 data receive	3.3V	I	
	17	TWI1_SCK	CAN1	CAN0 data transmit	3.3V	O	
	18	GND	/		0V		
	19	MICN	MICN	Microphone Differential -Input 3	3.3V	I	
	20	MICP	MICP	Microphone Differential + Input 3	3.3V	I	
	21	GND	/		0V		
	22	FMINR	FMINR	FMIN Right Input	3.3V	I	
	23	FMINL	FMINL	FMIN Left Input	3.3V	I	
	24	GND	/		0V		
	25	LINEINR	LINEINR	LINEIN Right Single-End Input	3.3V	I	
	26	LINEINL	LINEINL	LINEIN Left Single-End Input	3.3V	I	

27	GND	/		0V		
28	NC	/		/		
29	HPOUTR	HPOUTR	Headphone Right Output	3.3V	O	
30	HPOUTL	HPOUTL	Headphone Light Output	3.3V	O	
31	HPOUTFB	HPOUTFB	Pseudo Differential Headphone Ground Reference	3.3V	I	
32	GND	/		0V		
33	TV-IN0	TV-IN0	TV CVBS Input 0	1.8V	I	
34	TV-IN1	TV-IN1	TV CVBS Input 1	1.8V	I	
35	GND	/		0V		
36	GPADC0	GPADC0	ADC input	1.8V	AI	
37	TP-X1	TP-X1	Touch panel X1 input	1.8V	AI	1nF connects to ground
38	TP-X2	TP-X2	Touch panel X2 input	1.8V	AI	1nF connects to ground
39	TP-Y1	TP-Y1	Touch panel Y1 input	1.8V	AI	1nF connects to ground
40	TP-Y2	TP-Y2	Touch panel Y1 input	1.8V	AI	1nF connects to ground
41	GND	/		0V		
42	TV-OUT	TV-OUT	TV CVBS Output	3.3V	O	
43	GND	/		0V		
44	NC	/		/		
45	CARRIER_PWR_EN	/	External EN Output	3.3V	O	OD
46	PD20	PD20	GPIO	3.3V	I/O	
47	PD21	PD21	GPIO	3.3V	I/O	
48	PD22	PD22	GPIO	3.3V	I/O	
49	NC	/		/		
50	NC	/		/		
51	GND	/		0V		
52	PG11	PG11	GPIO	3.3V	I/O	
53	PG13	PG13	GPIO	3.3V	I/O	
54	SDC0-D0	SDC0-D0	SD0 data 0	3.3V	I/O	
55	SDC0-D1	SDC0-D1	SD0 data 1	3.3V	I/O	

56	SDC0-CMD	SDC0-CMD	SD0 command	3.3V	O	
57	SDC0-D3	SDC0-D3	SD0 data 3	3.3V	I/O	
58	SDC0-D2	SDC0-D2	SD0 data 2	3.3V	I/O	
59	SDC0-DET	SDC0-DET	SD0 card detect	3.3V	O	
60	GND	/		0V		
61	SDC0-CLK	SDC0-CLK	SD0 CLK	3.3V	O	
62	GND	/		0V		
63	VDD_SOM_3V3OUT	/	Power 3.3V out	3.3V	O	3.3V output, 500mA
64	NC	/		/		
65	GND	/		0V		
66	GND	/		0V		
67	GND	/		0V		
68	VDD_5V	/	Power 5V In	5V	I	
69	VDD_5V	/	Power 5V In	5V	I	
70	VDD_5V	/	Power 5V In	5V	I	
71	CLK24M_OUT	CLK24M_OUT	Digital Compensated Crystal Oscillator Clock Fanout	3.3V	O	
72	SYS-RST-OUT	SYS-RST-OUT	System reset	3.3V	I	
73	SYS-RST-IN	SYS-RST-IN	Hardware system reset	3.3V	I	
74	WDI	/	watchdog detection	3.3V	I	
75	GND	/		0V		
76	PG3	RGMII-TXCK	ETH0 Send clock	3.3V	O	
77	GND	/		0V		
78	PG14	RGMII-MDC	ETH0 MDIO clock	3.3V	O	
79	PG15	RGMII-MDIO	ETH0 MDIO data	3.3V	I/O	
80	PG4	RGMII-TXD0	ETH0 Data transmit 0	3.3V	O	
81	PG5	RGMII-TXD1	ETH0 Data transmit 1	3.3V	O	
82	PG12	RGMII-TXCTL	ETH0 Data transmit control bit	3.3V	O	
83	PG7	RGMII-TXD3	ETH0 Data transmit 3	3.3V	O	
84	PG6	RGMII-TXD2	ETH0 Data transmit 2	3.3V	O	
85	GND	/		0V		

86	PG9	RGMII-RXD3	ETH0 Data Receive 3	3.3V	I	
87	PG8	RGMII-RXD2	ETH0 Data Receive 2	3.3V	I	
88	PG10	RGMII-RXCK	ETH0 Receive clock	3.3V	I	
89	GND	/		0V		
90	PG0	RGMII-RXCTL	ETH0 Data reception control bit	3.3V	I	
91	PG2	RGMII-RXD1	ETH0 Data Receive 1	3.3V	I	
92	PG1	RGMII-RXD0	ETH0 Data Receive 0	3.3V	I	
93	GND	/		0V		
94	PE10	PE10	GPIO	3.3V	I/O	
95	PE11	PE11	GPIO	3.3V	I/O	
96	PWM5	PE13	PWM	3.3V	I/O	
97	GND	/		0V		
98	PE2	PE2	GPIO	3.3V	I/O	
99	PE12	PE12	GPIO	3.3V	I/O	
100	NC	/		3.3V		
101	PWM2	PE8	PWM	3.3V	I/O	
102	PWM3	PE9	PWM	3.3V	I/O	
103	NC	/		/		
104	GND	/		0V		
105	UART5_TX	PE6	UART5 Data transmit	3.3V	O	
106	UART5_RX	PE7	UART5 Data receive	3.3V	I	
107	UART4_TX	PE4	UART4 Data transmit	3.3V	O	
108	PE3	PE3	GPIO	3.3V	I/O	
109	UART4_RX	PE5	UART4 Data transmit	3.3V	I	
110	PE1	PE1	GPIO	3.3V	I/O	
111	PE0	PE0	GPIO	3.3V	I/O	
112	GND	/		0V		
113	USB0-DP	USB0-DP	USB0 Data+	/	A I/O	
114	USB0-DM	USB0-DM	USB0 Data-	/	A I/O	
115	GND	/		0V		
116	USB1-DP	USB1-DP	USB1 Data+	/	A I/O	
117	USB1-DM	USB1-DM	USB1 Data-	/	A I/O	
118	GND	/		0V		

119	GND	/		0V		
120	PD1	PD1	GPIO	3.3V	I/O	
121	PD0	PD0	GPIO	3.3V	I/O	
122	GND	/		0V		
123	PD3	PD3	GPIO	3.3V	I/O	
124	PD2	PD2	GPIO	3.3V	I/O	
125	GND	/		0V		
126	PD5	PD3	GPIO	3.3V	I/O	
127	PD4	PD2	GPIO	3.3V	I/O	
128	GND	/		0V		
129	PD7	PD7	GPIO	3.3V	I/O	
130	PD6	PD6	GPIO	3.3V	I/O	
131	GND	/		0V		
132	PD9	PD9	GPIO	3.3V	I/O	
133	PD8	PD8	GPIO	3.3V	I/O	
134	GND	/		0V		
135	PD11	PD11	GPIO	3.3V	I/O	
136	PD10	PD10	GPIO	3.3V	I/O	
137	GND	/		0V		
138	PD13	PD13	GPIO	3.3V	I/O	
139	PD12	PD12	GPIO	3.3V	I/O	
140	GND	/		0V		
L1	AVCC	AVCC	Internal audio reference level	1.8V	O	
L2	LRADC	LRADC	Low Rate ADC	1.8V	AI	Pull Up
L3	GPADC1	GPADC1	General Purpose ADC Input	1.8V	AI	
L4	NC					
L5	GND	/		0V		
L6	MIC-DET	MIC	Headphone MIC Detect	3.3V	I	No Pull Up
L7	MICIN1P	MICP	Microphone Differential +Input 1	3.3V	I	
L8	MICIN1N	MICN	Microphone Differential - Input 1	3.3V	I	
L9	MICIN2P	MICP	Microphone Differential +Input 2	3.3V	I	
L10	MICIN2N	MICN	Microphone Differential -	3.3V	I	

			Input 2			
L11	LINEOUTLP	LINE	Lineout Left Channel Positive Differential Output	1.8V	O	
L12	LINEOUTLN	LINE	Lineout Left Channel Negative Differential Output	1.8V	O	
L13	HP-DET	HP-DET	Headphone Jack Detect	1.8V	I	
L14	LINEOUTRP	LINE	Lineout Right Channel Positive Differential Output	1.8V	O	
L15	LINEOUTRN	LINE	Lineout Right Channel Negative Differential Output	1.8V	O	
L16	MBIAS	Main	First Bias Voltage Output For Main Microphone	1.8V	O	
L17	HBIAS	Headset	Second Bias Voltage Output For Headset Microphone	1.8V	O	
L18	NC					
L19	GND	/		0V		
L20	GND	/		0V		
L21	GND	/		0V		
L22	GND	/		0V		
L23	GND	/		0V		
L24	GND	/		0V		
L25	GND	/		0V		
L26	GND	/		0V		
L27	GND	/		0V		
L28	GND	/		0V		
L29	PE17	PE17	GPIO	3.3V	I/O	
L30	PE16	PE16	GPIO	3.3V	I/O	
L31	PE14	PE14	GPIO	3.3V	I/O	
L32	PE15	PE15	GPIO	3.3V	I/O	
L33	GND	/		0V		
L34	GND	/		0V		
L35	GND	/		0V		
L36	GND	/		0V		
L37	GND	/		0V		
L38	PC0	PC0	GPIO	3.3V	I/O	
L39	PC1	PC1	GPIO	3.3V	I/O	

	L40	NC					
	L41	GND	/		0V		
	L42	PB8	PB8	GPIO	3.3V	I/O	
	L43	PB0	PB0	GPIO	3.3V	I/O	
	L44	PB12	PB12	GPIO	3.3V	I/O	
	L45	PB1	PB1	GPIO	3.3V	I/O	
	L46	PB9	PB9	GPIO	3.3V	I/O	
	L47	PB11	PB11	GPIO	3.3V	I/O	
	L48	PB10	PB10	GPIO	3.3V	I/O	
	L49	GND	/		0V		
	L50	FEL	Boot	Boot Select	3.3V	I	

Table 3-1 MYC-YT113i Core board Pin List

4. Electrical Characteristics

4.1. Primary System Power (VDD_5V)

The main power supply of the MYC-YT113i core board is VDD_5V, which corresponds to the PIN68-70 pin of the stamp hole SMD pad. In order to ensure normal operation, the carried board must provide a voltage of 5V ± 5%, a current of about 1A, and ensure that the output capacity of the supply circuit can meet the power consumption of the core board. This section lists the power consumption and current of the core board under various conditions. Please reserve an appropriate margin when designing the power supply circuit.

Name	Description	Recommended Voltage
VDD_5V	Main supply voltage, 5V input, 2A	5V
VDD_3V3	3.3V output，500mA	3.3V

Table 4-1 External input / output voltage

4.2. Power Consumption

Conditon	Voltage(V)	Average Current(A)	Power Consumption (W)
no-load	5	0.104	0.52
Full-load (ENET*1+USB*2+Type-C*1+SD Card*1+aging)	5	0.172	0.86
mem (echo mem)	5	0.024	0.12
freeze (echo freeze)	5	0.064	0.32

Table 4-2 Power consumption parameters

4.3. GPIO DC Parameters

Parameter	Symbol	Min	Typical	Max	Units	description
High-lever DC input voltage	V_{IH}	0.7*VCC_{IO}	—	VCC_{IO}+0.3	V	—
Low-lever DC input voltage	V_{IL}	-0.3	—	0.3*VCC_{IO}	V	—
High-lever DC output voltage	V_{OH}	VCC_{IO}-0.3	—	VCC_{IO}	V	—
Low-lever DC output voltage	V_{OL}	0	—	0.2	V	—

Table 4-3 GPIO DC Parameters

5. System necessary circuit design

5.1. Boot

With the MYC-YT113i core board, you do not need to pay attention to the boot bit configuration when designing the baseboard. SD card is inserted and the card surface has been burned mirror, the development board will boot from SD card preferentially. After removing the MicroSD card, the development board can be booted from eMMC .

5.2. Burning firmware

Micro SD card circuit is recommended for the core board of MYC-YT113i to burn and update the firmware of the core board, and SMHC0 is recommended for signal interface. Please refer to Section 6.1.

5.3. Debug

It is recommended that the core board of MYC-YT113i use UART interface circuit to debug the software program of the core board. It is recommended that the signal interface use UART5. For details, please refer to Section 6.2.

5.4. Reset

With the MYC-YT113i core board, the SYS-RST-IN signal is drawn from the PIN 73 pin of the core board, the hardware system used for the core board resets the input signal, 3.3V level logic, and there is already a 10Kohm pull-up resistor in the core board.

6. Interfaces

6.1. SD

MYC-YT113i core board is equipped with three SD/MMC interfaces, SMHC0, SMHC1 and SMHC2. SMHC0 is commonly used to design MicroSD card signals; SMHC2 in the core board has been used to connect EMMC/SPI Nand Flash signals; SMHC1 is used for the RGMII network port due to pin multiplexing.

6.1.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	54	SDC0-D0	SDC0-D0	SD0 data 0	3.3V	I/O	
	55	SDC0-D1	SDC0-D1	SD0 data 1	3.3V	I/O	
	56	SDC0-CMD	SDC0-CMD	SD0 command	3.3V	O	
	57	SDC0-D3	SDC0-D3	SD0 data 3	3.3V	I/O	
	58	SDC0-D2	SDC0-D2	SD0 data 2	3.3V	I/O	
	59	SDC0-DET	SDC0-DET	SD0 card detect	3.3V	O	
	61	SDC0-CLK	SDC0-CLK	SD0 CLK	3.3V	O	

Table 6-1 SD/MMC PIN description

6.2. UART

MYC-YT113i core board processor has up to 6 serial ports. Due to the pin reuse of thechip, the core board is configured with two serial ports by default, UART4 and UART5.

The other 4 channels due to pin multiplexing into other functions; Among them, UART1,UART2 and UART3 are 4 lines with flow control (RTS and CTS signal) functions.

6.2.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	105	UART5_TX	PE6	UART5 Data transmit	3.3V	O	
	106	UART5_RX	PE7	UART5 Data receive	3.3V	I	
	107	UART4_TX	PE4	UART4 Data transmit	3.3V	O	
	109	UART4_RX	PE5	UART4 Data transmit	3.3V	I	

Table 6-2 UART PIN description

6.3. USB

The MYC-YT113i core board provides two USB2.0 devices. USB0 supports HOST and Device modes, while USB1 supports only HOST modes.

6.3.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	113	USB0-DP	USB0-DP	USB0 Data+	/	AI/O	
	114	USB0-DM	USB0-DM	USB0 Data-	/	AI/O	
	116	USB1-DP	USB1-DP	USB1 Data+	/	AI/O	
	117	USB1-DM	USB1-DM	USB1 Data-	/	AI/O	

Table 6-3 USB PIN description

6.4. CAN

The MYC-YT113i core board has a maximum of two CAN ports. Due to Pin reuse, one CAN0 bus interface is configured on the core board by default. If you want to use more CAN bus interfaces, please consult the chip manual or Pin List and modify the pin configuration in the driver.

6.4.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	15	CAN0-TX	CAN0	CAN0 data transmit	3.3V	O	
	16	CAN0-RX	CAN0	CAN0 data receive	3.3V	I	

Table 6-4 CAN PIN description

6.5. Ethernet

MYC-YT113i core board leads to a RGMII signal. When the user designs the carried board circuit, the Ethernet PHY circuit, transformer isolation circuit and RJ45 part of the circuit can be designed. CPU Ethernet interfaces support only RGMII and RMII.Can be between TXCLK and RXCLK a 4.7 pF capacitor in parallel, to reduce radiation.

6.5.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	76	PG3	RGMII-TXCK	ETH0 Send clock	3.3V	O	
	78	PG14	RGMII-MDC	ETH0 MDIO clock	3.3V	O	
	79	PG15	RGMII-MDIO	ETH0 MDIO data	3.3V	I/O	
	80	PG4	RGMII-TXD0	ETH0 Data transmit 0	3.3V	O	
	81	PG5	RGMII-TXD1	ETH0 Data transmit 1	3.3V	O	
	82	PG12	RGMII-TXCTL	ETH0 Data transmit control bit	3.3V	O	
	83	PG7	RGMII-TXD3	ETH0 Data transmit 3	3.3V	O	
	84	PG6	RGMII-TXD2	ETH0 Data transmit 2	3.3V	O	
	86	PG9	RGMII-RXD3	ETH0 Data Receive 3	3.3V	I	
	87	PG8	RGMII-RXD2	ETH0 Data Receive 2	3.3V	I	
	88	PG10	RGMII-RXCK	ETH0 Receive clock	3.3V	I	
	90	PG0	RGMII-RXCTL	ETH0 Data reception control bit	3.3V	I	
	91	PG2	RGMII-RXD1	ETH0 Data Receive 1	3.3V	I	
	92	PG1	RGMII-RXD0	ETH0 Data Receive 0	3.3V	I	

Table 6-5 Ethernet PIN description

6.6. LVDS

The MYC-YT113i core board has two LVDS display and output interfaces. LVDS0 supports single LVDS interface display. Supports dual LVDS0+LVDS1 display interfaces.

6.6.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	120	PD1	LVDS0-V0N	LVDS0-V0N	3.3V	I/O	
	121	PD0	LVDS0-D0P	LVDS0-D0P	3.3V	I/O	
	123	PD3	LVDS0-V1N	LVDS0-V1N	3.3V	I/O	
	124	PD2	LVDS0-D1P	LVDS0-D1P	3.3V	I/O	
	126	PD5	LVDS0-V2N	LVDS0-V2N	3.3V	I/O	
	127	PD4	LVDS0-D2P	LVDS0-D2P	3.3V	I/O	
	129	PD7	LVDS0-CKN	LVDS0-CKN	3.3V	I/O	
	130	PD6	LVDS0-CKP	LVDS0-CKP	3.3V	I/O	
	132	PD9	LVDS0-V3N	LVDS0-V3N	3.3V	I/O	
	133	PD8	LVDS0-D3P	LVDS0-D3P	3.3V	I/O	
-							
	135	PD11	LVDS1-V0N	LVDS1-V0N	3.3V	I/O	
	136	PD10	LVDS1-D0P	LVDS1-D0P	3.3V	I/O	
	138	PD13	LVDS1-V1N	LVDS1-V1N	3.3V	I/O	
	139	PD12	LVDS1-D1P	LVDS1-D1P	3.3V	I/O	
	2	PD14	LVDS1-V2N	LVDS1-V2N	3.3V	I/O	
	3	PD15	LVDS1-D2P	LVDS1-D2P	3.3V	I/O	
	5	PD16	LVDS1-CKN	LVDS1-CKN	3.3V	I/O	
	6	PD17	LVDS1-CKP	LVDS1-CKP	3.3V	I/O	
	8	PD18	LVDS1-V3N	LVDS1-V3N	3.3V	I/O	
	9	PD19	LVDS1-D3P	LVDS1-D3P	3.3V	I/O	

Table 6-6 RGB PIN description

6.7. I2C

The MYC-YT113i core board processor supports a maximum of four I2C (TWI) buses, in which I2C3 is used for E2PROM chips in the core board, and I2C3 is routed to the core board interface. By default, two I2C bus interfaces, I2C1 and I2C3, are configured on the core board.

If you want to use more I2C bus interfaces, consult the chip manual or Pin List and modify the pin configuration in the driver.

6.7.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	11	TWI3_SCK	TWI3	TWI3 clock	3.3V	O	
	12	TWI3_SDA	TWI3	TWI3 data	3.3V	I/O	
	13	TWI1_SDA	TWI1	TWI1 data	3.3V	I/O	
	17	TWI1_SCK	TWI1	TWI1 clock	3.3V	O	

Table 6-7 I2C PIN description

6.8. Audio

MYC-YT113i core board contains the analog audio CODE-C interface, which can provide 1 HPOUT L/R interface, 1 MICIN3 P/N, 1 LINEIN L/R, 1 FMIN L/R.

6.8.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	29	HPOUTR	HPOUTR	Headphone Right Output	3.3V	O	
	30	HPOUTL	HPOUTL	Headphone Light Output	3.3V	O	
	31	HPOUTFB	HPOUTFB	Pseudo Differential Headphone Ground Reference	3.3V	I/O	
	19	MICN	MICN	Microphone Differential -Input 3	3.3V	I	
	20	MICP	MICP	Microphone Differential + Input 3	3.3V	I	
	22	FMINR	FMINR	FMIN Right Input	3.3V	I	
	23	FMINL	FMINL	FMIN Left Input	3.3V	I	
	25	LINEINR	LINEINR	LINEIN Right Single-End Input	3.3V	I	
	26	LINEINL	LINEINL	LINEIN Left Single-End Input	3.3V	I	
	L6	MIC-DET	MIC	Headphone MIC Detect	3.3V	I	
	L7	MICIN1P	MICP	Microphone Differential +Input 1	3.3V	I	
	L8	MICIN1N	MICN	Microphone Differential - Input 1	3.3V	I	
	L9	MICIN2P	MICP	Microphone Differential +Input 2	3.3V	I	
	L10	MICIN2N	MICN	Microphone Differential - Input 2	3.3V	I	
	L11	LINEOUTLP	LINE	Lineout Left Channel Positive Differential Output	1.8V	O	
	L12	LINEOUTLN	LINE	Lineout Left Channel Negative Differential Output	1.8V	O	
	L14	LINEOUTRP	LINEOUTRP	Lineout Right Channel Positive Differential Output	3.3V	O	
	L15	LINEOUTRN	LINEOUTRN	Lineout Right Channel Negative Differential Output	3.3V	O	
	L16	MBIAS	Main	First Bias Voltage Output For Main Microphone	1.8V	O	
	L17	HBIAS	Headset	Second Bias Voltage Output For Headset Microphone	1.8V	O	

Table 6-8 Audio PIN description

6.9. ADC

MYC GPADC - YT113i core board support 2 road and 4 road TPADC, 1 road LRADC. GPADC has 12-bit resolution, a maximum 1Mhz sampling rate, and supports signal input ranges from 0 to 1.8V. TPADC supports a maximum 12-bit resolution, a sampling rate of 1Mhz, and input signals ranging from 0 to 1.8V. LRADC has six resolution, maximum 2 KHZ sampling rate, support the signal input range of 0-1.266 V, LRADC has draw out but there is no specific use.

6.9.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	L2	LRADC	LRADC	Low Rate ADC	1.8V	AI	
	L3	GPADC1	GPADC1	ADC input	1.8V	AI	
	36	GPADC0	GPADC0	ADC input	1.8V	AI	
	37	TP-X1	TP-X1	Touch panel X1 input	1.8V	AI	
	38	TP-X2	TP-X2	Touch panel X2 input	1.8V	AI	
	39	TP-Y1	TP-Y1	Touch panel Y1 input	1.8V	AI	
	40	TP-Y2	TP-Y2	Touch panel Y1 input	1.8V	AI	

Table 6-9 ADC PIN description

7. Package Information

7.1. Package Dimensions

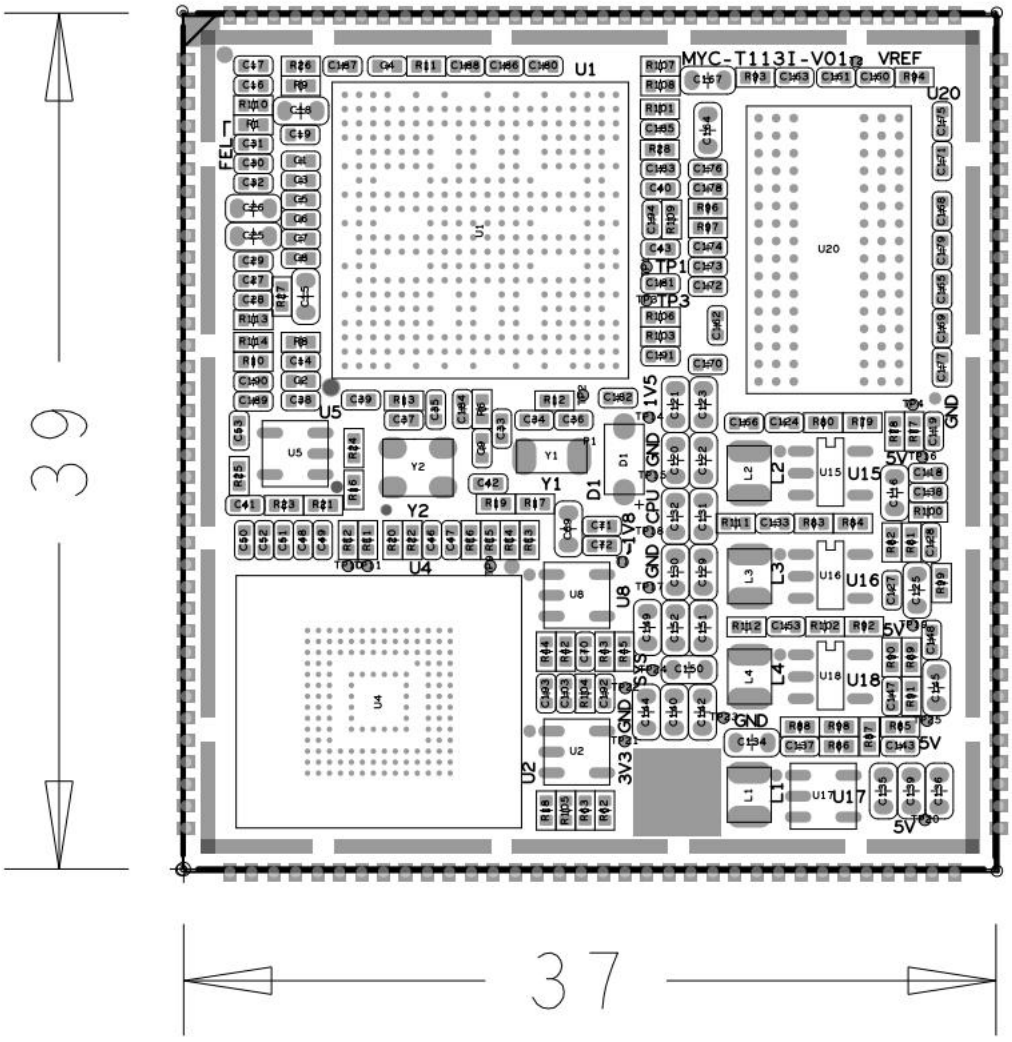

Figure 7-1 MYC-YT113i Top View

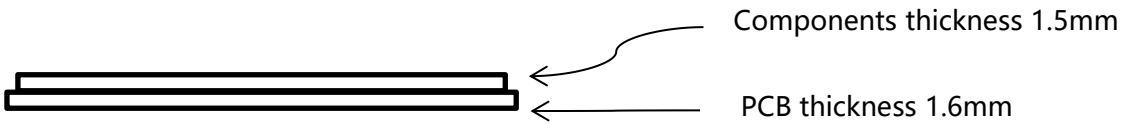

Figure 7-2 MYC-YT113i Side View

7.2. Carrier Board PCB Design

a. PCB thickness is recommended to be at least 1.6mm. Pay attention to the balance of copper coating. If PCB deformation occurs in the over furnace, it is recommended to use a carrier to fix the over furnace.

b. To ensure the quality of mounting and tinning, ensure that the PCB module is at least 3mm away from other components.

c. PCB packaging provided by MYIR Electronics is recommended.

8. Mount and storage requirements

8.1. Steel mesh design

1) It is recommended to open holes at a ratio of 1:1 for the circular pad with a thickness of 0.15mm tin; With a thickness of 0.18mm, the opening ratio is 1:0.8.

8.2. Storage requirement

Modules are shipped in vacuum sealed form, and the following conditions are required for storage:

1) The vacuum-sealed bag can be stored for 12 months when the ambient temperature is lower than 40℃ and the air humidity is less than 90%.

2) After opening the vacuum sealing bag, reflow welding can be carried out directly within 72 hours when the ambient temperature is lower than 30℃ and the air humidity is less than 10%.

Note: If the above conditions are not met, baking should be carried out before applying.

8.3. Baking method

Because the module packaging material cannot withstand high temperature, if necessary, please choose one of the following two methods to bake, to avoid affecting the welding quality of the module.

1) Baking in the original package: baking temperature is 40 ~ 60℃ and time is 5 ~ 7 days.

2) Transfer to high temperature resistant dish baking: baking temperature is 100 ~ 120, baking time is more than 48 hours.

8.4. Welding technology

1) If the plate to be mounted is double-sided device layout, it is recommended to put the core plate mounting process in the last stage.

2) It is recommended to set the preheating time of 160 ~ 200℃ to 60 ~ 120 seconds.

3) It is recommended that the temperature of reflow welding should be 235 ~ 245℃, and the maximum temperature should not exceed 250℃, and the reflow time should be controlled within 40 ~ 60 seconds.

4) The recommended temperature rise rate is 1-3 ℃/ s, and the temperature drop rate is 2-4 ℃/ s.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR’ s products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.

- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

MYIR Tech Limited

Headquarter Address: Room 04, 6th Floor, Building No.2, Fada Road, Yunli Smart Park, Bantian, Longgang District, Shenzhen, Guangdong, China 518129

Factory Address: Room 201, Block C, Shengjianli Industrial Park, Dafu Industrial Zone, Guanlan, Longhua District, Shenzhen, 518110, China

Website: www.myir.cn
Email: sales.en@myir.cn
Tel: +86-755-22984836