MYiR 米尔电子
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MYC-YT113i

Hardware Design Guide

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MYIR Electronics Limited

History

Version	Author	Participants	Date	Description
V1.0	Sender		20230804	Official release

Contents

1. Overview

This document is intended to help hardware engineers design board-level circuits based on the core module of MYC-YT113i. Please fully understand the content of this document before you begin your design. This document contains common information, such as reference design instructions, Layout suggestions, and design check items, to assist hardware engineers in designing.

The references used in this document are from the official website of MYIR Electronics and are included in the hardware documentation of MYC-YT113i. You can download them at any time from the following address.

http://d.myirtech.com/MYD-YT113i/

In addition, MYIR Electronics will also provide the following resources to facilitate your design:

- Core board / evaluation board product manual;
- Evaluation board principle graphical source file;
- Related device manuals.

1.1. Supported products

This document applies to all models of MYC-YT113i series core boards.

1.2. Disclaimer

- Some of reference designs in the document are based on MYIR electronic evaluation boards and cannot be guaranteed to be suitable for all application scenarios. If your product has special requirements for application scenarios or technical specifications, please adjust the design according to the actual situation.
- Reference design and layout in the document are recommended for reference only and do not necessarily contain all the matters needing attention. Please make adjustments according to the actual situation.
- MYIR shall not be liable for any form of technical endorsement or joint liability for any proposal contained in any document.

2. Power supply design

The design of the power supply system is very important in the design of embedded products. Engineers need to consider not only the basic electrical parameters of the power supply itself, but also the stability design of the power supply, such as electromagnetic compatibility, temperature range, safety design, three-proof design and other factors. Any negligent factor may cause the whole system to fail to work normally. Before starting the design of a power supply system for a new product, the engineer should thoroughly understand the actual requirements of the entire system, thoroughly demonstrate the feasible design solution based on cost and efficiency, and select an appropriate power supply method for the system.

2.1. reference circuit

The core plate needs to provide 5V voltage for normal operation, and the full load power consumption is close to 1W. Considering that the instantaneous current of the product is relatively large and the circuit performance may derate under high temperature conditions, the system cannot start normally if the power supply is insufficient. Therefore, the power supply design should leave a certain margin to ensure the stable and reliable operation of the system. It is recommended that a power chip of about 1A be used to power the core board alone. It is not recommended to use the power chip to drive loads other than the core board, especially some high-power load components.

LDO or DCDC can be used as the power chip. LDO has the advantages of simple use, low cost, low electromagnetic interference, but high calorific value. DCDC has the advantages of strong current output capacity, high conversion efficiency, low calorific value, but relatively large electromagnetic interference. If the input voltage is close to 5V, the LDO power chip can be used. If the input voltage is much different from 5V, the DCDC power chip is recommended.

The core board is supplied with 5V power. Please add energy storage capacitance and decoupling capacitance appropriately near the 5V voltage input pin of the core board. Reserve 0.25R resistors to assess core board power consumption. Use a multimeter in MV mode to measure the voltage at both ends. The current flowing through the resistance can be calculated by Ohm's law I=U/R, and the power consumption of the core board can be evaluated finally.

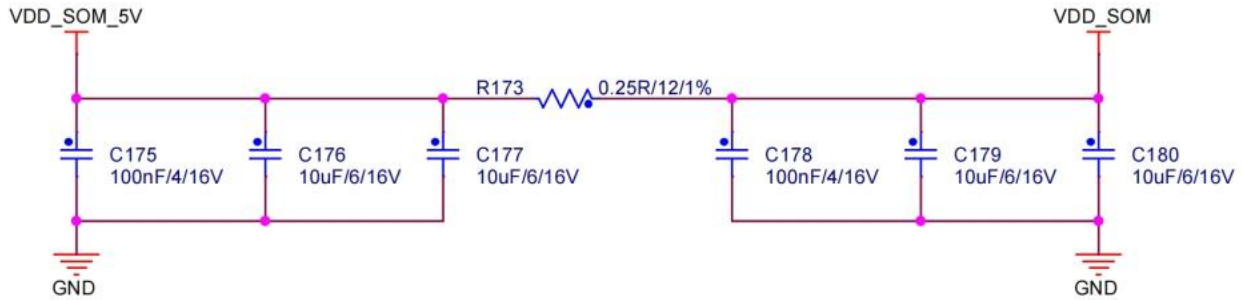


Figure 2-1 Core board 5V power supply

2.2. Power Protection

To ensure the reliability of the power supply system, it is not recommended to directly supply the external input voltage that has not been processed to each load terminal at the rear stage. You can refer to the protection circuit in the following figure to process the power supply before using it to improve the reliability and security of the input power supply and reduce electromagnetic interference. The baseboard input power supply in the reference design is 12V. As an example only, the input power supply value should be determined according to your actual requirements.

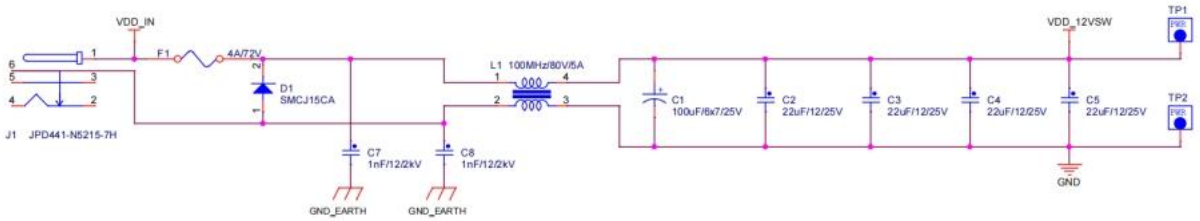


Figure 2-2 General power input circuit

2.3. Power Sequence

The power system design must follow certain power-on timing and corresponding steady-state regulations to ensure the reliable operation of the chip. In the design, it is recommended that the core board should be powered on first, and then the carried board peripheral I/O devices should be powered on. Failure to meet the power-on timing may lead to the following conditions：

- I/O current from the carried board peripheral backs up to the processor, which fails to start normally.
- The floor peripheral I/O current flows back to the processor, causing irreversible damage in the worst case.
- Powering on the mainboard Power on 5V for the core board, then 5V for the control board and 3V3.

2.4. Layout Guidelines

- The distance between different power planes should be at least 20mil;
- Widen the width of the power cord and ground wire as far as possible to meet the required rated current value, and the width of the feedback signal should not be too narrow, more than 10mil is recommended;
- If DCDC is used, it is not recommended to take signal cables below the inductance;
- If DCDC is used, the path of the current loop should be as short as possible, and the inductor and capacitor should be placed as close to the chip as possible, namely, the red and green paths in the following figure;

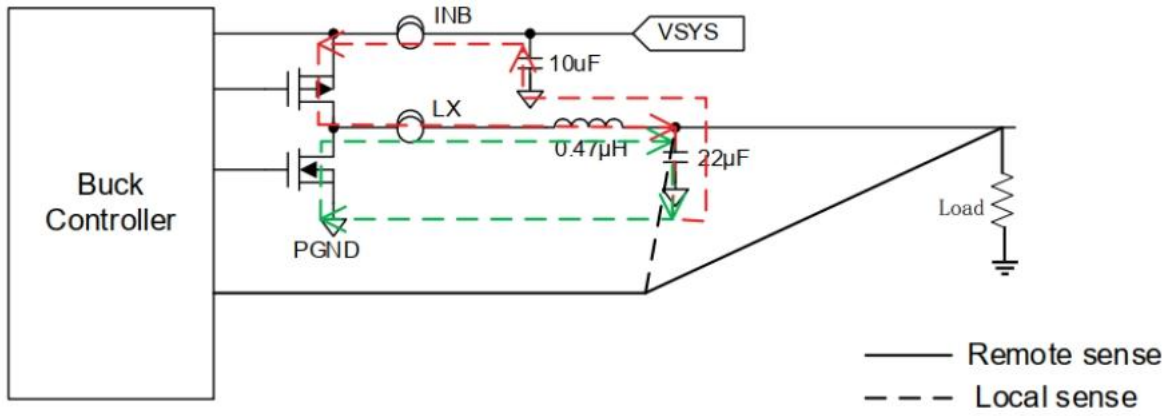


Figure 2-3 DCDC current back flow path

- If LDO is used, attention should be paid to the thermal resistance of LDO chip. Because the heat loss of LDO chip is relatively high, it is recommended to add grounding pads and make more grounding holes on the pads;
- Try to select the capacitance of small ESR at the output end;
- The power chip with digital ground and analog ground should be separated and connected only at a single point at the main power input, and the analog ground should not be connected to the grounding pad.

3. System necessary circuit design

3.1. Boot

With the MYC-YT113i core board, you do not need to pay attention to the boot bit configuration when designing the baseboard. SD card is inserted and the card surface has been burned mirror, the development board will boot from SD card preferentially. After removing the MicroSD card, the development board can be booted from eMMC.

3.2. Burning firmware

Micro SD card circuit is recommended for the core board of MYC-YT113i to burn and update the firmware of the core board, and SMHC0 is recommended for signal interface. Please refer to Section 5.1.

3.3. Debug

It is recommended that the core board of MYC-YT113i use UART interface circuit to debug the software program of the core board. It is recommended that the signal interface use UART5. For details, please refer to Section 5.2.

3.4. Reset

With the MYC-YT113i core board, the SYS-RST-IN signal is drawn from the PIN 73 pin of the core board, the hardware system used for the core board resets the input signal, 3.3V level logic, and there is already a 10Kohm pull-up resistor in the core board. Please refer to Section 4 for details.

4. Key Circuit Design

The MYC-YT113i core board provides special function pins, namely SYS-RST-IN and User Key. These signals are usually used for external keys. Table 4-1 describes the functions.

As the key signal is more sensitive, it is usually possible to use resistance and capacitance to form a simple RC filter. On the one hand, it can filter the jitter interference when the key is pressed, and at the same time filter the interference introduced by the outside to affect the reset signal. In a harsh electromagnetic environment, an ESD device can be connected in parallel to eliminate the electrostatic interference from the key and ensure more reliable operation of the system. If there is a more strict requirement for the elimination of shake, a logic circuit such as RS flip-flop can be considered to set up a reset circuit.

Special function pin	description
SYS-RST-IN	3.3V level logic. The core board has a design pull-up resistance of 10Kohm. Hardware reset input.
PE1	3.3V level logic. The user presses a button to generate an event/interrupt.

Table 4-1 Special function pins

4.1. reference circuit

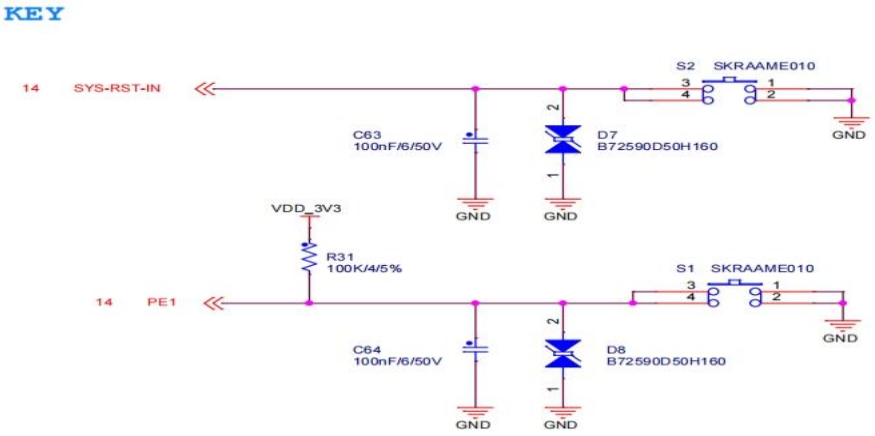


Figure 4-1 Key circuit

4.2. Layout Guidelines

- The width of reset signal line should not be too narrow, it is recommended not less than 8mil;
- Reset signal is sensitive signal, which is recommended to be surrounded by ground;
- Place TVS as close to the button as possible.

5. Interface circuit design

5.1. SD/MMC

MYC-YT113i core board is equipped with three SD/MMC interfaces, SMHC0, SMHC1 and SMHC2. SMHC0 is commonly used to design Micro SD card signals; SMHC2 can be used to design communication between SDIO interfaces; SMHC1 is used for the RGMII network port due to pin multiplexing.

5.1.1. reference circuit

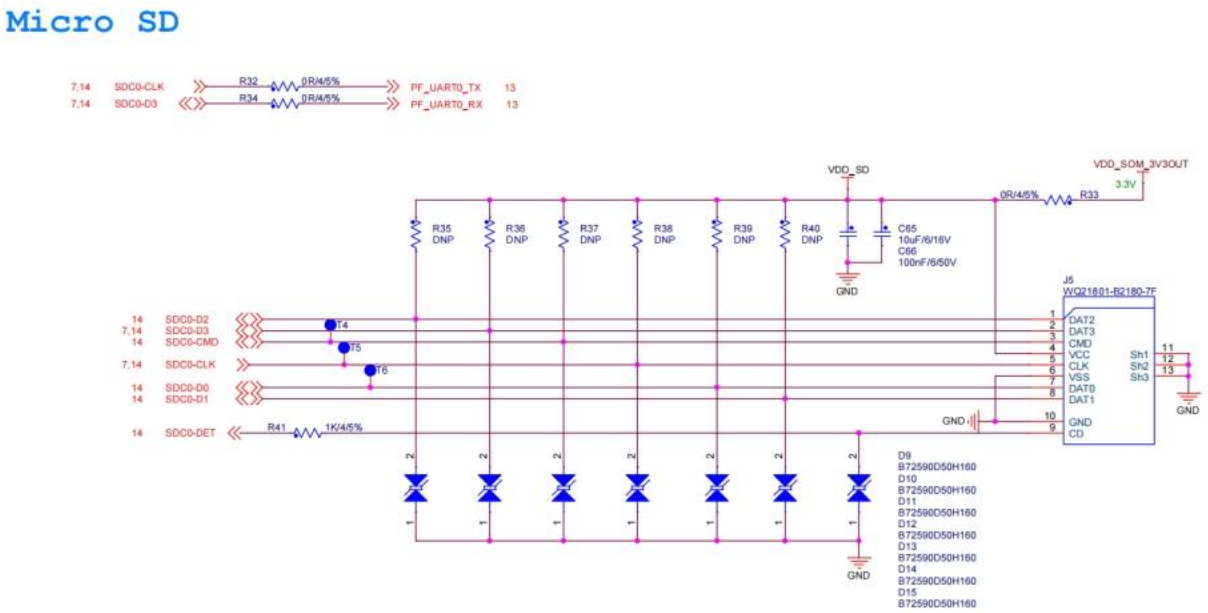


Figure 5-1 Micro SD Reference circuit

5.1.2. Layout Guidelines

- Interface signals need to do impedance control, using a single-end impedance of 50Ω;
- Data line control line as long as possible, error is less than ±100mil;
- If the wiring space is sufficient, the CLK signal should be processed as extensively as possible. If you can't do that, distance the clock signal from the other signals and follow the 3W rule.
- SDC-DET pin in series 1K resistance to improve ESD performance.
- The power supply of SD card is provided by the core board 3V3, and the burning can be started after power-on.

5.2. UART

MYC-YT113i core board processor has up to 6 serial ports. Due to the pin reuse of thechip, the core board is configured with two serial ports by default, UART4 and UART5.

The other 4 channels due to pin multiplexing into other functions; Among them, UART1,UART2 and UART3 support 4 lines, with flow control (RTS and CTS signal) function.

When the UART is used as the debugging serial port, connect it to the PC with a UARt-to-USB conversion cable. The following figure shows the common USB-to-UART TTL modules.

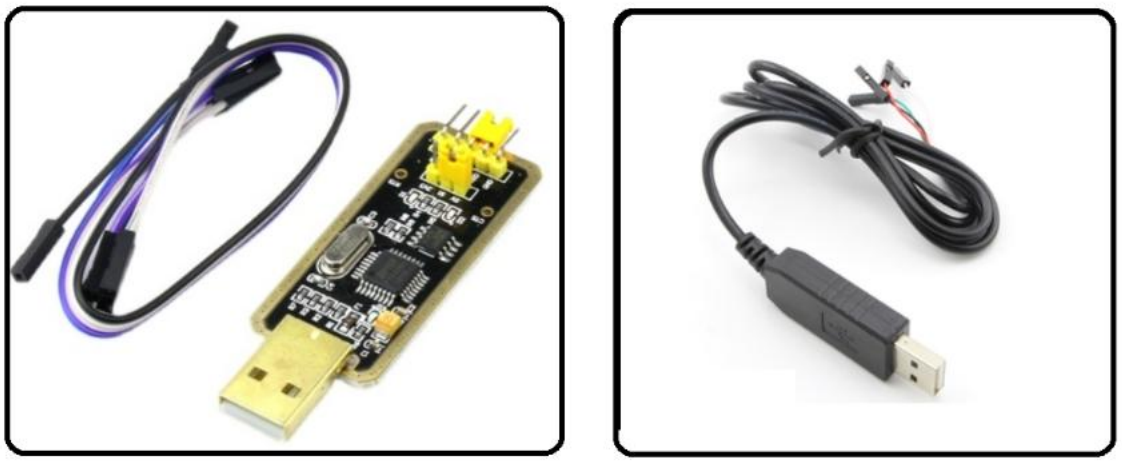


Figure 5-2 USB to UART TTL module

5.2.1. reference circuit

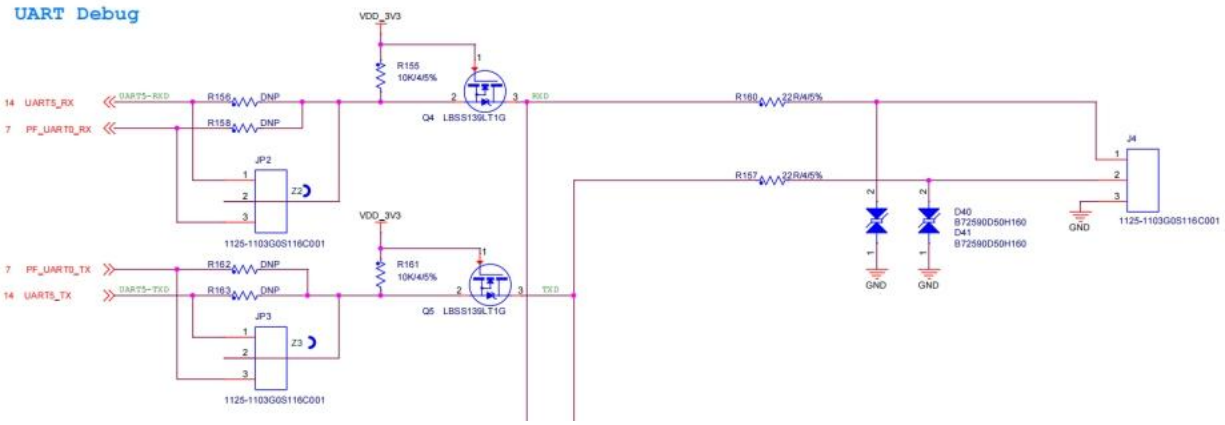


Figure 5-3 UART reference circuit

5.2.2. Layout Guidelines

- Keep sufficient spacing between signal and power plane before and after isolation;
- TVS tubes are placed next to connectors.

5.3. USB

The MYC-YT113i core board provides two USB2.0 devices. USB0 supports HOST and Device modes, while USB1 supports only HOST modes.

USB0 directly connects to the USB Type C seat son and supports OTG/DRP mode. Another USB B1 uses a USB2.0 HUB chip to expand four USB Host ports. Two of the fourexpanded ports are directly routed through the dual-layer USB Type A connector. The third circuit is used to connect 4G/5G modules. The fourth route is used to connect to the WIFI module.

USB signal is recommended with TVS tube, common mode inductor.

5.3.1. reference circuit

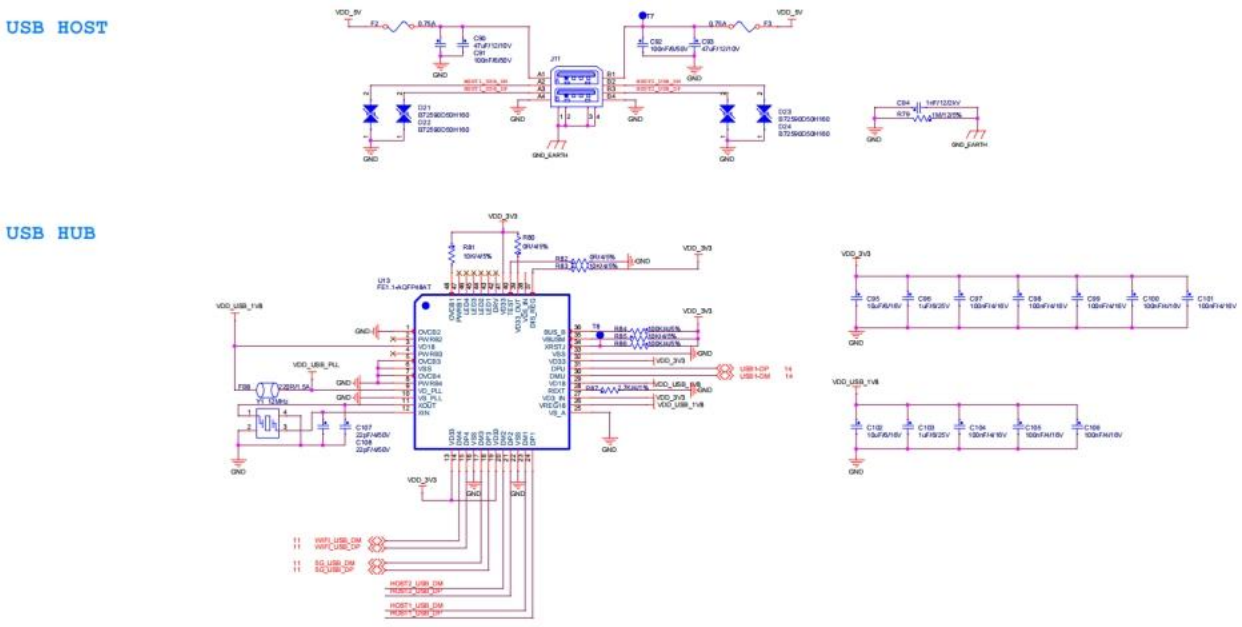
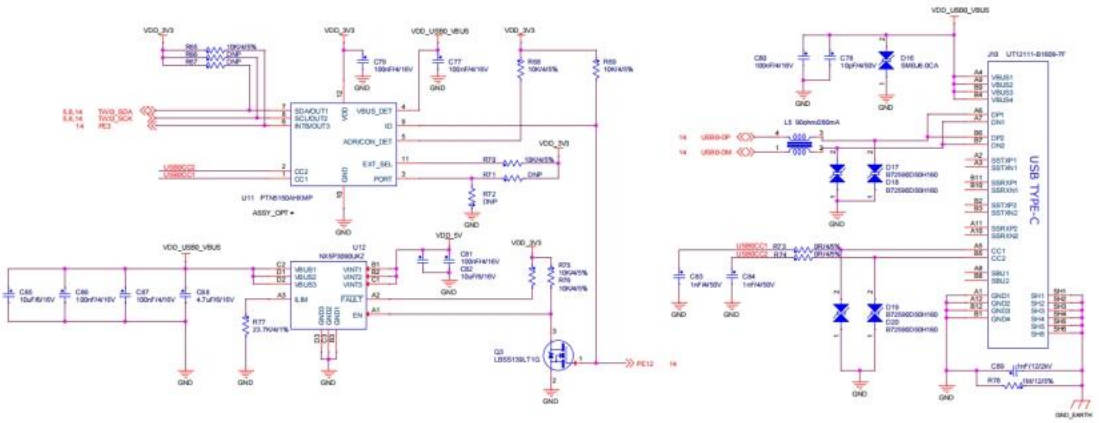


Figure 5-4 USB HUB and HOST reference circuit



Figur 5-5 USB DRP reference circuit

5.3.2. Layout Guidelines

- USB signal routing isometric control, error range ±25mil;
- The differential impedance of USB signal is controlled by 90Ω;
- USB signal cable as short as possible;
- Try not to change the layer of USB signal. If the layer is changed, the GND return through hole should be placed within 50mil away from the cross hole of the layer.
- Ensure that the reference plane is continuous, USB signal does not cross division;
- It is recommended that USB signals be routed on the TOP/BOTTOM layer.
- USB signal away from other clock, digital signal.

5.4. CAN

The MYC-YT113i core board has a maximum of two CAN ports. Due to PIN reuse, one CAN0 bus interface is configured on the core board by default. If you want to use more CAN bus interfaces, please consult the chip manual or PIN List and modify the pin configuration in the driver.

5.4.1. reference circuit

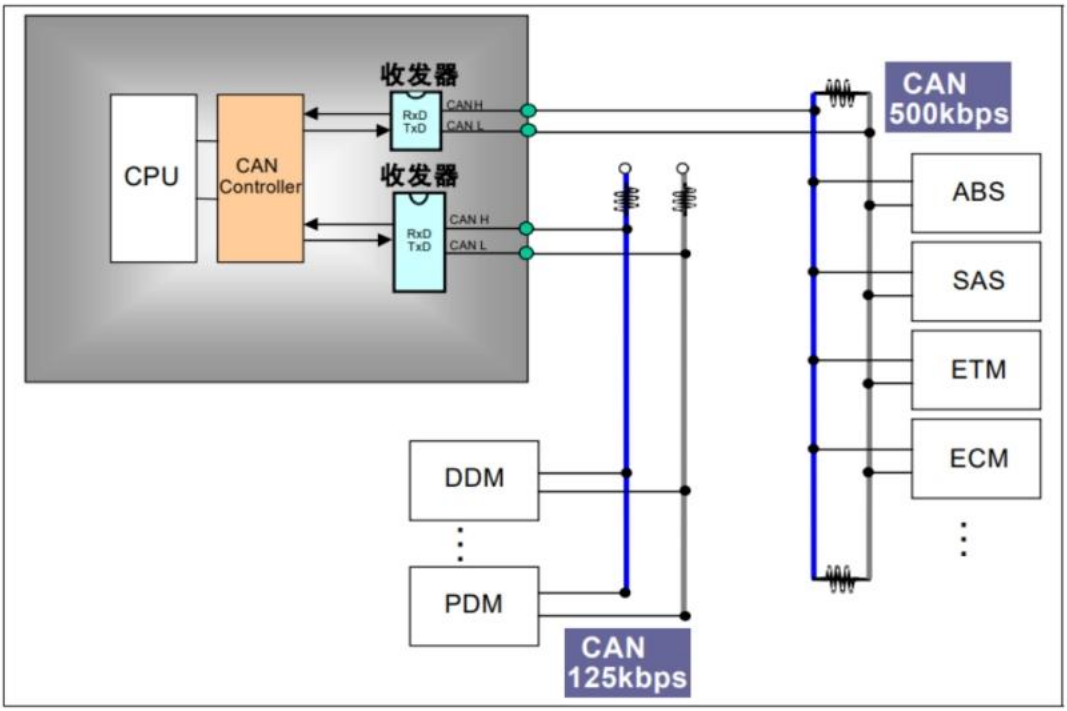


Figure 5-6 CAN reference circuit

5.4.2. Layout Guidelines

- CAN signal single-end impedance control 50Ω;
- CAN signal routing isometric control, error range ±25mil;
- Ensure continuity of the reference layer of the signal.

5.5. Ethernet

MYC-YT113i core board leads to a RGMII signal. When the user designs the carried board circuit, the Ethernet PHY circuit, transformer isolation circuit and RJ45 part of the circuit can be designed.

CPU Ethernet interfaces support only RGMII and RMII.

5.5.1. reference circuit

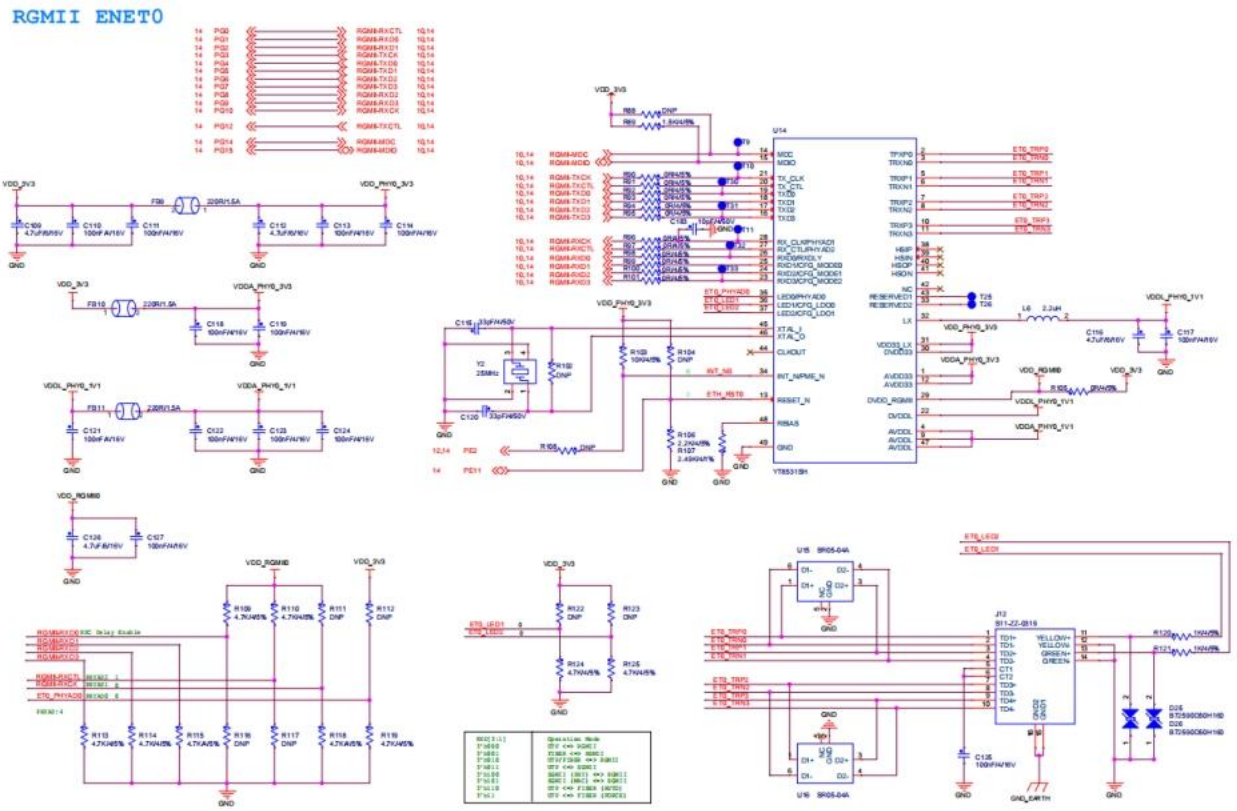


Figure 5-7 Ethernet reference circuit

5.5.2. Layout Guidelines

- RGMII difference pairs need to be controlled with equal spacing and equal length error ±5mil.
- PHY chip is placed near the core board and far away from the network transformer.
- The network transformer is placed near the RJ45 interface;
- The power pin decoupling capacitor of the PHY chip is placed near the PHY chip;
- Can be between TXCLK and RXCLK a 4.7 pF capacitor in parallel, to reduce radiation.

5.6. I2C

The MYC-YT113i core board processor supports a maximum of four I2C (TWI) buses, in which I2C3 is used for E2PROM chips in the core board, and I2C3 is routed to the core board interface. By default, two I2C bus interfaces, I2C1 and I2C3, are configured on the core board.

If you want to use more I2C bus interfaces, consult the chip manual or PIN List and modify the pin configuration in the driver. Several devices can be mounted under the same I2C main line. The following points should be paid attention to when designing the schematic diagram:

- Check whether the device address under the same bus is in conflict;
- Ensure that each I2C bus has a pair of pull-up resistors, the resistance value is recommended to be 2.2K~10K, but do not repeatedly add;
- Check whether the level of I2C interface of the device is 3.3V. If not, add the level shift circuit.
- The number of devices under the same bus should not be too large, otherwise it is possible to exceed the load capacitance limit of 400 pF required by the I2C specification and affect the signal waveform.

5.6.1. reference circuit

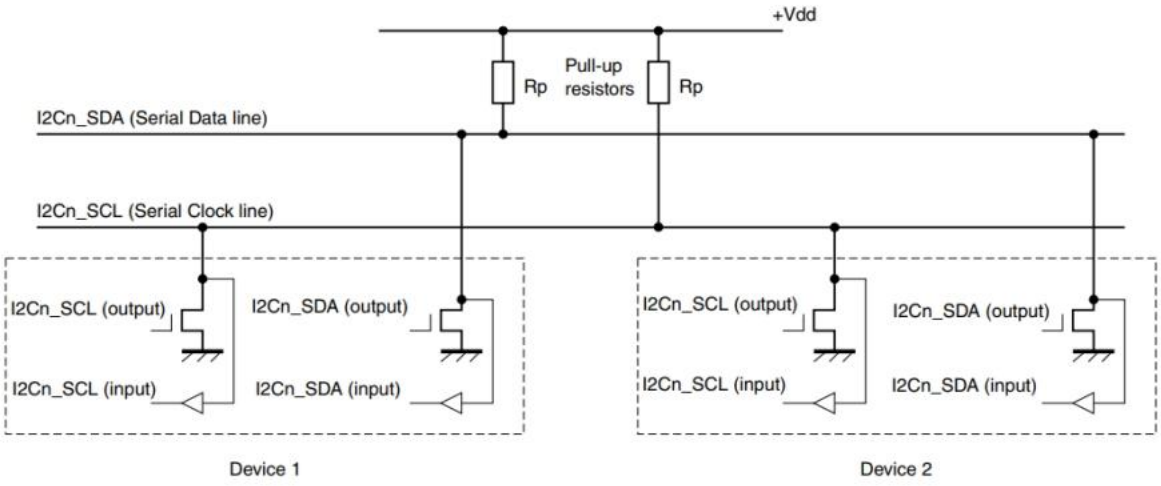


Figure 5-8 I2C reference circuit

5.6.2. Layout Guidelines

- The width of I2C signal line should not be too narrow, and it is recommended to be 6mil or above;
- I2C wiring should be planned before the location of each device, line not too winding, I2C line is too long, it will increase the Load effect of the bus;
- Avoid interference sources. The distance between adjacent lines should be at least 10mil.

5.7. LVDS

MYC-YT113i core board supports LVDS signal output. MYC-YT113i provides a Single Link LVDS0 interface, supporting 1366x768@60fps display output; In addition, two Single LVDS can form Dual Link LVDS interfaces to support higher display resolution 1920x1080@60fps.

MYIR has officially designed a 7 "LVDS MY-LVDS070C LCD module. The LCD module supports a resolution of 1024x600. For details, please refer to the website: https://www.myir-tech.com/product/my-lvds070c.htm

5.7.1. reference circuit

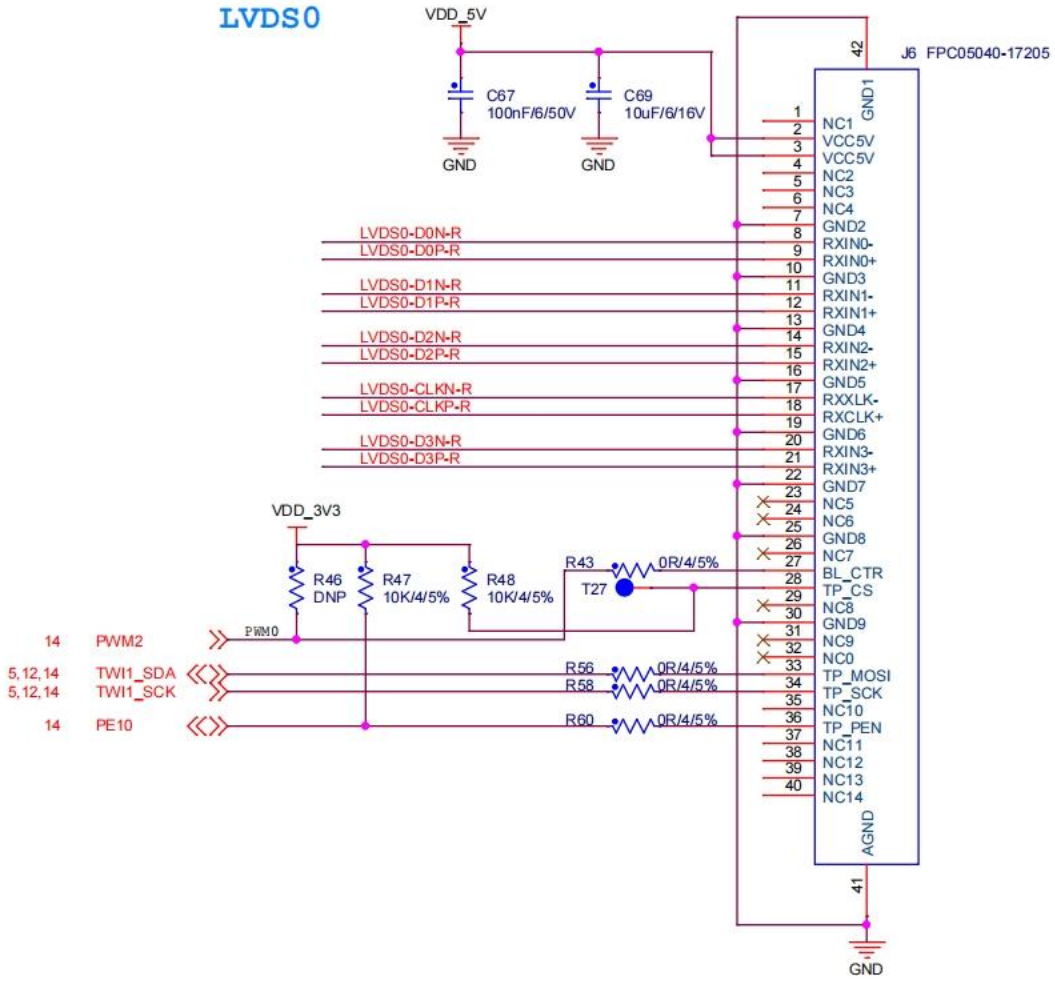


Figure 5-9 Single Link LVDS reference circuit

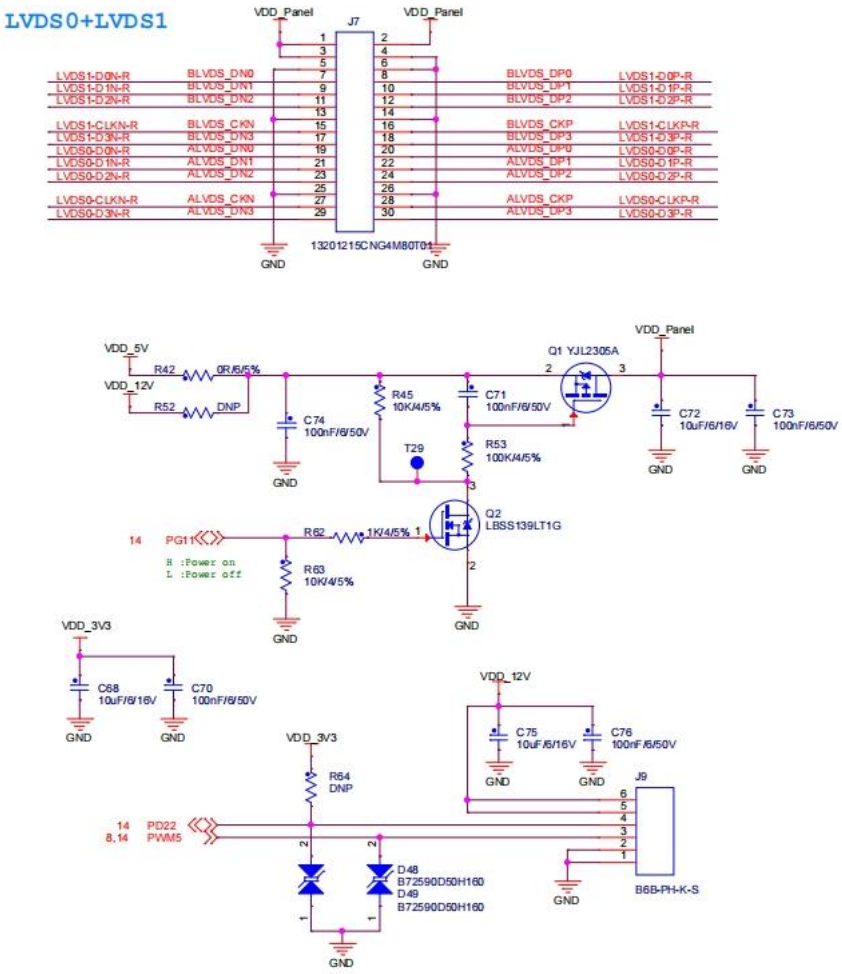


Figure 5-10 Dual Link LVDS reference circuit

5.7.2. Layout Guidelines

- The difference pair of data and time clock should follow the rule of equal length and distance, the error control of difference pair is +-5mil, and the difference impedance is 100 euros. Holes should be drilled less, and the P/N difference pairs should be made at the same time when the holes are drilled and the ground holes should be drilled around the difference pairs as much as possible.
- The data difference pairs need to take the clock difference pairs as reference for inter-group equi-length. Equal length +-50mil.
- The reference plane is complete, and the routing does not span the division.
- Use HD LVDS, power VDD_PANEL and GND to route thicker cables with a cable width of more than 50mil, and place a large-capacity energy storage capacitor near the connector.

5.8. Audio Out

MYC-YT113i core board native support Audio Out output. On its HPOUTL/R signal through the audio amplifier chip, through the platoon interface out.Chip concrete support two-way PCM/I2S digital audio interface, two-way audio output interface (LINE/HPOUT), 5 audio input interface (MICIN * 3, FMIN, LINEIN).

5.8.1. reference circuit

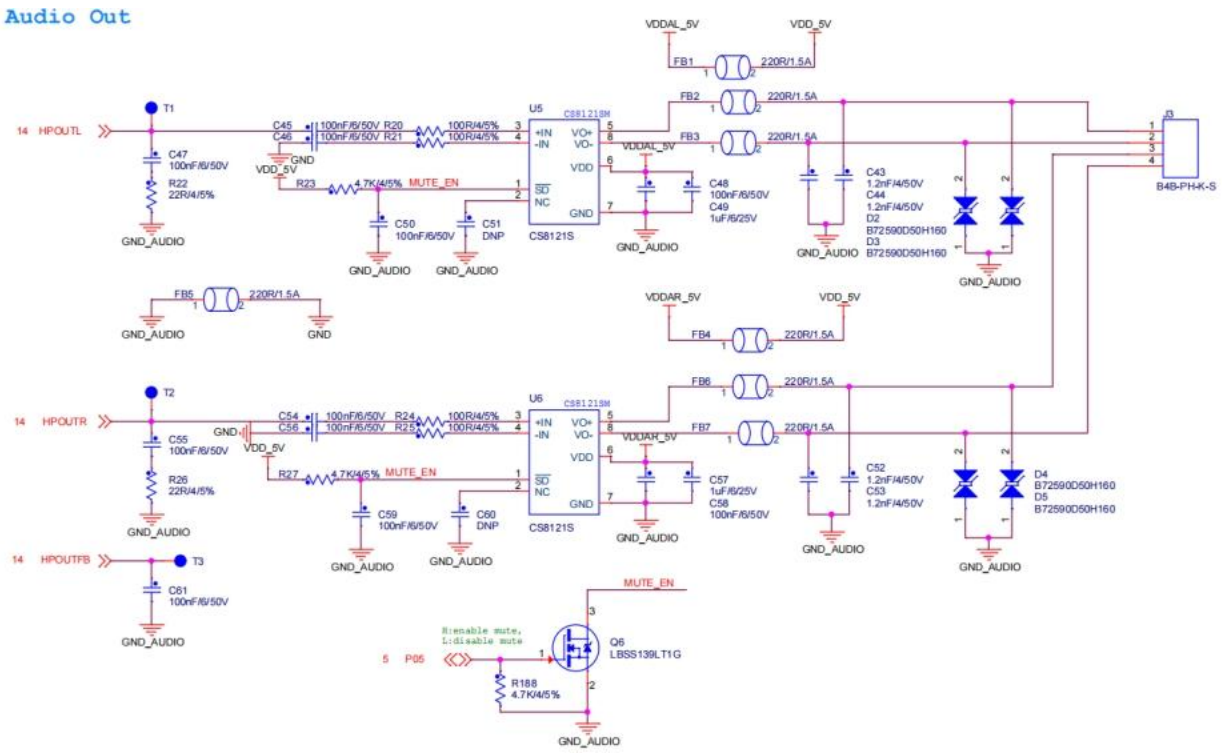


Figure 5-11 Audio Out reference circuit

5.8.2. Layout Guidelines

- The isolation points of GND_AUDIO and GND are star grounded and close to the power input end of the baseboard as far as possible.
- Audio circuit layout position away from interference sources, it is recommended to plan a separate area in PCB to place analog circuit;
- Audio Out belongs to analog audio signal, recommended 10mil and above.
- Note the distinction between analog and digital.

5.9. ADC

The MYC - YT113i core board support 2 TPADC and 4 GPADC, 1 LRADC . GPADC has 12-bit resolution, a maximum 1Mhz sampling rate, and supports signal input ranges from 0 to 1.8V. TPADC supports a maximum 12-bit resolution, a sampling rate of 1Mhz, and input signals ranging from 0 to 1.8V. LRADC has six resolution, maximum 2 KHZ sampling rate, support the signal input range of 0 ~ 1.266 V, LRADC has draw out but there is no specific use.

The reference circuit is used to evaluate the input function of G/TPADC.

5.9.1. reference circuit

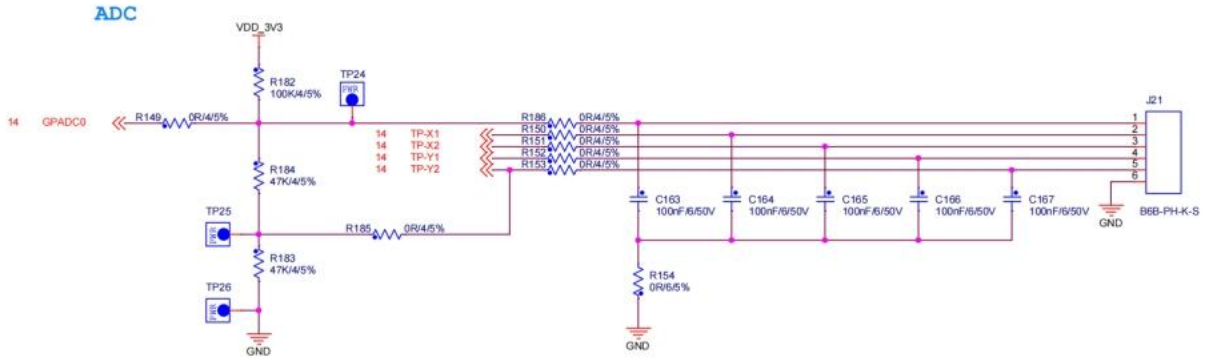


Figure 5-12 ADC reference circuit

5.9.2. Layout Guidelines

- Note the distinction between analog and digital;
- Analog input channel protection.
- LRADC pulls 51K to AVCC

5.10. RTC

The evaluation board is equipped with a backup battery holder that can be connected to button batteries. In case of power failure, the system can be used to maintain the operation of the RTC part. Its circuit structure is shown as follows:

5.10.1. reference circuit

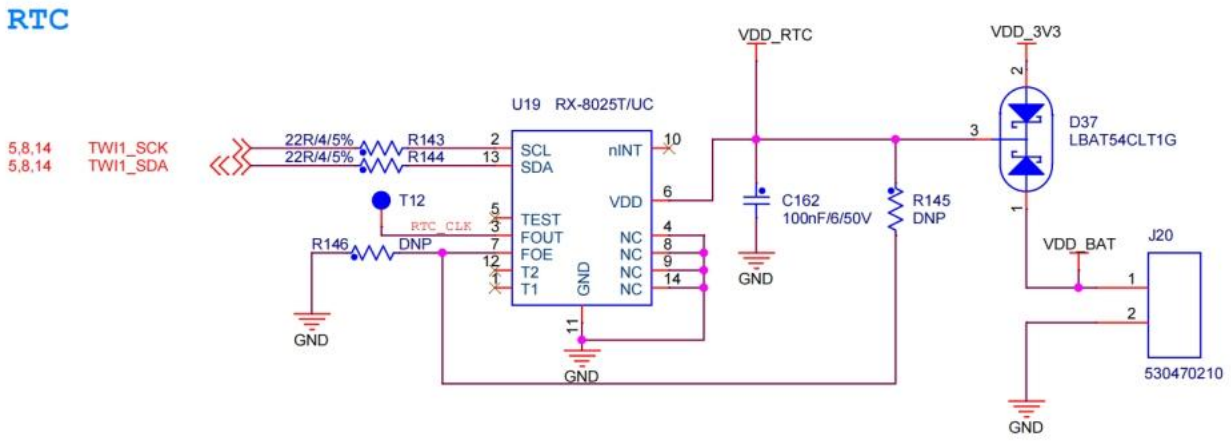


Figure 5-13 RTC reference circuit

5.10.2. Layout Guidelines

- C162 is placed close to J21;
- The width of I2C signal line should not be too narrow, and it is recommended to be 6mil or above;
- I2C wiring should be planned before the location of each device, the line should not be too winding.

6. Design check item

6.1. Power supply design

Check item	Recommended solution
Core board supply voltage	The recommended value is 5V and the absolute value is 4.5V-5.5V
Core board power decoupling capacitor	Use capacitors with 47uF and above value for core module power supply
IO level of carrier board peripherals	The IO voltage level of the peripheral should match the corresponding interface level of the core module
core module power sequence	It is recommended that the core module power start before the peripheral power
Temperature rise of power chip	Confirm the thermal resistance of the power chip, and calculate the maximum temperature rise of the power chip based on the power consumption of the core module to ensure that the final temperature is within the specified range of the power chip

Table 6-1 Power supply checklist

6.2. System startup circuit design

Check item	Recommended solution
Reset circuit	You are advised to connect the SYS-RST-IN pin
Micro SD circuit	SD card is convenient to burn procedures, it is recommended to keep

Table 6-2 System start up checklist

6.3. Peripheral circuits design

Category	Check box	Proposal
USB	Capacitance value of USB D+/D- signal ESD device	The capacitance value of ESD devices is recommended to be less than 2pF
	Whether the capacitor of the supply pin is added series resistance	The interface 5V capacitor requires a 1-ohm resistor in series to limit the voltage surge at the USB port
Ethernet (RGMII/ RMII)	PHY chip layout	Get as close to the core board layout as possible. Keep RGMII wiring as short as possible. RGMII sends and receives signals in separate groups, and Layout Layout within the same length +-25mil. There is no requirement between groups.
	PHY chip power supply	The PHY chip power supply is isolated by magnetic beads
	Clock signal source of the PHY chip	Use external active or passive crystal oscillator.
	Connection method of center tap on PHY side of network transformer	Depending on the type of PHY chip, it can be found in the chip manual. If the PHY is current-driven, the tap needs to be pulled up to the PHY supply voltage. If the PHY is voltage-driven, the tap does not need to be pulled up. If not found in the manual, use a reference circuit or reserved pull-up resistor
I2C	I2C pull-up resistance	The more the bus load devices, the smaller the resistance value should be, and the greater the resistance value should be. Recommended resistance value 1.5K/2.2K/4.7K;
	How many pull-up resistors are connected to each I2C signal cable	One or more can be used.
	What is the pull-up voltage	The pull-up resistor must be connected to the voltage matching the I/O level
MMC	Whether DATA and CMD signals are pulled up	Requires pull-up, 47K or 10K pull-up to 3.3V
CAN	Whether the CAN circuit needs to be isolated	Scenario Complex electrical environment high reliability requirements CAN interface cable length is long. If any of the preceding conditions are met, isolate the CAN converter and its power supply circuit

UART	UART signal connection	UART signal can not be directly connected to RS232\RS485 interface, the application of special conversion chip conversion can be connected to the corresponding interface

Table 6-3 peripheral circuits Check list

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory,

the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;

- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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