MYC-YT507H

Hardware Design Guide

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History

Version	Author	Participants	Date	Description
V1.0	Dana		20220415	Initial Version

Contents

1. Overview

This document is intended to assist hardware engineers in designing board-level circuits based on the MYC-YT507H core module. Please be fully aware of the document before you begin your design.The document contains common information such as design references, layout suggestions, and design checklists to assist hardware engineers.

Resources referenced in this document is from the MYIR Electronics website, included in the MYC-YT507H product information download page, you can download them in the following website: http://d.myirtech.com/MYD-YT507H/

In addition, MYIR Electronics the following resources to speed up your design:

- Core board / evaluation board product manual;
- Evaluation board principle graphical source file;
- Related device manuals.

1.1. Supported products

This document is suitable for all models of MYC-YT507H series core boards.

1.2. Disclaimer

- Some of reference designs in the document are based on MYIR electronic evaluation boards and cannot be guaranteed to be suitable for all application scenarios. If your product has special requirements for application scenarios or technical specifications, please adjust the design according to the actual situation.
- Reference design and layout in the document are recommended for reference only and do not necessarily contain all the matters needing attention. Please make adjustments according to the actual situation.
- MYIR shall not be liable for any form of technical endorsement or joint liability for any proposal contained in any document.

2. Power supply design

The design of the power supply system is of vital importance in the design of embedded products, engineers need to consider not only the basic electrical parameters of power itself, but also the stability of the power supply design, such as electromagnetic compatibility, temperature range, safety design, etc. Any neglect of these factors may lead to the entire system cannot work normally. Before starting to design a power supply system for a new product, the engineer should thoroughly understand the actual needs of the whole system, and comprehensively demonstrate a feasible design scheme based on cost and efficiency, so as to select an appropriate power supply method for the system.

2.1. Reference Design

The core board needs to provide 5V voltage for normal operation, and the average current is about 2A under full load condition. In order to ensure the stable and reliable operation of the system, it is recommended to use 3A power chip to supply power to the core board separately. It is not recommended to use this power chip to drive loads outside the core board, especially some high-power load devices.

The power supply chip can be LDO or DCDC. LDO has the advantages of simple use, low cost, small electromagnetic interference, but high calorific value. DCDC has the advantages of strong current output capacity, high conversion efficiency and low calorific value, but high electromagnetic interference. If the input voltage is close to 5V, use the LDO power chip. If the input voltage is different from 5V, use the DCDC power chip.

Core board 5V power supply, please increase the energy storage capacitor and decoupling capacitor appropriately near the core board 5V voltage input pin.

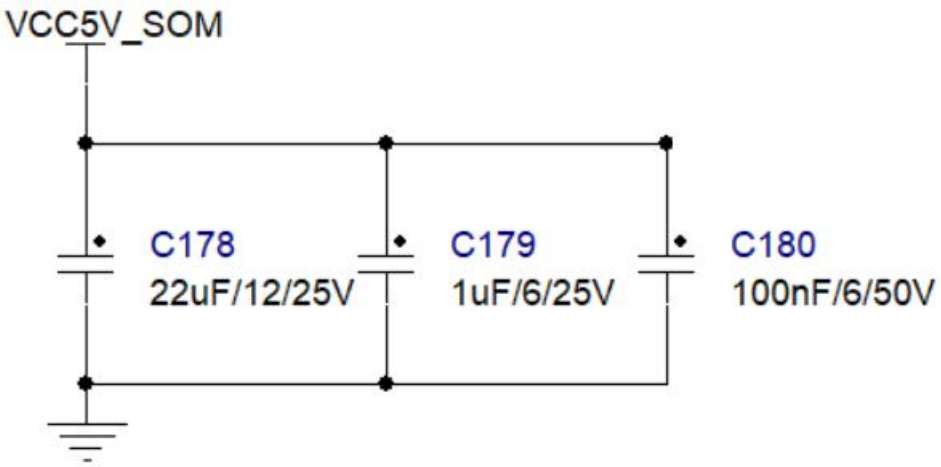

Figure 2-1 Core board 5V power supply

2.2. Power Protection

In order to ensure the reliability of the power supply system, it is not recommended to directly supply the external unopened input voltage directly to the input of the power supply chip, and the power supply can be processed after processing the power supply to improve the reliability of the input power supply. Safety and reduce electromagnetic interference. The bottom board input

power supply in the design is 12V, only as an example, the value of the input power should be determined according to your actual needs.

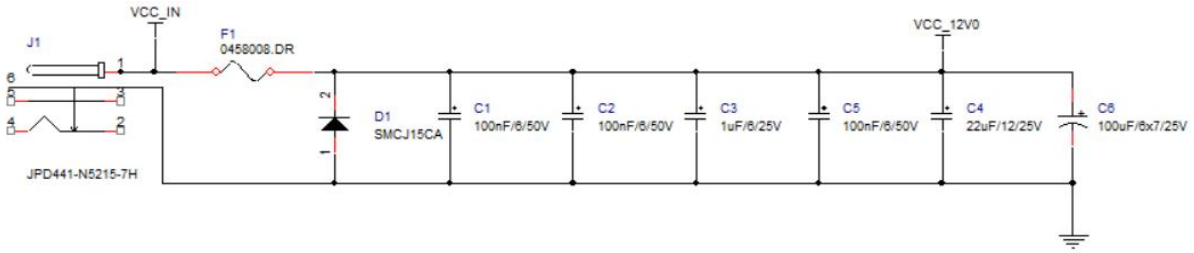

Figure 2-2 General power input circuit

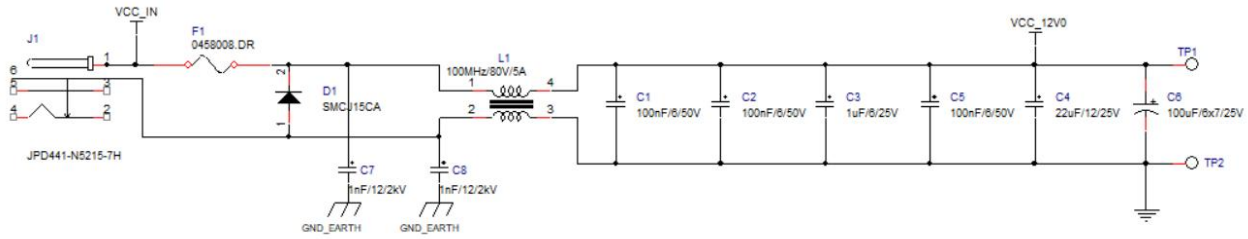

Figure 2-3 Power input circuit in noise-sensitive situations

2.3. Power Sequence

The MYC-YT507H core board and carrier board have power-on sequence requirements. Ensure that the core board is powered on first. It is recommended to enable power supply for 5V and 3.3V peripherals of the carrier board after initialization of the core board. Figure 2-4 shows the reference circuit.

The core board is reset at low level. When the reset signal rises, it indicates that the voltage inside the core board has been output stably, that is, the minimum system of the core board has been initialized when the reset signal rises (1.8V). When the reset signal rises, the MOS tube Q13 is turned on. Q13 turns on, Q14 turns on, and finally VDD_5V turns on.

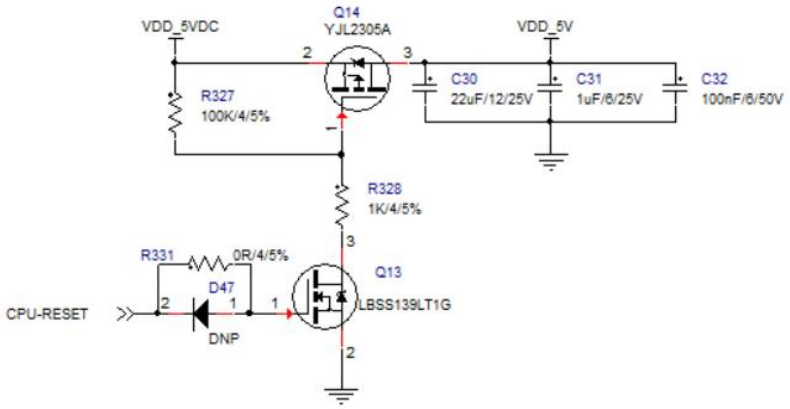

Figure 2-4 carrier board peripherals Power-on timing circuit

2.4. Layout Guidelines

- The distance between different power supply planes should be at least 20mil;
- Widen the width of the power line and ground wire as far as possible, to meet the required rated current value, the width of the feedback signal should not be too narrow, it is recommended to be more than 10mil;
- If DCDC is used, the signal line is not recommended in the area below the inductance;
- If DCDC is used, the current loop path should be as short as possible, and the inductor and capacitor should be placed as close to the chip as possible, i.e. the red and green paths in the figure below

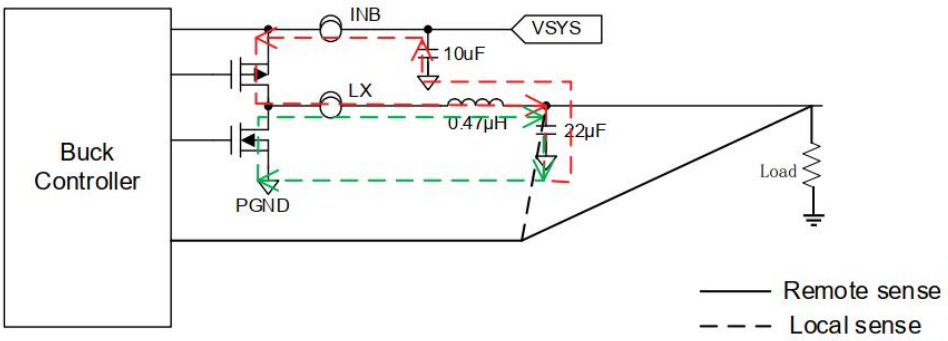

Figure 2-5 DCDC current backflow path

- If LDO is used, it is necessary to pay attention to the thermal resistance of the LDO chip, because the thermal resistance of the LDO chip is relatively high. It is recommended to add the grounding pad and make more ground vias on the grounding pad.
- Choose the capacitance of small ESR as far as possible
- The power chip with digital ground and analog ground shall be separated from each other and only connected at a single point at the input of the main power supply. The analog ground shall not be connected to the grounding pad.

3. Boot configure

After a power-on reset, the T507-H processor starts up by executing the program in the chip's internal BROM. BROM starts by reading the voltage level of the pin of BOOT SEL[4:0], and the levels of different combinations will enter the specific starting source.

BOOT SEL[4:0] pins do not add pull-up or pull-down design in the core board. But there is a 15K pull-up resistor inside the chip by default. MYC-YT507H core board start up mode mainly has eMMC start up, Micro SD card start up. See Table 3-1.

BOOT SEL[4:0]	Initial Boot Source	Description
11101	Micro SD-> eMMC	Boot from microSD card first, eMMC second
11110	Micro SD	Can only boot from Micro SD card

Table 3-1 Boot configure

3.1. Reference Design

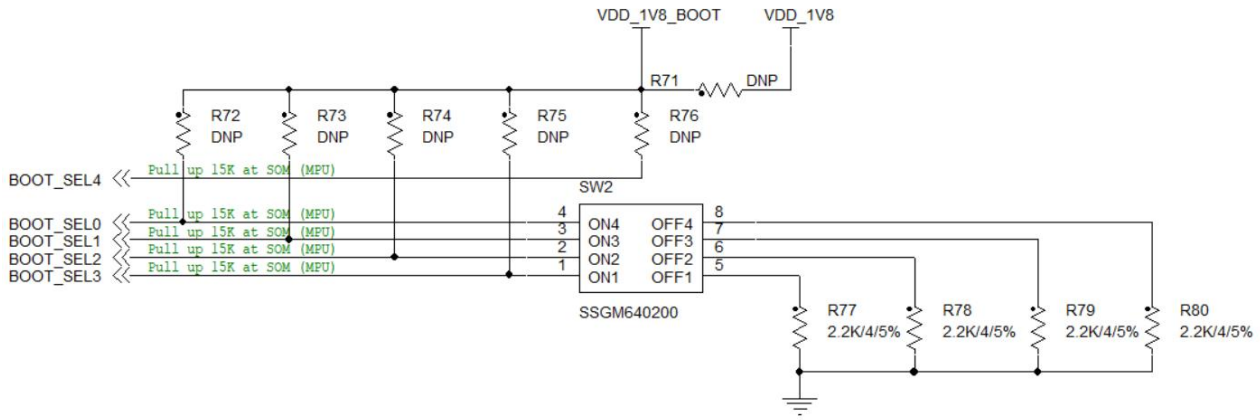

Figure 3-1 Boot configure reference design

4. Reset and key circuit design

MYC-YT507H core board provides 3 special pins, the function is Reset, ONOFF start off, FEL burning mirror. During design, it is suggested to reserve resistance and capacitor to form a simple RC filter to filter out the jitter interference when the key is pressed, while avoiding the interference introduced from the key to affect the reset signal.In the harsh electromagnetic environment, in order to eliminate the electrostatic interference from the key to ensure more reliable operation of the system, another ESD device can be connected in parallel. If there are more stringent requirements for chattering elimination, logic circuits such as RS flip-flops can be considered to build reset circuits.

Pin	Description
CPU-RESET (PIN 9)	POR power failure reset pin. RC reset circuit or hardware watchdog reset chip can be used to reset the output.
CPU-ONOFF (PIN 10)	Usually there is an external button. If you press the button for the first time, the system shuts down automatically. If you press the button again, the system starts up. When the system is in hibernation, press this key to wake up the system.
FEL (PIN L16)	The FEL signal is pulled up inside the CPU. After power-on, BROM detects the FEL level status. If a low level is detected, the T507-H enters download mode, and the system image can be downloaded through the USB port.

Figure 4-1 Reset and ONOFF pin function description

4.1. Reference Design

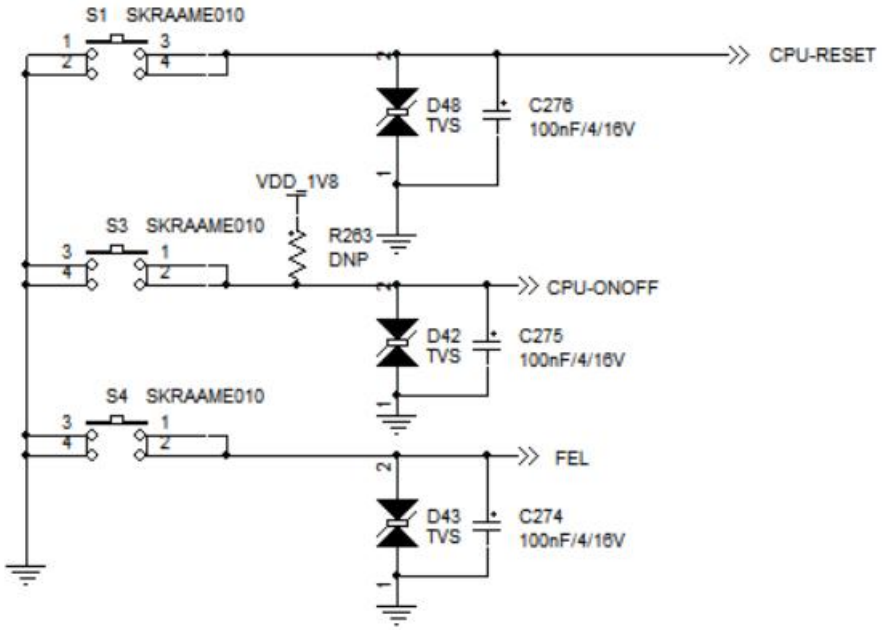

Figure 4-2 reset Reference design

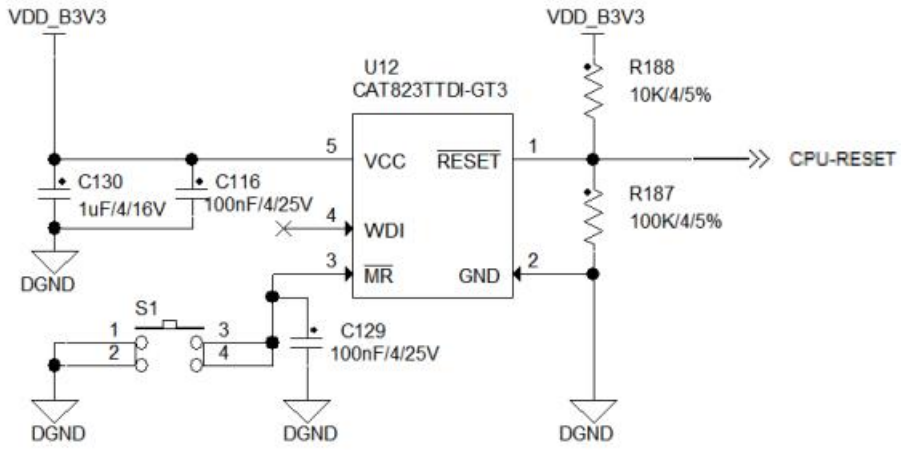

Figure 4-3 external hardware watchdog Resetting reference circuit

4.2. Layout Guidelines

- The width of reset signal line should not be too narrow, it is recommended not less than 8mil;
- Reset signal is sensitive signal, which is recommended to be surrounded by ground;
- Place TVS as close to the button as possible.

5. Interface circuit design

5.1. SMHC

SMHC stands for SD/MMC Host Controller. MYC-YT507H core board support leads to two SMHC interfaces. It is recommended to use the SMHC0 interface for Micro SD circuits and the SMHC1 to use peripherals with SDIO WIFI or other SDIO interfaces.

When designing the SD/SDIO/MMC card interface circuit, you only need to connect these interfaces to the SD/MMC card accordingly.Take the SMHC0 circuit as an example, see Figure 5-2.

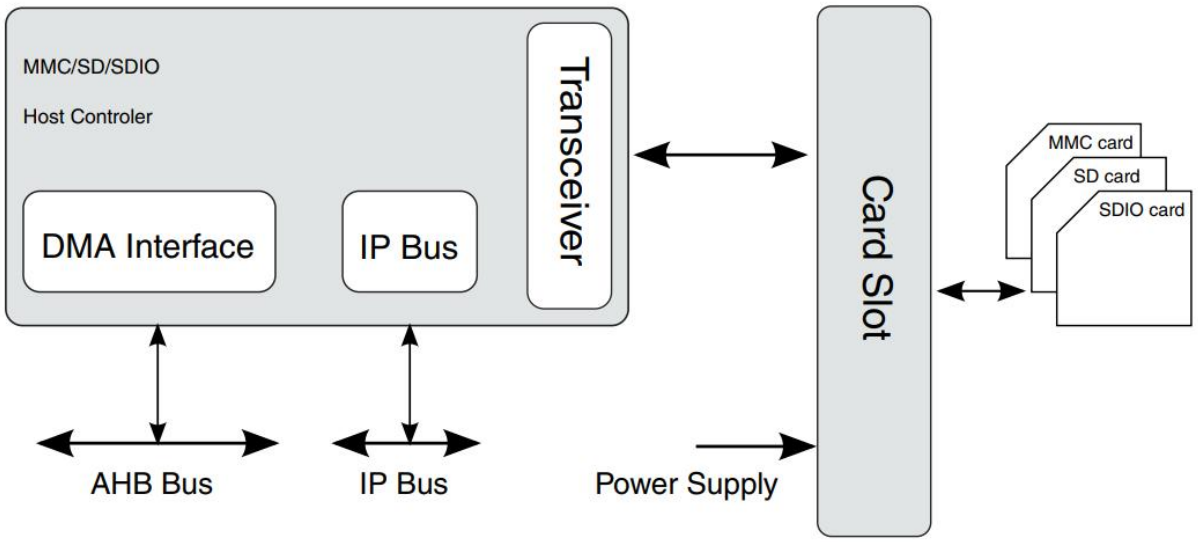

Figure 5-1 SD/SDIO/MMC interface

5.1.1. Reference design

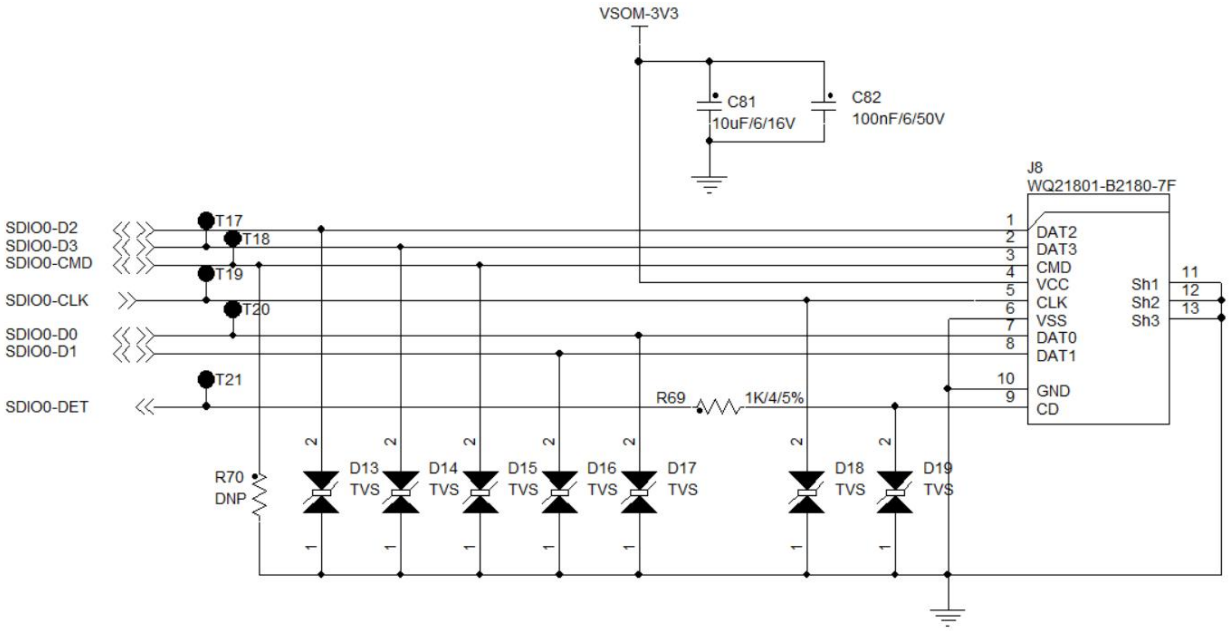

Figure 5-2 SD card Reference design

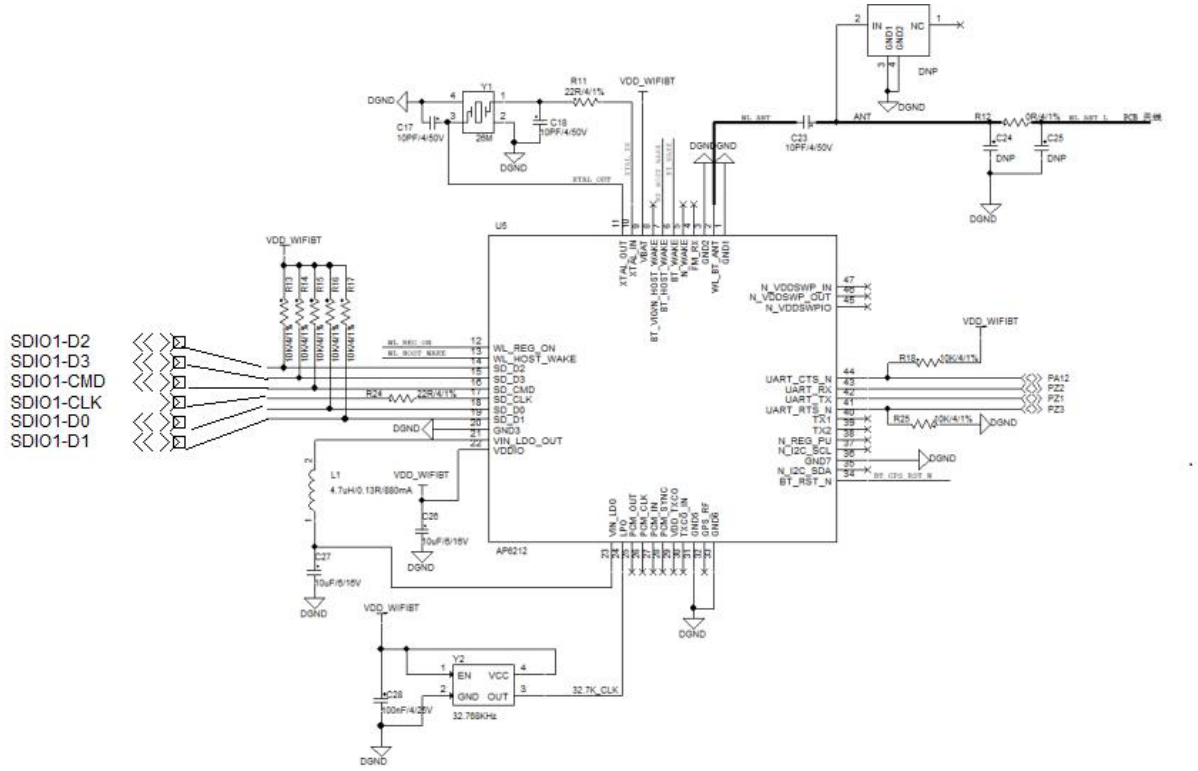

Figure 5-3 WIFI reference circuit

5.1.2. Layout guidelines

- Single-ended signal 50 Ω impedance;
- Trace match the data line and control line to be within 100 mils;
- SD1_CLK is recommended to be surrounded with ground. If not, ensure the distance between the clock signal and other signals follow 3W rule.
- Avoid placing other irrelevant devices and wiring in the U5 packaging area (including the BOTTOM layer);
- Y1 and Y2 clock signals are processed in the whole process, far away from other clocks and signals;
- Antenna signal WL_ANT, ANT and WIFI module are routed on the same layer to avoid layer change, and A GND back flow hole is added on both sides of the antenna routing, the distance between the GND holes is 50Ω, and the impedance is controlled. If 4 layers are designed, usually hollow out the second layer and use the third layer reference. The purpose of this is to increase the distance between the signal line and the reference plane so that the PCB line width of the signal line can be wider without affecting the 50Ω impedance control.
- The antenna seat element should be placed far away from the power supply and high frequency signal, and the distance from the antenna signal to the seat element should be as short as possible.

5.2. UART

The MYC-YT507H core board supports up to six serial ports. Due to the pin reuse of the chip, the core board only uses 4 channels of serial port by default, among which UART1 has flow control (RTS and CTS signal) function, and the other 3 channels of UART only have TXD and RXD by default.

In the reference design, UART signal can be used as follows: UART to RS232, UART to RS485, AND UART to USB.

When the UART is directly connected to the debugging serial port, the UART signal itself is TTL 3.3V level, so the UART to USB converter cable is needed to facilitate the connection with the PC. Figure 5-4 shows the common USB to UART TTL module.

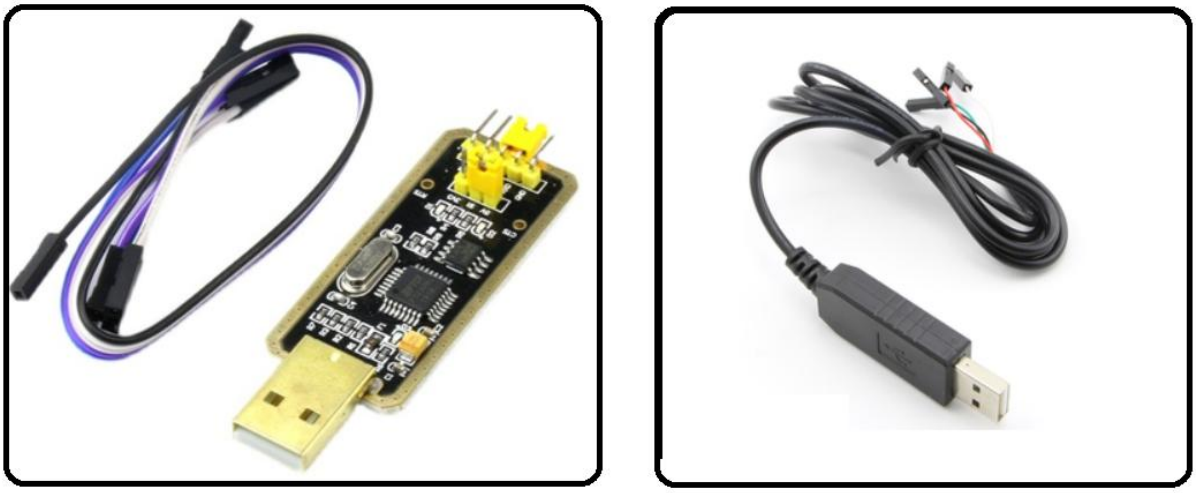

Figure 5-4 USB to UART TTL module

5.2.1. UART to RS232

In the reference circuit, The UART to RS232 chip is SP3232EY-L conversion chip of EXAR Company, and the signal isolation chip is ADUM1201BRZ chip of ADI Company. The converted RS232_TX/RX can be directly connected to the RS232 connector.

The 5V_ISO is produced by a special isolation power supply chip, and the B0505S-1WR2 isolation power supply of Jin Sheng yang is used in the reference circuit. Note That the power module has a minimum load value and a 10K resistance (R389) is required as the default load.

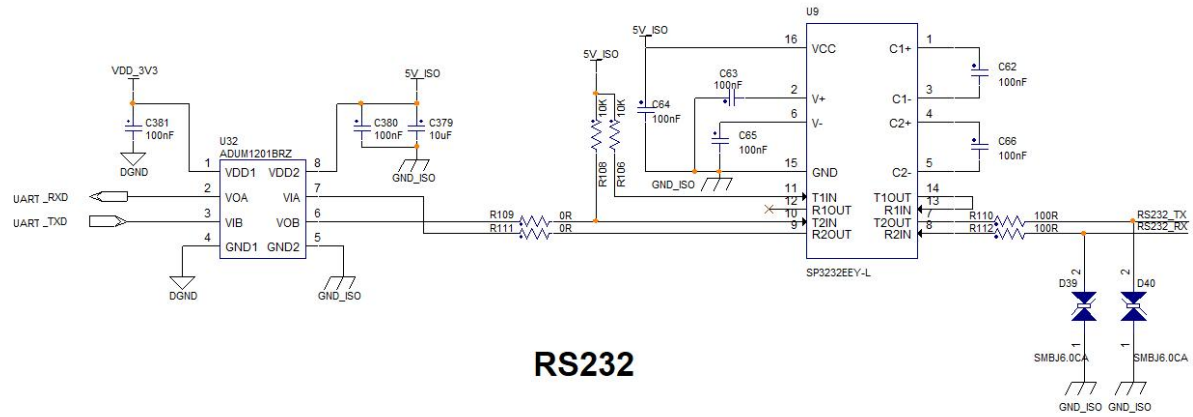

Figure 5-5 Isolate RS232 reference circuit

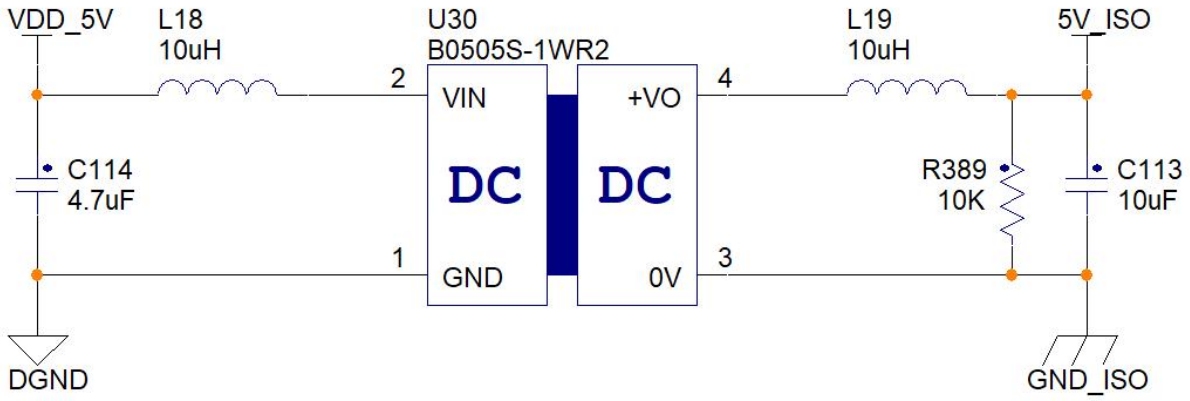

Figure 5-6 Isolating 5V power reference circuit

5.2.2. UART to RS485

Reference circuit UART to RS485 chip is TI ISO3802DW isolation conversion chip, the chip integrated signal isolation function, do not need to add additional signal isolation chip. The converted RS485_A/B can be directly connected to the RS485 connector.

The 5V_ISO is produced by a special isolation power supply chip, and the B0505S-1WR2 isolation power supply of Jin Shengyang is used in the reference circuit. Note that the power module has a minimum load value and a resistance of 10K (R389) is required as the default load.

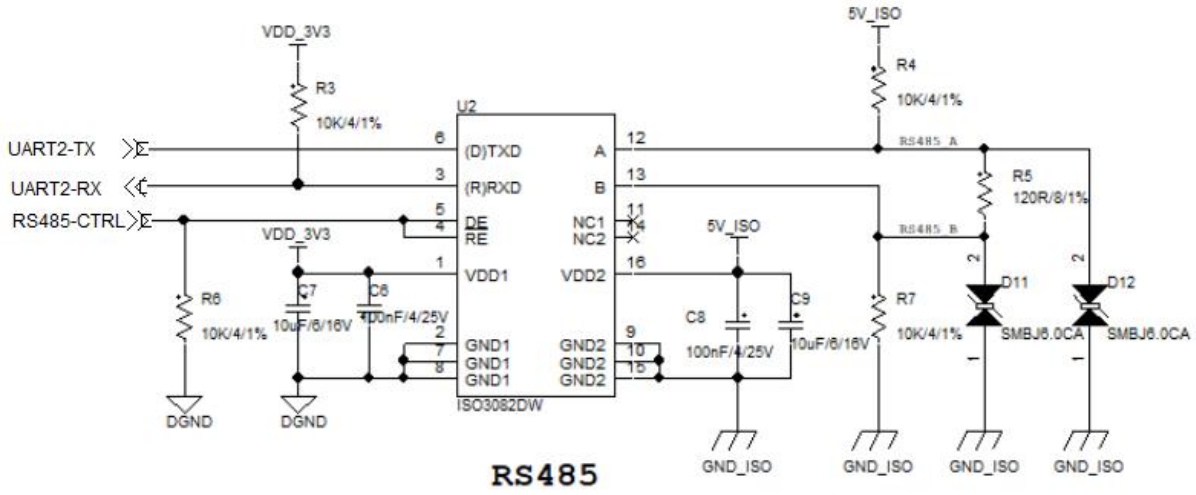

Figure 5-7 isolation rs485 reference circuit

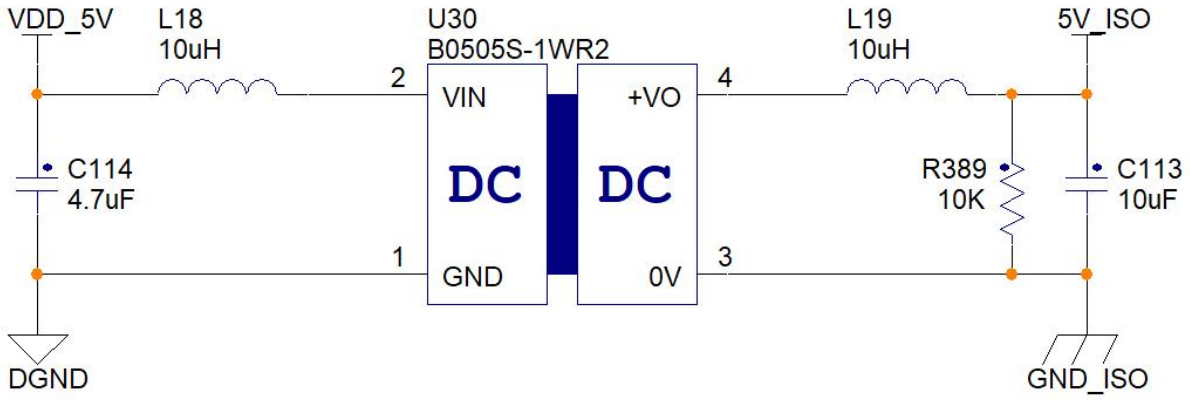

Figure 5-8 Isolating 5V power reference circuit

5.2.3. UART to USB

The reference circuit uses FT234xD-T conversion chip to convert UART debugging serial port signal to USB signal. USB interface adopts Type C USB connector, which is easy to plug and unplug.

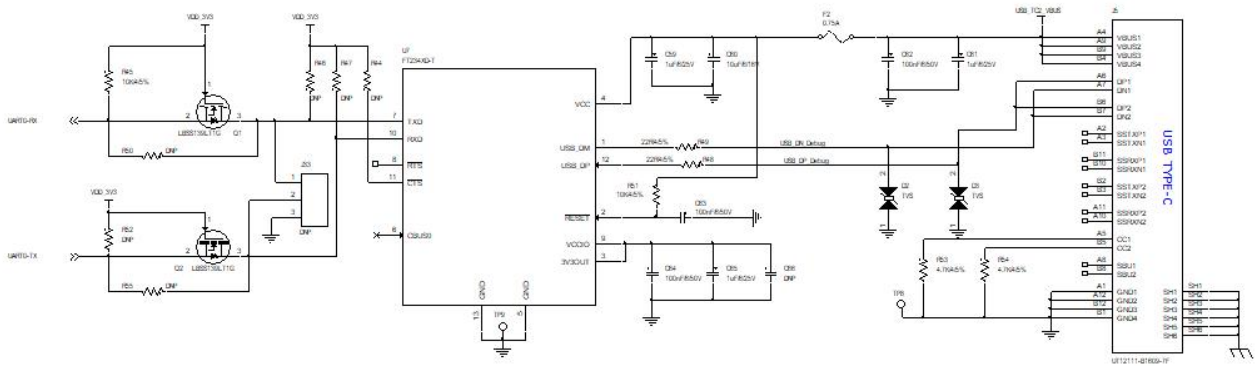

Figure 5-9 Debug serial port reference circuit

5.2.4. Layout Guidelines

- Keep sufficient spacing between signal and power plane before and after isolation;
- The 120 Ω resistor (R5) in the RS485 circuit is placed close to the conversion chip;
- TVS tube is placed close to connector;
- RS485 signal differential impedance 100 Ω, isometric control error ±300mil.
- USB signal differential impedance 90 Ω, isometric control error +-10mil.

5.3. USB

T507-H chip integrates USB2.0 Host controller and USB2.0 OTG controller. The Host controller can provide three USB2.0 Host interfaces, and the OTG controller provides one USB2.0 interface. MYC-YT507H core board brings it all out.

If users want to use THE OTG function of USB, they can use Micro USB port or Type C USB port.

It is recommended that a fuse be added between the power supply of the USB module and VDD_5V for protection. The reference circuit uses a 4-wire USB port. If a 5-wire USB port is used, the ID signal of the port needs to be connected to GND.

TVS tube and common-mode inductance are recommended for USB signal.

5.3.1. Reference Design

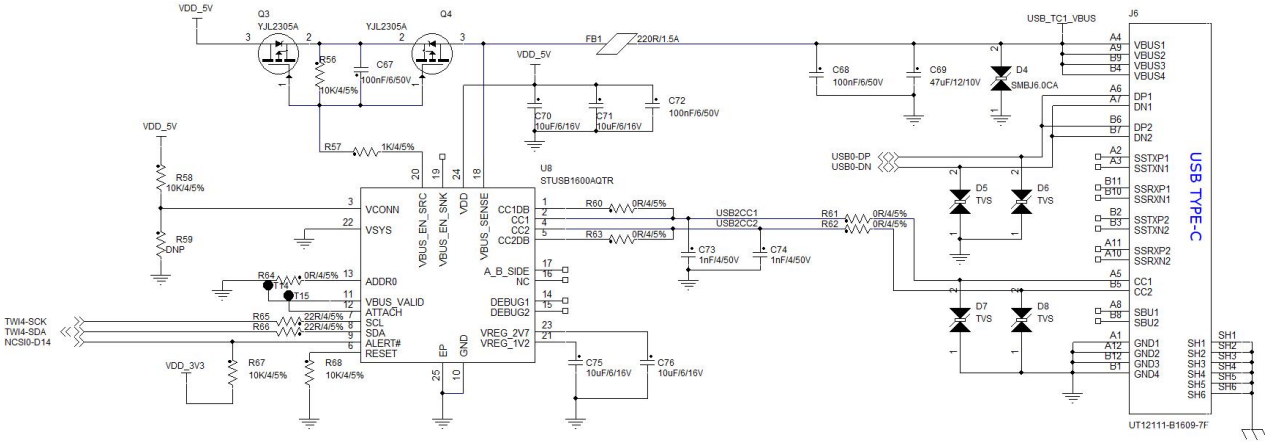

Figure 5-10 USB Type C Interface reference circuit

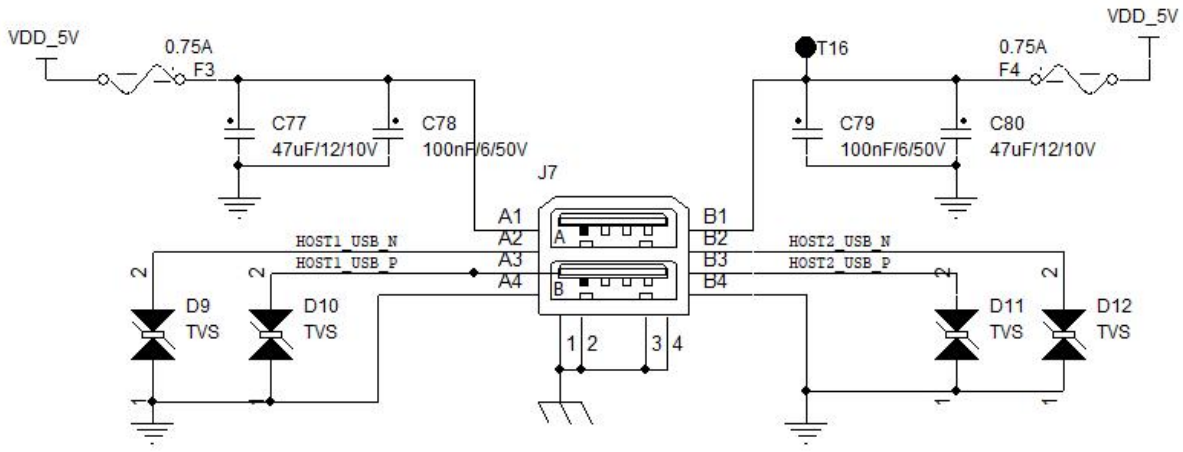

Figure 5-11 USB HOST Interface reference circuit

5.3.2. Layout Guidelines

- USB signal line does the equal length control, error range ± 10mil;

- Differential impedance of the USB signal is controlled by 90Ω;
- USB signal line as short as possible;
- USB signals as soon as possible, if the substation is changed, it is necessary to place the GND reflow via in the range of 200 mils from the changing layer.
- Ensure that the reference plane is continuous, the USB signal should not split;
- USB signal is recommended in TOP / BOTTOM layer;
- The USB signal is remote from other clocks and digital signals.

5.4. Ethernet

The MYC-YT507H core board provides two Ethernet MAC controllers. Contains one RMII interface and one RGMII interface (supporting RMII). Ethernet interface design requires proper network PHY chip.

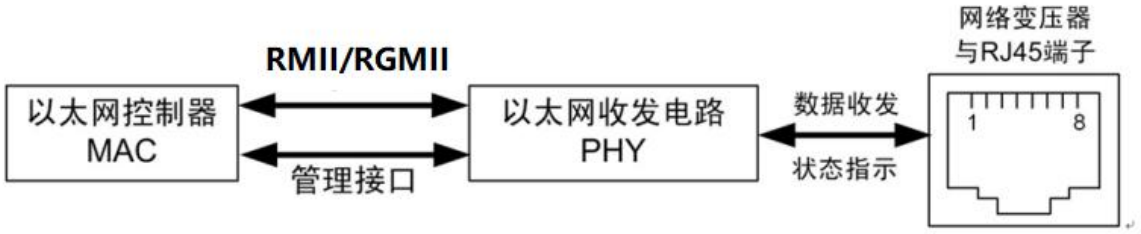

Figure 5-12 Ethernet reference circuit

5.4.1. Reference Design

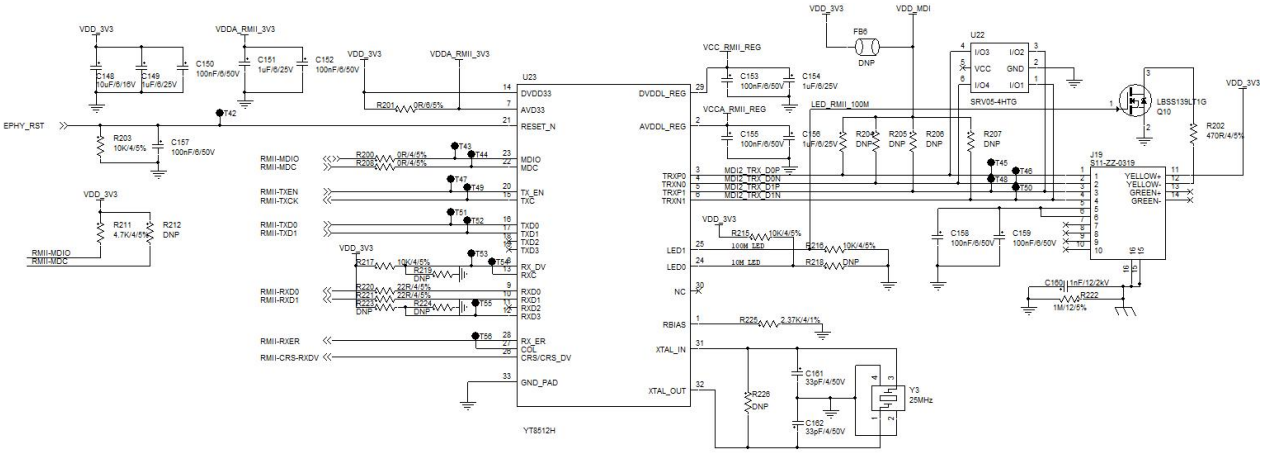

Figure 5-13 Ethernet RMII reference circuit

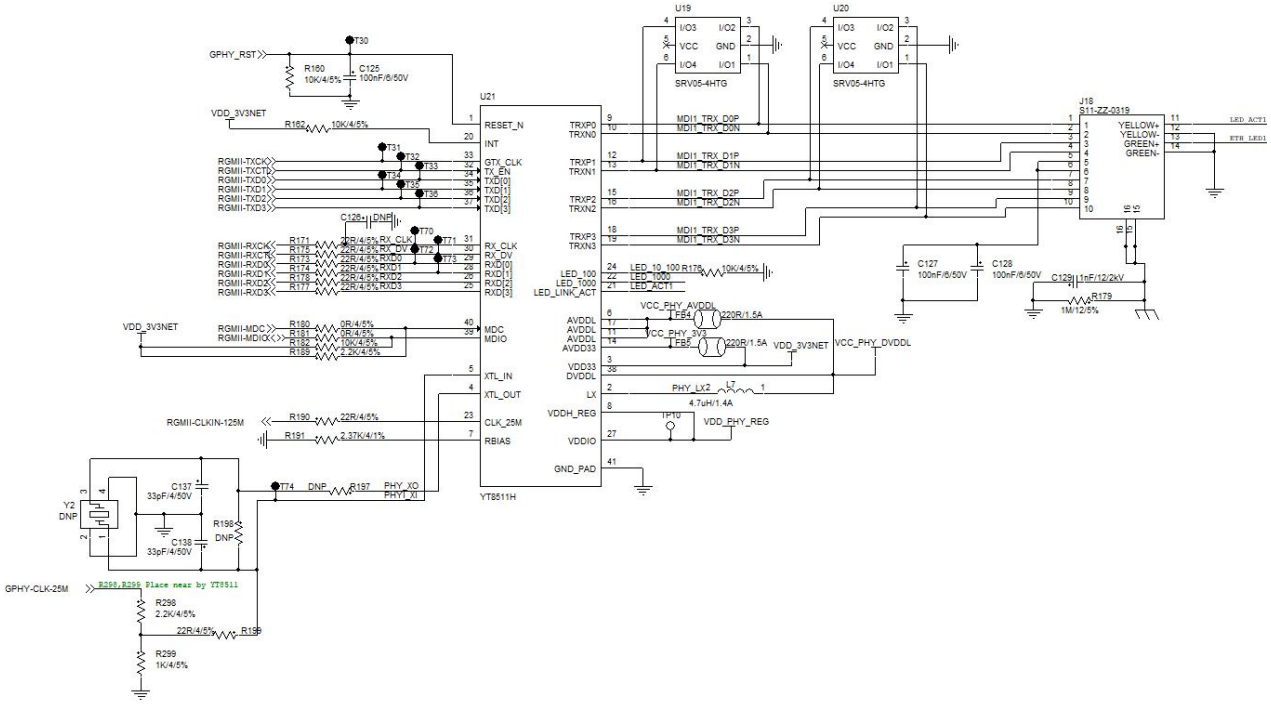

Figure 5-14 Ethernet RGMII reference circuit

5.4.2. Layout Guidelines

- RGMII signal isometric control, error ±25mil, line spacing more than 2W;
- Equal length control of RMII signal, error +-50mil, line spacing more than 2W;
- Network differential signal isometric control, difference internal error ±30mil, spacing of adjacent difference pairs more than 3W;
- PHY chip is placed close to the core plate and away from the network transformer;
- The network transformer is placed close to the RJ45 interface;
- The power pin decoupling capacitor of the PHY chip is placed close to the PHY chip;

5.5. MIPI CSI

MYC-YT507H provides a 4-lane MIPI CSI camera input interface. MIPI CSI interface supports 8M@30fps or 1080p@25fps. In order to improve the stability and reliability of the interface, ESD protection and common mode inductance filtering should also be considered when designing the interface circuit.

FPC interface is designed in the reference circuit, which can be used with the Module of MIPI CAMERA MY-CAM003M. The MYC-CAM003M module uses OV5640 chip and supports up to 5 megapixels. Please refer to the details http://www.myir-tech.com/product/my_cam003m.htm

5.5.1. Reference Design

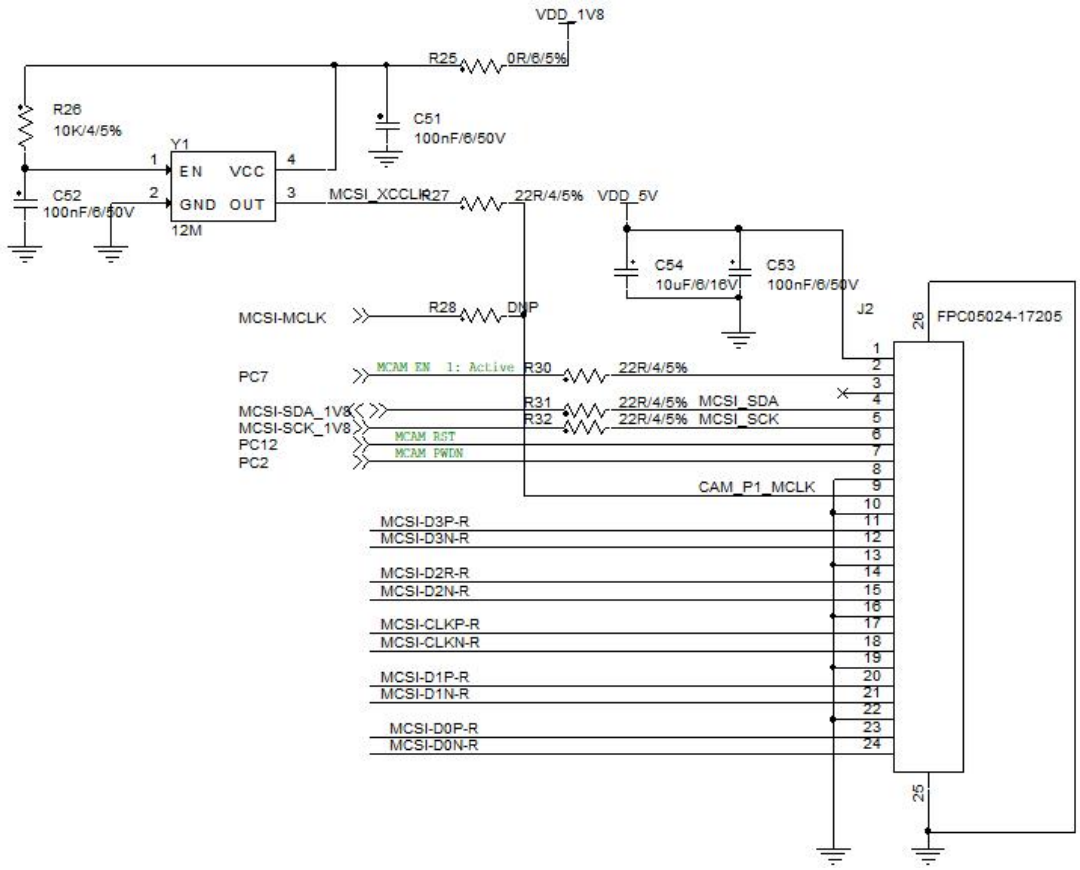

Figure 5-15 MIPI reference circuit

5.5.2. Layout Guidelines

- PN of each difference pair shall follow the isometric rule, the difference pair error control shall be +-5mil, and the difference impedance shall be 100 Euro. Less holes, in the hole change layer must ensure that P/N difference pair at the same time, and in the difference around the hole as much as possible
- Four data difference pairs and one clock difference pair need to make equal length between groups with the clock as reference. Isometric + - 50 mil.
- Data and clock difference pairs require complete reference ground planes.
- Isolate the area under the power supply, including the inner layer, and do not wire it.

5.6. Parallel CSI

The Parallel CSI interface of MYC-YT507H core board can support up to 5M@15fps or 1080p@30fps video input signal. Can support many video input interface such as BT656,BT601,BT1120, data bit width can support 8 bits, 16 bits, 32 bits. Due to pin multiplexing, the Parallel interface of MYC-YT507H core board chooses 8-bit data signal by default. It is recommended to use mile-Electronics my-CAM011B camera module with connection, please visit http://www.myir-tech.com/product/my_cam011b.htm to get detailed information about the module.

名称		参数
Active Array Size		1632 x 1212
Power Supply	Core	1.5VDC ± 5%
	Analog	2.6 ~ 3.0VDC
	I/O	1.7V to 3.0V
Power Requirements	Active	224 mW
	Standby	75 µA
Temperature Range	Operation	-20℃ to 70℃
	Stable Image	0℃ to 50℃
Output Formats (8-bit)		• YUV422/YCbCr422 • RGB565/555 • GRB422 • 8-/10-bit raw RGB data
Lens size		1/5"
Lens chief ray angle		25.7°
Maximum Image Transfer Rate	UXGA(1600x1200)	15 fps
	SVGA(800x600)	30 fps
	720p(1280x720)	30 fps
	1366x768	24 fps
Sensitivity		960mV/Lux -sec
S/N Ratio		36 dB
Dynamic Range		66 dB
Scan Mode		Progressive
Maximum Exposure Interval		1228 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		1.75 µm x 1.75 µm
Dark Current		4mV/s at 60℃
Well Capacity		6.3 Ke
Fixed Pattern Noise		1% of $V_{PEAK-TO-PEAK}$
Image Area		2856µm x 2121µm
Package Dimensions		4735µm x 4385µm

Figure 5-16 MY-CAM011B camera module specification

5.6.1. Reference Design

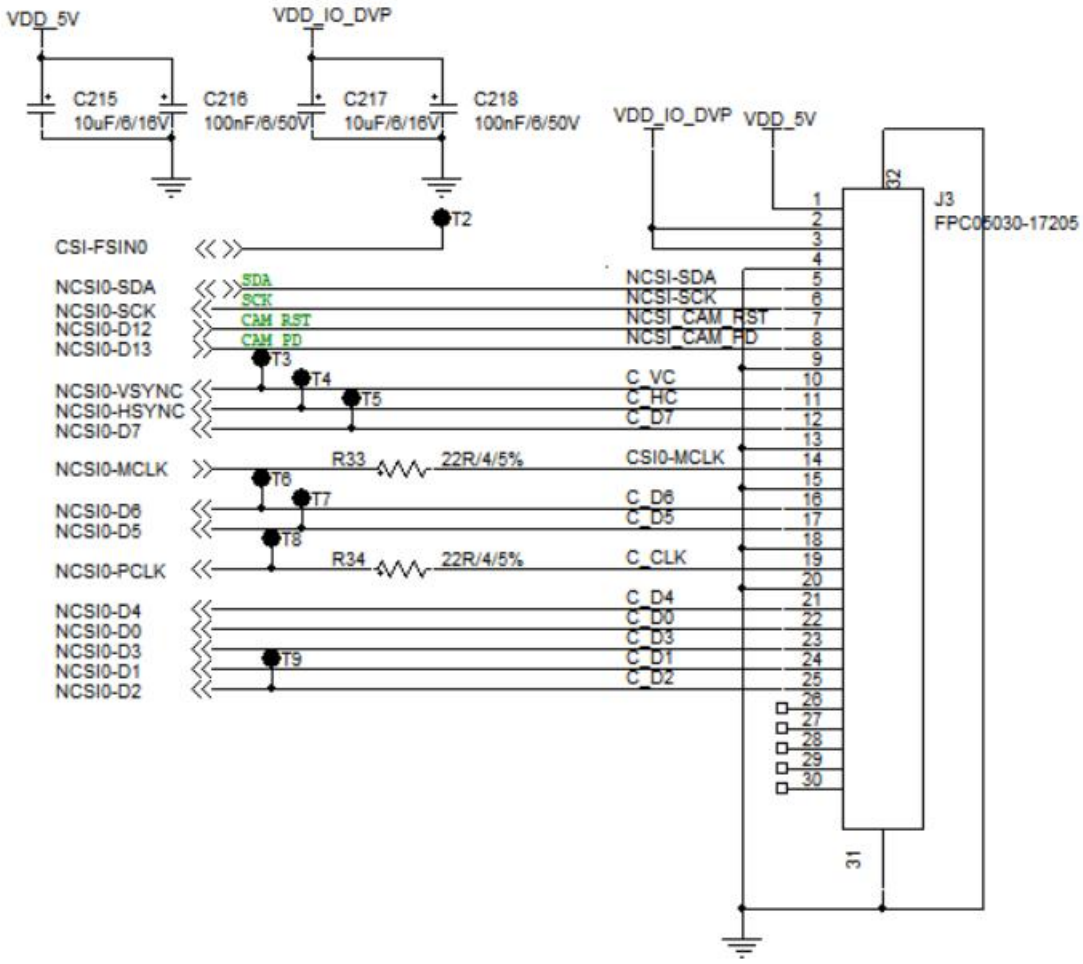

Figure 5-17 Parallel CSI Interface Reference Circuit

5.6.2. Layout guidelines

- Parallel CSI signal routing for equal length control, error range ± 100mil; It is recommended that the spacing between signal cables be at least 2W.

5.7. I2C

MYC-YT507H core board supports four I2C controllers and two modes, with the rate of 100Kbit/s in standard mode and 400Kbit/s in fast mode.

Several devices can be mounted on the same I2C main line. The following points should be paid attention to in schematic design:

- Check whether the device address under the same bus is in conflict;
- Ensure that each I2C bus has a pair of pull-up resistors, the resistance value is recommended to be 2.2K~10K, but do not repeatedly add;
- Check whether the level of I2C interface of the device is 3.3V. If not, add the level shift circuit.
- The number of devices under the same bus should not be too large, otherwise it is possible to exceed the load capacitance limit of 400 pF required by the I2C specification and affect the signal waveform.

5.7.1. Reference design

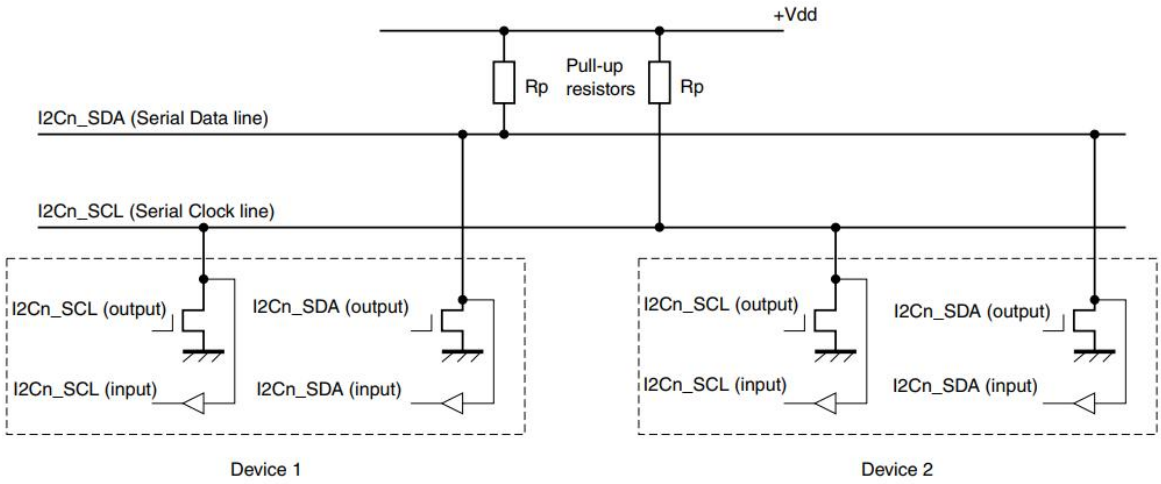

Figure 5-18 I2C reference design

5.7.2. Layout guidelines

- I2C signal line width should not be too narrow, it is recommended to be 6mil or above;
- The location of each I2C device should be planned before layout, if the length of I2C bus is too long will also cause the increase of the bus load capacitance;
- avoid the interference source line, adjacent the pitch of 10 mils.

5.8. LVDS

MYC-YT507H core board supports LVDS signal output. MYC-YT507H provides two Single Link LVDS interfaces to support 1366x768@60fps display output. In addition, two Single Link LVDS can form Dual Link LVDS to support higher display resolution 1920x1080@60fps.

MYIR officially designed a 7 inch LVDS MY-LVDS070C LCD module. The LCD module supports a resolution of 1024x600, please refer to the website for details http://www.myir-tech.com/product/my-lvds070c.htm

5.8.1. Reference design

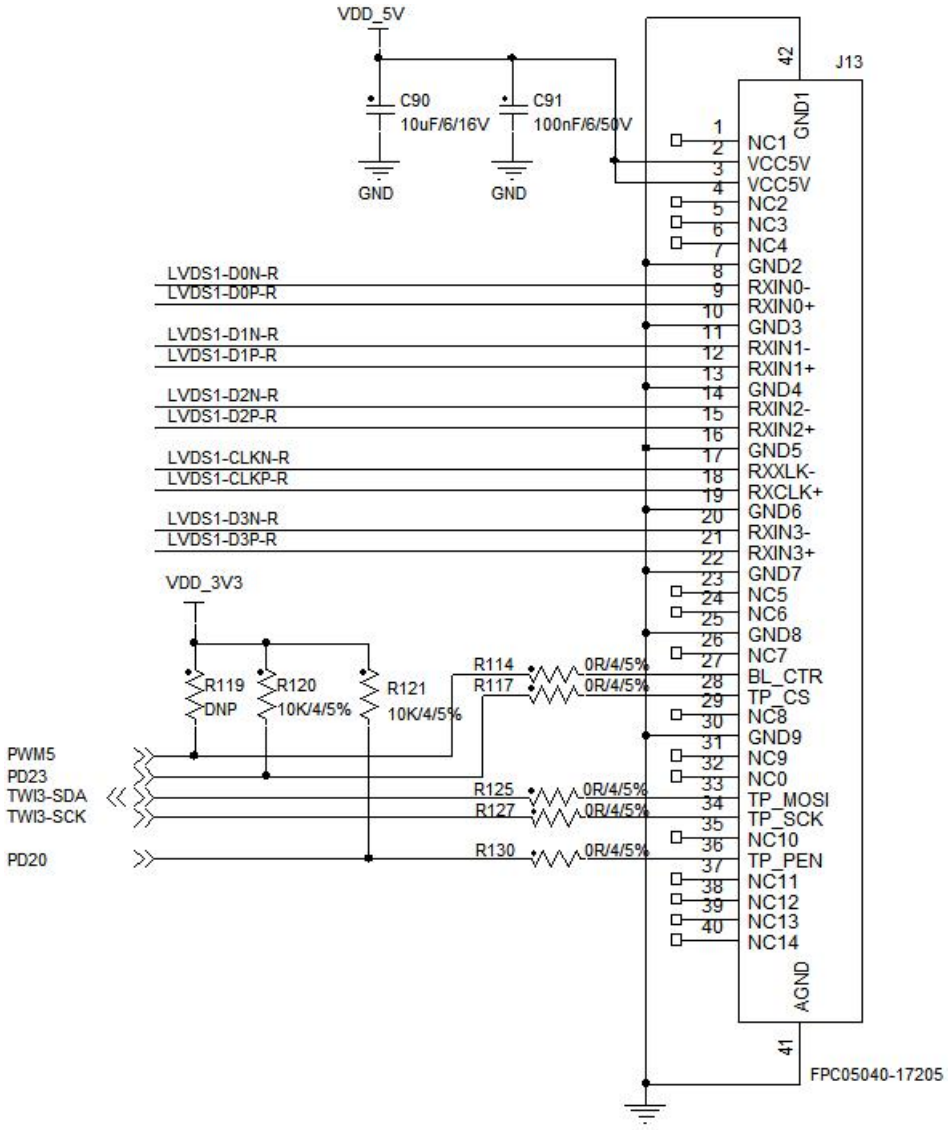

Figure 5-19 Single Link LVDS reference design

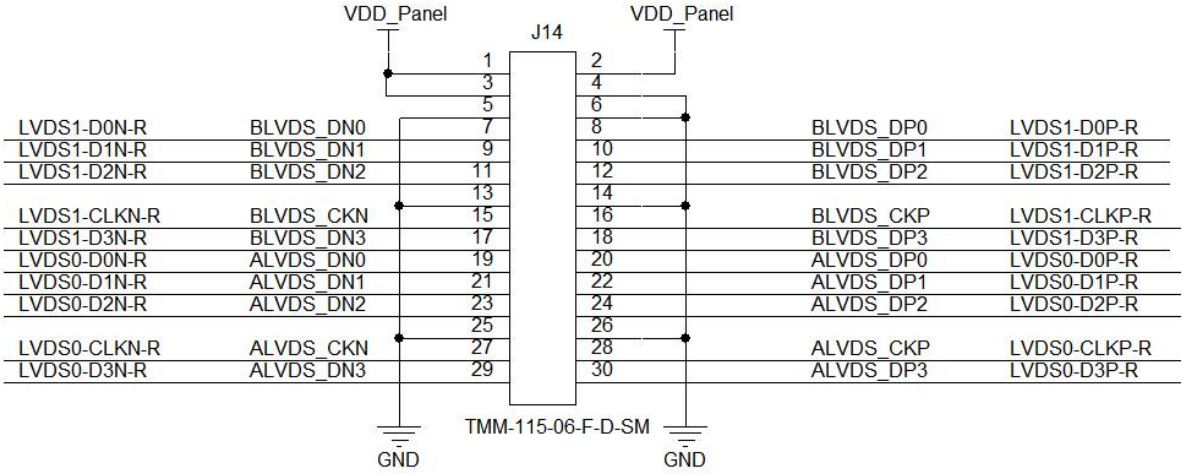

Figure 5-20 Dual Link LVDS reference design

5.8.2. Layout guidelines

- The difference pair of data and clock shall follow the rule of equal length and equal distance, the difference pair error control is +-5mil, and the difference impedance is 100 Ω. Less holes, in the hole change layer must ensure that P/N difference pair at the same time, and in the difference around the hole as much as possible
- Data difference pairs need to make equal length between groups with reference to clock difference pairs. Isometric + - 50 mil.
- The reference plane should be complete and the line should not be cut across.
- Use HD LVDS, power VDD_PANEL and GND cables are thick, and the recommended line width is more than 50mil, and place large capacity energy storage capacitor near the connector.

5.9. HDMI

MYC-YT507H core board native support one HDMI display output interface, the highest support 4K@60fps resolution.

5.9.1. Reference Design

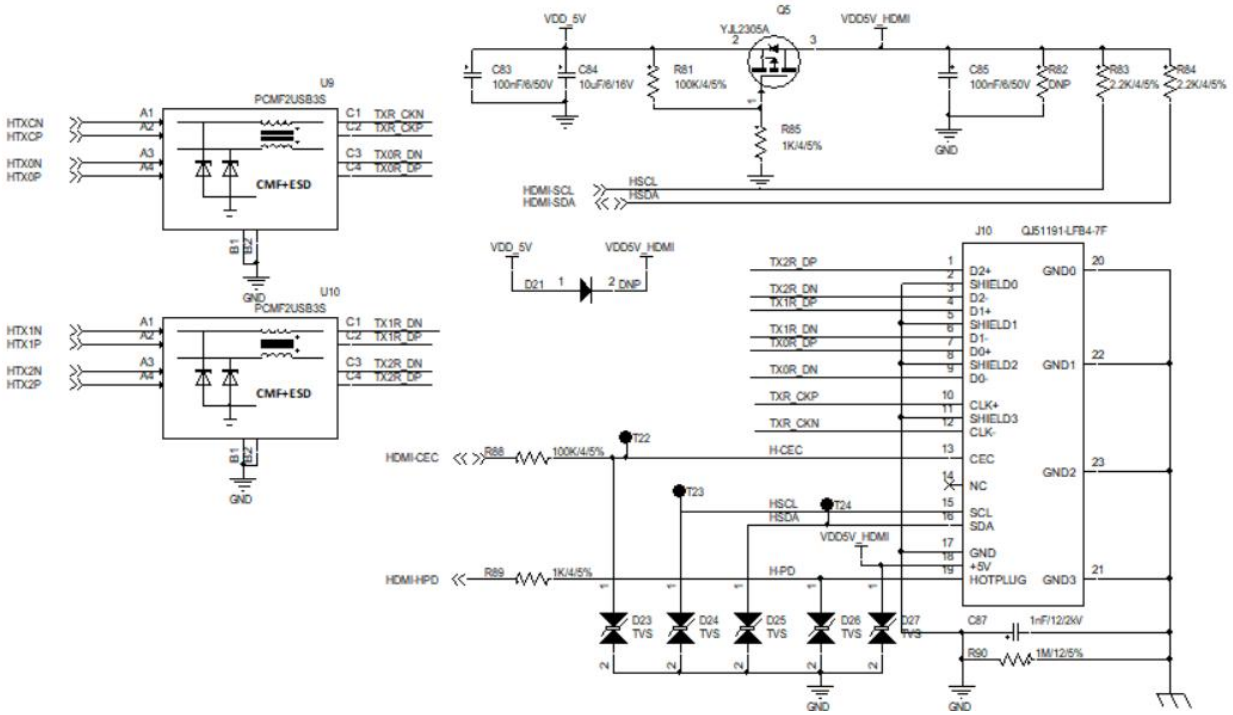

Figure 5-21 HDMI Display output reference circuit

5.9.2. Layout Guidelines

- Dynamic resistance (Rdy) of ESD device on HDMI differential line is less than 0.35Ω, parasitic capacitance is less than 0.35pF,
- The difference pair of data and clock shall follow the rule of equal length and equal distance, the difference pair error control is +-5mil, and the difference impedance is 100Ω. Less holes, in the hole change layer must ensure that P/N difference pair at the same time, and in the difference around the hole as much as possible
- Data difference pairs need to make equal length between groups with clock difference pairs as reference. Isometric + 25 mil.
- The reference plane should be complete and the line should not be cut across.

5.10. TV OUT

MYC-YT507H core board supports one TV-out (CVBS) output interface and supports NTSC and PAL modes.

5.10.1. Reference Design

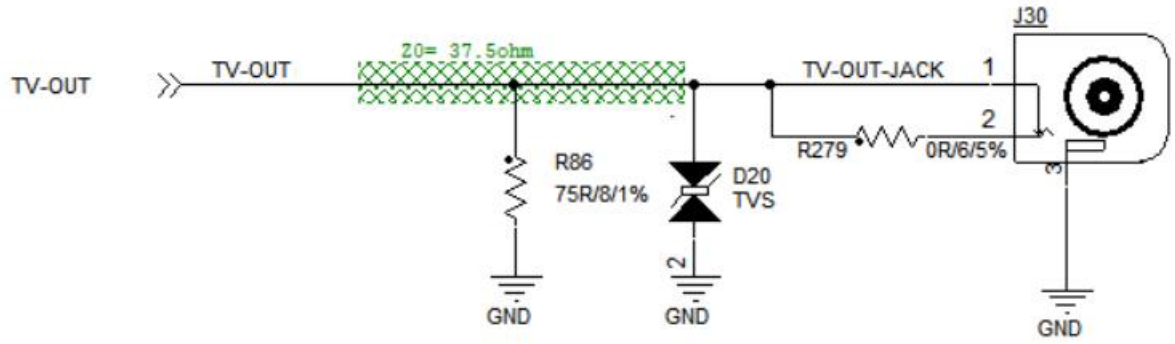

Figure 5-22 TV-OUT Display output reference circuit

5.10.2. Layout Guidelines

- TV-out wiring needs 75 Ω resistors in series and needs large package, because CVBS output current type, if the package is too small, it will heat up and burn OUT the resistance;
- TVS protection is recommended;
- 75 Ω, TVS and filter resistor capacitance are placed close to the seating element;
- TV-out signal line adopts 37.5 Ω impedance;
- TV-out signal cable shall be completely flat.

5.11. SPDIF-OUT

SPDIF, SONY / PHILIPS Digital Interface, SONY / PHILIPS Digital Audio Interface. SPDIF is a transmission specification for digital signals. It usually uses coaxial and optical fiber as transmission carriers. Coaxial uses electrical transmission and optical fiber uses optical transmission. In general, coaxial is recommended for short distance transmission. Optical fiber is recommended for long-distance transmission to avoid signal failure caused by distance. MYC-YT507H core board supports 1 channel SPDIF OUT digital audio output interface.

5.11.1. Reference Design

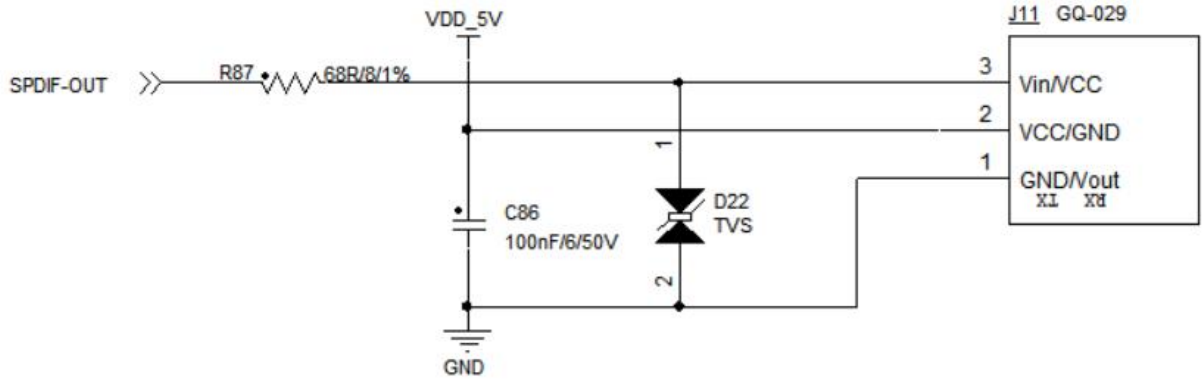

图 5-23 SPDIF-OUT output reference circuit

5.11.2. Layout Guidelines

- SPDIF-OUT signal routing shall adopt 50 ohm impedance control
- TVS protection is recommended;

5.12. AUDIO I2S

MYC-YT507H core board supports three I2S interfaces. In circuit design, I2S interface signal needs to be connected to the audio codec chip, and then connected to the headset and microphone.

In the reference circuit, the AUDIO_GND of the audio circuit is isolated from the DGND of the digital circuit by magnetic beads, and the capacitor of the power supply pin and the filter capacitor of the audio signal should also be connected to the AUDIO_GND.

5.12.1. Reference Design

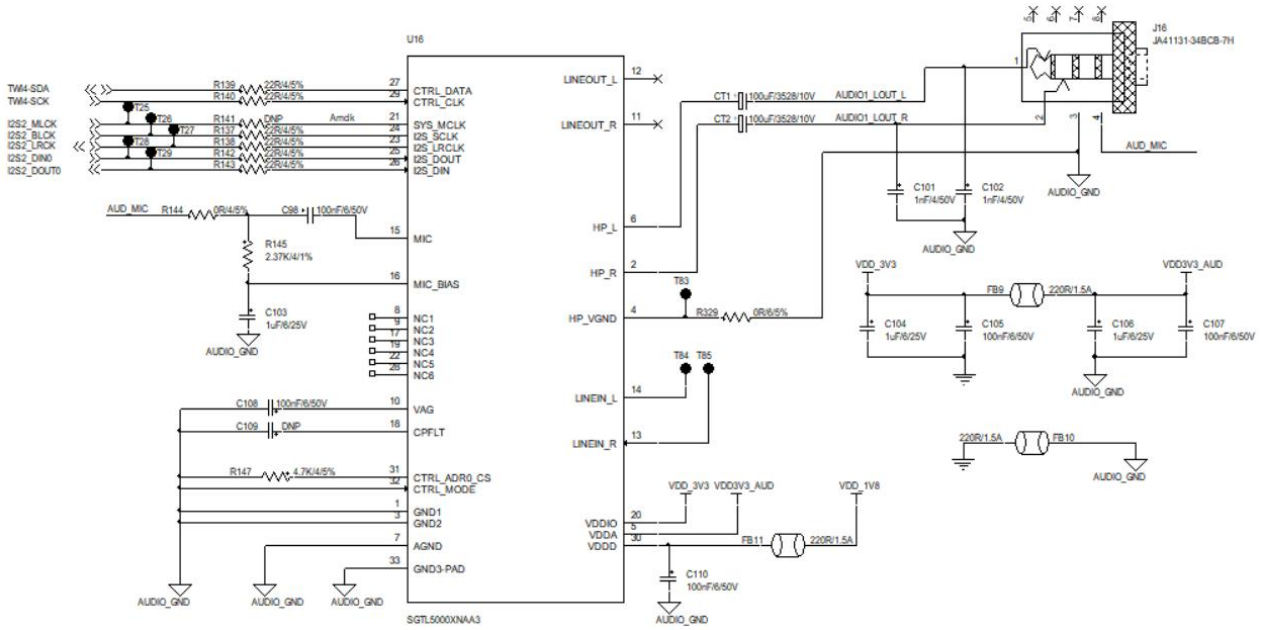

Figure 5-24 AUDIO Interface Reference Circuit

5.12.2. Layout Guidelines

- The isolation point (FB10) of AUDIO_GND and GND uses a star ground to close to the carrier board power input;
- The layout position of the audio circuit is remote from the source of interference, it is recommended to apply a region in the PCB to place analog circuitry separately;
- The audio chip is as close as possible to the headset and microphone jack, and the audio signal is as short as possible.

5.13. Line OUT

T507-H native supports line Out output. MYC-YT507H core board is directly connected to the line Out interface.

5.13.1. Reference Design

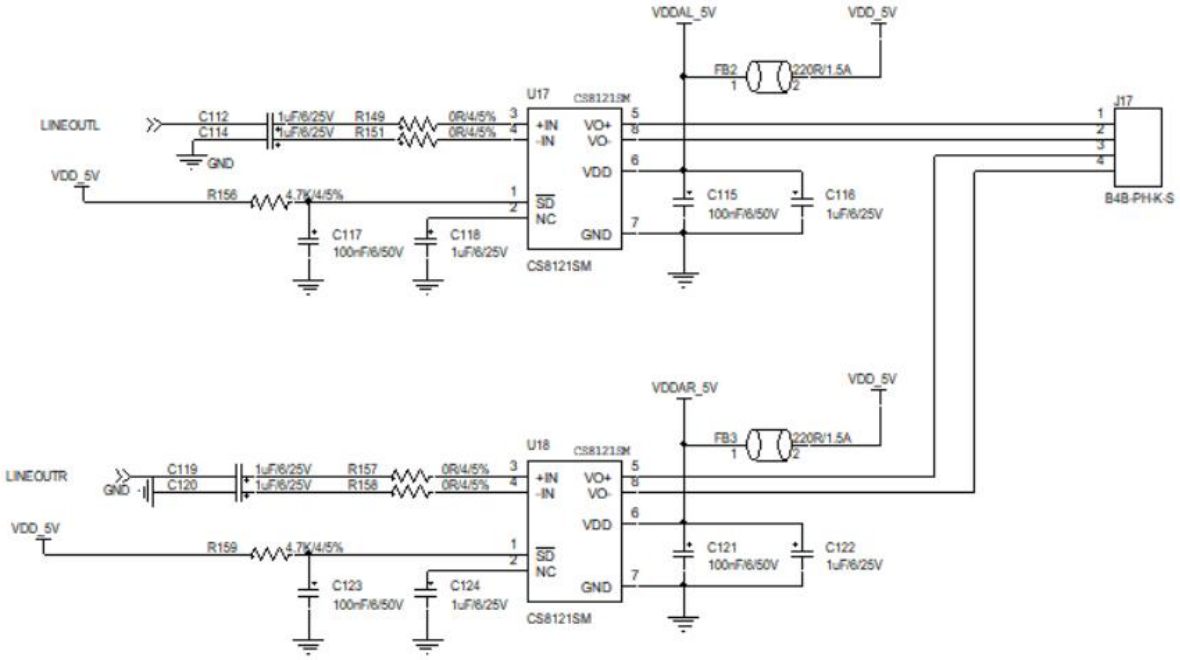

图 5-25 Line Out 接口参考电路

5.13.2. Layout Guidelines

- Line Out belongs to analog audio signal, and 10mil or above is recommended.
- Pay attention to the distinction between analog and digital ground.

5.14. ADC

MYC-YT507H core board supports GPADC and LRADC. GPADC has a 12-bit resolution, a maximum sampling rate of 1Mhz, and supports a signal input range of 0~1.8V. LRADC supports a maximum resolution of 6 bits and a sampling rate of 2Khz. The corresponding LRADC supports a range of 0~ 1.35v input signals.

The reference circuit is used to evaluate the input function of GPADC.

5.14.1. Reference Design

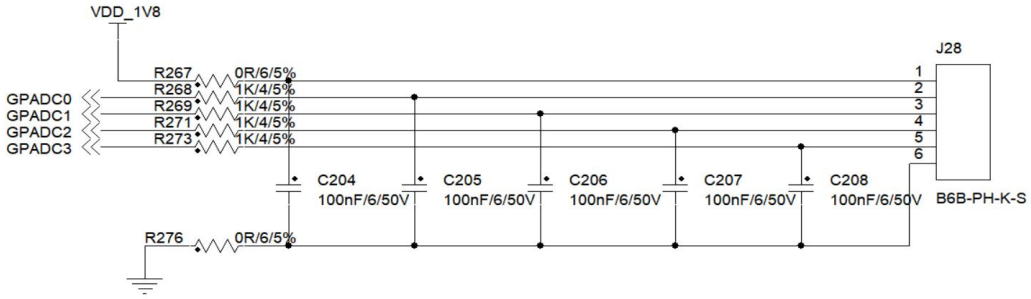

Figure 5-26 ADC Reference Circuit

5.14.2. Layout Guidelines

- Pay attention to the distinction between analog and digital ground.
- Protection of analog input channels

6. Design checklist

6.1. Power supply design

Check box	Proposal
1. core module supply voltage	The recommended value is 5V and the absolute value is 4.5V-5.5V
2. Decoupling capacitance	Use capacitors with 47uF and above value for core module power supply
3. IO level of carrier board peripherals	The IO voltage level of the peripheral should match the corresponding interface level of the core module
4. core module power sequence	It is recommended that the core module power start before the peripheral power
5. Power chip temperature rise	Confirm the thermal resistance of the power chip, and calculate the maximum temperature rise of the power chip based on the power consumption of the core module to ensure that the final temperature is within the specified range of the power chip

Table 6-1 Power supply checklist

6.2. system start up Check

Check box	Proposal
BOOT SEL[4:0] pin configuration	The configuration depends on the start up mode of the product
CPU-Reset	You can suspend or draw out the connection button.
Micro SD card circuit	Micro SD card for easy batch firing procedures. Recommend leaving
FEL download circuit	Download port: USB0

Table 6-2 System start up checklist

6.3. Peripheral circuits design

Category	Check box	Proposal
USB	Capacitance value of USB D+/D- signal ESD device	The capacitance value of ESD devices is recommended to be less than 2pF
	Whether the capacitor of the supply pin is added series resistance	The interface 5V capacitor requires a 1-ohm resistor in series to limit the voltage surge at the USB port
Ethernet (RGMII)	PHY chip layout	● Get as close to the core board layout as possible. Keep RGMII wiring as short as possible. ● RGMII sends and receives signals in separate groups, and Layout Layout within the same length +-25mil. There is no requirement between groups.
	PHY chip power supply	The PHY chip power supply is isolated by magnetic beads
	Clock signal source of the PHY chip	Use external active or passive crystal oscillator.
	Connection method of center tap on PHY side of network transformer	Depending on the type of PHY chip, it can be found in the chip manual. If the PHY is current-driven, the tap needs to be pulled up to the PHY supply voltage. If the PHY is voltage-driven, the tap does not need to be pulled up. If not found in the manual, use a reference circuit or reserved pull-up resistor
I2C	I2C pull-up resistance	The more the bus load devices, the smaller the resistance value should be, and the greater the resistance value should be. Recommended resistance value 1.5K/2.2K/4.7K;
	How many pull-up resistors are connected to each I2C signal cable	One or more can be used.
	What is the pull-up voltage	The pull-up resistor must be connected to the voltage matching the I/O level
MMC	Whether DATA and CMD signals are pulled up	Requires pull-up, 47K or 10K pull-up to 3.3V
CAN	Whether the CAN circuit needs to be isolated	Scenario Complex electrical environment high reliability requirements CAN interface cable length is long. If any of the preceding conditions are met, isolate the CAN converter and its power supply circuit
UART	UART signal connection	UART signal can not be directly connected to RS232\RS485 interface, the application of special conversion chip conversion can be connected to the corresponding interface

Table 6-3 peripheral circuits Check list

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;

- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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