



LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT9611

2-Port MIPI to HDMI1.4 Converter

Datasheet



1. Features

● Dual-Port MIPI® DSI/CSI Receiver

- Compliant with D-PHY1.2 ,DSI1.3/CSI-2 1.00 and DCS 1.02.00
- 1~2 Configurable Port
- 1 Clock Lane and 1~4 Configurable Data Lanes
- 80Mb/s~2Gb/s per Data Lane
- Data Port ,Data Lane and Polarity Swapping
- Internal Rterm Calibration with Less than 5% Error
- Programmable Equalization
- Burst Mode and Non-Burst Mode Supported
- Dual Port Odd-Even Mode and Left-Right Mode Supported
- Support up to 24-bit RGB and YUV Data Format

● HDMI1.4 Transmitter

- Compliant with HDMI1.4 and HDCP1.4
- Resolution Up to 4K 30Hz
- Programmable output swing and pre-emphasis
- Fully hardware-controlled or optional software-controlled HDCP operations
- Integrated CEC controller
- Integrated EDID shadow RAM and embedded EDID
- 5V tolerance DDC/HPD I/Os
- Both AC-coupling and DC-coupling Supported

● Miscellaneous

- 1.8V and 3.3V Power Supply
- Support 100KHz and 400KHz I2C Slave
- Support MIPI DCS Config

- Support up to 8-CH SPDIF/I2S Audio Input
- Temperature Range: -40°C ~ +85°C
- 64-pin QFN 7.5*7.5 package

2. General Description

The LT9611 MIPI® DSI/CSI to HDMI1.4 bridge features a dual-port MIPI® D-PHY receiver front-end configuration with 4 data lanes per port operating at 2Gbps per data lane and a maximum input bandwidth of 16Gbps.

The bridge provides a HDMI data output with optional S/PDIF or 8-channel I2S serial audio input. Its high fidelity 8-channel I2S can transmit stereo up to a 192kHz sampling rate. The S/PDIF can carry stereo LPCM audio or compressed audio, including Dolby® Digital and DTS®.

The LT9611 is fabricated in advanced CMOS process and implemented in a small outline 7.5mmx7.5mm QFN64 package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Personal media players
- Gaming
- Camera systems

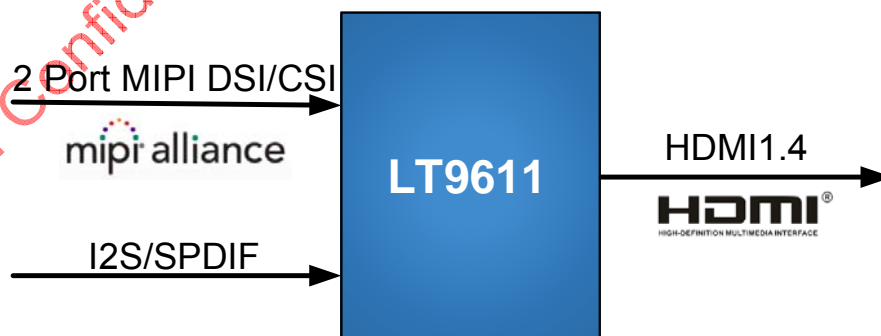


Figure 3.1 LT9611 Typical Application Diagram

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4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT9611	-40°C to +85°C	QFN64 (7.5*7.5)	Tray

5. IC Version Information

Table 5.1 IC Version Information

Version	Mark
LT9611 U1	GT231310U1C
LT9611 U2	GT231726U1C
	GTXXXXXXU2C

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6. Revision History

Version	Owner	Content	Date
R1.0	Y C	Initial datasheet creation	04/05/2017
R1.1	G W	Change MIPI RX description	08/04/2017
R1.2	Y C	1. Change MIPI RX supported data type description 2. Add power consumption information	09/19/2017
R1.3	Y C	Add ESD information	10/10/2017
R1.4	Y C	Add IC version information	12/13/2017
R1.5	Y C	Delete Embeded EEPROM description	02/27/2018

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7. Pinning Information

7.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with $100\Omega \pm 10\%$ differential impedance. Maximum trace length mismatch should be less than 2.5mil and keep total trace length to a minimum for all differential traces. It is highly recommended to route differential pairs on top or bottom layer with no vias on signal path.

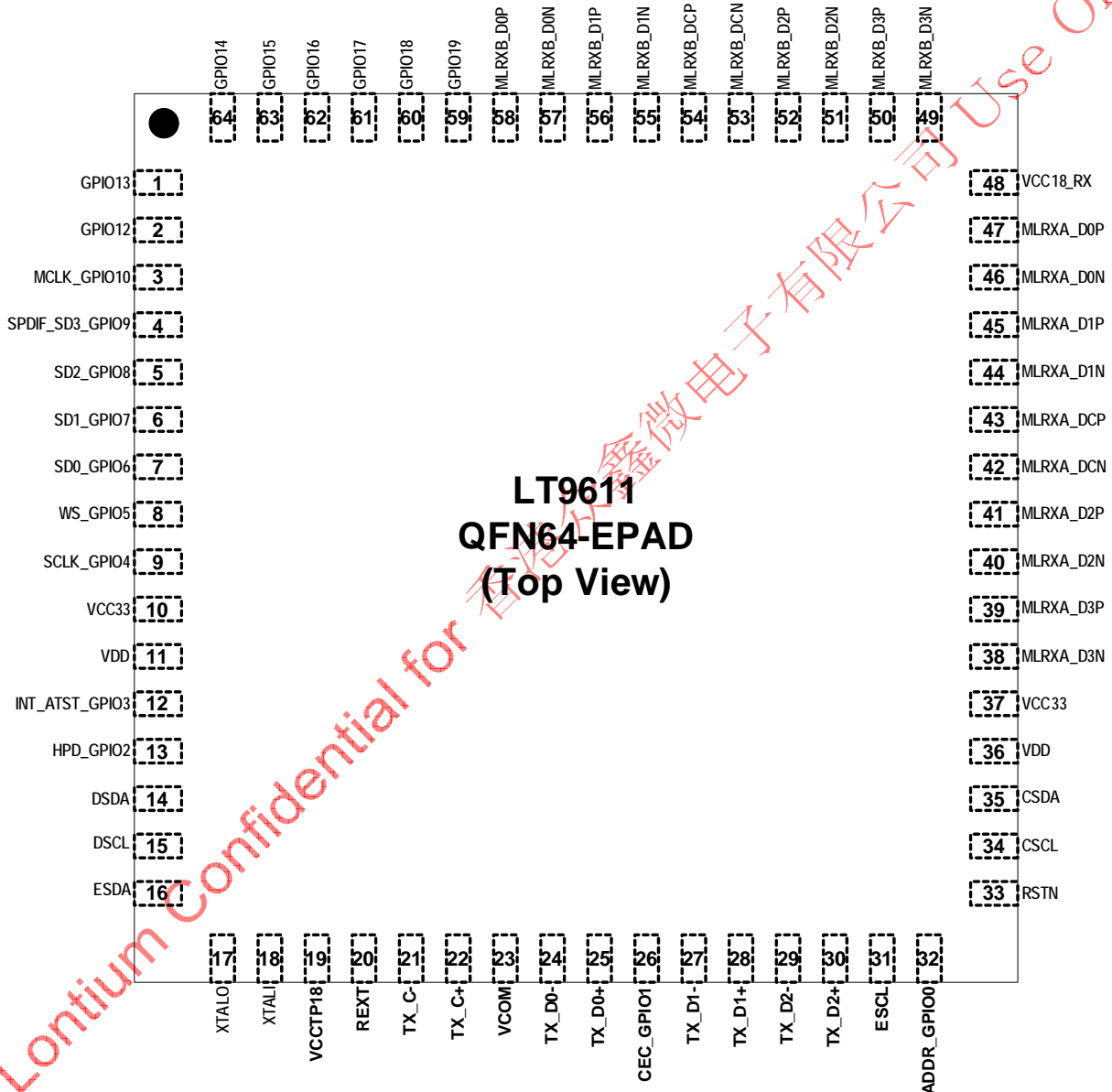


Figure 7.1.1 Pin Configuration

To minimize the power supply noise floor, at least one $0.1\mu\text{F}$ and one $0.01\mu\text{F}$ decoupling capacitor is recommended to be installed near all the LT9611 1.8V/3.3V power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power input pins must be minimized.

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7.2 Pin Description

Table 7.2.1 Pin Description

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
38,39	MLRXA_D3N MLRXA_D3P	Analog	I	MIPI Port-A RX Lane-3 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
40,41	MLRXA_D2N MLRXA_D2P	Analog	I	MIPI Port-A RX Lane-2 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
42,43	MLRXA_DCN MLRXA_DCP	Analog	I	MIPI Port-A RX Lane-C Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
44,45	MLRXA_D1N MLRXA_D1P	Analog	I	MIPI Port-A RX Lane-1 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
46,47	MLRXA_D0N MLRXA_D0P	Analog	I/O	MIPI Port-A RX Lane-0 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
49,50	MLRXB_D3N MLRXB_D3P	Analog	I	MIPI Port-B RX Lane-3 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
51,52	MLRXB_D2N MLRXB_D2P	Analog	I	MIPI Port-B RX Lane-2 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
53,54	MLRXB_DCN MLRXB_DCP	Analog	I	MIPI Port-B RX Lane-C Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
55,56	MLRXB_D1N MLRXB_D1P	Analog	I	MIPI Port-B RX Lane-1 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
57,58	MLRXB_D0N MLRXB_D0P	Analog	I/O	MIPI Port-B RX Lane-0 Input MIPI input of polarity swappable differential pairs up to 2.0Gb/s.
21,22	TX_C- TX_C+	Analog	O	HDMI TX Lane-C Output HDMI output of differential pairs up to 340MHz.
24,25	TX_D0- TX_D0+	Analog	O	HDMI TX Lane-0 Output HDMI output of differential pairs up to 3.4Gb/s.
27,28	TX_D1- TX_D1+	Analog	O	HDMI TX Lane-1 Output HDMI output of differential pairs up to 3.4Gb/s.
29,30	TX_D2- TX_D2+	Analog	O	HDMI TX Lane-2 Output HDMI output of differential pairs up to 3.4Gb/s.
3,4,5,6,7,8,9	MCLK_GPIO10 SPDFI_SD3_G PIO9 SD2_GPIO8 SD1_GPIO7 SD0_GPIO6 WS_GPIO5 SCLK_GPIO4	LVTTTL	I/O	AUDIO SPDIF/I2S Input In default, these pins are configured as audio input. It can be configured as CSI RAW Data parallel output.

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PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
12	INT_ATST_GPIO3	LVTTL OPD	O	Interrupt Request Output In default, this pin is configured as interrupt request output. It can be configured as analog test signal output and debug gpio output.
13	HDP_GPIO2	LVTTL OPD Schmitt	I/O	HDMI HPD 5V Tolerant Input HDMITX hot-plug detect input. 5V tolerance. It can be configured as gpio output for digital test.
14,15	DSDA DSCL	Schmitt OPD	I/O	HDMI DDC Communication 5V Tolerant Input/Output HDMI DDC serial data input/output and clock output. 5V tolerance.
16,31	ESDA ESCL	Schmitt OPD	I/O	EEPROM I2C Input/Output This pair is dedicated to loading HDCP Key Sets.
17,18	XTALO XTALI	Analog	O/I	27M Crystal oscillator interface
20	REXT	Analog	I/O	BandGap External Resistor External 2K(1%) resistor for setting internal reference current.
23	VCOM	Analog	I/O	HDMI TX AC-couple mode biasing common ground When use DC-couple mode, just let it floating. When use AC-couple mode, just follow the reference design.
26	CEC_GPIO1	LVTTL OPD Schmitt	I/O	HDMI CEC In/Out Open-Drain Output and Schmitt Trigger Input. It can be configured as gpio output for digital test.
32	ADDR_GPIO0	Analog LVTTL	I/O	I2C Device Address Select In default, this pin is configured as I2C address select. It can be configured as gpio output for digital test.
33	RST_N	Schmitt	I	Hardware Reset Input Chip reset signal. Active LOW.
34,35	CSCL CSDA	Schmitt OPD	I/O	I2C Serial Clk and Data In/Out It serves as 3.3V/1.8V serial port clk and data IO slave for register access.
48	VCC18_RX	PWR	I/O	1.8V MIPI RXPHY Power 1.8V power for MIPI RXPHY.
19	VCC18_TX	PWR	I/O	1.8V HDMI TXPHY and TXPLL Power 1.8V power for HDMI TXPHY and TXPLL.
11,36	VDD	PWR	I/O	1.8V Power 1.8V power for digital block.
10,37	VCC33	PWR	I/O	3.3V IO/ESD Power 3.3V power for IO/ESD.
1,2,59,60,61 62,63,64	GPIO13 GPIO12 GPIO19 GPIO18 GPIO17 GPIO16 GPIO15 GPIO14	LVTTL	I/O	GPIO for CSI RAW Data it can be configured as CSI RAW Data parallel output.
65	#EPAD	—	—	EPAD Connect to VSS on PCB.

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8. Function Description

8.1 Function Block Diagram

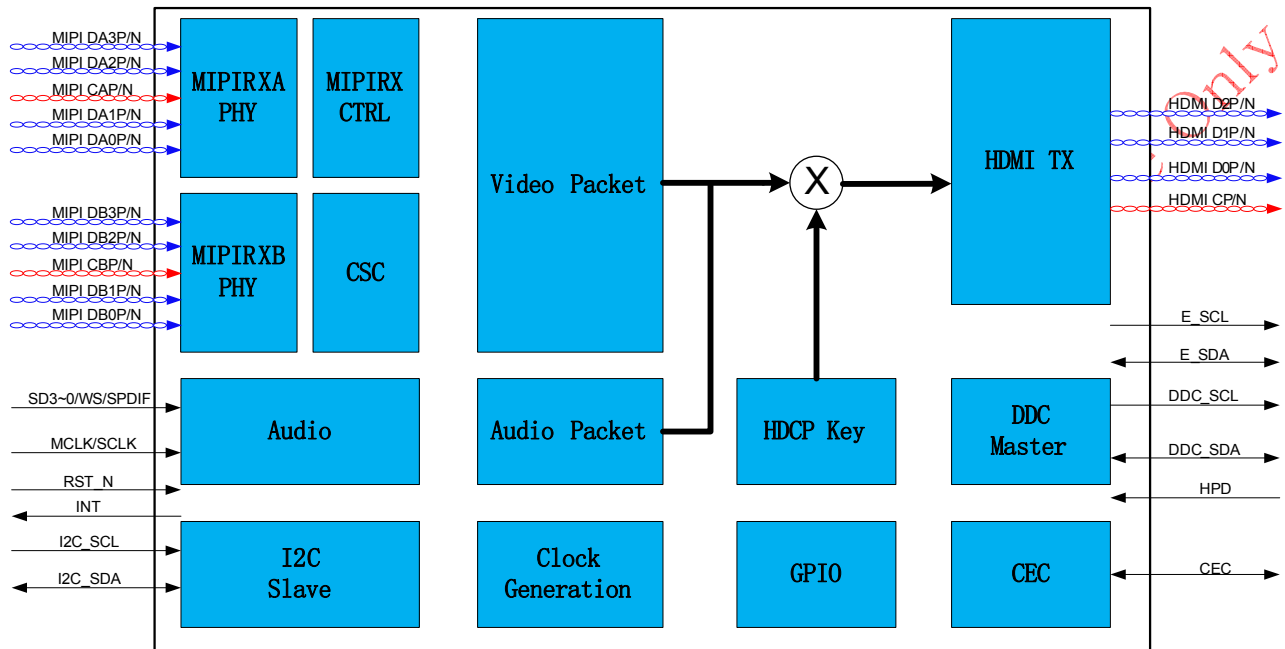
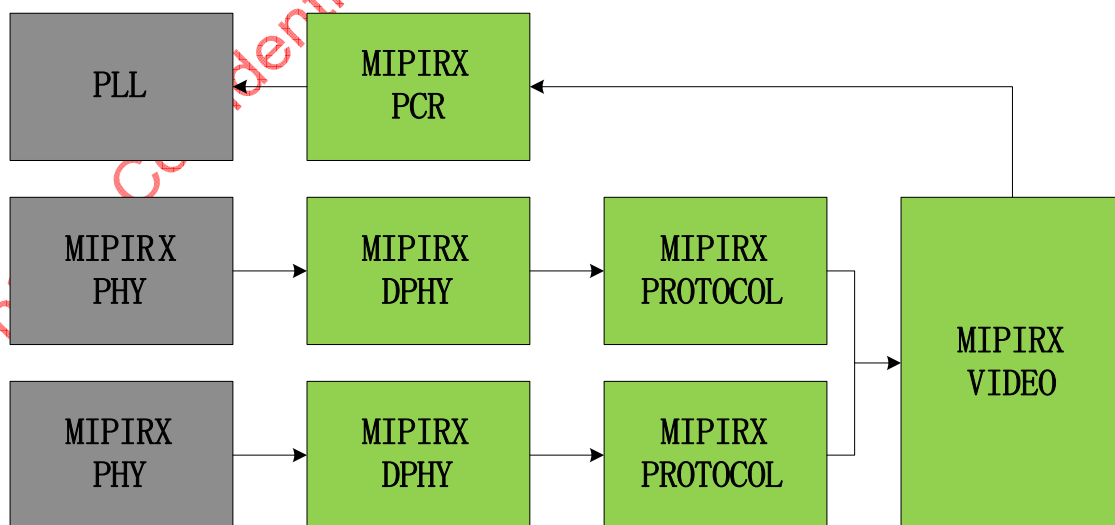


Figure 8.1.1 Function Block Diagram

8.2 Detailed Description

8.2.1 Dual Port MIPI RX



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Figure 8.2.1.1 Dual Port MIPI RX Block Diagram

MIPIRX PHY provide LP Data and HS Data for MIPIRX DPHY;
 MIPIRX DPHY LP Data is used to make a distinction between Low Power Mode and High Speed Mode;
 MIPIRX DPHY HS Data is used to low level protocol and lane merge, it support Lane Swap and Port Swap, it also support De-skew Calibration when data rate greater than 1500 Mbps;
 MIPIRX PROTOCOL is used to analysis short package and long package, and restore video data;
 MIPIRX PACKET is used to rebuild video timing;
 MIPIRX PCR is used to rebuild pixel clock.
 MIPI RX support video format for DSI/CSI :

Table 8.2.1.1 Video Data Type

	0E	1E	2E	3E	0D	1D	2C	0C	1C	3D
DSI	rgb565	rgb666	rgb666L	rgb888	rgb30	rgb36	yuv_16	yuv_20	yuv_24	yuv420
0	R[4:0]	R[5:0]	R	R	R	R	C[11:4]	C[7:0]	C[7:0]	C
1	G[5:0]	G[5:0]	G	G	G	G	Y[11:4]	Y[3:0],C[11:8]	Y[3:0],C[11:8]	Y0
2	B[4:0]	B[5:0]	B	B	B	B		Y[11:4]	Y[11:4]	Y1

	22	23	24	1E	1A	2A	2B	
CSI	rgb565	rgb666	rgb888	yuv422_8	yuv420_legacy	raw8	raw10	yuv422_10
0	B[4:0]	B[5:0]	B	Cb1	C	P1	P1[9:2]	Cb1[9:2]
1	G[5:0]	G[5:0]	G	Y1	Y0	P2	P2[9:2]	Y1[9:2]
2	R[4:0]	R[5:0]	R	Cr1	Y1	P3	P3[9:2]	Cr1[9:2]
				Y2			P4[9:2]	Y2[9:2]
							P4/3/2/1[1:0]	P4/3/2/1[1:0]

Note:For CSI raw data input,the HDMI output is not available,we just support raw data parallel output from the GPIOs.

For Dual Port application, the LT9611 support both odd-even mode and left-right mode as bellow.

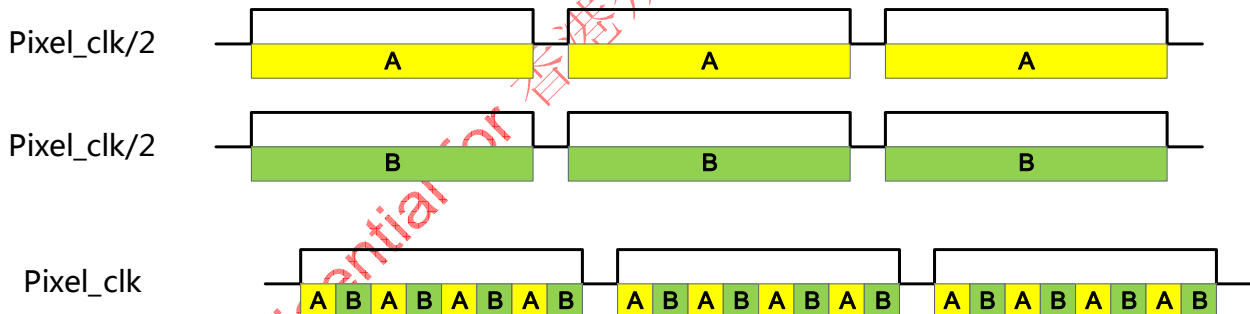


Figure 8.2.1.2 Dual Port MIPI RX Odd-Even Mode

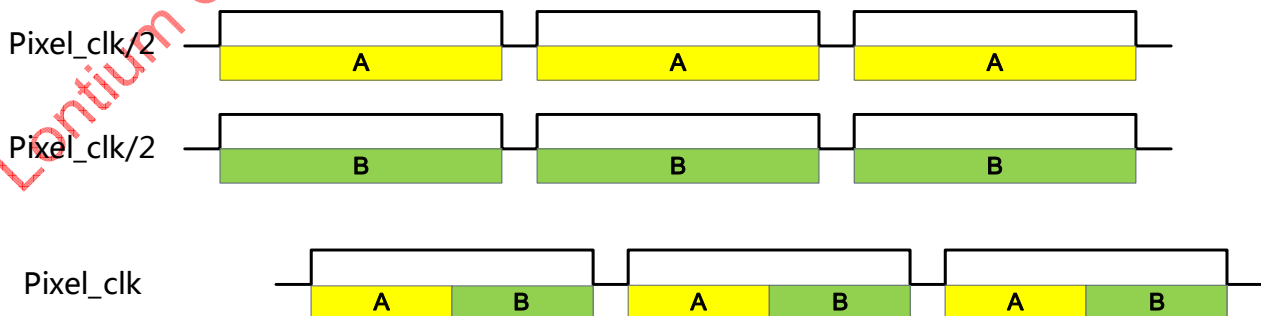


Figure 8.2.1.3 Dual Port MIPI RX Left-Right Mode

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8.2.2 DCS Write and Read Registers

All registers in LT9611 can be accessed via DCS Generic Short Packets optionally, as shown below:

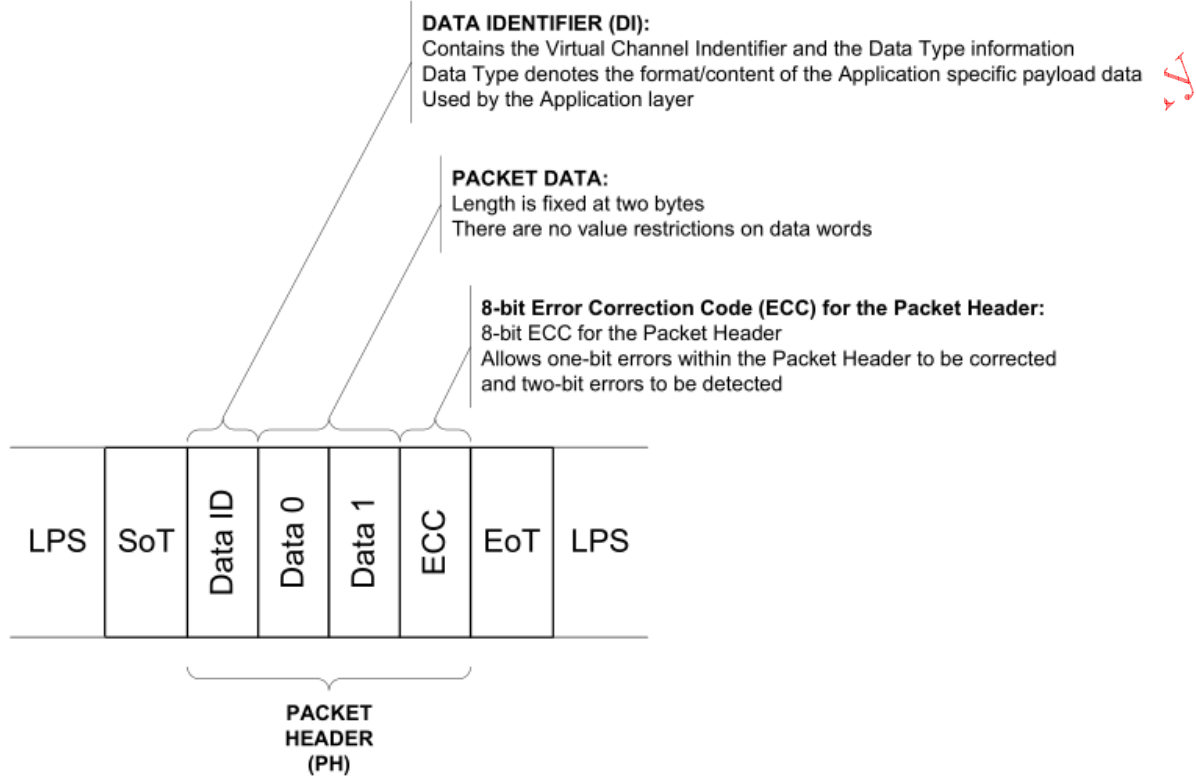


Figure 8.2.2.1 Short Packet Structure

Table 8.2.2.1 Packet Data Type

Source	Data Type	Description	Packet Size
Processor-sourced Packets	0x03	Generic Short WRITE, 1 parameter	Short
	0x13	Generic Short WRITE, 2 parameters	Short
	0x14	Generic READ, 1 parameter	Short
Peripheral-sourced Packets	0x11	Generic Short READ Response, 1 byte returned	Short

The source must use 0x13 to send two address parameters, and use 0x03 to send one data parameter.

For example, if you want to write the address 0x8300 with h55, just as follow:

13 83 00 ecc

03 55 00 ecc

And if you want to read the address 0x8300 register value, just as follow:

14 83 00 ecc

11 01 00 ecc

Noted: the read address (0x14 and 0x11) can be configured via the write command.

8.2.3 Color Space Conversion (YCbCr to RGB)

Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers YCbCr to RGB color space conversion (CSC). This provides maximum flexibility.

RGB - YCbCr Equations: SDTV

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The basic equations to convert between 8-bit digital R'G'B' data with a 16–235 nominal range (Studio RGB) and YCbCr are:

$$\begin{aligned} Y &= 0.299R' + 0.587G' + 0.114B' \\ Cb &= -0.172R' - 0.339G' + 0.511B' + 128 \\ Cr &= 0.511R' - 0.428G' - 0.083B' + 128 \\ R' &= Y + 1.371(Cr - 128) \\ G' &= Y - 0.698(Cr - 128) - 0.336(Cb - 128) \\ B' &= Y + 1.732(Cb - 128) \end{aligned}$$

RGB - YCbCr Equations: HDTV

The basic equations to convert between 8-bit digital R'G'B' data with a 16–235 nominal range (Studio RGB) and YCbCr are:

$$\begin{aligned} Y &= 0.213R' + 0.715G' + 0.072B' \\ Cb &= -0.117R' - 0.394G' + 0.511B' + 128 \\ Cr &= 0.511R' - 0.464G' - 0.047B' + 128 \\ R' &= Y + 1.540(Cr - 128) \\ G' &= Y - 0.459(Cr - 128) - 0.183(Cb - 128) \\ B' &= Y + 1.816(Cb - 128) \end{aligned}$$

8.2.4 Pixel Repetition

Video formats with native pixel rates below 25 Mpixels/sec require pixel-repetition in order to be carried across a TMDS link. 720x480i and 720x576i video format timings shall always be pixel-repeated. The HDMI Source indicates the use of pixel-repetition with the Pixel Repetition (PR0:PR3) field in the AVI InfoFrame.

This field indicates to the HDMI Sink how many repetitions of each unique pixel are transmitted. In non-repeated formats, this value is zero.

For pixel-repeated formats, this value indicates the number of pixels that may be discarded by the Sink without losing real image content.

The Source shall always accurately indicate the pixel repetition count being used. The use of the Pixel Repetition field is optional for HDMI Sink.

During pixel-doubling (TR_PIXEL_RPT = 1), all of the data sent across during the first pixel period will be repeated during the second pixel period. The third pixel period will then represent the second actual pixel and so on.

8.2.5 Audio Data Processing Flow

The LT9611 supports two to eight audio channels through four I2S inputs as well as one SPDIF input of audio data. The SPDIF stream is processed by a separate SPDIF processing block. The SPDIF processing block consists of SPDIF Frame sync detection and data decode block, FIFOs to store the received data, validity, parity, user's data and channel status bits for both the left and right channels. It also has a single bit FIFO which is used to store the information regarding the first frame detection. A depth of 16 for each of FIFOs is sufficient. The SPDIF sync detection, data decoding and loading of the decoded data are done synchronous to the SPDIF clock. The SDPIF clock is twice the SPDIF bit-rate. This selection is done to ease the implementation of the sync detection and data decoding. The reading of the data is done by the TMDS clock. The TMDS clock and SPDIF clock are assumed to be asynchronous with each other. To ensure that the write pointer of the FIFO is not corrupted when mapped from SPDIF to TMDS clock domain, the write pointer is grey coded. It is also mandatory to double re-time the write pointer in the TMDS clock domain.

In addition to the SPDIF processing block, the audio data packetization also has a header byte generation block. This block is responsible for generation of the header bytes for the audio packet.

The four I2S inputs allow transmission of 8-channel uncompressed audio data at up to 192 kHz sample rate. Four FIFOs are to store the received data.

The appropriate registers must be configured to describe the format of audio being input into the LT9611. This information is passed over the HDMI link in the CEA-861B Audio Info (AI) packets.

Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports up to 2-channel 192 kHz or 8-channel 96 kHz. The I2S pins must also be 'coherent' with MCLK.

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MCLK frequencies support various audio sample rates as shown in Table 8.2.5.1.

Table 8.2.5.1 Supported MCLK Frequencies

Audio Sample Rate, Fs							
8-Channel I2S and 2-Channel S/PDIF Supported Rates							
2-Channel I2S Supported Rates							
Multiple of Fs	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.869 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		
768	18.432 MHz	16.394 MHz	12.288 MHz	67.738 MHz	73.728 MHz		
1024	24.576 MHz	45.158 MHz	49.152 MHz				
1152	36.864 MHz	50.803 MHz	55.296 MHz				

Audio data carried across the HDMI link, which is driven by a TMDS (video) clock only, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

In many video source devices, the audio and video clocks are generated from a common clock

(coherent clocks). In this situation, there exists a rational (integer divided by integer) relationship between these two clocks. The HDMI clock regeneration architecture can take advantage of this rational relationship and can also work in an environment where there is no such relationship between these two clocks, that is, where the two clocks are truly asynchronous or where their relationship is unknown.

The Source shall determine the fractional relationship between the video clock and an audio reference clock.

The exact relationship between the two clocks will be:

$$128 \cdot f_s = f_{\text{TMDS_CLK}} \cdot N / \text{CTS}$$

The CTS value generated by the HDMI source is used by the HDMI sync to re-generate the audio sample clock. The CTS is generated according to the equation $128 \cdot f_s = \text{pixel clock} \cdot N / \text{CTS}$, where f_s is the audio sample clock. In other words the CTS is generated by counting the number of pix clocks in $128 \cdot f_s / N$ duration. This can be implemented using simple counters. The CTS counter has to be a 20bit counter and is initialized (to zero) after every $128 \cdot f_s / N$ clocks.

The $128 \cdot f_s$ and pixel clock have to be treated as asynchronous with respect to each other and appropriate care is to be taken during synchronization.

8.2.6 HDCP

The LT9611 includes HDCP 1.4(High - Bandwidth Digital Content Protection) circuitry. The HDCP protocol ensures protection from unauthorized duplication of copyrighted media content.

The LT9611 employs a HDCP encryption engine. It contains the encryption logic for all HDMI data (audio, video, and control). Hardware - implemented HDCP authentication and encryption for audio and video reduce external micro - controller overhead. HDCP encryption and authentication may be performed following device initialization. When using the LT9611, system manufacturers need to provide external key sets through a memory device, for example an EEPROM.

The HDCP encryption engine contains all the necessary logic to encrypt the incoming audio and video data. The encryption process is entirely controlled by the system microcontroller/microprocessor through a set sequence of register reads and writes. HDCP keys and Key Selector Value (KSV) stored in the external memory are used in the encryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to encrypt the audio/video data.



9. Specification

9.1 Absolute Maximum Conditions

Table 9.1.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TXPLL VDD	1.8V Power Supply Voltage	-0.3		2.0	V
VCC33	3.3V Power Supply Voltage	-0.3		3.63	V
V _I	CMOS Terminal Input Voltage Range	-0.3		2.0	V
V _O	CMOS Terminal Output Voltage Range	-0.3		2.0	V
T _s	Storage Temperature	-55		125	°C
ESD	HBM Elastostatic Discharge Level		4K		V

Notes:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.

2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

9.2 Normal Operating Conditions

Table 9.2.1 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VDD	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCC33	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VCC _N	Power Supply Voltage Noise			50	mV
T _A	Operating Free-air Temperature	-40	27	85	°C

9.3 DC Characteristics

Table 9.3.1 DC Characteristics

MIPI HS Line Receiver DC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
VIDTH	Differential input high voltage threshold			70	mV
VIDTL	Differential input low voltage threshold	-70			mV
VIHHS	Single ended input high voltage			460	mV
VILHS	Single ended input low voltage	-40			mV
VCMRXDC	Input common mode voltage	70		330	mV
RTERM	Differential input impedance	80		125	Ω
MIPI LP Line Receiver DC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
VIL	Input low voltage			550	mV
VIH	Input high voltage, data rate < 1.5Gbps	880			mV
	Input high voltage, data rate > 1.5Gbps	740			mV
VHYST	Input hysteresis	25			mV
HDMI Transmitter DC Specifications					

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Symbol	Parameter	MIN	TYP	MAX	Unit
VOFF	Single-ended standby (off) output voltage	AVCC-10		AVCC+10	mV
VH	Single-ended output high level voltage	AVCC-200		AVCC+10	mV
VL	Single-ended output low level voltage	AVCC-700		AVCC-400	mV
VSWING	Single-ended output data swing	400		600	mV
RTERM	AC couple single-ended impedance	40		60	Ω

9.4 AC Characteristics

Table 9.4.1 AC Characteristics

MIPI HS Line Receiver AC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
Δ VCMRX(HF)	Common mode interference beyond 450MHz			50	mVpp
Δ VCMRX(LF)	Common mode interference between 50MHz and 450MHz.	-50		50	mVpp
Ccm	Common mode termination			60	pF
Rterm	Termination Resister	80	100	125	Ω
MIPI LP Line Receiver AC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
HDMI Transmitter AC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
T_Intra_Pair_Skew	Intra-pair skew			0.15 Tbit	ps
T_Inter_Pair_Skew	Inter-pair skew			0.2 Tcharacter	ns
Tr/Tf	Rise time / fall time	75			ps
DUTY	TMDS clock duty cycle	40	50	60	%
T_jitter	Maximum TMDS clock jitter			0.25Tbit	ps
Audio AC Timing Specifications					
Fs_I2S	I2S Sample Rate	32		192	kHz
TsCKCYC	I2S Cycle Time			1.0	UI
TsCKDUTY	I2S Duty Cycle	90%		110%	
Ti2SSU	I2S Setup Time	15			ns
Ti2SHD	I2S Hold Time	0			ns
Fs_SPDIF	SPDIF Sample Rate	32		96	kHz
TsPCYC	SPDIF Cycle Time			1.0	UI
TsPDUTY	SPDIF Duty Cycle	90%		110%	
FmCLKCYC	MCLK Cycle Time			75	MHz
TmCLKDUTY	MCLK Duty Cycle	40%		60%	
TAUDDLY	Audio Pipeline Delay		30	70	us

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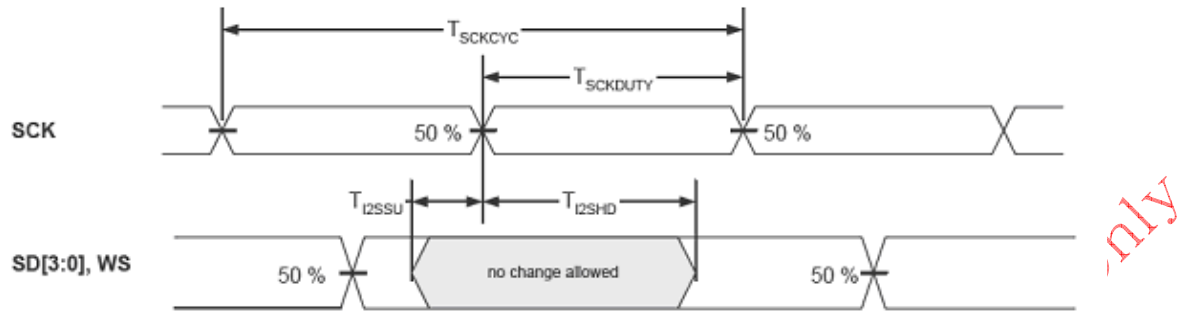


Figure 9.4.1 I2S Input Timings

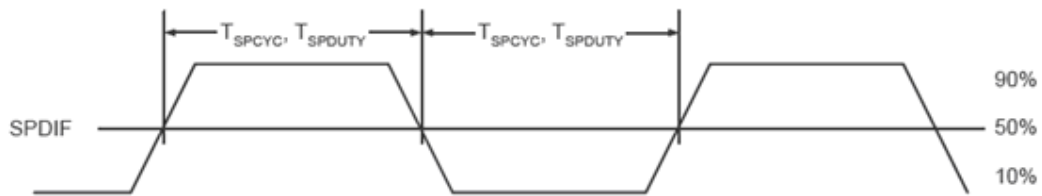


Figure 9.4.2 S/PDIF Input Timings

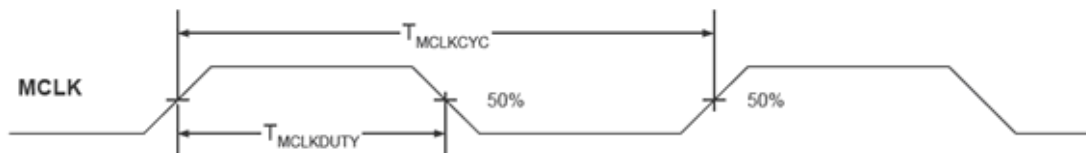


Figure 9.4.3 MCLK Timings

9.5 Power Consumption

Table 9.5.1 Power Consumption

Symbol	Test Condition	Power Consumption	Unit
I _{VCC18}	Dual Port MIPI to HDMI 4K30Hz	280	mA
I _{VCC33}		7	mA
I _{VCC18}	single Port MIPI to HDMI 4K30Hz	235	mA
I _{VCC33}		7	mA
I _{VCC18}	single Port MIPI to HDMI 1080P	145	mA
I _{VCC33}		7	mA

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9.6 Power-up and Reset Sequence

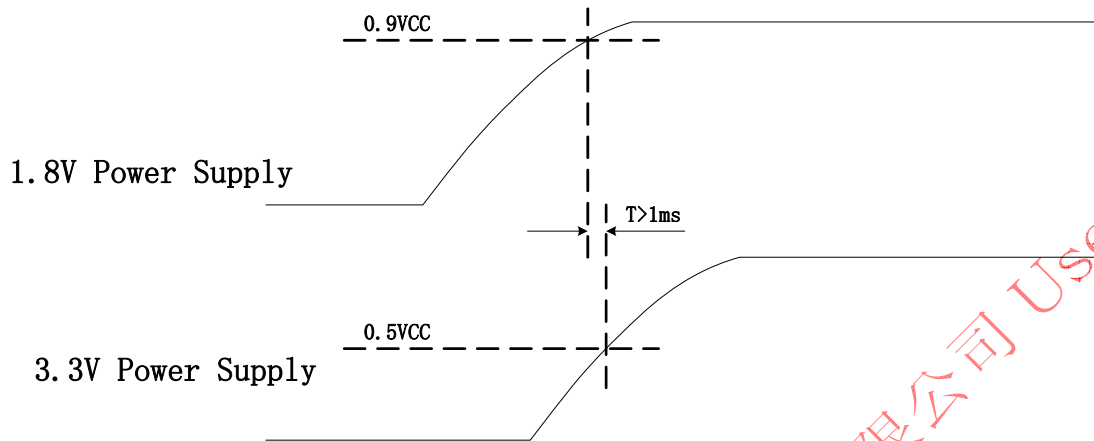


Figure 9.6.1 Power-up and Reset Sequence



10. Package Information

10.1 ePad Enhancement

The LT9611 is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

10.2 Package Dimensions

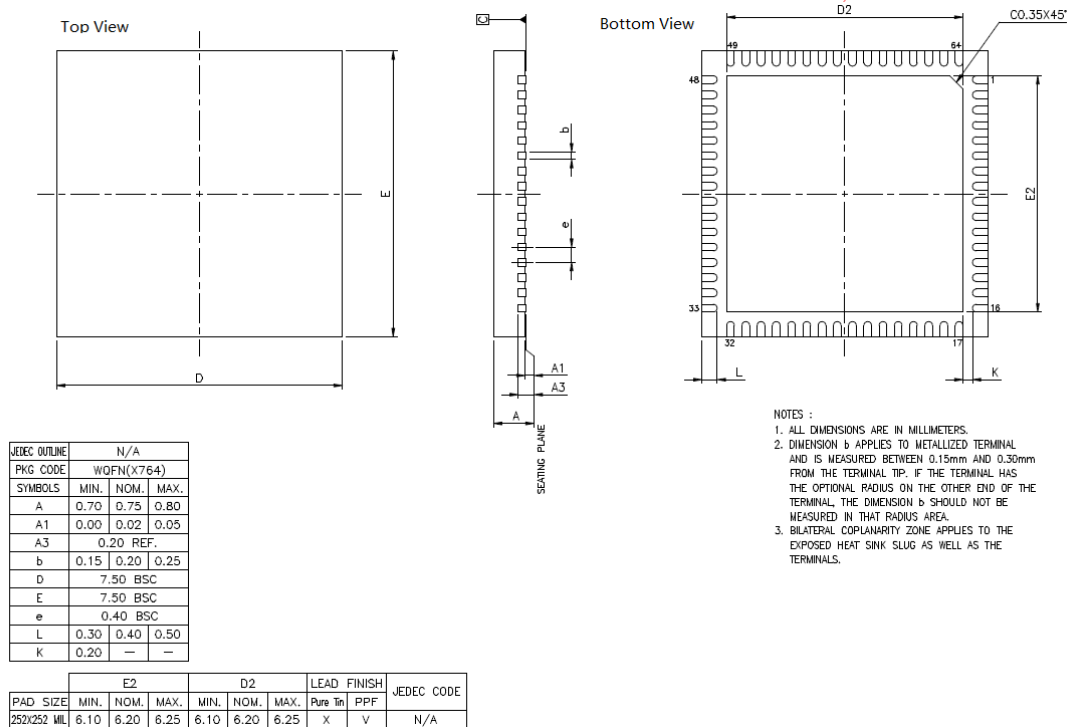


Figure 10.2.1 Package Dimensions



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