



# LPDDR4/4X Datasheet

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**RS256M32LS4D1BNR-46BT**  
**200-ball**

**Revision 1.0**

**May. 5. 2023**

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## Revision History

| Version | Date     | Changes                     |
|---------|----------|-----------------------------|
| V1.0    | 2023-5-5 | Basic spec and architecture |

**Notes:** *This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.*

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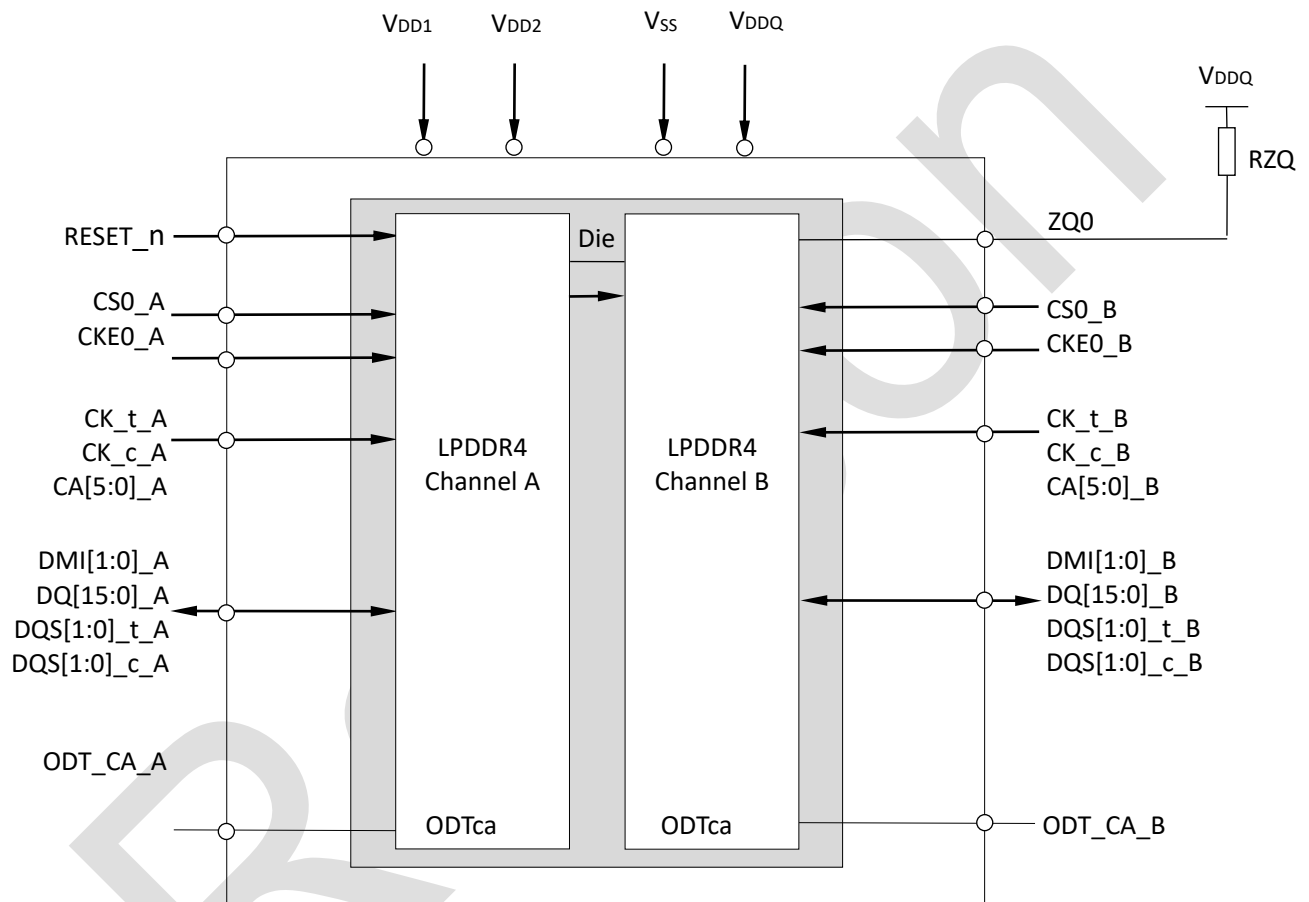
# 1. Product Overview

## 1.1. Feature Overview

- Ultra-low-voltage core and I/O power supplies
  - $V_{DD1}$  = 1.70-1.95V; 1.80V nominal
  - $V_{DD2}$  = 1.06-1.17V; 1.10V nominal
  - $V_{DDQ}$  = 0.57-0.65V; 0.60V nominal Or  $V_{DDQ}$  = 1.06-1.17V; 1.10V nominal
- Frequency range
  - 2133-10 MHz (data rate range per pin:4266-20Mbps)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD / ADR entry
- Bidirectional / differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL / WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.53 GB / s per die x16 channel
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- $V_{DD1}/V_{DD2}/V_{DDQ}$ : 1.80V/1.10V/0.60V or 1.10V
- Array configuration
  - 256 Meg x 32 (2 channels x 16 I/O)
  - 256M32 x 1 die in package
- FBGA “green” package
  - 200-ball FBGA (10mm x15mm x1.0mm Max)
- Speed grade,cycle time
  - 468ps@ RL = 36/40
- Operating temperature range
  - -25°C to + 85°C

## 2. Physical Specifications

### 2.1. Function Block Diagram



Single-Die, Dual-Channel, Single-Rank Package Block Diagram

## 2.2. Package ballout & Addressing

### 200-Ball Dual-Channel, Single-Rank Discrete FBGA

|    | 1    | 2        | 3        | 4      | 5    | 6 | 7 | 8      | 9      | 10       | 11      | 12   |
|----|------|----------|----------|--------|------|---|---|--------|--------|----------|---------|------|
| A  | DNU  | DNU      | VSS      | VDD2   | ZQ_A |   |   | NC     | VDD2   | VSS      | DNU     | DNU  |
| B  | DNU  | DQ0_A    | VDDQ     | DQ7_A  | VDDQ |   |   | VDDQ   | DQ15_A | VDDQ     | DQ8_A   | DNU  |
| C  | VSS  | DQ1_A    | DMIO_A   | DQ6_A  | VSS  |   |   | VSS    | DQ14_A | DMI1_A   | DQ9_A   | VSS  |
| D  | VDDQ | VSS      | DQS0_t_A | VSS    | VDDQ |   |   | VDDQ   | VSS    | DQS1_t_A | VSS     | VDDQ |
| E  | VSS  | DQ2_A    | DQS0_c_A | DQ5_A  | VSS  |   |   | VSS    | DQ13_A | DQS1_c_A | DQ10_A  | VSS  |
| F  | VDD1 | DQ3_A    | VDDQ     | DQ4_A  | VDD2 |   |   | VDD2   | DQ12_A | VDDQ     | DQ11_A  | VDD1 |
| G  | VSS  | ODT_CA_a | VSS      | VDD1   | VSS  |   |   | VSS    | VDD1   | VSS      | DNU     | VSS  |
| H  | VDD2 | CA0_A    | NC       | CS0_A  | VDD2 |   |   | VDD2   | CA2_A  | CA3_A    | CA4_A   | VDD2 |
| J  | VSS  | CA1_A    | VSS      | CKE0_A | NC   |   |   | CK_t_A | CK_c_A | VSS      | CA5_A   | VSS  |
| K  | VDD2 | VSS      | VDD2     | VSS    | NC   |   |   | DNU    | VSS    | VDD2     | VSS     | VDD2 |
| L  |      |          |          |        |      |   |   |        |        |          |         |      |
| M  |      |          |          |        |      |   |   |        |        |          |         |      |
| N  | VDD2 | VSS      | VDD2     | VSS    | DNU  |   |   | DNU    | VSS    | VDD2     | VSS     | VDD2 |
| P  | VSS  | CA1_B    | VSS      | CKE0_B | NC   |   |   | CK_t_B | CK_c_B | VSS      | CA5_B   | VSS  |
| R  | VDD2 | CA0_B    | NC       | CS0_B  | VDD2 |   |   | VDD2   | CA2_B  | CA3_B    | CA4_B   | VDD2 |
| T  | VSS  | ODT_CA_B | VSS      | VDD1   | VSS  |   |   | VSS    | VDD1   | VSS      | RESET_n | VSS  |
| U  | VDD1 | DQ3_B    | VDDQ     | DQ4_B  | VDD2 |   |   | VDD2   | DQ12_B | VDDQ     | DQ11_B  | VDD1 |
| V  | VSS  | DQ2_B    | DQS0_c_B | DQ5_B  | VSS  |   |   | VSS    | DQ13_B | DQS1_c_B | DQ10_B  | VSS  |
| W  | VDDQ | VSS      | DQS0_t_B | VSS    | VDDQ |   |   | VDDQ   | VSS    | DQS1_t_B | VSS     | VDDQ |
| Y  | VSS  | DQ1_B    | DMIO_B   | DQ6_B  | VSS  |   |   | VSS    | DQ14_B | DMI1_B   | DQ9_B   | VSS  |
| AA | DNU  | DQ0_B    | VDDQ     | DQ7_B  | VDDQ |   |   | VDDQ   | DQ15_B | VDDQ     | DQ8_B   | DNU  |
| AB | DNU  | DNU      | VSS      | VDD2   | VSS  |   |   | VSS    | VDD2   | VSS      | DNU     | DNU  |
|    | 1    | 2        | 3        | 4      | 5    | 6 | 7 | 8      | 9      | 10       | 11      | 12   |

Top View

  LPDDR4\_A(Channel A)
   LPDDR4\_B(Channel B)
   ZQ,ODT\_CA,RESET
   Supply
   Ground

## 2.3. Pad Definition

“\_A” and “\_B” indicate DRAM channels. “\_A” pads are present in all devices while “\_B” pads are present in dual channel SDRAM devices only.

LPDDR4X pad definitions are the same as LPDDR4, except ODT\_CA pins as described in the following Table

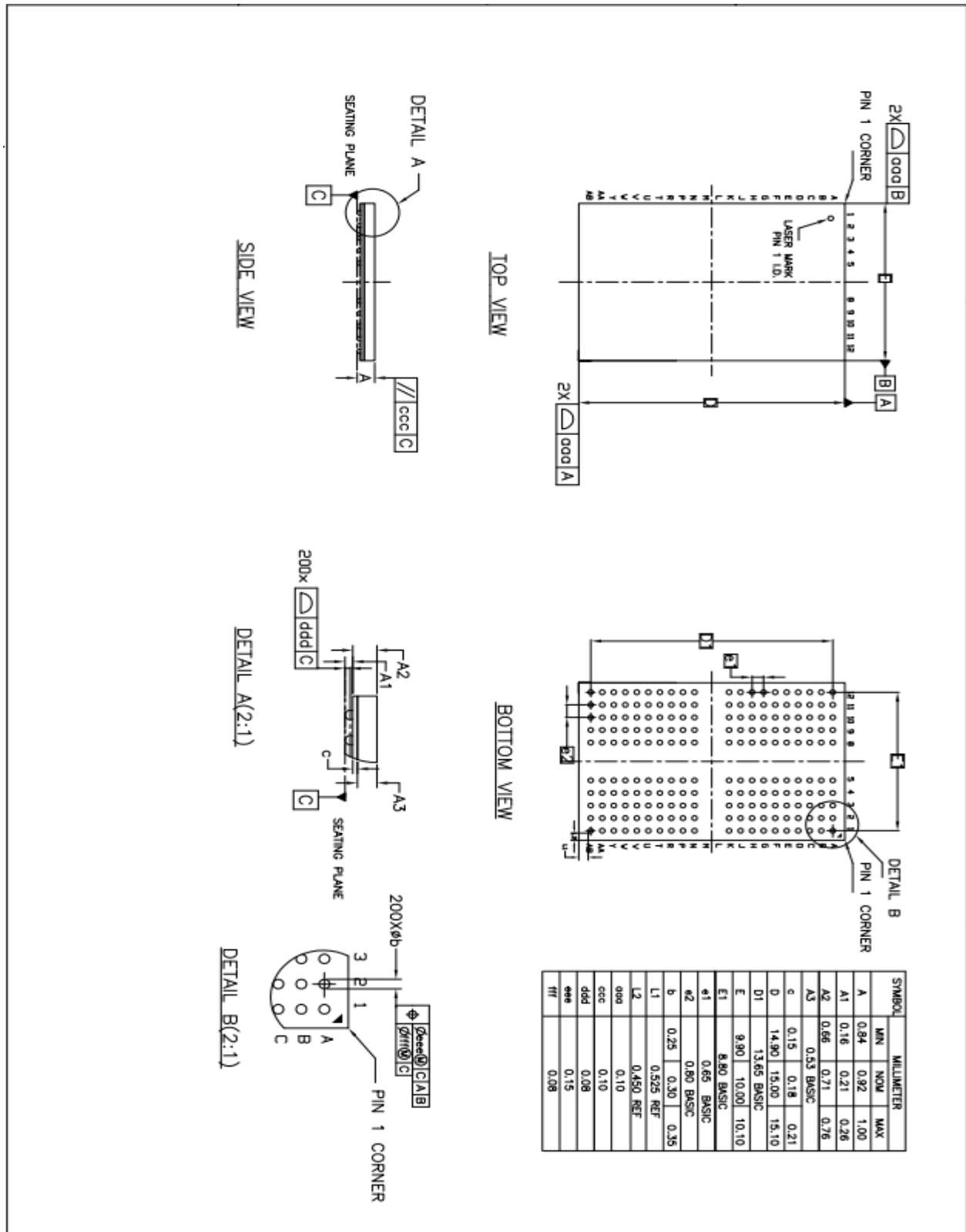
| Symbol   | Type  | Description  |
|--|-------|--|
| CK_t_A, CK_c_A<br>CK_t_B, CK_c_B                             | Input | <b>Clock:</b> CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c.AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.   |
| CKE0_A, CKE1_A<br>CKE0_B, CKE1_B                             | Input | <b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.   |
| CS0_A, CS1_A<br>CS0_B, CS1_B                                 | Input | <b>Chip select:</b> Each channel (A, B) has its own CS signals.  |
| CA[5:0]_A<br>CA[5:0]_B                                       | Input | <b>Command/address inputs:</b> Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.  |
| ODT_CA_A<br>ODT_CA_B   | Input | <b>CA ODT Control:</b> The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.   |
| DQ[15:0]_A<br>DQ[15:0]_B                                     | I/O   | <b>Data input/output:</b> Bidirectional data bus.  |
| DQS[1:0]_t_A<br>DQS[1:0]_c_A<br>DQS[1:0]_t_B<br>DQS[1:0]_c_B | I/O   | <b>Data strobe:</b> DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.   |
| DMI[1:0]_A<br>DMI[1:0]_B                                     | I/O   | <b>Data mask/Data bus inversion:</b> DMI is a dual use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals. |

| Symbol   | Type      | Description   |
|--|-----------|---|
| ZQ0, ZQ1   | Reference | <b>ZQ calibration reference:</b> Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V <sub>DDQ</sub> through a 240Ω ±1% resistor. |
| V <sub>DDQ</sub> , V <sub>DD1</sub> , V <sub>DD2</sub> | Supply    | <b>Power supplies:</b> Isolated on the die for improved noise immunity.   |
| V <sub>SS</sub>  | Supply    | <b>Ground reference:</b> Power supply ground reference.   |
| RESET_n  | Input     | <b>RESET:</b> When asserted LOW, the RESET pin resets all channels of the die.  |
| DNU  | –         | <b>Do not use:</b> Must be grounded or left floating.   |
| NC   | –         | <b>No connect:</b> Not internally connected.  |



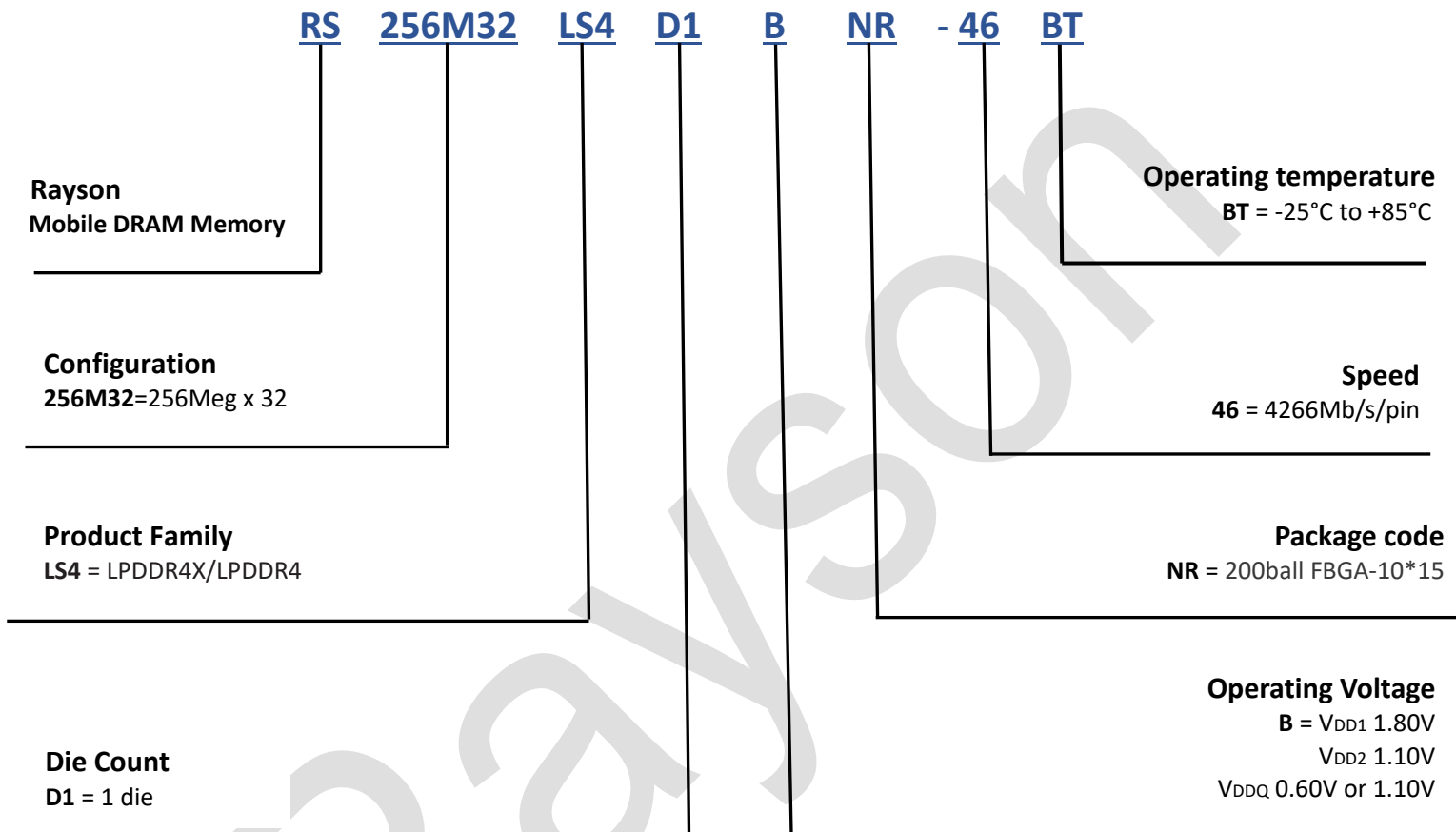
## 2.4. Discrete Package Dimension

10mm X15mm (Package Code: NR)



## 3. Core Specifications

### 3.1. Part Number Decoding



### 3.2. Ordering Options

Table 1: Key Timing Parameters

| Speed Grade | Clock Rate (MHz) | Data Rate (Mb/s/pin) | WRITE Latency |       | READ Latency |             |
|-------------|------------------|----------------------|---------------|-------|--------------|-------------|
|             |                  |                      | Set A         | Set B | DBI Disabled | DBI Enabled |
| -46         | 2133             | 4266                 | 18            | 34    | 36           | 40          |

Table 2: Part Number List

| Part Number           | Total Density | Data Rate    | Operating temperature |
|-----------------------|---------------|--------------|-----------------------|
| RS256M32LS4D1BNR-46BT | 1GB(8Gb)      | 4266Mb/s/pin | -25°C to + 85°C       |

Table 3: Refresh Requirement Parameters

| Parameter  | Symbol        | 4Gb Per Channel | unit |
|--|---------------|-----------------|------|
| REFRESH cycle time (all banks)                             | $t_{RFCab}$   | 180             | ns   |
| REFRESH cycle time (per bank)                              | $t_{RFCpb}$   | 90              | ns   |
| Per bank refresh to per bank refresh time (different bank) | $t_{PBR2PBR}$ | 90              | ns   |

### 3.3. Die Addressing Table

| Configuration     |   | 256M32 (8Gb/package)                         |
|-------------------|---|--|
| Die Configuration | Channel A, rank 0                       | x16 mode × 1 die<br>(dual channel)           |
|                   | Channel B, rank 0                       |  |
|                   | Channel A, rank 1                       | -  |
|                   | Channel B, rank 1                       |  |
| Die Addressing    | Memory density (per die)                | 8Gb  |
|                   | Memory density (per channel)            | 4Gb  |
|                   | Configuration                           | 32Mb × 16 DQ × 8 banks<br>x 2channels x1rank |
|                   | Number of channels (per die)            | 2  |
|                   | Number of ranks per channel             | 1  |
|                   | Number of banks (per channel)           | 8  |
|                   | Number of rows (per channel)            | 32,768                                       |
|                   | Number of columns<br>(fetch boundaries) | 64   |
|                   | Page size (bytes)                       | 2048   |
|                   | Channel density (bits per channel)      | 4,294,967,296                                |
|                   | Total density (bits per die)            | 8,589,934,592                                |
|                   | Bank address                            | BA[2:0]                                      |
|                   | Row address                             | R[14:0]                                      |
|                   | Column address                          | C[9:0]                                       |
|                   | Burst starting address boundary         | 64-bit                                       |

**Notes:** 1、Refer to Package Block Diagrams section in Product specification and SDRAM Addressing Section in General LPDDR4X specification.  
2、Refer to Byte Mode section for further information

### 3.4. Mode Register Contents

| MR0 |     |  |
|-----|-----|--|
| OP7 |     | <b>0b:</b> Both legacy and modified refresh mode supported |
| OP6 |     |  |
| OP5 |     |  |
| OP4 |     |  |
| OP3 |     |  |
| OP2 |     |  |
| OP1 |     |  |
| OP0 | REF |  |

| MR3 |      |  |
|-----|------|--|
| OP7 |      | <b>0b:</b> PPR protection disabled<br>(default)<br><b>1b:</b> Reserved |
| OP6 |      |  |
| OP5 |      |  |
| OP4 |      |  |
| OP3 |      |  |
| OP2 | PPRP |  |
| OP1 |      |  |
| OP0 |      |  |

| MR4 |          |   |
|-----|----------|---|
| OP7 |          | <b>0b:</b> Disable (default)<br>1b:Reserved |
| OP6 |          |   |
| OP5 |          |   |
| OP4 |          |   |
| OP3 | SR Abort |   |
| OP2 |          |   |
| OP1 |          |   |
| OP0 |          |   |

| MR5 |                 |                      |
|-----|-----------------|----------------------|
| OP7 | Manufacturer ID | 0000 0001b : Samsung |
| OP6 |                 |                      |
| OP5 |                 |                      |
| OP4 |                 |                      |
| OP3 |                 |                      |
| OP2 |                 |                      |
| OP1 |                 |                      |
| OP0 |                 |                      |

| MR6 |              |            |
|-----|--------------|------------|
| OP7 | Revision ID1 | 0000 0101b |
| OP6 |              |            |
| OP5 |              |            |
| OP4 |              |            |
| OP3 |              |            |
| OP2 |              |            |
| OP1 |              |            |
| OP0 |              |            |

| MR8 |           |   |
|-----|-----------|---|
| OP7 | I/O width | <b>OP[7:6] = 00b:</b> x16/channel                           |
| OP6 |           |   |
| OP5 | Density   | <b>OP[5:2] = 0010b:</b><br>8Gb per die<br>(4Gb per channel) |
| OP4 |           |   |
| OP3 |           |   |
| OP2 |           |   |
| OP1 |           |   |
| OP0 |           |   |

| MR13 |     |  |
|------|-----|--|
| OP7  |     | <b>0b:</b> Normal operation (default)<br><b>1b:</b> Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6 |
| OP6  |     |  |
| OP5  |     |  |
| OP4  |     |  |
| OP3  |     |  |
| OP2  | VR0 |  |
| OP1  |     |  |
| OP0  |     |  |

**Notes:** 1、 The contents of MR0, MR[6:3], MR8, MR13 will reflect information specific to each in these package

2、 Other bits not defined above and other mode registers are referred to in Mode Register Assignments and Definitions section.