



Industrial LPDDR4 Datasheet

ATL4B1G32M5R-53IT
ATL4B1G32M5R-53KT

200-ball FBGA

Revision 1.0

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Revision History

Version	Date	Changes
V1.0	2024-1-10	Basic spec and architecture

Notes: *This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.*



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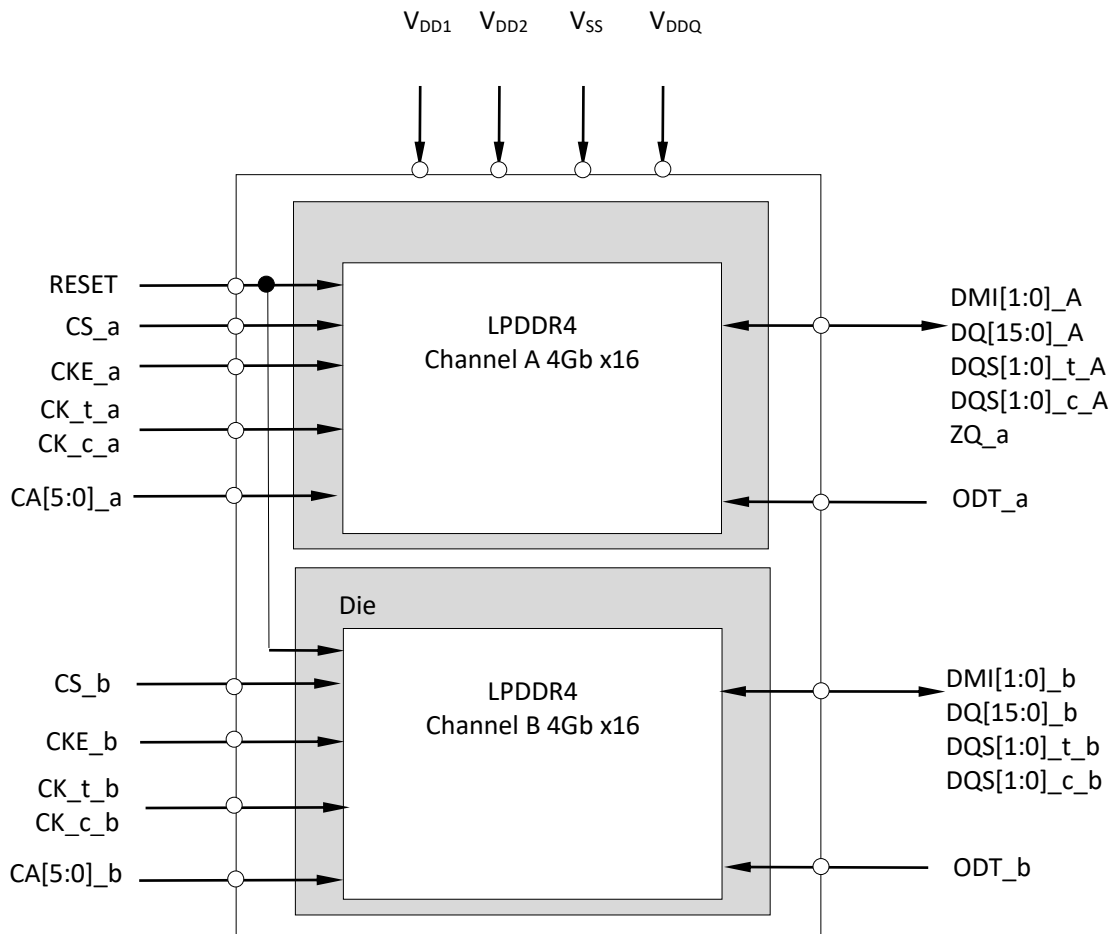
1. Product Overview

1.1. Feature Overview

- Ultra-low-voltage core and I/O power supplies
 - $V_{DD1} = 1.70\text{-}1.95\text{V}$; 1.80V nominal
 - $V_{DD2} = 1.06\text{-}1.17\text{V}$; 1.10V nominal
 - $V_{DDQ} = 1.06\text{-}1.17\text{V}$; 1.10V nominal
- Frequency range
 - 1866 -10 MHz (data rate range per pin:3733-20Mbps)
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD / ADR entry
- Programmable READ and WRITE latencies (RL / WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Refresh and Self Refresh Modes
- Partial-array self refresh (PASR) and Temperature Compensated Self Refresh
- Selectable output drive strength (DS)
- 2 channel composition per die
- RoHS-compliant, “green” packaging
- $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.80V/1.10V/1.10V
- Array configuration
 - 256Meg x 32 (2 channels x 16 I/O)
- FBGA “green” package
 - 200-ball FBGA (10mm x 15mm x Seated height 1mm Max)
- Speed grade, cycle time
 - 0.536ns@RL32, tRCD18ns, tRP18ns
- Operating temperature range
 - -40°C to + 85°C Industrial
 - -25°C to + 85°C

2. Physical Specifications

2.1. Function Block Diagram



Dual-Die, Dual-Channel Package, Single-Rank Block Diagram



2.2. Package ballout & Addressing

200-Ball Dual-Channel, Single -Rank Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V _{SS}	V _{DD2}	ZQ _a			NC	V _{DD2}	V _{SS}	DNU	DNU
B	DNU	DQ0 _a	V _{DDQ}	DQ7 _a	V _{DDQ}			V _{DDQ}	DQ15 _a	V _{DDQ}	DQ8 _a	DNU
C	V _{SS}	DQ1 _a	DMI0 _a	DQ6 _a	V _{SS}			V _{SS}	DQ14 _a	DMI1 _a	DQ9 _a	V _{SS}
D	V _{DDQ}	V _{SS}	DQS0 _{t_a}	V _{SS}	V _{DDQ}			V _{DDQ}	V _{SS}	DQS1 _{t_a}	V _{SS}	V _{DDQ}
E	V _{SS}	DQ2 _a	DQS0 _{c_a}	DQ5 _a	V _{SS}			V _{SS}	DQ13 _a	DQS1 _{c_a}	DQ10 _a	V _{SS}
F	V _{DD1}	DQ3 _a	V _{DDQ}	DQ4 _a	V _{DD2}			V _{DD2}	DQ12 _a	V _{DDQ}	DQ11 _a	V _{DD1}
G	V _{SS}	ODT_CA _a	V _{SS}	V _{DD1}	V _{SS}			V _{SS}	V _{DD1}	V _{SS}	DNU	V _{SS}
H	V _{DD2}	CA0 _a	NC	CS _a	V _{DD2}			V _{DD2}	CA2 _a	CA3 _a	CA4 _a	V _{DD2}
J	V _{SS}	CA1 _a	V _{SS}	CKE _a	NC			CK _{t_a}	CK _{c_a}	V _{SS}	CA5 _a	V _{SS}
K	V _{DD2}	V _{SS}	V _{DD2}	V _{SS}	DNU			DNU	V _{SS}	V _{DD2}	V _{SS}	V _{DD2}
L												
M												
N	V _{DD2}	V _{SS}	V _{DD2}	V _{SS}	DNU			DNU	V _{SS}	V _{DD2}	V _{SS}	V _{DD2}
P	V _{SS}	CA1 _b	V _{SS}	CKE _b	NC			CK _{t_b}	CK _{c_b}	V _{SS}	CA5 _b	V _{SS}
R	V _{DD2}	CA0 _b	NC	CS _b	V _{DD2}			V _{DD2}	CA2 _b	CA3 _b	CA4 _b	V _{DD2}
T	V _{SS}	ODT_CA _b	V _{SS}	V _{DD1}	V _{SS}			V _{SS}	V _{DD1}	V _{SS}	RESET _n	V _{SS}
U	V _{DD1}	DQ3 _b	V _{DDQ}	DQ4 _b	V _{DD2}			V _{DD2}	DQ12 _b	V _{DDQ}	DQ11 _b	V _{DD1}
V	V _{SS}	DQ2 _b	DQS0 _{c_b}	DQ5 _b	V _{SS}			V _{SS}	DQ13 _b	DQS1 _{c_b}	DQ10 _b	V _{SS}
W	V _{DDQ}	V _{SS}	DQS0 _{t_b}	V _{SS}	V _{DDQ}			V _{DDQ}	V _{SS}	DQS1 _{t_b}	V _{SS}	V _{DDQ}
Y	V _{SS}	DQ1 _b	DMI0 _b	DQ6 _b	V _{SS}			V _{SS}	DQ14 _b	DMI1 _b	DQ9 _b	V _{SS}
AA	DNU	DQ0 _b	V _{DDQ}	DQ7 _b	V _{DDQ}			V _{DDQ}	DQ15 _b	V _{DDQ}	DQ8 _b	DNU
AB	DNU	DNU	V _{SS}	V _{DD2}	V _{SS}			V _{SS}	V _{DD2}	V _{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

Top View

LPDDR4_A(Channel A) LPDDR4_B(Channel B) ZQ,ODT_CA,RESET Supply Ground



2.3. Pad Definition

“_A” and “_B” indicate DRAM channels. “_A” pads are present in all devices while “_B” pads are present in dual channel SDRAM devices only.

LPDDR4X pad definitions are the same as LPDDR4, except ODT_CA pins as described in the following Table

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on corssing of the positive edge of CK_t and the negative edge of CK_c.AC timings for CA parameters are referenced to CK. Each channel (A, B) has its own clock pair.
CKE_A CKE_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel(A & B) has its own CKE signal.
CS_A CS_B	Input	Chip select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	Command/address inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A & B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A DMI[1:0]_B	I/O	Data mask/Data bus inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.



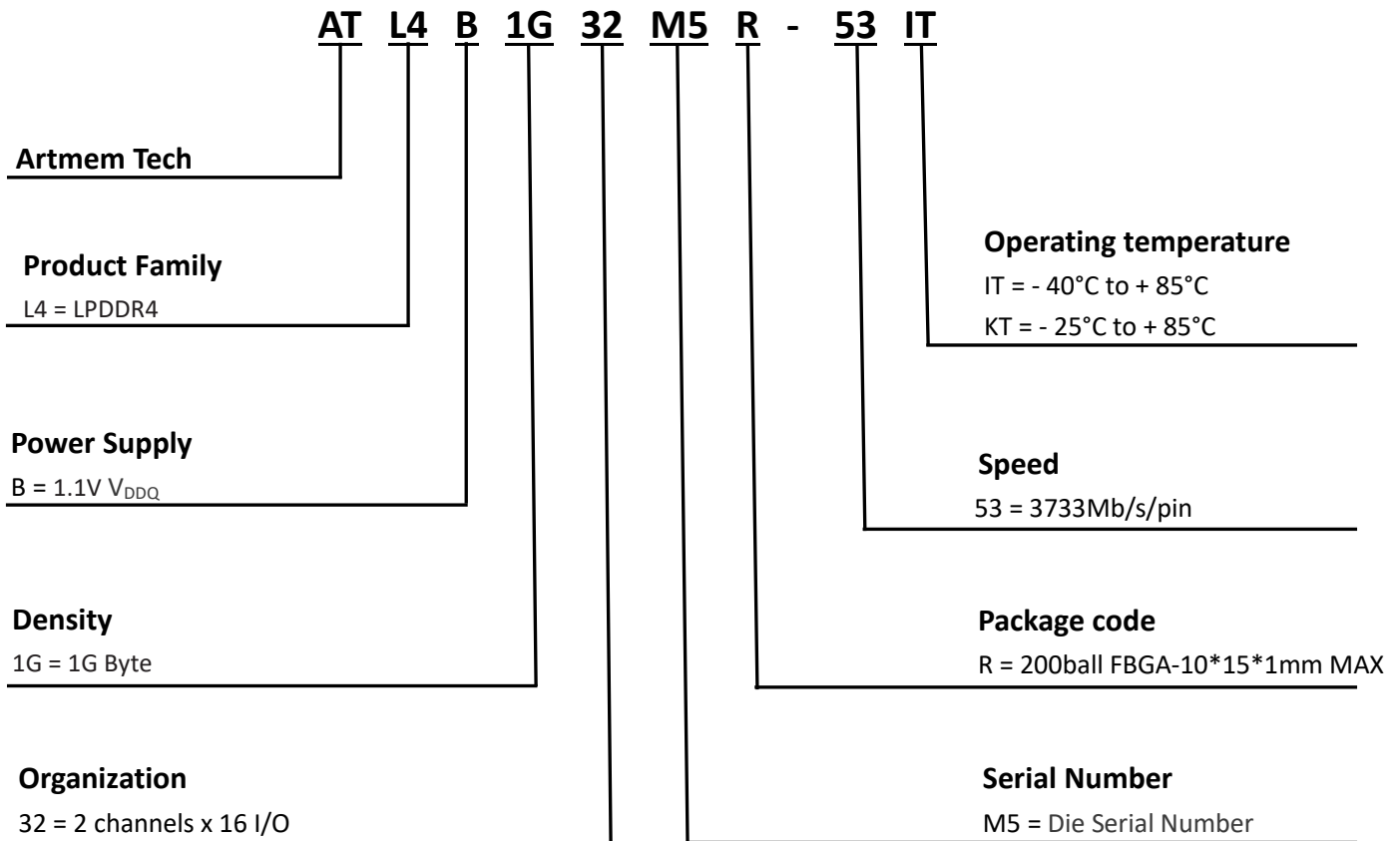
Symbol	Type	Description
ZQ_a	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor.
V _{DDQ} , V _{DD1} , V _{DD2}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets both channels of the die.
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.

[illegible]



3. Core Specifications

3.1. Part Number Decoding



Note1: LPDDR4: $V_{DD1} = 1.80V$; $V_{DD2} = 1.10V$; $V_{DDQ} = 1.10V$;



3.2. Ordering Options

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency		READ Latency	
			Set A	Set B	DBI Disabled	DBI Enabled
-53	1866	3733	16	30	32	36

Table 2: Part Number List

Part Number	Total Density	Data Rate	Operating temperature
ATL4B1G32M5R-53IT	1GB(8Gb)	3733 Mb/s/pin	-40°C to + 85°C
ATL4B1G32M5R-53KT	1GB(8Gb)	3733 Mb/s/pin	-25°C to + 85°C

Table 3: Refresh Requirement Parameters

Parameter	Symbol	8Gb Single-Channel Die	unit
REFRESH cycle time (all banks)	^t RFCab	180	ns
REFRESH cycle time (per bank)	^t RFCpb	90	ns



3.3. Die Addressing Table

Configuration		1G32 (8Gb/package)
Die Configuration	Channel A, Rank 0	x16 mode × 1 die (dual channel)
	Channel B, Rank 0	
Die Addressing	Memory density (per die)	8Gb
	Memory density (per channel)	8Gb
	Configuration	32Mb × 16DQ × 8 banks × 2 channels
	Number of channels (per die)	2
	Number of banks (per channel)	8
	Channel density (bits per channel)	4,294,967,296
	Total density (bits per die)	8,589,934,592
	Bank address	BA0-BA2
	Row address	R0-R14
	Column address	C0-C9

Notes :

- 1) Refer to Package Block Diagram section in Product specification and SDRAM Addressing Section in General LPDDR4X specification.
- 2) The lower two column addresses (C0-C1) are assumed to be “zero” and are not transmitted on the CA bus.
- 3) Row and Column Address values on the CA bus that are not used for a particular density be at valid logic levels.



3.4. Mode Register Contents

MR0 _Device Information (MA<7:0> = 00H)		
OP7	CATR	
OP6	(RFU)	OP[0] = 0B: Both legacy & modified refresh mode supported
OP5	PPR	OP[0] = 1B: Only modified refresh mode supported
OP4	RZQI	OP[4:3] = 00B: RZQ self-test not supported
OP3		OP[4:3] = 01B: ZQ-pin may connect to VSSQ or float
OP2	(RFU)	OP[4:3] = 10B: ZQ-pin may short to VDDQ
OP1		OP[4:3] = 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VSSQ or float, nor short to VDDQ)
OP0	Refresh mode	OP[5] = 0B: PPR not supported
		OP[5] = 1B: PPR supported
		OP[7] = 0B: CA for this rank is not terminated
		OP[7] = 1B: CA for this rank can be terminated

MR1 _Device Feature 1 (MA<7:0> = 01H)		
OP7	RPST	OP[1:0] = 00B: BL=16 Sequential (default) OP[1:0] = 01B: BL=32 Sequential OP[1:0] = 10B: BL=16 or 32 Sequential (on-the-fly) All others: Reserved
OP6	nWR (for AP)	OP[2] = 0B: Reserved OP[2] = 1B: WR Pre-ample = 2×Tck OP[3] = 0B: RD Pre-ample = Static (default) OP[3] = 1B: RD Pre-ample = Toggle OP[6:4] = 000B: nWR = 6 (default)
OP5		OP[6:4] = 001B: nWR = 10
OP4		OP[6:4] = 010B: nWR = 16
OP3	RD-PRE	OP[6:4] = 011B: nWR = 20
OP2	WR-PRE	OP[6:4] = 100B: nWR = 24 OP[6:4] = 101B: nWR = 30
OP1	BL	OP[6:4] = 110B: nWR = 34 OP[6:4] = 111B: nWR = 40
OP0		OP[7] = 0B: RD Post-ample = 0.5×tCK (default) OP[7] = 1B: RD Post-ample = 1.5×tCK



MR2_Device Feature 2 (MA<7:0> = 02H)		
OP7	WR Lev	OP[7] = 0B: Disabled (default) OP[7] = 1B: Enabled OP[6] = 0B: WL Set "A" (default) OP[6] = 1B: WL Set "B" WL Set "A" (MR2 OP[6]=0B)
OP6	WLS	OP[5:3] = 000B: WL=4 (Default) OP[5:3] = 001B: WL=6 OP[5:3] = 010B: WL = 8 OP[5:3] = 011B: WL = 10
OP5	WL	OP[5:3] = 100B: WL = 12 OP[5:3] = 101B: WL = 14 OP[5:3] = 110B: WL = 16 OP[5:3] = 111B: WL = 18
OP4		WL Set "B" (MR2 OP[6]=1B) OP[5:3] = 000B:WL=4 OP[5:3] = 001B:WL=8 OP[5:3] = 010B:WL=12
OP3		OP[5:3] = 011B:WL=18 OP[5:3] = 100B:WL=22 OP[5:3] = 101B:WL=26 OP[5:3] = 110B:WL=30 OP[5:3] = 111B:WL=34
OP2	RL	RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0B) OP[2:0] = 000B: RL=6, nRTP=8 (Default) OP[2:0] = 001B: RL=10, nRTP=8 OP[2:0] = 010B: RL=14, nRTP=8 OP[2:0] = 011B: RL=20, nRTP=8 OP[2:0] = 100B: RL=24, nRTP=10 OP[2:0] = 101B: RL=28, nRTP=12 OP[2:0] = 110B: RL=32, nRTP=14 OP[2:0] = 111B: RL=36, nRTP=16
OP1		RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1B) OP[2:0] = 000B: RL= 6, nRTP=8 OP[2:0] = 001B: RL= 12, nRTP=8 OP[2:0] = 010B: RL= 16, nRTP=8 OP[2:0] = 011B: RL= 22, nRTP=8 OP[2:0] = 100B: RL= 28, nRTP=10 OP[2:0] = 110B: RL= 32, nRTP=12 OP[2:0] = 110B: RL= 36, nRTP=14 OP[2:0] = 111B: RL= 40, nRTP=16
OP0		

MR3_I/O Configuration 1 (MA<7:0> = 03H):		
OP7	DBI-WR	OP[7] = 0B: Disabled (default) OP[7] = 1B: Enabled OP[6] = 0B: Disabled (default) OP[6] = 1B: Enabled
OP6	DBI-RD	OP[5:3] = 000B: RFU OP[5:3] = 001B: RZQ/1 OP[5:3] = 010B: RZQ/2 OP[5:3] = 011B: RZQ/3 OP[5:3] = 100B: RZQ/4
OP5	PDDS	OP[5:3] = 101B: WL = 14 RZQ/5 OP[5:3] = 110B: RZQ/6(default) OP[5:3] = 111B: Reserved
OP4		
OP3		
OP2	PPRP	OP[2] = 0B: PPR protection enabled (default) OP[2] = 1B: PPR protection enabled
OP1	WR PST	OP[1] = 0B: WR Post-amble = 0.5xtCK (default) OP[1] = 1B: WR Post-amble = 1.5xtCK (Vendor specific function)
OP0	PU-CAL	OP[0] = 0B: VDDQ/2.5 OP[0] = 1B: VDDQ/3 (default)

**ATL4B1G32M5R-53IT/ ATL4B1G32M5R-53KT****MR5_Basic Configuration 1 (MA<7:0> = 05H)**

OP7	LPDDR4 Manufacturer ID	OP[7:0] = 0000 0001B : Samsung
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR6_Basic Configuration 2 (MA<7:0> = 06H)

OP7	Revision ID-1	OP[7:0] = 0000 0101B : F-version
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR7_Basic Configuration 3 (MA<7:0> = 07H)

OP7	Revision ID-2	OP[7:0] = 0000 0000B: A-version
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR8_Basic Configuration 4 (MA<7:0> = 08H)

OP7	I/O width	OP[7:6] = 00B: x16 (per channel) All Others: Reserved
OP6		OP[5:2] = 0000B: 4Gb per die (2Gb per channel) OP[5:2] = 0001B: 6Gb per die (3Gb per channel)
OP5	Density	OP[5:2] = 0010B: 8Gb per die (4Gb per channel)
OP4		OP[5:2] = 0011B: 12Gb per die (6Gb per channel)
OP3		OP[5:2] = 0100B: 16Gb per die (8Gb per channel)
OP2		OP[5:2] = 0102B: 24Gb per die (12Gb per channel)
OP1	Type	OP[5:2] = 0110B: 32Gb per die (16Gb per channel)
OP0		All Others: Reserved OP[1:0] = 00B: S16 SDRAM (16n pre-fetch) All Others: Reserved

**MR13_CBT,RPT,VRO,VRCG,RRO,DM_DIS,FSP-WR, FSP-OP (MA<7:0> = 0DH)**

OP7	FSP-OP	OP[7] = 0B: Frequency-Set-Point [0] (default) OP[7] = 1B: Frequency-Set-Point [1] OP[6] = 0B: Frequency-Set-Point [0] (default) OP[6] = 1B: Frequency-Set-Point [1] OP[5] = 0B: Data Mask Operation Enabled (default) OP[5] = 1B: Data Mask Operation Disabled OP[4] = 0B: Disable codes 001 and 010 in MR4 OP[2:0] OP[4] = 1B: Enable all codes in MR4 OP[2:0] OP[3] = 0B: Normal operation (default) OP[3] = 1B: VREF fast response (high current) mode OP[2] = 0B: Normal operation (default) OP[2] = 1B: Output the VREF(CA) and VREF(DQ) values on DQ bits OP[1] = 0B : Disable (default) OP[1] = 1B: Enable OP[0] = 0B: Normal Operation (default) OP[0] = 1B: Command Bus Training Mode Enabled
OP6	FSP-WR	
OP5	DMD	
OP4	RRO	
OP3	VRCG	
OP2	VRO	
OP1	RPT	
OP0	CBT	

MR24_TRR (MA<7:0> = 18H)

OP7	TRR Mode	OP[7] = 0B: Disabled (default) OP[7] = 1B: Enabled OP[6:4] = 000B: Bank 0 OP[6:4] = 001B: Bank 1 OP[6:4] = 010B: Bank 2 OP[6:4] = 011B: Bank 3 OP[6:4] = 100B: Bank 4 OP[6:4] = 101B: Bank 5 OP[6:4] = 110B: Bank 6 OP[6:4] = 111B: Bank 7 OP[7] = 0B: OP[2:0] define MAC value OP[7] = 1B: Unlimited MAC value 2), 3) OP[2:0] = 000B: Unknown when bit OP3 =0 1) Unlimited when bit OP3=1 2) OP[2:0] = 001B: 700K OP[2:0] = 010B: 600K OP[2:0] = 011B: 500K OP[2:0] = 100B: 400K OP[2:0] = 101B: 300K
OP6	TRR mode BAn	
OP5		
OP4		
OP3	Unlimited MAC	OP[2:0] = 110B: 200K OP[2:0] = 111B: Reserved
OP2	MAC Value	
OP1		
OP0		



Notes: 1、 *The contents of MR0, MR[6:5], MR8, and MR13 will reflect information specific to each in these package*

2、 *Other bits not defined above and other mode registers are referred to in Mode Register Assignments and Definitions section.*