

MYC-LD25X Product Manual



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MYIR Electronics Limited

History

Version	Author	Participants	Date	Description
V1.0	Bai		20240814	Initial release
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1. Overview

The STM32MP25x Series Processor is an industrial application chip, Arm® based dual Cortex®-A35-1.5GHz+Cortex®-M33 MPU, AI, 3D GPU, Extensive Peripheral Extensions: Gigabit Ethernet interfaces*3, CAN*3, USB2.0(OTG)*1, USB2.0(HOST)*1, SDIO3.0*3, UART*8, I2C*8, I3C*4, SPI*8, 16-bit FMC*1; Rich multimedia resources: Support 24-bit RGB display, 4 channel MIPI DSI Signal, Currently, one LVDS display is supported, Max support 2048*1536@60FPS, 2-channel MIPICSI signal; The VPU supports H.264/VP8 1920*1080@60FPS.

Based on the STM32MP25x series chip as the main Processor, MYIR Electronics launched a new Product: MYC-LD25X. The minimum MPU system is mainly concentrated on a SOM, which is convenient for customers to develop; Have a good software development environment, kernel support open source operating system Linux; For high-end industrial HMI, edge computing gateway, new energy charging pile, energy storage EMS system, industrial automation PLC, motion controller and other scenarios.



Figure 1-1 MYC-LD25X SOM Top side

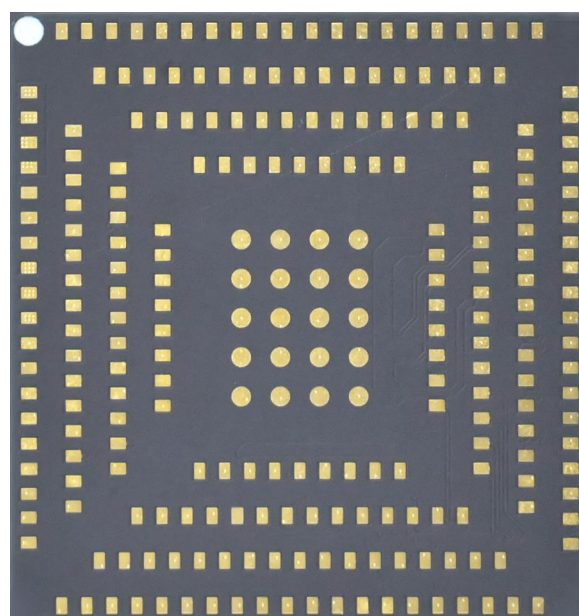


Figure 1-2 MYC-LD25X SOM Bottom side

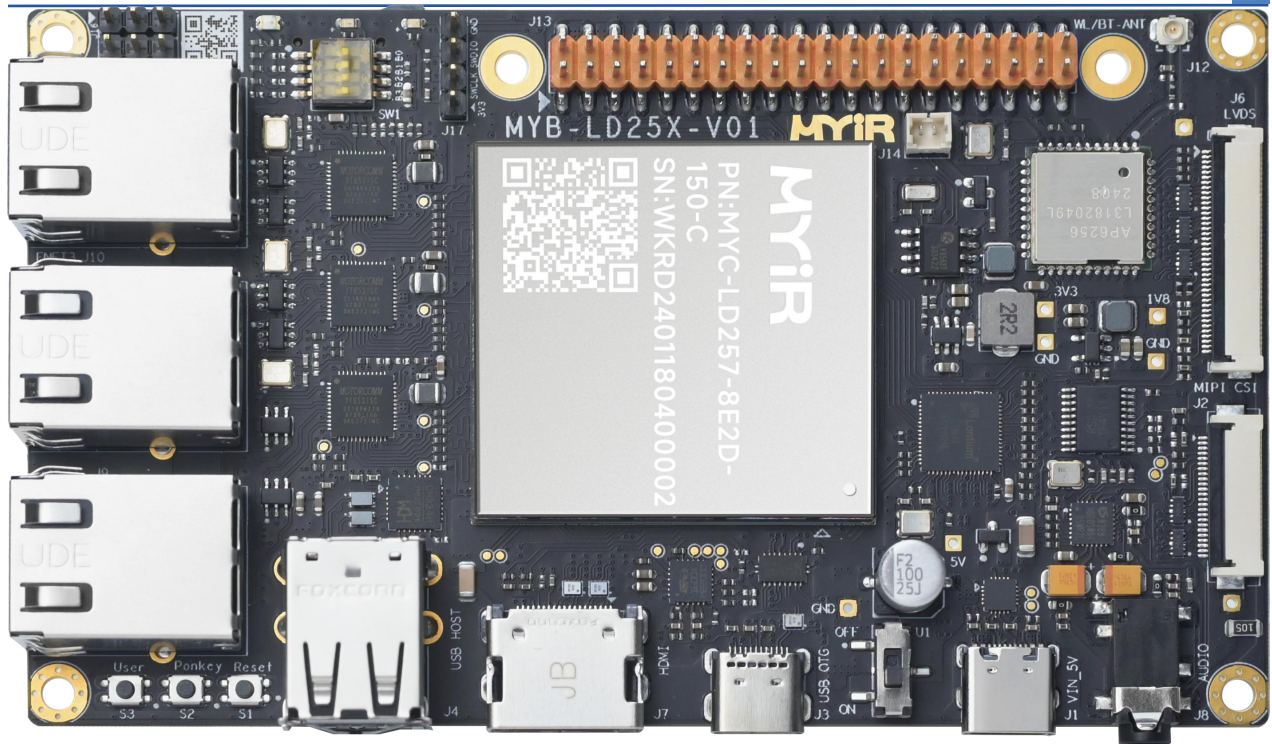


Figure 1-3 MYD-LD25X evaluation board

Resource	Parameter description
CPU	<ul style="list-style-type: none"> based on the high-performance single or dual-core Arm® Cortex®-A35 64-bit RISC core operating at up to 1.5 GHz. embed a Cortex®-M33 32-bit RISC core operating at up to 400 MHz frequency
GPU	<ul style="list-style-type: none"> Optional VeriSilicon GC8000UL up to 900 MHz
NPU	
On-chip ROM	<ul style="list-style-type: none"> 128 Kbytes (only for Cortex-A35)
External storage	<ul style="list-style-type: none"> supporting external memories up to 32-Gbit density (4 Gbytes) 16- or 32-bit DDR3L up to 1066 MHz 16- or 32-bit LPDDR4 or DDR4 up to 1200 MHz
Video engine	<ul style="list-style-type: none"> Decoder (VDEC) /Encoder (VENC) <ul style="list-style-type: none"> H264/VP8 up to 1080p60 JPEG 500 Mpixel/s Video RAM <ul style="list-style-type: none"> Up to 128 Kbytes
Video input	Camera interface <ul style="list-style-type: none"> CSI-2 + RGB/RawBayer parallel CSI-2 serial (CSI+ DCMIPP) <ul style="list-style-type: none"> 2× data lanes 2.5 Gbit/s each, path shared with DCMIPP Parallel RGB/RawBayer (DCMIPP) <ul style="list-style-type: none"> Up to 120 MHz, path shared with CSI. Image signal processing (ISP) <ul style="list-style-type: none"> embedded inside DCMIPP Parallel RGB (DCMI) <ul style="list-style-type: none"> Up to 80 MHz
Display output	LCD-TFT (LTDC) <ul style="list-style-type: none"> Up to 314 MHz pixel clock (when used with DSI or LVDS) Parallel interface <ul style="list-style-type: none"> Up to 24-bits 150 MHz pixel clock (up to 1080p60) Display serial interface (DSI) <ul style="list-style-type: none"> 4× data lanes 2.5 Gbit/s each (up to 1536p60) LVDS display interface (LVDS) <ul style="list-style-type: none"> Up to dual-link of 4× data lanes 1.1 Gbit/s each (up to 1536p60)
Audio	SAI <ul style="list-style-type: none"> 4 (up to 8 audio channels), with I2S master/slave, PCM input Audio digital filter (ADF) <ul style="list-style-type: none"> 1 input channel with 1 filter and sound-activity detection
Safety Engine	<ul style="list-style-type: none"> TrustZone peripherals, active tamper, environmental monitors, display secure layers, hardware accelerators Complete resource isolation framework

connection	<ul style="list-style-type: none"> • Up to three CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TTCAN) • one USB 2.0 high-speed Host with embedded 480 Mbits/s PHY • one USB 2.0/3.0 high-speed/SuperSpeed dual role data with embedded 480 Mbits/s and 5 Gbits/s PHY (5 Gbits/s PHY shared with PCI Express) • one PCI Express with embedded 5 Gbits/s PHY (PHY shared with USB 3.0 SuperSpeed) ● Up to three Gigabit Ethernet interfaces <ul style="list-style-type: none"> • one Gigabit Ethernet GMAC with one PHY interface (optional) • one Gigabit Ethernet GMAC with one external PHY interface, optionally internally connected to one embedded Ethernet switch providing two external phy interfaces • TSN, IEEE 1588v2 hardware, MII/RMII/RGMII
PMIC	<ul style="list-style-type: none"> ● Power Management IC, WFQFN 56L (6.5x6.5x0.9 mm) package
package	<ul style="list-style-type: none"> ● TFBGA 424 Pin ● 14 mm x 14 mm size, 0.5 mm pitch

Table 2-1 STM32MP25X Resources

Refer to the chip manual for details.

2.2. SOM Features

Item	features
CPU series	STM32MP25x
CPU Part Number	STM32MP257DAK3
DDR storage	LPDDR4:1/2GB
EMMC	8GB
CPU Processor	dual-core Cortex-A35@1.5 GHz,Cortex-M33@400MHz
Core plate size	37mm*39mm
interface type	LGA 252 PIN
PCB board specifications	12 layer plate design, gold sinking Process production

Table 2-2 Major parameter

2.3. system chart

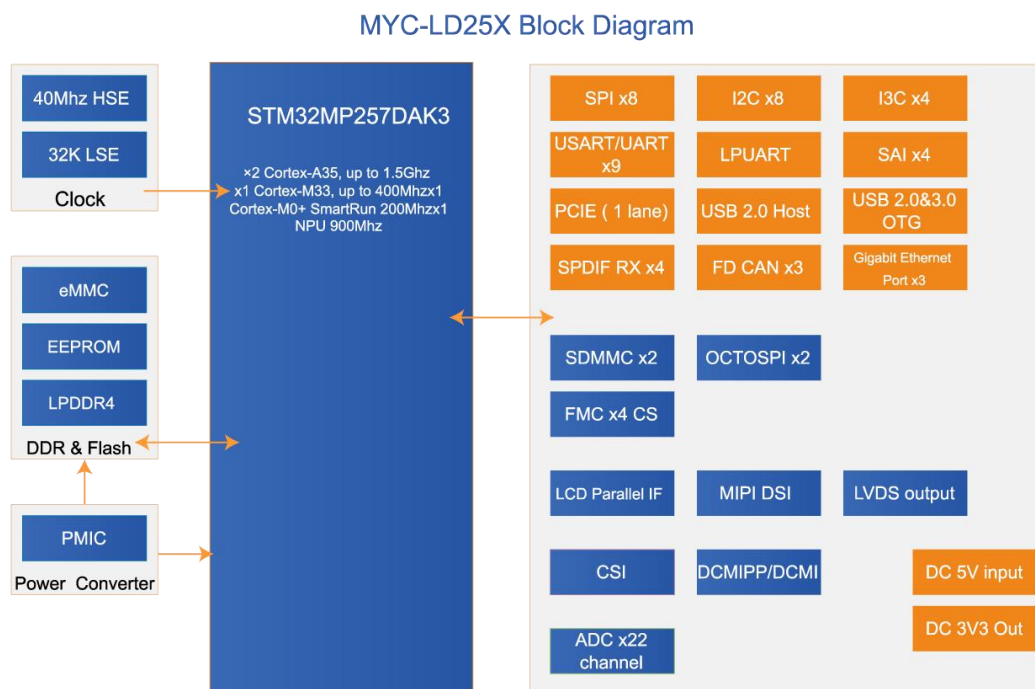


Figure 2-2 MYC-LD25X SOM block diagram

2.4. Standard model

The MYC-LD25X Series SOM contains 4 standard product models: they have some differences in operating temperature and memory parameters, and customers can choose the appropriate model according to their needs. For batch requirements, MYIR provides customized Services with optional SOM Parameters.

model Item	MYC-LD257-8E1D-150-C	MYC-LD257-8E2D-150-C
master chip	STM32MP257DAK3	STM32MP257DAK3
Main chip series	STM32MP25x	STM32MP25x
memory	LPDDR4:1GB	LPDDR4:2GB
eMMC	8GB	8GB
Core	2 x Cortex-A35+Cortex-M33	2 x Cortex-A35+Cortex-M33
basic frequency	A35 1.5GHz, M33 400Mhz	A35 1.5GHz, M33 400Mhz
video output	MIPI DSI x 1 LVDS x 2 RGB x1	MIPI DSI x 1 LVDS x 2 RGB x1
Audio	SAI x 4	SAI x 4
MIPI CSI	1	1
SD/MMC	2	2
USB	USB2.0 HOST x 1 USB2.0 OTG x 1	USB2.0 HOST x 1 USB2.0 OTG x 1
Ethernet	RGMII x 3	RGMII x 3
UART	9	9
I2C	7	7
I3C	4	4
CAN	3	3
SPI	8	8
JTAG	1	1
SWD	1	1
GPIO	Up to 128	Up to 128
voltage	+5V	+5V

machine size	37mm * 39mm	37mm * 39mm
operating temperature	0°C - +70°C	0°C - +70°C
Pin number	LGA 252 Pin	LGA 252 Pin
Certifications	CE ROHS	CE ROHS

Table 2-3 MYC-LD25X SOM selection Table 1

model Item	MYC-LD257-8E1D-150-I	MYC-LD257-8E2D-150-I
master chip	STM32MP257DAK3	STM32MP257DAK3
Main chip series	STM32MP25x	STM32MP25x
memory	LPDDR4:1GB	LPDDR4:2GB
eMMC	8GB	8GB
core	2 x Cortex-A35+Cortex-M33	2 x Cortex-A35+Cortex-M33
basic frequency	A35 1.5GHz, M33 400Mhz	A35 1.5GHz, M33 400Mhz
video output	MIPI DSI x 1 LVDS x 2 RGB x1	MIPI DSI x 1 LVDS x 2 RGB x1
Audio	SAI x 4	SAI x 4
MIPI CSI	1	1
SD/MMC	2	2
USB	USB2.0 HOST x 1 USB2.0 OTG x 1	USB2.0 HOST x 1 USB2.0 OTG x 1
Ethernet	RGMII x 3	RGMII x 3
UART	9	9
I2C	7	7
I3C	4	4
CAN	3	3
SPI	8	8
JTAG	1	1

SWD	1	1
GPIO	Up to 128	Up to 128
voltage	+5V	+5V
machine size	37mm * 39mm	37mm * 39mm
operating temperature	-40°C - +85°C	-40°C - +85°C
Pin number	LGA 252 Pin	LGA 252 Pin
Certifications	CE ROHS	CE ROHS

Table 2-5 MYC-LD25X SOM selection Table 2

Note: The blue background represents the interface type supported by the SOM module; The grey background represents the others. The selection table is the maximum resource extracted from the SOM and there may be a reuse relationship.

3. Pin Description

3.1. Appearance diagram

The MYC-LD25X SOM is welded to the base board in the form of an SMD patch, The back of the SOM is the LGA sealing pad, There are 252 pins, For details about the package design of the SOM, see the Package Information section.

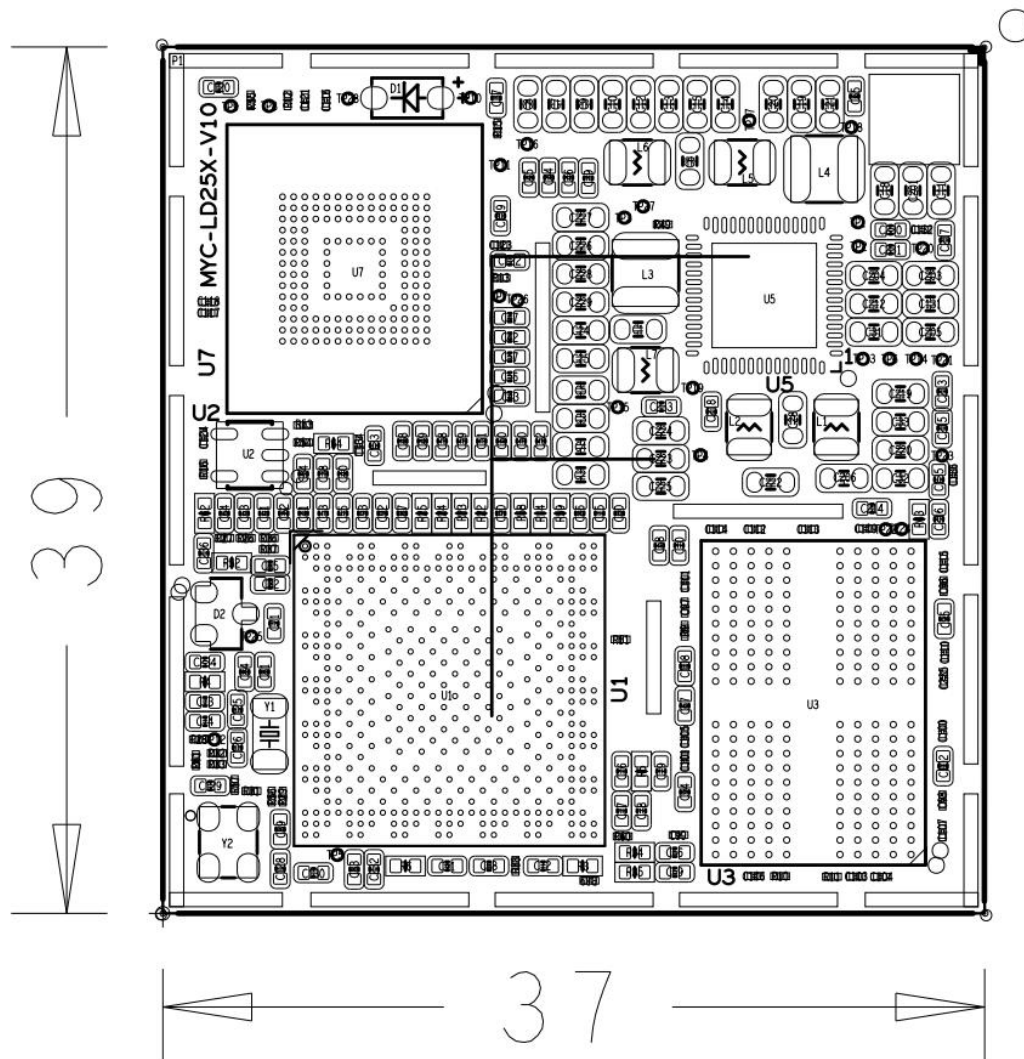


Figure 3-1 SOM pin diagram (Top side,Unit: mm)

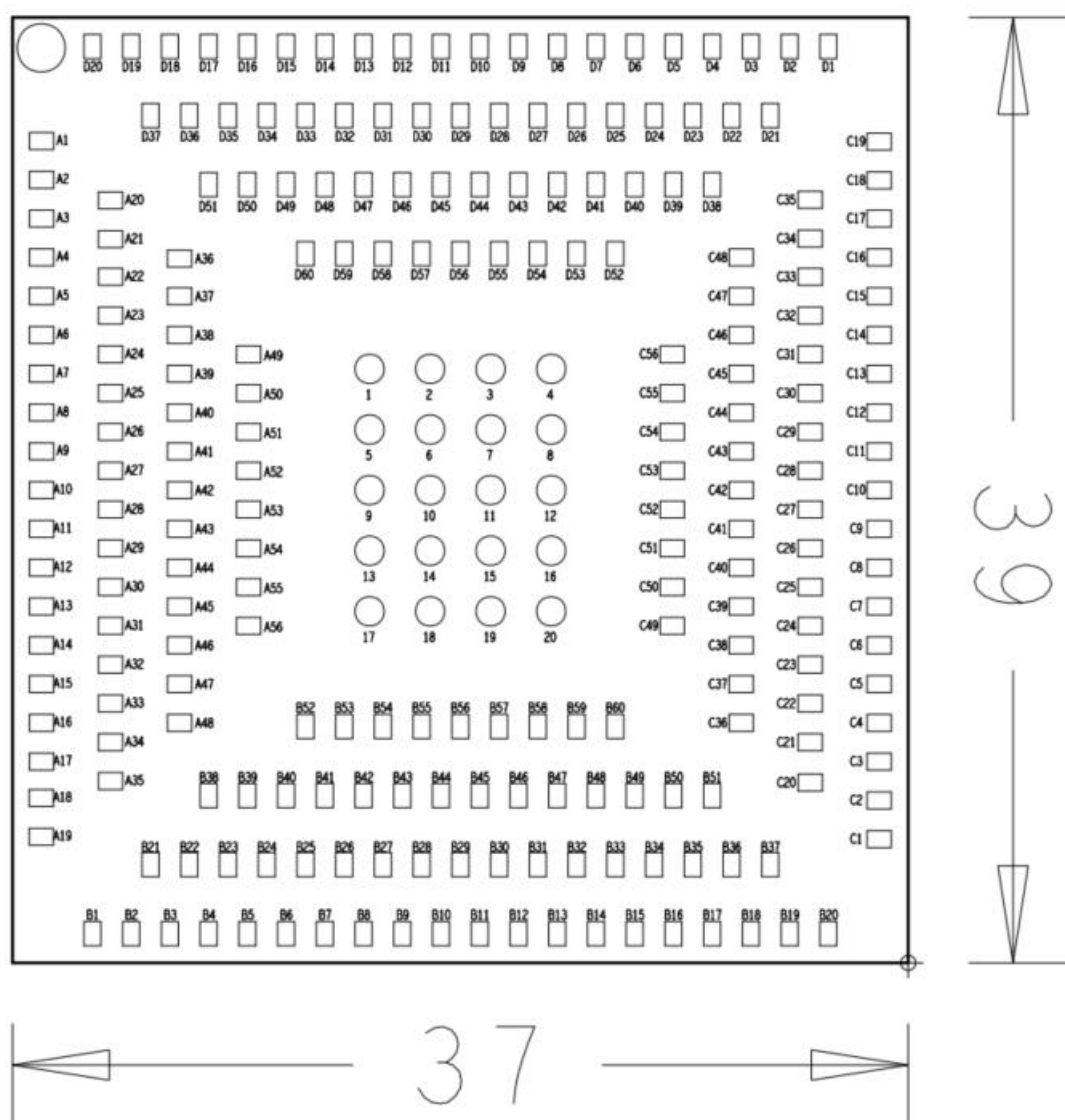


Figure 3-2 SOM pin diagram (Bottom side) ,Unit(mm)

3.2. Pin List

MYC-LD25X SOM interface pin definition is shown in the following table. The pin functions of the BSP development kit are configured according to "Default functions" in the following table. If the default pin functions need to be changed, please modify the relevant driver configuration code; otherwise uncertain exceptions such as driver conflicts may occur.

The SOM Pin mapping table describes the basic definition of the pin, and the Pin List table in the Excel version of the hardware manual contains detailed information about the pin reuse function.

Note: A: analog signal or special pin; I: output; O: Input; I/O: Input/output

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
A1	VSYS_5V	/	5V input	5V	I	
A2	VSYS_5V	/	5V input	5V	I	
A3	VSYS_5V	/	5V input	5V	I	
A4	VSYS_5V	/	5V input	5V	I	
A5	GND	/	GND			
A6	GND	/	GND			
A7	GND	/	GND			
A8	VDD_3V3	/	3.3V output	3.3V	O	
A9	VDD_SDCARD	/	3.3V output	3.3V	O	
A10	VDDIO_SDCARD	/	3.3V output	3.3V	O	
A11	PB3_TIM20_CH3	B14	Used as GPIO	3.3V	O	
A12	PD11_UART4_TX	A15	Used as GPIO	3.3V	O	
A13	PB6_UART4_RX	C13	Used as GPIO	3.3V	O	
A14	PA8_USART2_RX	AA17	Data Receive	3.3V	I	Debugging serial port
A15	PD6	A18	Used as GPIO	3.3V	O	
A16	GND	/	GND			
A17	PB7_I2S3_CK	C11	sampling clock signal	3.3V	O	
A18	UCPD_CC2	AA19	UCPD_CC2	-	A	
A19	UCPD_CC1	AB18	UCPD_CC1	-	A	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
A20	GND	/	GND			
A21	NC	/	/			
A22	NC	/	/			
A23	NC	/	/			
A24	GND	/	GND			
A25	PG4_ADC1_INP4	AD6	Used as GPIO	3.3V	O	
A26	PB0_TIM16_CH1	B13	Used as GPIO	3.3V	O	
A27	PB2_TIM20_CH2N	A14	Used as GPIO	3.3V	O	
A28	PB15	AE6	Used as GPIO	3.3V	O	
A29	PD8_TIM1_CH4	C16	chip select	3.3V	O	
A30	PH4_BOOTFAILN_UART7_TX	AB16	Used as GPIO	3.3V	O	
A31	PA4_USART2_TX	AG17	data transmission	3.3V	O	Debugging serial port
A32	PD4	C18	Used as GPIO	3.3V	O	
A33	PD7	D20	Used as GPIO	3.3V	O	
A34	PB11_FDCAN1_RX	A11	CAN1 bus signal input	3.3V	I	
A35	PB9_FDCAN1_TX	F10	CAN1 bus data transmission	3.3V	O	
A36	GND	/	GND			
A37	NC	/	/			
A38	PF12_I2S1_SDI	P4	Audio data signal input	3.3V	I	
A39	JTCK_SWCLK	AA5	JTAG clock signal	3.3V	I	
A40	PONKEY_N	/	Wake up function	3.3V	O	
A41	PG1_I2C3_SCL	AD4	I2C3 data signal	3.3V	I/O	
A42	PG2_I2C3_SDA	AG5	I2C3 clock signal output	3.3V	O	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
A43	PH5_TIM2_CH1	AG18	Used as GPIO	3.3V	O	
A44	PD0_UART7_RX	B17	Used as GPIO	3.3V	O	
A45	PD9_I2S1_SDO	C15	Audio data signal output	3.3V	O	
A46	PD10	C17	Used as GPIO	3.3V	O	
A47	PD1_FDCAN3_RX	A19	Used as GPIO	3.3V	O	
A48	PD2_FDCAN3_TX	D12	Used as GPIO	3.3V	O	
A49	PG6_I2S1_CK	T3	Audio sampling clock signal	3.3V	O	
A50	PB13_SDMMC3_CK	A26	SDMMC3 Clock signal	3.3V	O	
A51	PD12_SDMMC3_CMD	B26	SDMMC3 Sends commands and replies	3.3V	O	
A52	PB12_SDMMC3_D2	C26	SDMMC3 Data 2 signal	3.3V	I/O	
A53	PI11_SDMMC3_D3	B27	SDMMC3 Data 3 signal	3.3V	I/O	
A54	PB14_SDMMC3_D0	C27	SDMMC3 Data 0 signal	3.3V	I/O	
A55	PD13_SDMMC3_D1	D25	SDMMC3 Data 1 signal	3.3V	I/O	
A56	PD5_TIM1_CH3N	B18	Used as GPIO	3.3V	O	
B1	PA14_ETH1_RGMII_RX_CLK	AB12	RGMII1 Receive the clock signal	3.3V	I	
B2	PH11_ETH1_RGMII_TXD3	AE14	RGMII1 Sends data 3	3.3V	O	
B3	PH10_ETH1_RGMII_TXD2	AF14	RGMII1 Sends data 2	3.3V	O	
B4	PH13_ETH1_RGMII_RXD3	AG13	RGMII1 Receive data 3	3.3V	I	
B5	PA15_ETH1_RGMII_TXD0	AE13	RGMII1 Sends data 0	3.3V	O	
B6	PC1_ETH1_RGMII_TXD1	AG14	RGMII1 Sends data 1	3.3V	O	
B7	PCIE-CLKP-IN	AE25	PCIE Differential clock signal input +	-	A	
B8	PCIE-CLKN-IN	AE26	PCIE Differential clock signal input -	-	A	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
B9	PCIE-CLKP-OUT	AF26	PCIE Differential clock signal output+	-	A	
B10	PCIE-CLKN-OUT	AG26	PCIE Differential clock signal output -	-	A	
B11	USBH_N	AG21	USB2.0 data Differential signal -	3.3V	I/O	
B12	USBH_P	AF21	USB2.0 data Differential signal +	3.3V	I/O	
B13	COMBOPHY_TX1P	AE24	USB3.0 data Differential signal +	-	A	
B14	COMBOPHY_TX1N	AD24	USB3.0 data Differential signal -	-	A	
B15	PC10_ETH2_RGMII_TXD3	AG10	RGMII2 Send data 3	3.3V	O	
B16	PF4_ETH2_CLK	AF10	RGMII2 Outputs the clock signal	3.3V	O	
B17	PC8_ETH2_RGMII_TXD1	AG9	RGMII2 Send data 1	3.3V	O	
B18	PC7_ETH2_RGMII_TXD0	AF9	RGMII2 Send data 0	3.3V	O	
B19	PC9_ETH2_RGMII_TXD2	AE9	RGMII2 Send data 2	3.3V	O	
B20	PF9_ETH2_RGMII_RXD2	AE8	RGMII2 Receive data 2	3.3V	I	
B21	PA11_ETH1_RGMII_RX_CTL	AD12	RGMII1 Receive the data control signal	3.3V	I	
B22	PA13_ETH1_RGMII_TX_CTL	AD14	RGMII1 sends a data control signal	3.3V	O	
B23	PF1_ETH1_RGMII_RXD0	AE11	RGMII1 Receive data 0	3.3V	I	
B24	PC2_ETH1_RGMII_RXD1	AE12	RGMII1 Receive data 1	3.3V	I	
B25	PH12_ETH1_RGMII_RXD2	AF13	RGMII1 Receive data 2	3.3V	I	
B26	PA5_ETH3_RGMII_RX_CLK	AE17	RGMII3 Receive clock signals	3.3V	I	
B27	PA6_ETH3_RGMII_TXD0	AF18	RGMII3 Sends data 0	3.3V	O	
B28	PA2_ETH3_RGMII_RX_CTL	AF17	RGMII3 Receive the data control signal	3.3V	I	
B29	COMBOPHY_RX1N	AF25	USB3.0 Receive data Differential signals -	-	A	
B30	COMBOPHY_RX1P	AG25	USB3.0 Receive data Differential signals +	-	A	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
B31	USB3DR_DP	AF22	USB3 data Differential signal +	3.3V	I/O	
B32	USB3DR_DM	AG22	USB3 data Differential signal -	3.3V	I/O	
B33	PF8_ETH2_RGMII_CLK125	AE10	RGMII2 Indicates the clock signal	3.3V	I	
B34	PC11_ETH2_RGMII_RXD3	AD8	RGMII2 Receive data 3	3.3V	I	
B35	PC4_ETH2_RGMII_TX_CTL	AC9	RGMII2 Receive the data control signal	3.3V	I	
B36	PC12_ETH2_RGMII_RXD1	AE7	RGMII2 Receive data 1	3.3V	I	
B37	PG0_ETH2_RGMII_RXD0	AF7	RGMII2 Receive data 0	3.3V	I	
B38	PC0_ETH1_RGMII_GTX_CLK	AB14	RGMII1 sends a clock signal	3.3V	O	
B39	PA12_ETH1_PHY_INTN	AC13	Used as GPIO	3.3V	O	
B40	PF2_ETH1_MDIO	AC15	RGMII1 Manages data signals	3.3V	I/O	
B41	PH3_ETH3_RGMII_TXD3	AE19	RGMII3 sends data signal 3	3.3V	O	
B42	GND	/	GND			
B43	PH6_ETH3_RGMII_TXD2	AF19	RGMII3 sends data signal 2	3.3V	O	
B44	PA7_ETH3_RGMII_TXD1	AE18	RGMII3 sends data signal 1	3.3V	O	
B45	PA1_ETH3_PHY_INTN	AC19	Used as GPIO	3.3V	O	
B46	PC6_ETH2_MDC	AB10	RGMII2 Manages data clock signals	3.3V	O	
B47	PF5_ETH2_PHY_INTN	AA11	Used as GPIO	3.3V	O	
B48	PC5_ETH2_MDIO	AD10	RGMII2 Manages data signals	3.3V	I/O	
B49	PF6_ETH2_RGMII_RX_CLK	AC7	RGMII2 Receive the clock signal	3.3V	I	
B50	PF7_ETH2_RGMII_GTX_CLK	AB8	RGMII2 sends the clock signal	3.3V	O	
B51	PC3_ETH2_RGMII_RX_CTL	AA9	RGMII2 Receive the data control signal	3.3V	I	
B52	PA10_ETH3_RGMII_RXD1	AE15	RGMII3 Data Receive signal 1	3.3V	I	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
B53	PH7_ETH3_RGMII_RXD2	AE16	RGMII3 Data Receive signal 2	3.3V	I	
B54	PA3_ETH3_RGMII_TX_CTL	AD18	RGMII3 sends data control signals	3.3V	O	
B55	PH2_ETH3_RGMII_GTX_CLK	AC17	RGMII3 sends a clock signal	3.3V	O	
B56	PH8_ETH3_RGMII_RXD3	AD16	RGMII3 Data Receive signal 3	3.3V	I	
B57	PA9_ETH3_RGMII_RXD0	AF15	RGMII3 Data Receive signal 0	3.3V	I	
B58	PF0_ETH1_MDC	AA15	RGMII1 Manages data clock signals	3.3V	O	
B59	PH9_ETH1_RGMII_CLK125	AA13	RGMII1 Indicates the clock signal	3.3V	I	
B60	PF3_ETH1_CLK	AF11	RGMII1 Clock signal	3.3V	O	
C1	LVDS1_CLK_N	K2	LVDS1 Differential clock signal -	1.8V	O	
C2	LVDS1_CLK_P	K1	LVDS1 Differential clock signal +	1.8V	O	
C3	LVDS1_TX1_N	H4	LVDS1 Differential data signal 1 -	1.8V	O	
C4	LVDS1_TX1_P	H3	LVDS1 Differential data signal 1 +	1.8V	O	
C5	LVDS1_TX0_N	G3	LVDS1 Differential data signal 0 -	1.8V	O	
C6	LVDS1_TX0_P	G2	LVDS1 Differential data signal 0 +	1.8V	O	
C7	LVDS2_CLK_N	F2	LVDS2 Differential clock signal -	1.8V	O	
C8	LVDS2_CLK_P	F1	LVDS2 Differential clock signal +	1.8V	O	
C9	LVDS2_TX1_N	C3	LVDS2 Differential data signal 1 -	1.8V	O	
C10	LVDS2_TX1_P	C2	LVDS2 Differential data signal 1 +	1.8V	O	
C11	LVDS2_TX0_N	B2	LVDS2 Differential data signal 0 -	1.8V	O	
C12	LVDS2_TX0_P	B1	LVDS2 Differential data signal 0 +	1.8V	O	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
C13	DSI_D3_N	B6	DSI Differential data signal 3 -	1.8V	I	
C14	DSI_D3_P	A6	DSI Differential data signal 3 +	1.8V	I	
C15	PZ6_SPI8_NSS	V4	Used as GPIO	3.3V	O	
C16	PZ3	Y6	Used as GPIO	3.3V	O	
C17	PZ2	W5	Used as GPIO	3.3V	O	
C18	PZ9_I2C8_SDA	U3	I2C8 data signal	3.3V	I/O	
C19	PZ4_I2C8_SCL	V3	I2C8 clock signal	3.3V	O	
C20	LVDS1_TX3_N	L3	LVDS1 Differential data signal 3 -	1.8V	O	
C21	LVDS1_TX3_P	L2	LVDS1 Differential data signal 3 +	1.8V	O	
C22	LVDS1_TX2_N	J2	LVDS1 Differential data signal 2 -	1.8V	O	
C23	LVDS1_TX2_P	J1	LVDS1 Differential data signal 2 +	1.8V	O	
C24	LVDS2_TX3_N	E2	LVDS2 Differential data signal 3 -	1.8V	O	
C25	LVDS2_TX3_P	E1	LVDS2 Differential data signal 3 +	1.8V	O	
C26	LVDS2_TX2_N	D3	LVDS2 Differential data signal 2 -	1.8V	O	
C27	LVDS2_TX2_P	E3	LVDS2 Differential data signal 2 +	1.8V	O	
C28	CSI_D0_N	A3	CSI Differential data signal 0 -	1.8V	O	
C29	CSI_D0_P	B3	CSI Differential data signal 0 +	1.8V	O	
C30	DSI_D0_N	C9	DSI Differential data signal 0 -	1.8V	I	
C31	DSI_D0_P	B9	DSI Differential data signal 0 +	1.8V	I	
C32	PD3_SDMMC1_DET	G13	SD card detects signal	3.3V	I	
C33	SDMMC1_D3	C19	SDIO data signal 3	3.3V	I/O	
C34	SDMMC1_CK	C21	SDIO clock signal	3.3V	O	
C35	SDMMC1_D0	B21	SDIO data signal 0	3.3V	I/O	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
C36	BOOT3	AB2	Boot item 3	3.3V	O	BOOT
C37	BOOT1	AA3	Boot item 1	3.3V	O	BOOT
C38	BOOT2	AB1	Boot item 2	3.3V	O	BOOT
C39	BOOT0	Y3	Boot item 0	3.3V	O	BOOT
C40	GND	/	GND			
C41	CSI_CLK_N	D4	CSI Differential clock signal -	1.8V	O	
C42	CSI_CLK_P	C4	CSI Differential clock signal +	1.8V	O	
C43	CSI_D1_N	C5	CSI Differential data signal 1 -	1.8V	O	
C44	CSI_D1_P	B5	CSI Differential data signal 1 +	1.8V	O	
C45	PB5_I2C2_SCL	C14	Used as GPIO	3.3V	O	
C46	SDMMC1_D2	B19	SDIO data Signal 2	3.3V	I/O	
C47	SDMMC1_CMD	C20	SDIO control instruction signal	3.3V	O	
C48	SDMMC1_D1	C22	SDIO data signal 1	3.3V	I/O	
C49	PG3_ADC1_INP3	AA7	Used as GPIO	3.3V	O	
C50	DSI_CLK_N	C8	DSI Differential clock signal -	1.8V	I	
C51	DSI_CLK_P	C7	DSI Differential clock signal +	1.8V	I	
C52	DSI_D2_N	A7	DSI Differential data signal 2 -	1.8V	I	
C53	DSI_D2_P	B7	DSI Differential data signal 2 +	1.8V	I	
C54	PB4_I2C2_SDA	B15	I2C2 data signal	3.3V	I/O	
C55	DSI_D1_N	A10	DSI Differential data signal 1 -	1.8V	I	
C56	DSI_D1_P	B10	DSI Differential data signal 1 +	1.8V	I	
D1	PZ7	V2	Used as GPIO	3.3V	O	
D2	PI8	U5	Used as GPIO	3.3V	O	
D3	PI3_USART1_CTS	N7	Used as GPIO	3.3V	O	
D4	PZ8	V1	Used as GPIO	3.3V	O	
D5	PI0	L7	Used as GPIO	3.3V	O	
D6	PI4	P6	Used as GPIO	3.3V	O	
D7	PZ5_SPI8_SCK	R5	Used as GPIO	3.3V	O	

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
D8	JTMS_SWIO	AE2	JTAG mode Select pin	3.3V	I/O	
D9	VDD_3V3BAT_IN	T6	Internal RTC power input	3.3V	I	
D10	JTDI	AE3	JTAG data entry pin	3.3V	I	
D11	RST_N	AE1	CPU reset signal	3.3V	I	
D12	JTRST_N	AF3	JTAG reset pin	3.3V	I	
D13	JTDO_SWDO	AC2	JTAG data output pin	3.3V	O	
D14	PG7_I2S1_WS	U2	I2S1 slice selection signal	3.3V	O	
D15	PF14_USART6_RX	P3	Serial port 6 Receive data signals	3.3V	I	
D16	PF13_USART6_TX	P2	Serial port 6 sends data signals	3.3V	O	
D17	GND	/	GND			
D18	/	/	/			
D19	/	/	/			
D20	GND	/	GND			
D21	PI2	N5	Used as GPIO	3.3V	O	
D22	PI9_FDCAN2_TX	U1	Used as GPIO	3.3V	O	
D23	PI10_FDCAN2_RX	D16	Used as GPIO	3.3V	O	
D24	PB10_I2S3_SDI	B11	I2S3 data input signal	3.3V	I	
D25	PB8_I2S3_SDO	D8	I2S3 data output signal	3.3V	O	
D26	PB1_I2S3_WS	C12	I2S3 slice selection signal	3.3V	O	
D27	PF10_UART8_TX	AE5	Used as GPIO	3.3V	O	
D28	PF11_UART8_RX	AE4	Used as GPIO	3.3V	O	
D29	PG11_SPI7_MOSI	N2	SPI7 Main out and in	3.3V	I/O	
D30	PG13_SPI7_SCK	P1	SPI7 clock signal	3.3V	I/O	
D31	GND	/	GND			
D32	/	/	/			
D33	PF15_USART6_CTS	R2	Band flow control sends an allow signal	3.3V	O	
D34	PG5_USART6_RTS	R3	Band flow control sends a	3.3V	I	



Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
			request signal			
D35	GND	/	GND			
D36	PG12_SPI7_MISO	N3	SPI7 Main in and out	3.3V	I/O	
D37	GND	/	GND	0V		
D38	PI6_USART3_TX	J3	Used as GPIO	3.3V	O	
D39	PI7_USART3_RX	J5	Used as GPIO	3.3V	O	
D40	PI1_SPI7_NSS	M6	SPI7 slice select signal	3.3V	I/O	
D41	PZ1_SPI8_MISO	U7	Used as GPIO	3.3V	O	
D42	/	/	/			
D43	GND	/	GND			
D44	/	/	/			
D45	/	/	/			
D46	PG9_UART5_TX	M3	Serial port 5 sends data signals	3.3V	O	
D47	PG10_UART5_RX	M4	Serial port 5 Receive data signals	3.3V	I	
D48	/	/	/			
D49	GND	/	GND			
D50	/	/	/			
D51	/	/	/			
D52	PZ0_SPI8_MOSI	T4	Used as GPIO	3.3V	O	
D53	PI5_UART9_RX	K4	Serial port 9 Receive data signals	3.3V	O	
D54	PG8_UART9_TX	L5	Serial port 9 sends data signals	3.3V	I	
D55	PG15_USART1_RX	K6	Serial port 1 Receive data signals	3.3V	O	
D56	PG14_USART1_TX	N1	Serial port 1 sends data signals	3.3V	I	
D57	/	/	/			
D58	GND	/	GND			

Pin	Signal	CPU number	Default function description	Voltage	I/O	remark
D59	/	/	/			
D60	/	/	/			
1	GND	/	GND			
2	GND	/	GND			
3	GND	/	GND			
4	GND	/	GND			
5	GND	/	GND			
6	GND	/	GND			
7	GND	/	GND			
8	GND	/	GND			
9	GND	/	GND			
10	GND	/	GND			
11	GND	/	GND			
12	GND	/	GND			
13	GND	/	GND			
14	GND	/	GND			
15	GND	/	GND			
16	GND	/	GND			
17	GND	/	GND			
18	GND	/	GND			
19	GND	/	GND			
20	GND	/	GND			

Table 3-1 MYC-LD25X SOM Pin List

4. Electrical specification

4.1. Main power supply

The main power supply of the MYC-LD25X SOM is VSYS_5V, They correspond to the four pins A1, A2, A3 and A4 of the LGA package. In order to ensure normal operation, the evaluation board must provide a voltage of $5V \pm 5\%$ and a current of about 2A to ensure that the output capacity of the power supply circuit can meet the power consumption of the SOM. This section lists the power consumption and current of the SOM under various conditions. Please reserve an appropriate margin when designing the power supply circuit.

Note: Ensure that the SOM is powered on first, and the evaluation board is powered on again, Otherwise the current is poured back into the GPIO, which will cause the processor to fail to start.

power network	describe	Recommended voltage value
VSYS_5V	Main supply voltage, 5V input, 2-3A	5V
VDD_3V3_OUT	SOM 3.3V output, max output 500mA	3.3V
VDD_SDCARD	SOM 3.3V output, max output 300mA	3.3V
VDDIO_SDCARD	It currently shares the same network with VDD_3V3_OUT, Customized to 1.8V, need to contact sales	3.3V

Table 4-1 External input and output voltage

4.2. Power consumption

operating conditions	Supply voltage (V)	Average current (A)	Total power consumption (W)
The no-load phase	5V	0.181	0.904
The Full-load phase (ENET*2+USB*2+HDMI+MIP I CSI camera+otg+SD Card*1 +aging)	5V	0.35	1.750
The Full-load phase (ENET*2+USB*2+LVDSI+MIP I CSI camera+otg+SD Card*1 +aging)	5V	0.378	1.892
The mem is dormant (echo mem)	5V	0.0176	0.088
freeze hibernation (echo freeze)	The software does not support Freeze hibernation mode		

Table 4-2 Power consumption parameter

4.3. GPIO DC features

Parameter	Symbol	Min	Typical	Max	Units	description
High-lever DC output voltage	$V_{OH(1.8V)}$	1.4	—	1.8	V	
	$V_{OH(3.3V)}$	2.8	—	3.3	V	
Low-lever DC output voltage	$V_{OL(1.8V)}$	—	—	0.4	V	
	$V_{OL(3.3V)}$	0	—	0.4	V	
High-lever DC input voltage	$V_{IH(1.8V)}$	1.17	—	2.1	V	
	$V_{IH(3.3V)}$	2	—	3.6	V	
Low-lever DC input voltage	$V_{IL(1.8V)}$	-0.3	—	0.36	V	
	$V_{IL(3.3V)}$	-0.3	—	0.63	V	

Table 4-3 I/O DC characteristics

5. System necessary circuit design

5.1. Boot configuration circuit

With the MYC-LD25X SOM, When designing the BOOT option, you can use a dip switch or jumper cap. The processor can be started according to the corresponding boot item (EMMC, SD card). evaluation board design The pull-up resistance must be reserved for the BOOT option. The recommended power supply is 3V3 output by the SOM, Boot 3-Boot 0 output by the SOM is low by default, Users can design according to their needs.

5.2. Burn firmware circuit

MicroSD Card circuit is recommended for the MYC-LD25X SOM to burn and update the firmware, and SDMMC1 is recommended for the signal interface. To burn the firmware, you need to set the boot item to start from the SD card, and the factory default is that the image has been burned. Refer to the MicroSD Card section in Section 6.1.

5.3. Debug circuit

The recommended debugging serial ports for MYC-LD25X SOM are UART2 and UART5. UART2 and UART5 are debugging serial ports by default and cannot be replaced with other debugging serial ports. Generally, UART2 is used for software debugging ARM.

5.4. Reset circuit

With the MYC-LD25X SOM, the RESET signal is led out by the PIN D11 pin of the SOM, which is used for the hardware system of the to reset the input signal, 3.3V level logic, and the evaluation board design is best with logical isolation to prevent external interference.

6. Interface specification

6.1. SD/MMC interface

The MYC-LD25X SOM is equipped with three SD/MMC interfaces, namely SDMMC1, SDMMC2 and SDMMC3. SDMMC1 is usually used to design MicroSD card signals; SDMMC2 has been used to connect EMMC signals in the core board. SDMMC3 is a 3.3V level and can be used to design a communication interface between modules with an SDIO interface.

6.1.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	C34	SDMMC1_CK	C21	SDMMC1 clock signal	3.3V	O	
	C35	SDMMC1_D0	B21	SDMMC1 data signal 0	3.3V	I/O	
	C48	SDMMC1_D1	C22	SDMMC1 data signal 1	3.3V	I/O	
	C46	SDMMC1_D2	B19	SDMMC1 data signal 2	3.3V	I/O	
	C33	SDMMC1_D3	C19	SDMMC1 data signal 3	3.3V	I/O	
	C47	SDMMC1_CMD	C20	SDMMC1 Control command signal	3.3V	O	
	C32	PD3_SDMMC1_DET	G13	SD card detects signal	3.3V	I	
-	A50	PB13_SDMMC3_CK	A26	SDMMC3 clock signal	3.3V	O	
	A54	PB14_SDMMC3_D0	C27	SDMMC3 data signal 0	3.3V	I/O	
	A55	PD13_SDMMC3_D1	D25	SDMMC3 data signal 1	3.3V	I/O	
	A52	PB12_SDMMC3_D2	C26	SDMMC3 data signal 2	3.3V	I/O	
	A53	PI11_SDMMC3_D3	B27	SDMMC3 data signal 3	3.3V	I/O	
	A51	PD12_SDMMC3_CMD	B26	SDMMC3 Control command signal	3.3V	O	

Table 6-1 SD/MMC interface PIN definitions

6.2. UART interface

MYC-LD25X SOM Processor with up to 9 serial ports (5xUART+4xUSART),The SOM draws all of these pins out,The SOM is configured with five serial ports by default,The two serial ports USART2 and UART5 are debugging serial ports by default,one configuration for WIFI module communication,The other two lead to a 2.54MM spaced 2*20 Pin double row,It can be externally connected to the Raspberry PI module,If you want to use more serial ports, consult the chip manual or pin list and modify the pin configuration in the driver.

6.2.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
	D56	PG14_USART1_TX	N1	Serial port 1 sends data signals	3.3V	I	
	D55	PG15_USART1_RX	K6	Serial port 1 Receive data signals	3.3V	O	
	A31	PA4_USART2_TX	AG17	Serial port 2 sends data signals	3.3V	I	
	A14	PA8_USART2_RX	AA17	Serial port 2 Receive data signals	3.3V	O	
	D46	PG9_UART5_TX	M3	Serial port 5 sends data signals	3.3V	O	
	D47	PG10_UART5_RX	M4	Serial port 5 Receive data signals	3.3V	I	
	D16	PF13_USART6_TX	P2	Serial port 6 sends data signals	3.3V	O	
	D15	PF14_USART6_RX	P3	Serial port 6 Receive data signals	3.3V	I	
	D33	PF15_USART6_CTS	R2	Band flow control sends an allow signal	3.3V	O	
	D34	PG5_USART6_RTS	R3	Band flow control sends a request signal	3.3V	I	
	D54	PG8_UART9_TX	L5	Serial port 9 sends data signals	3.3V	O	
	D53	PI5_UART9_RX	K4	Serial port 9 Receive data signals	3.3V	I	

Table 6-2 UART interface PIN Definition

6.3. USB interface

The MYC-LD25X SOM Provides one USB2.0 HOST and one USB2.0 OTG. USB3DR Supports HOST, Device Mode, burning Program can only use USB3DR port, USBH only supports HOST mode, USB2.0 maximum speed of 480Mbps.

6.3.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	B11	USBH_N	AG21	USBH data Differential signal -	3.3V	I/O	
	B12	USBH_P	AF21	USBH data Differential signal +	3.3V	I/O	
	B31	USB3DR_DP	AF22	USB3DR data Differential signal +	3.3V	I/O	
	B32	USB3DR_DM	AG22	USB3DR data Differential signal -	3.3V	I/O	
	B13	COMBOPHY_TX1P	AE24	Send data Differential signal +	-	A	
	B14	COMBOPHY_TX1N	AD24	Send data Differential signal -	-	A	
	B30	COMBOPHY_RX1P	AF17	Receive data Differential signal +	-	A	
	B29	COMBOPHY_RX1N	AF25	Receive data Differential signal -	-	A	

Table 6-3 USB interface PIN definition

6.4. CAN interface

The MYC-LD25X SOM leads three CAN FD bus signals, and one leads to a 2*20 Pin double-row pin with a 2.54MM pitch, which CAN be connected to the Raspberry PI module. The external CAN transceiver will convert the TX and RX level signals into voltage Differential signals to connect to the CAN bus, and communicate with the equipment with CAN interface. The other two multiplexes are GPIO, if you want to use more CAN bus interfaces, please consult the chip manual or Pin List, and modify the pin configuration in the driver.

6.4.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	A35	PB9_FDCAN1_TX	F10	CAN1 bus data transmission	3.3V	O	
	A34	PB11_FDCAN1_RX	A11	CAN1 bus data Receive	3.3V	I	
	D22	PI9_FDCAN2_TX	D16	Used as IO port	3.3V	O	
	D23	PI10_FDCAN2_RX	B11	Used as IO port	3.3V	O	
	A48	PD2_FDCAN3_TX	D12	Used as IO port	3.3V	O	
	A47	PD1_FDCAN3_RX	A19	Used as IO port	3.3V	O	

Table 6-4 CAN interface PIN definition

6.5. Ethernet interface

Three RGMII signals are generated from the MYC-LD25X SOM. Currently the CPU Ethernet interface is configured in RGMII mode. Supports a maximum of three Gigabit Ethernet ports (1 Gigabit Ethernet GMAC with one external PHY interface, 1 Gigabit Ethernet GMAC with one external PHY interface with optional internal connection to an embedded Ethernet switch with two external PHY interfaces). When the user designs the evaluation board circuit, it is necessary to design the Ethernet PHY circuit, the transformer isolation circuit and the RJ45 part of the circuit.

6.5.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Volt age	I/O	Comments
	B58	PF0_ETH1_MDC	AA15	RGMII1 Manages data clock signals	3.3V	O	Shared with RGMII3
	B40	PF2_ETH1_MDIO	AC15	RGMII1 Manages data signals	3.3V	I/O	Shared with RGMII3
	B38	PC0_ETH1_RGMII_GTX_CLK	AB14	RGMII1 sends a clock signal	3.3V	O	
	B22	PA13_ETH1_RGMII_TX_CTL	AD14	RGMII1 Transmitter control signal	3.3V	O	
	B5	PA15_ETH1_RGMII_TXD0	AE13	RGMII1 Data signal 0 at the sender end	3.3V	O	
	B6	PC1_ETH1_RGMII_TXD1	AG14	RGMII1 Sender data signal 1	3.3V	O	
	B3	PH10_ETH1_RGMII_TXD2	AF14	RGMII1 Sender data signal 2	3.3V	O	
	B2	PH11_ETH1_RGMII_TXD3	AE14	RGMII1 Sender data signal 3	3.3V	O	
	B1	PA14_ETH1_RGMII_RX_CLK	AB12	RGMII1 Clock signal of the receive end	3.3V	I	
	B21	PA11_ETH1_RGMII_RX_CTL	AD12	RGMII1 receive control signal	3.3V	I	
	B23	PF1_ETH1_RGMII_RXD0	AE11	RGMII2 receive data signal 0	3.3V	I	
	B24	PC2_ETH1_RGMII_RXD1	AE12	RGMII1 receive data signal 1	3.3V	I	
	B25	PH12_ETH1_RGMII_RXD2	AF13	RGMII1 receive data signal 2	3.3V	I	
	B4	PH13_ETH1_RGMII_RXD3	AG13	RGMII1 receive data signal 3	3.3V	I	
	B39	PA12_ETH1_PHY_INTN	AC13	Used as an IO port signal	3.3V	O	
	D6	PI4	P6	Used as an IO port signal	3.3V	O	
	B60	PF3_ETH1_CLK	AF11	Unused	3.3V	O	

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
	B59	PH9_ETH1_RGMII_CLK125	AA13	RGMII1 Indicates the clock signal	3.3V	I	
	B46	PC6_ETH2_MDC	AB10	RGMII2 Manages data clock signals	3.3V	O	
	B48	PC5_ETH2_MDIO	AD10	RGMII2 Manages data signals	3.3V	I/O	
	B50	PF7_ETH2_RGMII_GTX_CLK	AB8	RGMII2 sends the clock signal	3.3V	O	
	B35	PC4_ETH2_RGMII_TX_CTL	AC9	RGMII2 Transmitter control signal	3.3V	O	
	B18	PC7_ETH2_RGMII_TXD0	AF9	RGMII2 Sender data signal 0	3.3V	O	
	B17	PC8_ETH2_RGMII_TXD1	AG9	RGMII2 Sender data signal 1	3.3V	O	
	B19	PC9_ETH2_RGMII_TXD2	AE9	RGMII2 Sender data signal 2	3.3V	O	
	B15	PC10_ETH2_RGMII_TXD3	AG10	RGMII2 Sender data signal 3	3.3V	O	
	B49	PF6_ETH2_RGMII_RX_CLK	AC7	RGMII2 Clock signal of the receive end	3.3V	I	
	B51	PC3_ETH2_RGMII_RX_CTL	AA9	RGMII2 receive control signal	3.3V	I	
	B37	PG0_ETH2_RGMII_RXD0	AF7	RGMII2 receive data signal 0	3.3V	I	
	B36	PC12_ETH2_RGMII_RXD1	AE7	RGMII2 receive data signal 1	3.3V	I	
	B20	PF9_ETH2_RGMII_RXD2	AE8	RGMII2 receive data signal 2	3.3V	I	
	B34	PC11_ETH2_RGMII_RXD3	AD8	RGMII2 receive data signal 3	3.3V	I	
	B47	PF5_ETH2_PHY_INTN	AA11	Used as an IO port signal	3.3V	O	
	A27	PB2_TIM20_CH2N	A14	Used as an IO port signal	3.3V	O	
	B16	PF4_ETH2_CLK	AF10	Unused	3.3V	O	
	B33	PF8_ETH2_RGMII_CLK125	PF8	RGMII2 Indicates the clock signal	3.3V	I	
	B55	PH2_ETH3_RGMII_GTX_CLK	AC17	RGMII3 sends a clock signal	3.3V	O	
	B54	PA3_ETH3_RGMII_TX_CTL	AD18	RGMII3 Transmitter control signal	3.3V	O	
	B27	PA6_ETH3_RGMII_TXD0	AF18	RGMII3 Transmitter data signal 0	3.3V	O	
	B44	PA7_ETH3_RGMII_TXD1	AE18	RGMII3 Transmitter data signal 1	3.3V	O	

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
	B43	PH6_ETH3_RGMII_TXD2	AF19	RGMII3 Transmitter data signal 2	3.3V	O	
	B41	PH3_ETH3_RGMII_TXD3	AE19	RGMII3 Transmitter data signal 3	3.3V	O	
	B26	PA5_ETH3_RGMII_RX_CLK	AE17	RGMII3 Clock signal of the receive end	3.3V	I	
	B28	PA2_ETH3_RGMII_RX_CTL	AF17	RGMII3 Receiver control signal	3.3V	I	
	B57	PA9_ETH3_RGMII_RXD0	AF15	RGMII3 receive data signal 0	3.3V	I	
	B52	PA10_ETH3_RGMII_RXD1	AE15	RGMII3 receive data signal 1	3.3V	I	
	B53	PH7_ETH3_RGMII_RXD2	AE16	RGMII3 receive data signal 2	3.3V	I	
	B56	PH8_ETH3_RGMII_RXD3	AD16	RGMII3 receive data signal 3	3.3V	I	
	B45	PA1_ETH3_PHY_INTN	AC19	Used as an IO port signal	3.3V	O	
	A46	PD10	C17	Used as an IO port signal	3.3V	O	

Table 6-5 PIN Definition of Ethernet interface

6.6. I2C interface

The MYC-LD25X SOM Processor supports a maximum of 8 I2C buses, of which I2C2 is used for the E2PROM chip in the SOM, I2C7 is used for the PMIC chip in the SOM, I2C7 can not be used, the other 7 I2C are drawn from the SOM, available for use.

If you want to use more I2C bus interfaces, consult the chip manual or Pin List and modify the pin configuration in the driver.

6.6.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	C45	PB5_I2C2_SCL	C14	I2C2 clock signal	3.3V	O	
	C54	PB4_I2C2_SDA	B15	I2C2 data signal	3.3V	I/O	
	A41	PG1_I2C3_SCL	AD4	I2C3 clock signal	3.3V	O	
	A42	PG2_I2C3_SDA	AG5	I2C3 data signal	3.3V	I/O	
	C19	PZ4_I2C8_SCL	V3	I2C8 clock signal	3.3V	O	
	C18	PZ9_I2C8_SDA	U3	I2C8 data signal	3.3V	I/O	

Table 6-6 I2C Interface PIN Definition

6.7. I2S interface

MYC-LD25X SOM leads to 3 I2S interface, the default configuration of 2, another I2S interface pin reuse other functions, if you want to use more I2S interface, please refer to the chip manual or pin list and modify the pin configuration in the driver.

6.7.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	A49	PG6_I2S1_CK	T3	I2S1 clock signal	3.3V	O	
	D14	PG7_I2S1_WS	U2	I2S1 slice selection signal	3.3V	O	
	A45	PD9_I2S1_SDO	C15	I2S1 data output signal	3.3V	O	
	A38	PF12_I2S1_SDI	P4	I2S1 data input signal	3.3V	I	
	A17	PB7_I2S3_CK	C11	I2S3 clock signal	3.3V	O	
	D26	PB1_I2S3_WS	C12	I2S3 slice selection signal	3.3V	O	
	D25	PB8_I2S3_SDO	D8	I2S3 data output signal	3.3V	O	
	D24	PB10_I2S3_SDI	B11	I2S3 data input signal	3.3V	I	

Table 6-7 I2S Interface PIN Definition

6.8. LVDS interface

The MYC-LD25X SOM has two LVDS display output interfaces. Single-channel LVDS interface display, respectively rate 1080x1920@60Hz, dual-channel LVDS interface display resolution up to 1536p60HZ, later support the same screen display.

6.8.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
	C1	LVDS1_CLK_N	K2	LVDS1 Differential clock signal -	1.8V	O	
	C2	LVDS1_CLK_P	K1	LVDS1 Differential clock signal +	1.8V	O	
	C5	LVDS1_TX0_N	G3	LVDS1 Differential data signal 0 -	1.8V	O	
	C6	LVDS1_TX0_P	G2	LVDS1 Differential data signal 0 +	1.8V	O	
	C3	LVDS1_TX1_N	H4	LVDS1 Differential data signal 1 -	1.8V	O	
	C4	LVDS1_TX1_P	H3	LVDS1 Differential data signal 1 +	1.8V	O	
	C22	LVDS1_TX2_N	J2	LVDS1 Differential data signal 2 -	1.8V	O	
	C23	LVDS1_TX2_P	J1	LVDS1 Differential data signal 2 +	1.8V	O	
	C20	LVDS1_TX3_N	L3	LVDS1 Differential data signal 3 -	1.8V	O	
	C21	LVDS1_TX3_P	L2	LVDS1 Differential data signal 3 +	1.8V	O	
	C7	LVDS2_CLK_N	F2	LVDS2 Differential clock signal -	1.8V	O	
	C8	LVDS2_CLK_P	F1	LVDS2 Differential clock signal +	1.8V	O	
	C11	LVDS2_TX0_N	B2	LVDS2 Differential data signal 0 -	1.8V	O	
	C12	LVDS2_TX0_P	B1	LVDS2 Differential data signal 0 +	1.8V	O	
	C9	LVDS2_TX1_N	C3	LVDS2 Differential data signal 1 -	1.8V	O	
	C10	LVDS2_TX1_P	C2	LVDS2 Differential data signal 1 +	1.8V	O	
	C26	LVDS2_TX2_N	D3	LVDS2 Differential data signal 2 -	1.8V	O	
	C27	LVDS2_TX2_P	E3	LVDS2 Differential data signal 2 +	1.8V	O	
	C24	LVDS2_TX3_N	E2	LVDS2 Differential data signal 3 -	1.8V	O	
	C25	LVDS2_TX3_P	E1	LVDS2 Differential data signal 3 +	1.8V	O	

Table 6-8 LVDS Interface PIN Definition

6.9. MIPI CSI interface

MYC-LD25X SOM supports 1 MIPI CSI interface, can be designed as 1 MIPI CSI, 2 channels of data, used as camera input signal.

6.9.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	C42	CSI_CLK_P	C4	CSI clock signal +	1.8V	I	
	C41	CSI_CLK_N	D4	CSI clock signal -	1.8V	I	
	C29	CSI_D0_P	B3	CSI data signal 0 +	1.8V	I	
	C28	CSI_D0_N	A3	CSI data signal 0 -	1.8V	I	
	C44	CSI_D1_P	B5	CSI data signal 1 +	1.8V	I	
	C43	CSI_D1_N	C5	CSI data signal 1 -	1.8V	I	

Table 6-9 MIPI CSI interface PIN Definition

6.10. MIPI DSI interface

MYC-LD25X SOM Supports 1*MIPI DSI interface, can be designed as 1* MIPI DSI, 4 channels of data, used as DSI output signal, also use the conversion chip MIPI DSI output into HDMI video output, you can refer to the design of the backboard.

6.10.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	C51	DSI_CLK_P	C7	DSI clock signal +	1.8V	O	
	C50	DSI_CLK_N	C8	DSI clock signal -	1.8V	O	
	C31	DSI_D0_P	C9	DSI data signal 0 +	1.8V	O	
	C30	DSI_D0_N	B3	DSI data signal 0 -	1.8V	O	
	C56	DSI_D1_P	B10	DSI data signal 1 +	1.8V	O	
	C55	DSI_D1_N	A10	DSI data signal 1 -	1.8V	O	
	C53	DSI_D2_P	B7	DSI data signal 2 +	1.8V	O	
	C52	DSI_D2_N	A7	DSI data signal 2 -	1.8V	O	
	C14	DSI_D3_P	A6	DSI data signal 3 +	1.8V	O	
	C13	DSI_D3_N	B6	DSI data signal 3 -	1.8V	O	

Table 6-10 MIPI DSI pin definition

6.11. SPI interface

MYC-LD25X SOM leads to 8 SPI interfaces, the default is only configured with 1 SPI interface, other SPI interfaces are currently reused into other functions, if you want to use more SPI ports, please refer to the chip manual or pin list and modify the pin configuration in the driver.

6.11.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	D30	PG13_SPI7_SCK	P1	SPI7 clock signal	3.3V	I/O	
	D40	PI1_SPI7_NSS	M6	SPI7 slice select signal	3.3V	I/O	
	D36	PG12_SPI7_MISO	N3	SPI7 Main in and out	3.3V	I/O	
	D29	PG11_SPI7_MOSI	N2	SPI7 Main out and in	3.3V	I/O	

Table 6-11 SPI pin definition

6.12. JTAG interface

The MYC-LD25X SOM Provides a JTAG interface for connecting to the external JTAG debugging device.

6.12.1. Pin definition

Tag Number	SOM PIN	Signal	CPU PIN	Default function description	Voltage	I/O	Comments
-	D10	JTDI	AE3	JTAG data entry pin	3.3V	I	
	D12	JTRST_N	AF3	JTAG reset pin	3.3V	I	
	D13	JTDO_SWDO	AC2	JTAG data output pin	3.3V	O	
	A39	JTCK_SWCLK	AA5	JTAG clock signal	3.3V	I	
	D8	JTMS_SWDIO	AE2	JTAG mode Select pin	3.3V	I/O	

Table 6-12 JTAG pin definition

7. Package information

7.1. Machine dimension

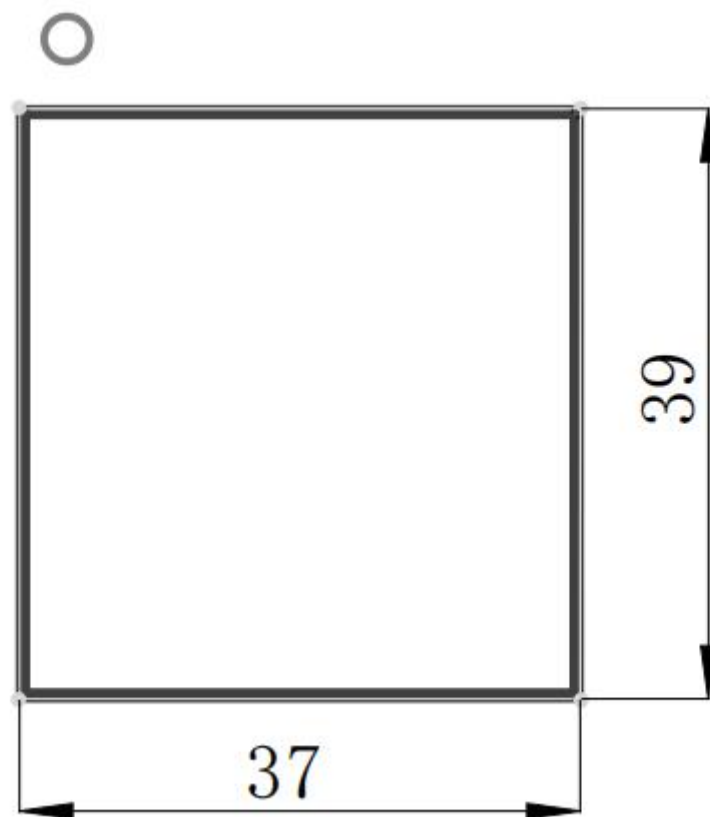


Figure 7-1 Top view of MYC-LD25X SOM(Unit: mm)

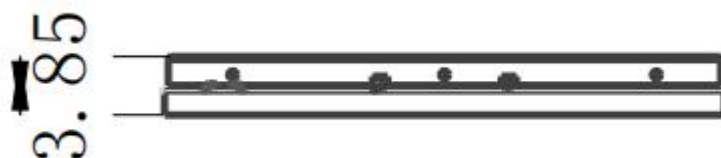


Figure 7-2 MYC-LD25X SOM side view

7.2. Pin spacing

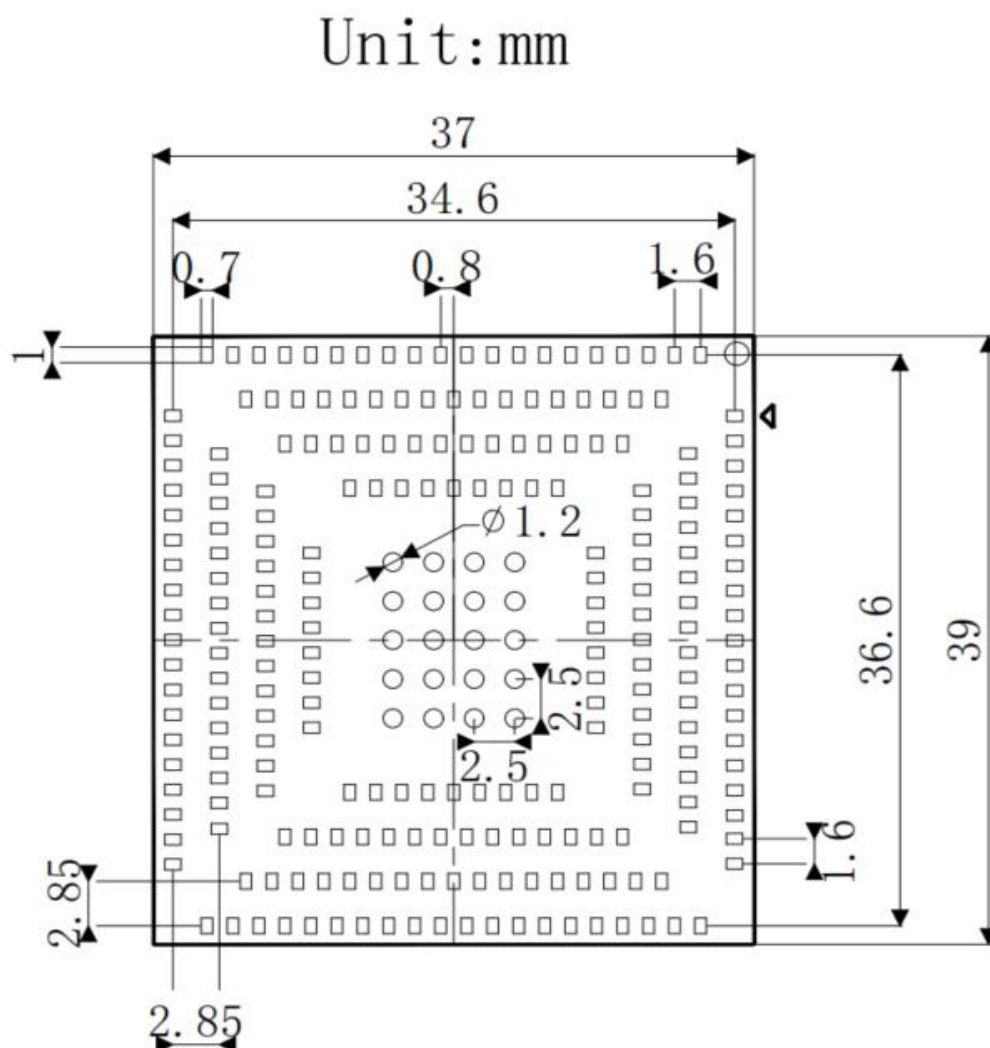


Figure 7-3 Footprint on base board for populate SOM(unit: mm)

7.3. SOM PCB requirements

- a) The warpage of PCB is IPC2 class standard, requiring at least 0.75%.
- b) Symmetrical lamination is required, and the residual copper rate of the symmetrical layer should be close.
- c) Recommended PCB thickness of at least 1.6mm, pay attention to the balance of copper coating, such as PCB deformation in the furnace, it is recommended to use a vehicle to fix the furnace.
- d) In order to ensure the quality of mounting and tinning, please ensure that the distance between the module and other components on the PCB is at least 3mm.
- e) PCB package provided by MYIR Electronics is recommended.

8. Mount and store

8.1. Steel mesh design

- a) The opening requirements of LGA pad steel mesh are recommended to shrink the inside of the pad by 10%, and have a thickness of 0.18mm step.

8.2. Storage requirement

Modules are shipped in vacuum sealed form and storage is subject to the following conditions:

- a) When the ambient temperature is below 40 °C and the air humidity is less than 90%, the vacuum sealed bag can be stored for 12 months.
- b) When the vacuum sealing bag is opened, the ambient temperature is lower than 30°C and the air humidity is less than 30%, the reflow welding can be carried out directly within 72 hours.

Note: If the above conditions are not met, baking should be carried out before the patch.

8.3. Baking method

Because the module packaging material can not withstand high temperature, if necessary, please choose 1 of the following 2 ways to bake, to avoid affecting the welding quality of the module.

- a) Baking of the original package: the baking temperature is 40 ~ 60°C, and the time is 5 ~ 7 days.
- b) Transfer to high temperature tray baking: baking temperature is 100 ~ 120, baking time is more than 48 hours.

8.4. Welding technology

- a) If the substrate to be mounted is double-sided device layout, it is recommended to put the core board mounting process in the last stage.
- b) It is recommended that the preheating area (160 ~ 200°C) be set to 60 ~ 120 seconds.
- c) The recommended reflow temperature is 235 ~ 245 °C , the maximum

cannot exceed 250°C, and the reflow time is recommended to be controlled within 40 ~ 90 seconds.

d) The recommended temperature rise rate is 1 ~ 3°C/ s, and the temperature drop rate is 2 ~ 4°C/ s.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the module design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
 - Hardware or software problems occurred during customers' own development;
 - Problems occurred when customers compile or run the OS which is tailored by themselves;
 - Problems occurred during customers' own applications development;
 - Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receive the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.

- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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