



MYC-LT527M

Hardware Design Guide



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MYIR Electronics Limited



History

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Contents

History	2
Contents	3
1. Overview	7
1.1. Supported products	7
1.2. Disclaimer	7
2. Power supply design	8
2.1. reference circuit	8
2.2. Power Protection	9
2.3. Power Sequence	9
2.4. Layout Guidelines	9
3. System necessary circuit design	11
3.1. Boot	11
3.2. Burning firmware	11
3.3. Debug	11
3.4. Reset	11
4. Key Circuit Design	12
4.1. reference circuit	12
4.2. Layout Guidelines	13
5. Interface circuit design	14



5.1. SD/MMC	14
5.1.1. reference circuit	14
5.1.2. Layout Guidelines	14
5.2. UART	15
5.2.1. reference circuit	15
5.2.2. Layout Guidelines	15
5.3. USB	16
5.3.1. reference circuit	16
5.3.2. Layout Guidelines	16
5.4. Ethernet	17
5.4.1. reference circuit	17
5.4.2. Layout Guidelines	17
5.5. I2C	18
5.5.1. reference circuit	18
5.5.2. Layout Guidelines	18
5.6. LVDS	19
5.6.1. reference circuit	19
5.6.2. Layout Guidelines	19
5.7. Audio Out	20
5.7.1. reference circuit	20
5.7.2. Layout Guidelines	20
5.8. RTC	21
5.8.1. reference circuit	21
5.8.2. Layout Guidelines	21



5.9. WIFI	22
5.9.1. reference circuit	22
5.9.2. Layout Guidelines	22
5.10. DSI	23
5.10.1. reference circuit	23
5.10.2. Layout Guidelines	23
5.11. HDMI	24
5.11.1. reference circuit	24
5.11.2. Layout Guidelines	24
5.12. eDP	25
5.12.1. reference circuit	25
5.12.2. Layout Guidelines	25
5.13. MIPI CSI	26
5.13.1. reference circuit	26
5.13.2. Layout Guidelines	26
5.14. Raspberries pie interface	27
5.14.1. reference circuit	27
5.14.2. Layout Guidelines	27
5.15. LED	28
5.15.1. reference circuit	28
5.15.2. Layout Guidelines	28
6. Design check item	29
6.1. Power supply design	29



6.2. System startup circuit design	29
6.3. Peripheral circuits design	30
Warranty & Technical Support Services	31



1. Overview

This document is intended to help hardware engineers design board-level circuits based on the core module of MYC-LT527M. Please fully understand the content of this document before you begin your design. This document contains common information, such as reference design instructions, Layout suggestions, and design check items, to assist hardware engineers in designing.

The references used in this document are from the official website of MYIR Electronics and are included in the hardware documentation of MYC-LT527M. You can download them at any time from the following address.

<http://d.myirtech.com/MYD-LT527/>

In addition, MYIR Electronics will also provide the following resources to facilitate your design:

- ◆ Core board / evaluation board product manual;
- ◆ Evaluation board principle graphical source file;
- ◆ Related device manuals.

1.1. Supported products

This document applies to all models of MYC-LT527M series core boards.

1.2. Disclaimer

- ◆ Some of reference designs in the document are based on MYIR electronic evaluation boards and cannot be guaranteed to be suitable for all application scenarios. If your product has special requirements for application scenarios or technical specifications, please adjust the design according to the actual situation.
- ◆ Reference design and layout in the document are recommended for reference only and do not necessarily contain all the matters needing attention. Please make adjustments according to the actual situation.
- ◆ MYIR shall not be liable for any form of technical endorsement or joint liability for any proposal contained in any document.

2. Power supply design

The design of the power supply system is very important in the design of embedded products. Engineers need to consider not only the basic electrical parameters of the power supply itself, but also the stability design of the power supply, such as electromagnetic compatibility, temperature range, safety design, three-proof design and other factors. Any negligent factor may cause the whole system to fail to work normally. Before starting the design of a power supply system for a new product, the engineer should thoroughly understand the actual requirements of the entire system, thoroughly demonstrate the feasible design solution based on cost and efficiency, and select an appropriate power supply method for the system.

2.1. reference circuit

The core plate needs to provide 5V voltage for normal operation, and the full load power consumption is close to 5.5W. Considering that the instantaneous current of the product is relatively large and the circuit performance may derate under high temperature conditions, the system cannot start normally if the power supply is insufficient. Therefore, the power supply design should leave a certain margin to ensure the stable and reliable operation of the system. It is recommended that a power chip of about 2-3A be used to power the core board alone. It is not recommended to use the power chip to drive loads other than the core board, especially some high-power load components.

LDO or DCDC can be used as the power chip. LDO has the advantages of simple use, low cost, low electromagnetic interference, but high calorific value. DCDC has the advantages of strong current output capacity, high conversion efficiency, low calorific value, but relatively large electromagnetic interference. If the input voltage is close to 5V, the LDO power chip can be used. If the input voltage is much different from 5V, the DCDC power chip is recommended.

The core board is supplied with 5V power. Please add energy storage capacitance and decoupling capacitance appropriately near the 5V voltage input pin of the core board. Reserve 0.01R resistors to assess core board power consumption. Use a multimeter in MV mode to measure the voltage at both ends. The current flowing through the resistance can be calculated by Ohm's law $I=U/R$, and the power consumption of the core board can be evaluated finally.

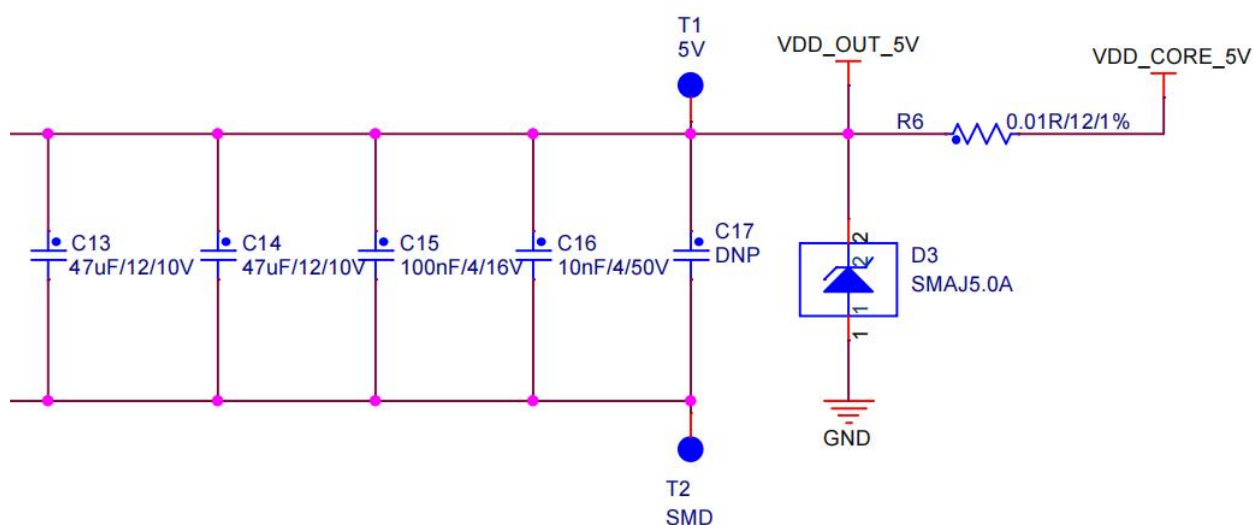


Figure 2-1 Core board 5V power supply

2.2. Power Protection

To ensure the reliability of the power supply system, it is not recommended to directly supply the external input voltage that has not been processed to each load terminal at the rear stage. You can refer to the protection circuit in the following figure to process the power supply before using it to improve the reliability and security of the input power supply and reduce electromagnetic interference. The baseboard input power supply in the reference design is 12V. As an example only, the input power supply value should be determined according to your actual requirements.

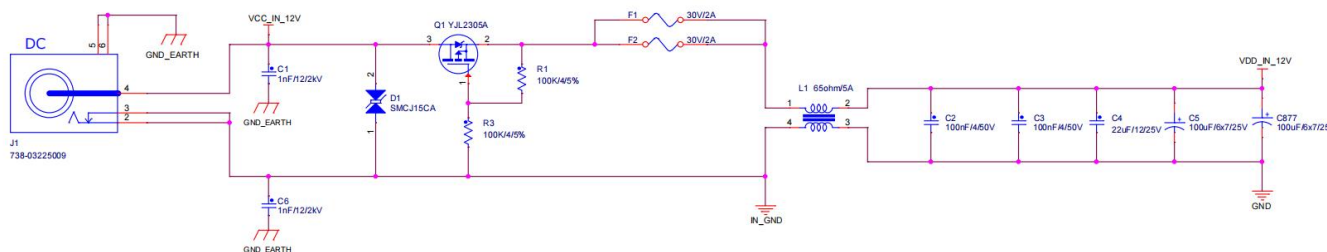


Figure 2-2 General power input circuit

2.3. Power Sequence

The power system design must follow certain power-on timing and corresponding steady-state regulations to ensure the reliable operation of the chip. In the design, it is recommended that the core board should be powered on first, and then the carried board peripheral I/O devices should be powered on. Failure to meet the power-on timing may lead to the following conditions:

- ◆ I/O current from the carried board peripheral backs up to the processor, which fails to start normally.
- ◆ The floor peripheral I/O current flows back to the processor, causing irreversible damage in the worst case.
- ◆ Powering on the mainboard Power on 5V for the core board, then 5V for the control board and 3V3.

2.4. Layout Guidelines

- ◆ The distance between different power planes should be at least 20mil;
- ◆ Widen the width of the power cord and ground wire as far as possible to meet the required rated current value, and the width of the feedback signal should not be too narrow, more than 10mil is recommended;
- ◆ If DCDC is used, it is not recommended to take signal cables below the inductance;
- ◆ If DCDC is used, the path of the current loop should be as short as possible, and the inductor and capacitor should be placed as close to the chip as possible, namely, the red and green paths in the following figure;

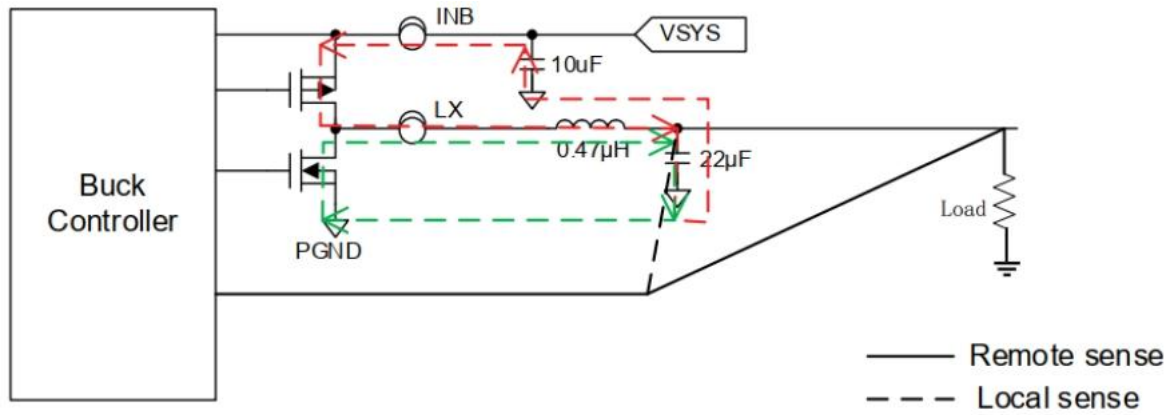


Figure 2-3 DCDC current back flow path

- ◆ If LDO is used, attention should be paid to the thermal resistance of LDO chip. Because the heat loss of LDO chip is relatively high, it is recommended to add grounding pads and make more grounding holes on the pads;
- ◆ Try to select the capacitance of small ESR at the output end;
- ◆ The power chip with digital ground and analog ground should be separated and connected only at a single point at the main power input, and the analog ground should not be connected to the grounding pad.



3. System necessary circuit design

3.1. Boot

With the MYC-LT527M core board, you do not need to pay attention to the boot bit configuration when designing the baseboard. SD card is inserted and the card surface has been burned mirror, the development board will boot from SD card preferentially. After removing the MicroSD card, the development board can be booted from eMMC.

3.2. Burning firmware

Micro SD card circuit is recommended for the core board of MYC-LT527M to burn and update the firmware of the core board, and SMHC0 is recommended for signal interface. Please refer to Section 5.1.

3.3. Debug

It is recommended that the core board of MYC-LT527M use UART interface circuit to debug the software program of the core board. It is recommended that the signal interface use UART5. For details, please refer to Section 5.2.

3.4. Reset

With the MYC-LT527M core board, the RESET signal is led out by the PIN C65 pin of the core board, which is used for the hardware system of the core board to reset the input signal, Core board directly internal pull-up input, and the logic chip is used to open the leakage output of the core board to isolate external interference. Please refer to Section 4 for details. Reset pin level is 1.8V.



4. Key Circuit Design

The MYC-LT527M core board provides special function pins, namely KEY_RESET、PWM-12、FEL、PWRON. These signals are usually used for external keys. Table 4-1 describes the functions.

As the key signal is more sensitive, it is usually possible to use resistance and capacitance to form a simple RC filter. On the one hand, it can filter the jitter interference when the key is pressed, and at the same time filter the interference introduced by the outside to affect the reset signal. In a harsh electromagnetic environment, an ESD device can be connected in parallel to eliminate the electrostatic interference from the key and ensure more reliable operation of the system. If there is a more strict requirement for the elimination of shake, a logic circuit such as RS flip-flop can be considered to set up a reset circuit.

Special function pin	description
KEY_RESET	1.8V level logic. The core board pulls down the 1nF capacitor. Hardware reset input.
PWM-12	3.3V level logic. The user presses a button to generate an event/interrupt.
FEL	Force the burn button to work with USB0 to burn.
PWRON	Wake key

Table 4-1 Special function pins

4.1. reference circuit

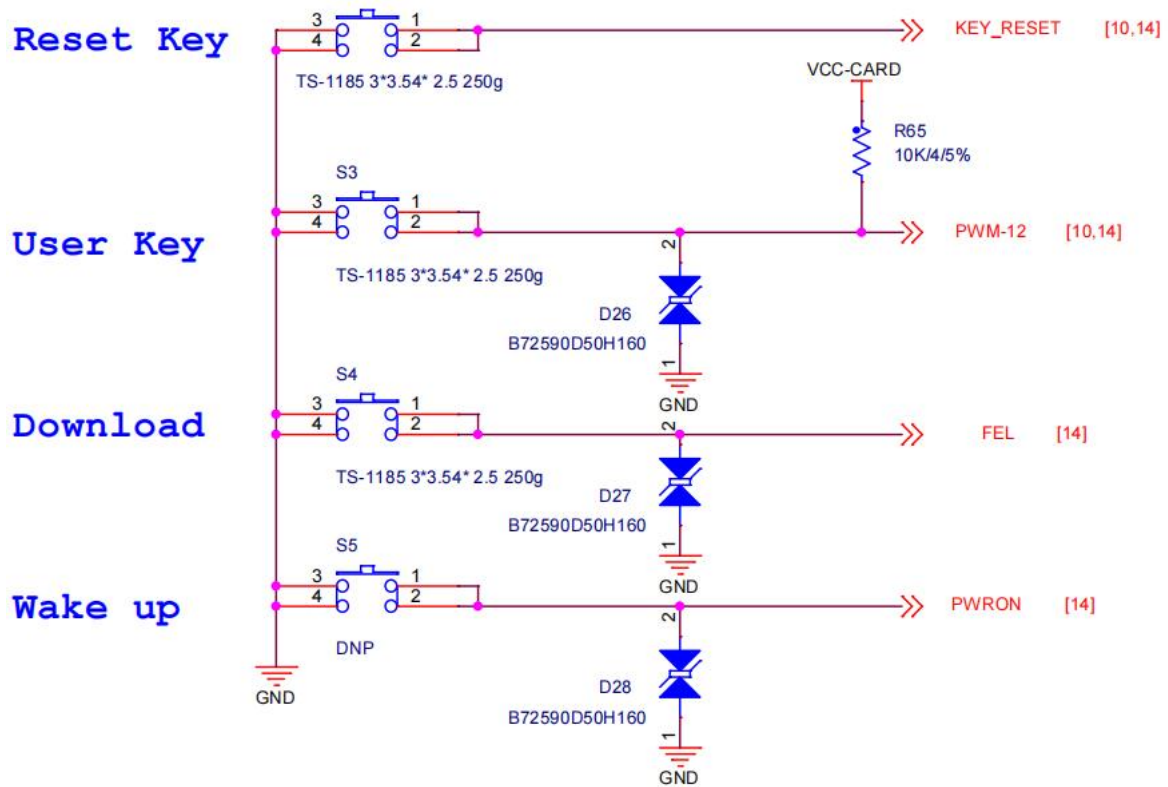


Figure 4-1 Key circuit

4.2. Layout Guidelines

- ◆ The width of reset signal line should not be too narrow, it is recommended not less than 8mil;
- ◆ Reset signal is sensitive signal, which is recommended to be surrounded by ground;
- ◆ Place TVS as close to the button as possible.



5. Interface circuit design

5.1. SD/MMC

MYC-LT527M The core board is equipped with three SD/MMC interfaces, SMHC0, SMHC1, and SMHC2. SMHC0 is commonly used to design MicroSD card signals; SMHC2 has been used on the core board for EMMC signals; SMHC1 uses the BLUE module on the development board. The specific application depends on the design requirements.

5.1.1. reference circuit

TF Card

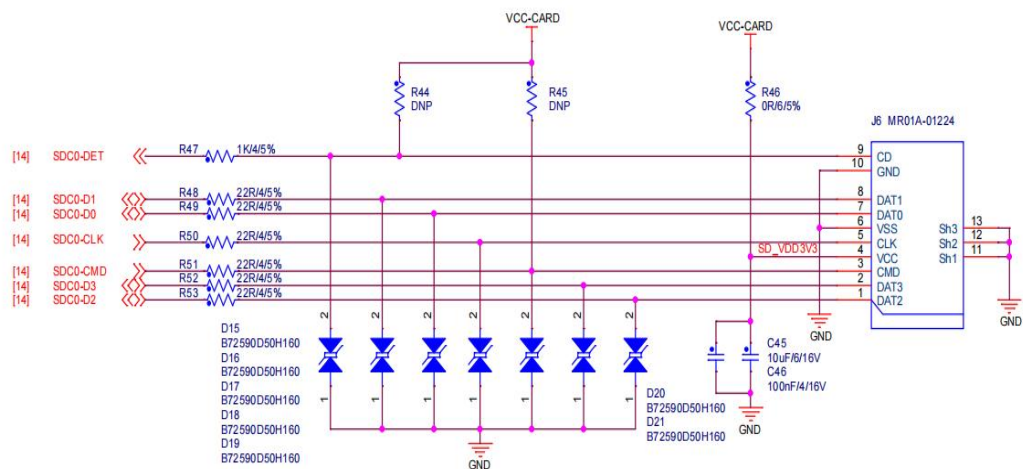


Figure 5-1 Micro SD Reference circuit

5.1.2. Layout Guidelines

- ◆ Interface signals need to do impedance control, using a single-end impedance of 50Ω;
- ◆ Data line control line as long as possible, error is less than $\pm 100\text{mil}$;
- ◆ If the wiring space is sufficient, the CLK signal should be processed as extensively as possible. If you can't do that, distance the clock signal from the other signals and follow the 3W rule.
- ◆ SDC-DET pin in series 1K resistance to improve ESD performance.
- ◆ The power supply of SD card is provided by the core board 3V3.



5.2. UART

MYC-LT527M core board processor has up to 10 serial ports. The core board is configured with one serial port by default, UART0; In the other 9 channels, UART1, UART2, UART3, UART4 and UART7 support 4 lines, with flow control (RTS and CTS signal) function. The development board also designed a serial port S-UART0-TX/RX for debugging PL/M bank.

When the UART is used as the debugging serial port, connect it to the PC with a UART-to-USB conversion cable. The following figure shows the common USB-to-UART TTL modules.

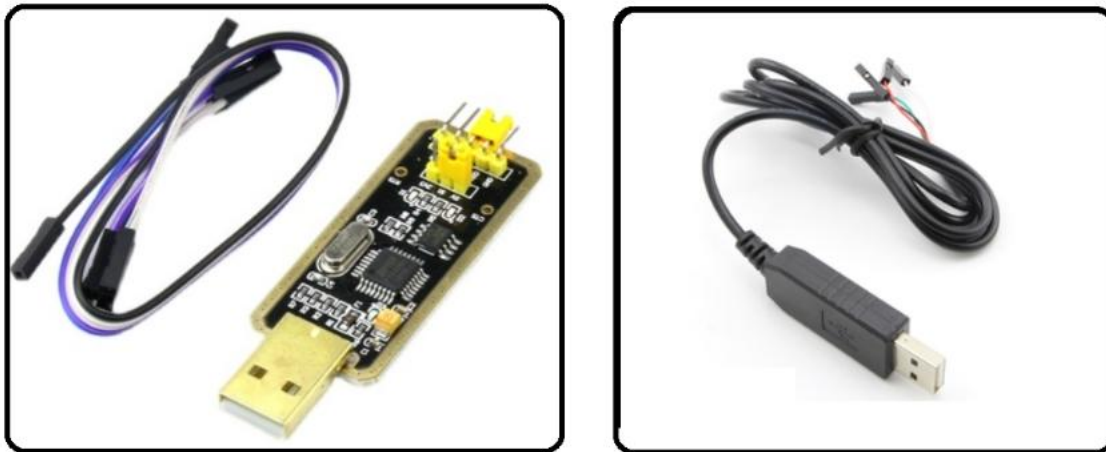


Figure 5-2 USB to UART TTL module

5.2.1. reference circuit

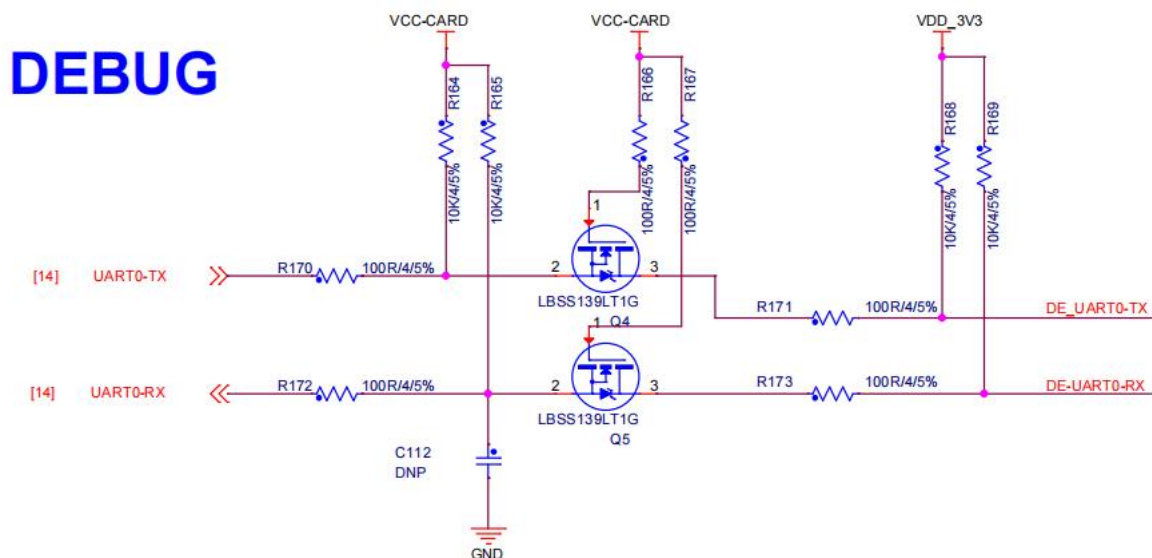


Figure 5-3 UART reference circuit

5.2.2. Layout Guidelines

- ◆ Keep sufficient spacing between signal and power plane before and after isolation;
- ◆ TVS tubes are placed next to connectors.



5.3. USB

The MYC-LT527M core board provides two USB2.0 channels and one USB3.0 channels. USB0 supports HOST and Device modes, while USB1 supports only HOST modes. USB2 supports HOST and Device modes.

USB0 and 2 are directly connected to the USB Type A seat and support OTG/DRP mode. The other USB1 is directly connected to the 2.54mm, 2x20 double row of pins. USB signal is recommended with TVS tube, common mode inductor.

5.3.1. reference circuit

USB0 & USB3.0

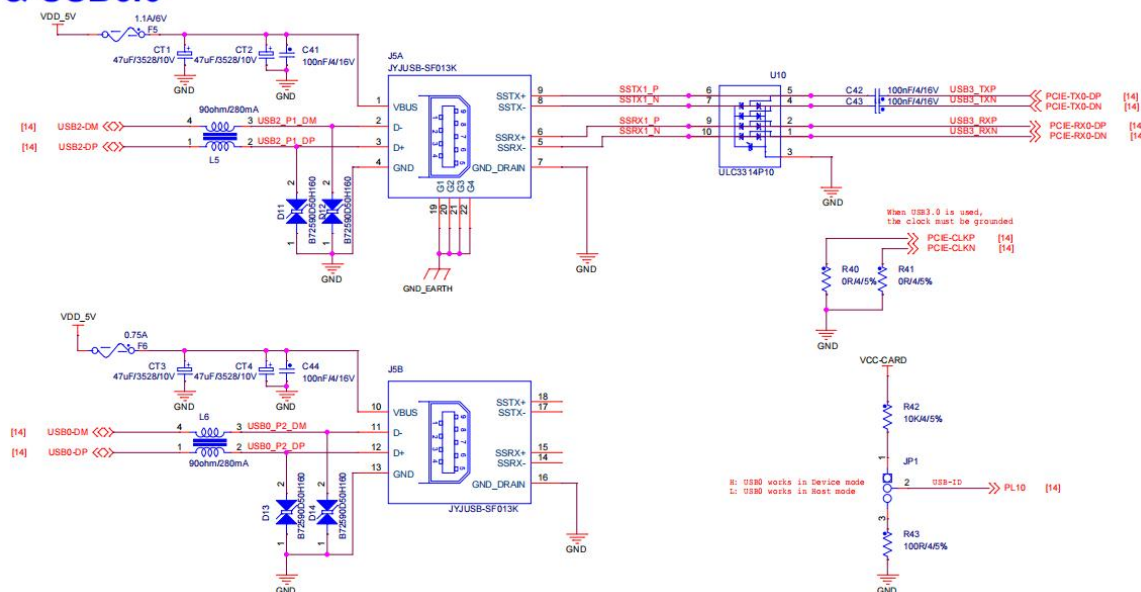


Figure 5-4 USB HUB and HOST reference circuit

5.3.2. Layout Guidelines

- ◆ USB signal routing isometric control, error range $\pm 25\text{mil}$;
- ◆ The differential impedance of USB signal is controlled by 90Ω ;
- ◆ USB signal cable as short as possible;
- ◆ Try not to change the layer of USB signal. If the layer is changed, the GND return through hole should be placed within 50mil away from the cross hole of the layer.
- ◆ Ensure that the reference plane is continuous, USB signal does not cross division;
- ◆ It is recommended that USB signals be routed on the TOP/BOTTOM layer.
- ◆ USB signal away from other clock, digital signal.

5.5. I2C

The MYC-LT527M core board processor supports a maximum of four I2C (TWI) buses, of which I2C1 is used for the E2PROM chip in the core board, and the other three are led to the core board interface.

If you want to use more I2C bus interfaces, consult the chip manual or PIN List and modify the pin configuration in the driver. Several devices can be mounted under the same I2C main line. The following points should be paid attention to when designing the schematic diagram:

- ◆ Check whether the device address under the same bus is in conflict;
- ◆ Ensure that each I2C bus has a pair of pull-up resistors, the resistance value is recommended to be 2.2K~10K, but do not repeatedly add;
- ◆ Check whether the level of I2C interface of the device is 3.3V. If not, add the level shift circuit.
- ◆ The number of devices under the same bus should not be too large, otherwise it is possible to exceed the load capacitance limit of 400 pF required by the I2C specification and affect the signal waveform.

5.5.1. reference circuit

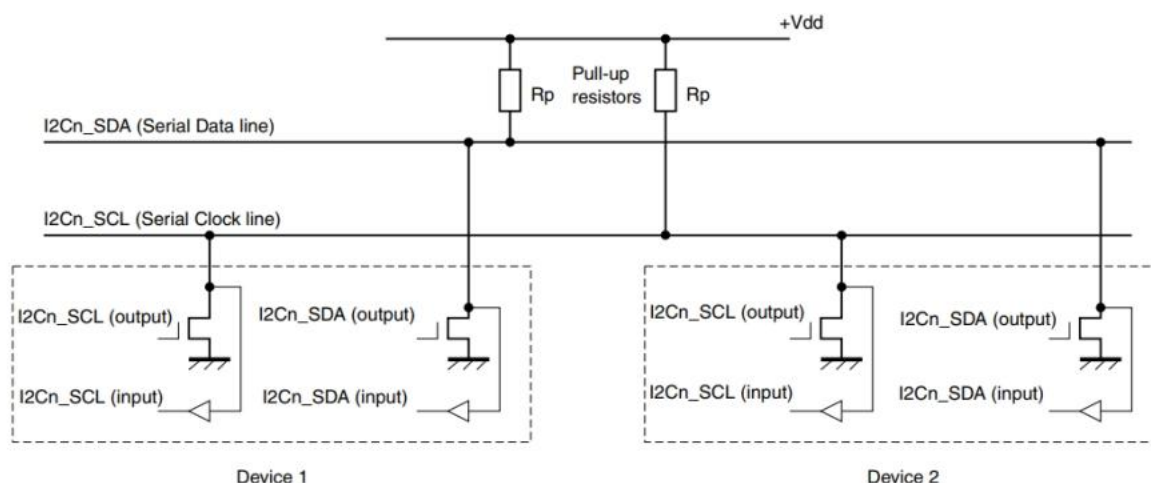


Figure 5-6 I2C reference circuit

5.5.2. Layout Guidelines

- ◆ The width of I2C signal line should not be too narrow, and it is recommended to be 6mil or above;
- ◆ I2C wiring should be planned before the location of each device, line not too winding, I2C line is too long, it will increase the Load effect of the bus;
- ◆ Avoid interference sources. The distance between adjacent lines should be at least 10mil.

5.6. LVDS

MYC-LT527M core board supports LVDS signal output. MYC-LT527M provides a Single Link LVDS0 interface and supports 1366x768@60fps display output. In addition, two Single LVDS can form a Dual Link LVDS interface to support higher display resolution 1920x1080@60fps. The development board single-channel LVDS1 is designed for DSI signals. 3.3V level when normal IO port is used.

MYIR has officially designed a 7 inches LVDS MY-LVDS070C LCD module. The LCD module supports a resolution of 1024x600.

For details, please refer to the website: <https://www.myir-tech.com/product/my-lvds070c.htm>

5.6.1. reference circuit

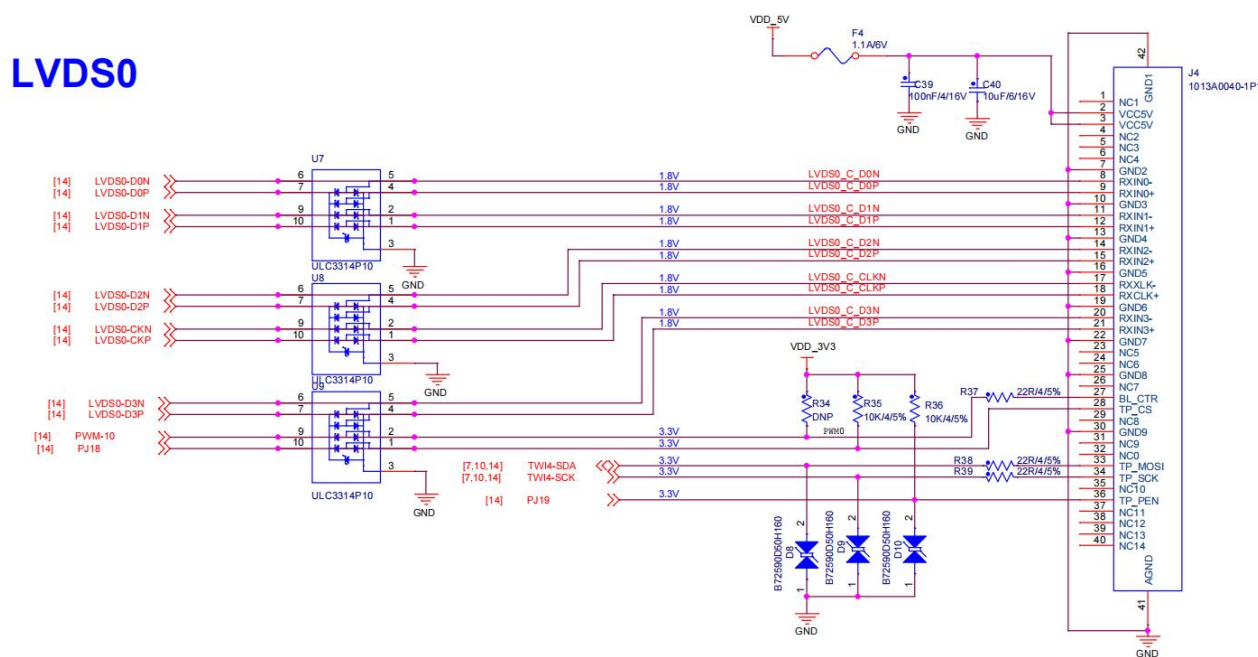


Figure 5-7 Single Link LVDS reference circuit

5.6.2. Layout Guidelines

- ◆ The difference pair of data and time clock should follow the rule of equal length and distance, the error control of difference pair is $\pm 10\text{mil}$, and the difference impedance is 100 euros. Holes should be drilled less, and the P/N difference pairs should be made at the same time when the holes are drilled and the ground holes should be drilled around the difference pairs as much as possible.
- ◆ The data difference pairs need to take the clock difference pairs as reference for inter-group equi-length. Equal length $\pm 50\text{mil}$.
- ◆ The reference plane is complete, and the routing does not span the division.
- ◆ Use HD LVDS, power VDD_PANEL and GND to route thicker cables with a cable width of more than 50mil, and place a large-capacity energy storage capacitor near the connector.



5.7. Audio Out

MYC-LT527M core board native support Audio Out output. HPOUTL/R is connected to the headphone seat. The chip supports four PCM/I2S digital audio interfaces, two audio output interfaces (LINE/HPOUT), and three audio input interfaces MICIN*3.

5.7.1. reference circuit

Audio

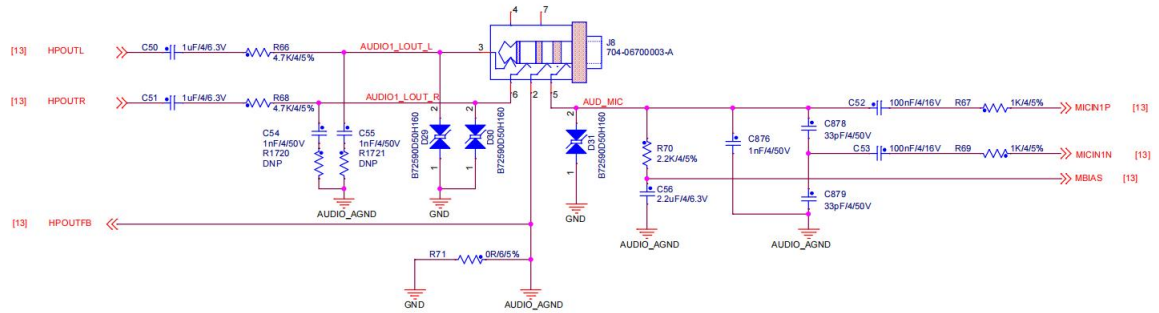


Figure 5-8 Audio Out reference circuit

5.7.2. Layout Guidelines

- ◆ The isolation points of GND_AUDIO and GND are star grounded and close to J8 as far as possible.
- ◆ Audio circuit layout position away from interference sources, it is recommended to plan a separate area in PCB to place analog circuit;
- ◆ Audio Out belongs to analog audio signal, recommended 10mil and above.
- ◆ Note the distinction between analog and digital.



5.8. RTC

The MYC-LT527M core board is equipped with a backup battery holder that can be connected to a button battery. When the system fails to power, it can be used to maintain the operation of the RTC part, and its circuit structure is shown as follows:

5.8.1. reference circuit

RTC

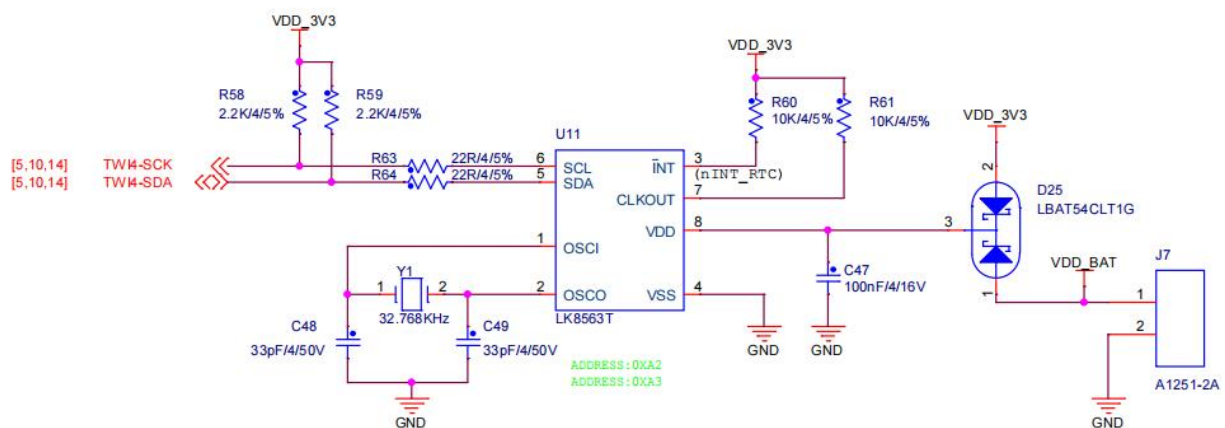


Figure 5-9 RTC reference circuit

5.8.2. Layout Guidelines

- ◆ C47 is placed close to J7;
- ◆ The width of I2C signal line recommended to be 6mil or above;
- ◆ I2C wiring should be planned before the location of each device, It is best to lay out and walk in a straight line .



5.10. DSI

The MYC-LT527M core board is designed with a DSI interface and adopts a 40pin flap FPC seat with a pitch of 0.5mm. This interface uses IO LVDS1, level 1V8, resolution 1366x768@60Hz. 3.3V level when normal IO port is used.

5.10.1. reference circuit

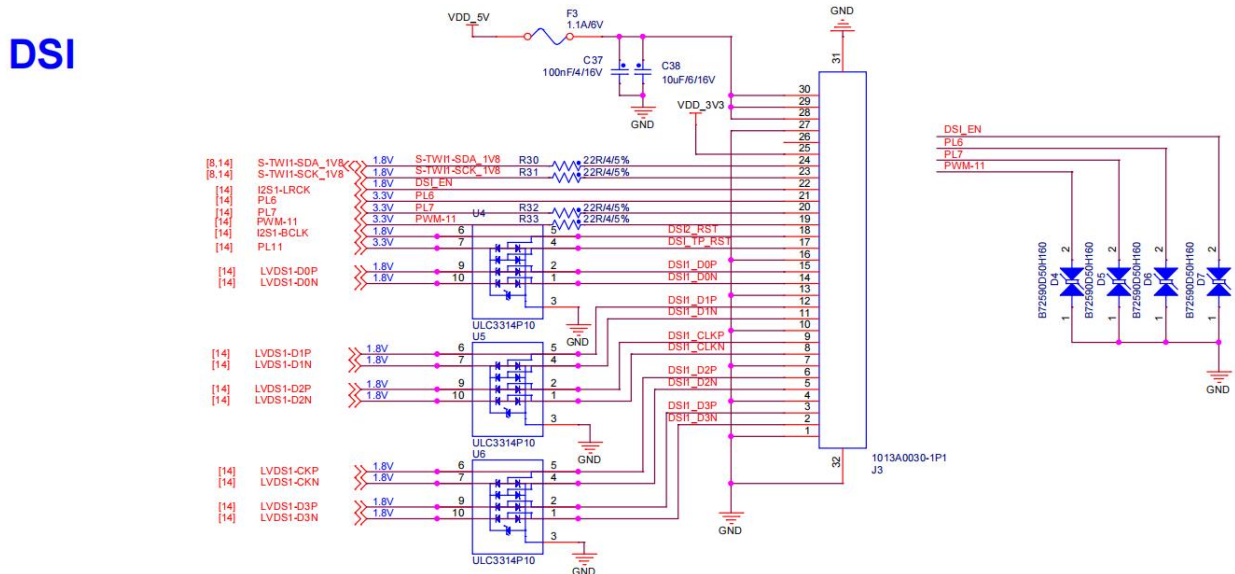


Figure 5-11 DSI reference circuit

5.10.2. Layout Guidelines

- ◆ LVDS differential signal needs to control 100 Ohm impedance, internal isometric control within $\pm 5\text{mil}$, group isometric control within $\pm 20\text{mil}$;
- ◆ If layers need to be changed, the accompanying ground holes should be placed 10mil away from the p/n layer change through the holes, and the accompanying ground holes of p/n should be placed symmetrically;
- ◆ LVDS differential signals need to be in the same group and the same layer, and there should be a complete power reference plane, and should not be divided across.



5.11. HDMI

The MYC-LT527M core board is designed with one HDMI interface. The 5V power supply of HDMI must be connected with a Schottky diode in series to prevent leakage at the end of the device after shutdown. Please choose a Schottky diode with reduced on-voltage. Support 3840x2160, 1920x1080, 1280x720fps resolution.

5.11.1. reference circuit

HDMI

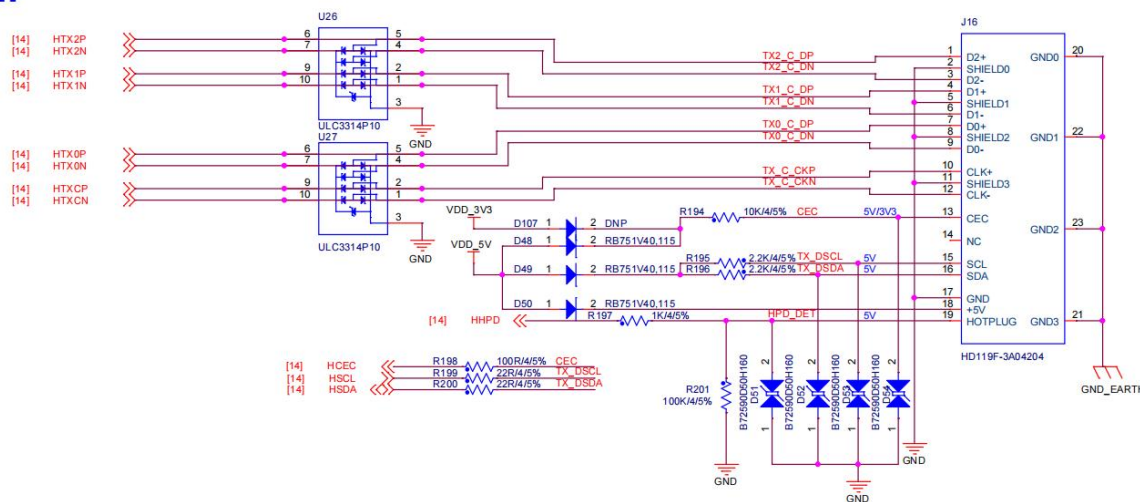


Figure 5-12 HDMI reference circuit

5.11.2. Layout Guidelines

- ◆ HDMI signal routing isometric control, error range $\pm 25\text{mil}$. The ESD device must be close to the HDMI seat.
- ◆ The distance between adjacent difference pairs of HDMI signal routes is more than 3W.
- ◆ HDMI signal cable as short as possible; The power pin ripple is less than 50mV.
- ◆ The HDMI signal should not be changed as far as possible. If the layer is changed, the GND return through hole should be placed within 50mil from the layer through hole;
- ◆ The HDMI ground pin is recommended to be directly connected to the chassis



5.12. eDP

MYC-LT527M core board design 1 eDP interface, resolution 2.5k@60Hz. 1, 2, and 4 lane transfers with a maximum transfer rate of 2.7 Gbit/s. Color depth: 8bit and 10bit per channel. reference circuit.shutdown. Please choose a Schottky diode with reduced on-voltage. Support 3840x2160, 1920x1080, 1280x720fps resolution.

5.12.1. reference circuit

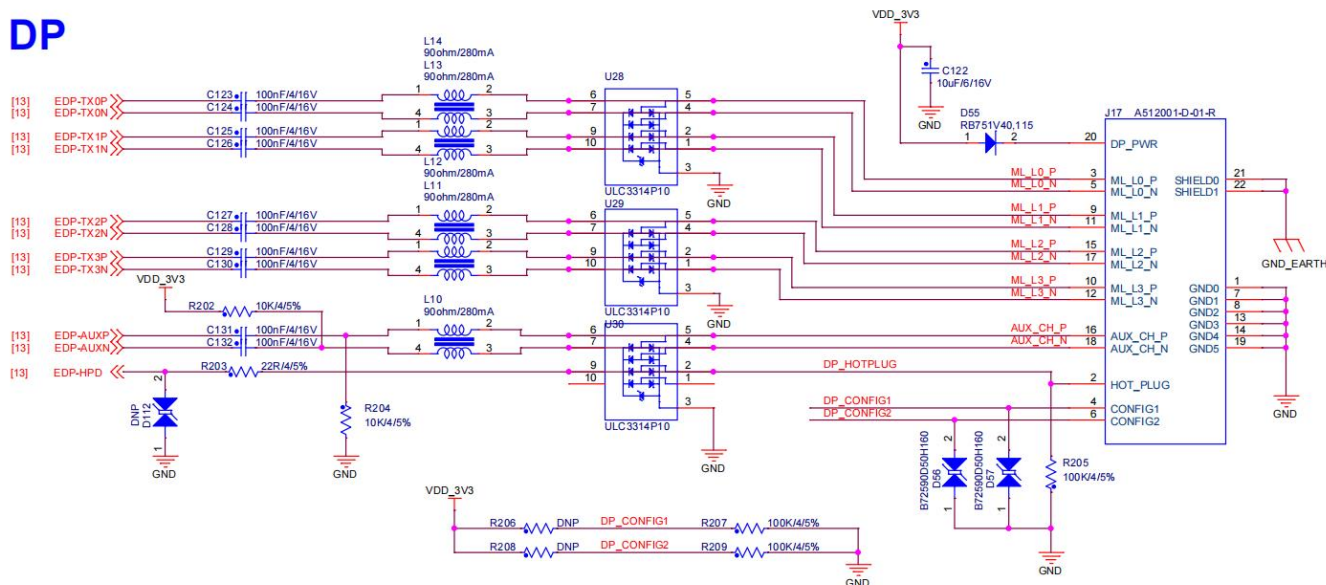


Figure 5-13 eDP reference circuit

5.12.2. Layout Guidelines

- ◆ If layers need to be changed, the accompanying ground holes should be placed 10mil away from the p/n layer change through the holes, and the accompanying ground holes of p/n should be placed symmetrically;
- ◆ The eDP differential signal should be in the same group and the same layer, and should have a complete power reference plane, and should not be divided across.
- ◆ The eDP differential signal needs to control 100 Ohm impedance, and the internal isometric length is controlled within $\pm 5\text{mil}$, and the internal isometric length is controlled within $\pm 25\text{mil}$; For details, see Baseboard design rules.

5.13. MIPI CSI

The MYC-LT527M core board is designed with 2 MIPI CSI interfaces and its level is 1V8 level. The maximum input for CSI is 8M@30fps, the maximum pixel clock for parallel CSI interface is 148.5MHz, and the maximum input for BT656 interface is 4*720P@30fps in clock dual-edge sampling mode. The camera interface uses a 0.5mm FPC row seat, and users can choose MY-CAM004M camera module from Mir Technology. 3.3V level when normal IO port is used.

The FPC connector is selected as the camera input interface, and the connector model is 1013A0024-1P1.

5.13.1. reference circuit

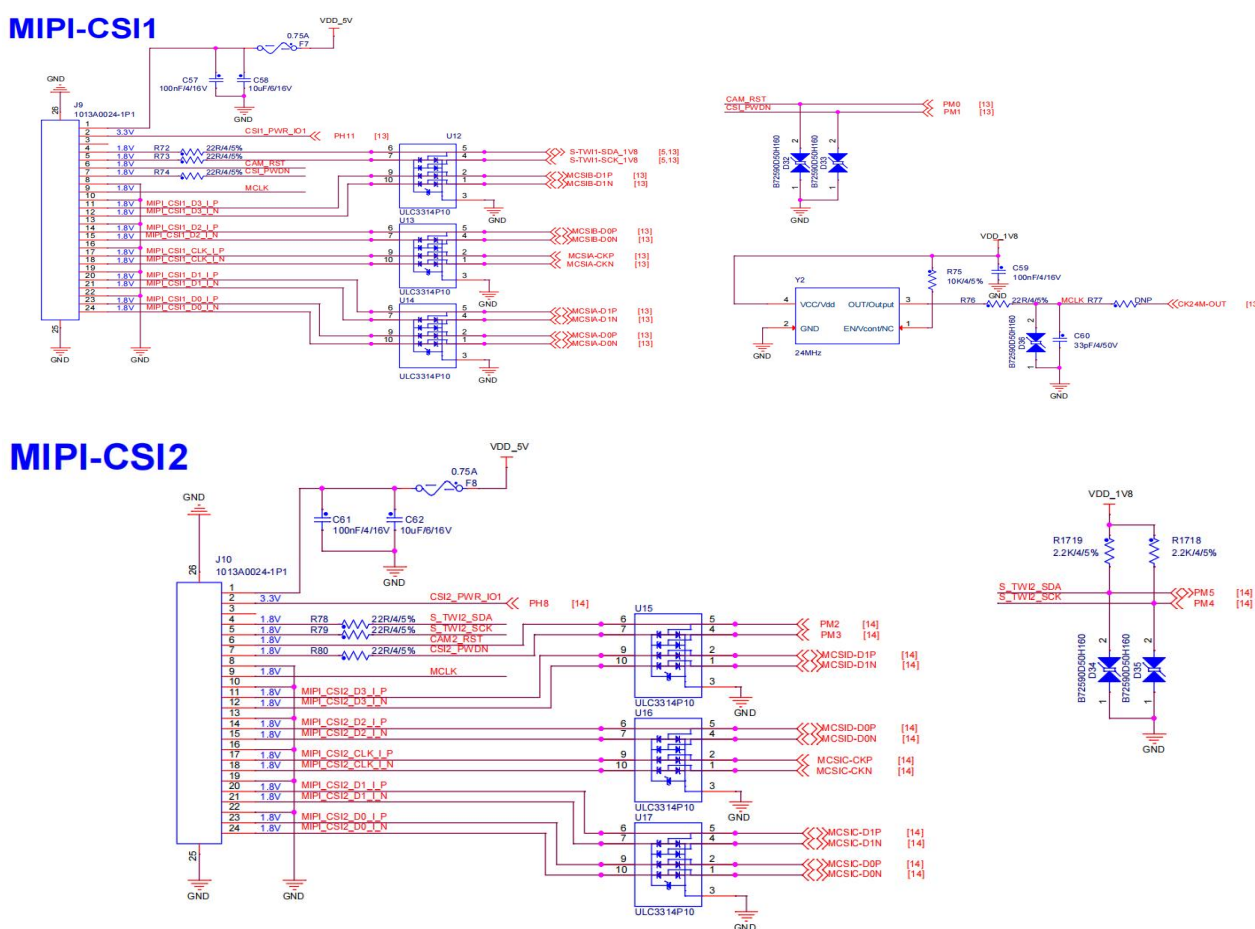


Figure 5-14 MIPI CSI reference circuit

5.13.2. Layout Guidelines

- ◆ The CSI differential signal needs to control 100 Ohm impedance, and the internal isometric length is controlled within $\pm 5\text{mil}$, and the internal isometric length is controlled within $\pm 25\text{mil}$;
- ◆ If layers need to be changed, the accompanying ground holes should be placed 10mil away from the p/n layer change through the holes, and the accompanying ground holes of p/n should be placed symmetrically;
- ◆ CSI differential signals should be in the same group and at the same layer, and should have a complete power reference plane, and should not be divided across.

5.14. Raspberries pie interface

The MYC-LT527M core board is designed with two 2x20 pins with a 2.54mm spacing, one of which is a standard Raspberry PI wire sequence interface. The other way is a custom interface, which is also the same double-row pin: 2xI2C, 2xSPI, 4xUART, 1xUSB. This interface can expand an expansion board, mill also designed the expansion board, details can consult sales.

5.14.1. reference circuit

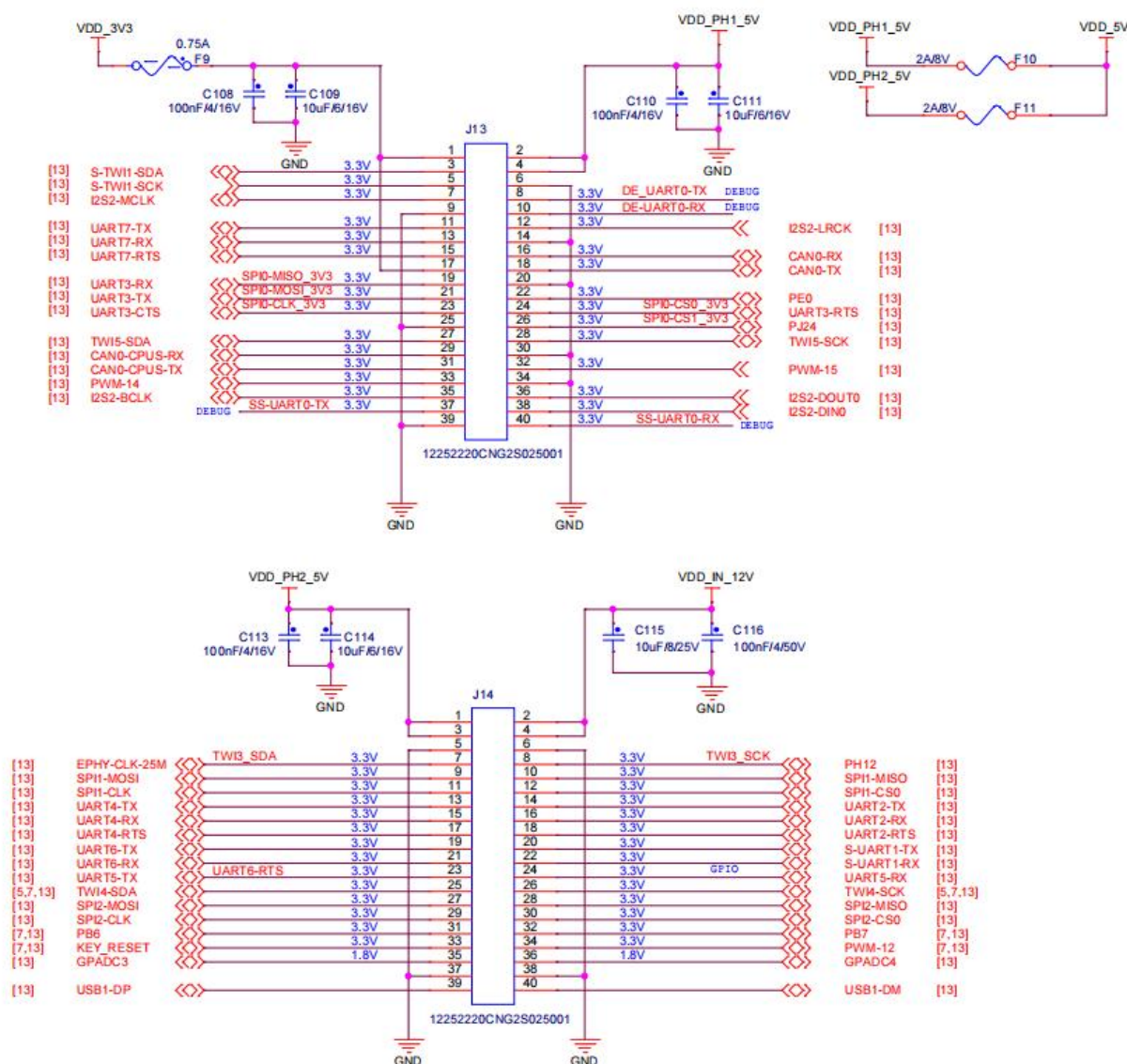


Figure 5-15 reference circuit

5.14.2. Layout Guidelines

- ◆ Double rows of needles should not be placed too close to the edge of the board, leaving a suitable spacing.
- ◆ 1 screen printing must be marked clearly to prevent stupor.



5.15. LED

The MYC-LT527M core board is designed with 3 LED lights, one is a 5V power indicator, one is a running indicator, and one is a user indicator.

5.15.1. reference circuit

LED

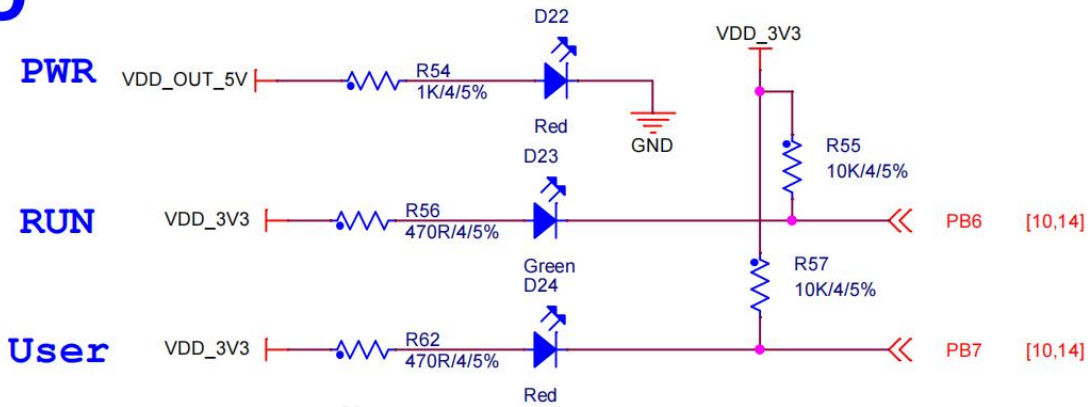


Figure 5-16 LED reference circuit

5.15.2. Layout Guidelines

- ◆ Three lights are placed together.
- ◆ Screen printing of the three indicators should be clearly marked.



6. Design check item

6.1. Power supply design

Check item	Recommended solution
Core board supply voltage	The recommended value is 5V and the absolute value is 4.5V-5.5V
Core board power decoupling capacitor	Use capacitors with 47uF and above value for core module power supply
IO level of carrier board peripherals	The IO voltage level of the peripheral should match the corresponding interface level of the core module
core module power sequence	It is recommended that the core module power start before the peripheral power
Temperature rise of power chip	Confirm the thermal resistance of the power chip, and calculate the maximum temperature rise of the power chip based on the power consumption of the core module to ensure that the final temperature is within the specified range of the power chip

Table 6-1 Power supply checklist

6.2. System startup circuit design

Check item	Recommended solution
Reset circuit	You are advised to connect the KEY-RESET pin
Micro SD circuit	SD card is convenient to burn procedures, it is recommended to keep

Table 6-2 System start up checklist



6.3. Peripheral circuits design

Category	Check box	Proposal
USB	Capacitance value of USB D+/D- signal ESD device	The capacitance value of ESD devices is recommended to be less than 2pF
	Whether the capacitor of the supply pin is added series resistance	The interface 5V capacitor requires a 1-ohm resistor in series to limit the voltage surge at the USB port
Ethernet (RGMII/ RMII)	PHY chip layout	Get as close to the core board layout as possible. Keep RGMII wiring as short as possible. RGMII sends and receives signals in separate groups, and Layout Layout within the same length +-25mil. There is no requirement between groups.
	PHY chip power supply	The PHY chip power supply is isolated by magnetic beads
	Clock signal source of the PHY chip	Use external active or passive crystal oscillator.
	Connection method of center tap on PHY side of network transformer	Depending on the type of PHY chip, it can be found in the chip manual. If the PHY is current-driven, the tap needs to be pulled up to the PHY supply voltage. If the PHY is voltage-driven, the tap does not need to be pulled up. If not found in the manual, use a reference circuit or reserved pull-up resistor
I2C	I2C pull-up resistance	The more the bus load devices, the smaller the resistance value should be, and the greater the resistance value should be. Recommended resistance value 1.5K/2.2K/4.7K;
	How many pull-up resistors are connected to each I2C signal cable	One or more can be used.
	What is the pull-up voltage	The pull-up resistor must be connected to the voltage matching the I/O level
SDIO	Whether DATA and CMD signals are pulled up	Requires pull-up, 47K or 10K pull-up to 3.3V
HDMI	The I2C of the processor	Can be directly connected to the HDMI connector, without level conversion, need to pull up 2.2K resistor.

Table 6-3 peripheral circuits Check list



Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory,



the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;



- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.



For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.



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