T527
User Manual

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深圳市米尔电子有限公司myir2021

Revision History

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About This Document

Purpose and Scope

This document describes the features, logical structures, functions, operating modes, and related registers of each module about T527. For details about the interface timings and related parameters, the pins, pin usages, performance parameters, and package dimension, please refer to the *T527_Datasheet*.

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Programmers in writing code or modifying the Allwinner provided code

Revision Number Definition

Revision 0.10-0.1x

This document is released based on the experimental sample(s). Therefore, it may be modified, calibrated and supplemented hereafter.

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If you have any questions about the document, please contact us to confirm and obtain the latest version.

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

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Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Reset Value Conventions

In the register definition tables:

If other column value in the row of a bit or multiple bits is "/", this bit of these multiple bits are unused.

If the default value of a bit or multiple bits is "UDF", this default value is undefined.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

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The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression, X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

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1 Product Description

1.1 Overview

T527 series features high-performance octa-core CortexTM-A55 AI platform SoCs for the electronic commercial, industrial, and automotive fields. The chip family integrates octa-core Cortex™-A55 CPU, a HiFi4 DSP, 2 Tops NPU, G57 MC1 GPU, 32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X DRAM, high-speed interfaces (PCIe2.1 and USB3.1), automotive interface (CAN), multi video output interfaces (2*RGB/2*Dual-LVDS/2*MIPI-DSI/HDMI/eDP), and video input interfaces (MIPI CSI). The chip family supports 4K@60fps H.265 decoder, 4K@30fps H.264 decoder,4K@25fps H.264 encoder, DI, and SmartColor system, which provides users with smooth experience and professional AI visual effect. T527 series can be used in Content sharing and self-service interactive terminals, Smart manufacturing, and other electronic commercial and industrial devices.

1.2 Device Differences

The T527 series is configured with different sets of features in different devices. The feature differences across different devices are shown in the following table.

Table 1-1 Device Feature Differences

Device	NPU
T527H02X0DCH	Support
T527H00X0DCH	Not Support

NOTE

The terms “T527”and “T527 Series” are used in the following document to refer to the all devices listed in Table 1-1.

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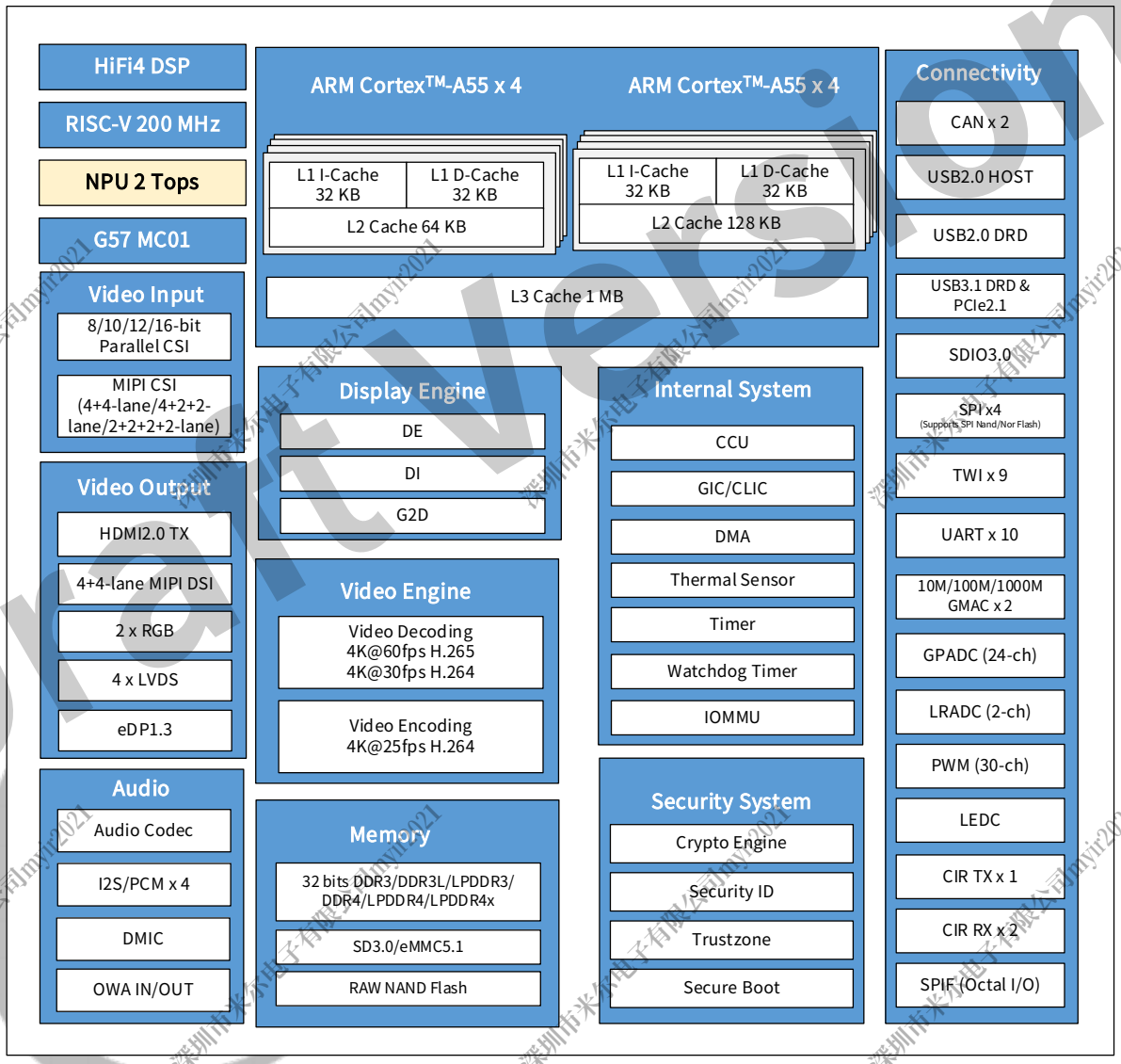
1.3 Block Diagram

The following figure shows the system block diagram of the T527.

Figure 1-1 T527 System Block Diagram



NOTE

A pale yellow box indicates that this module is only for T527H02X0DCH.

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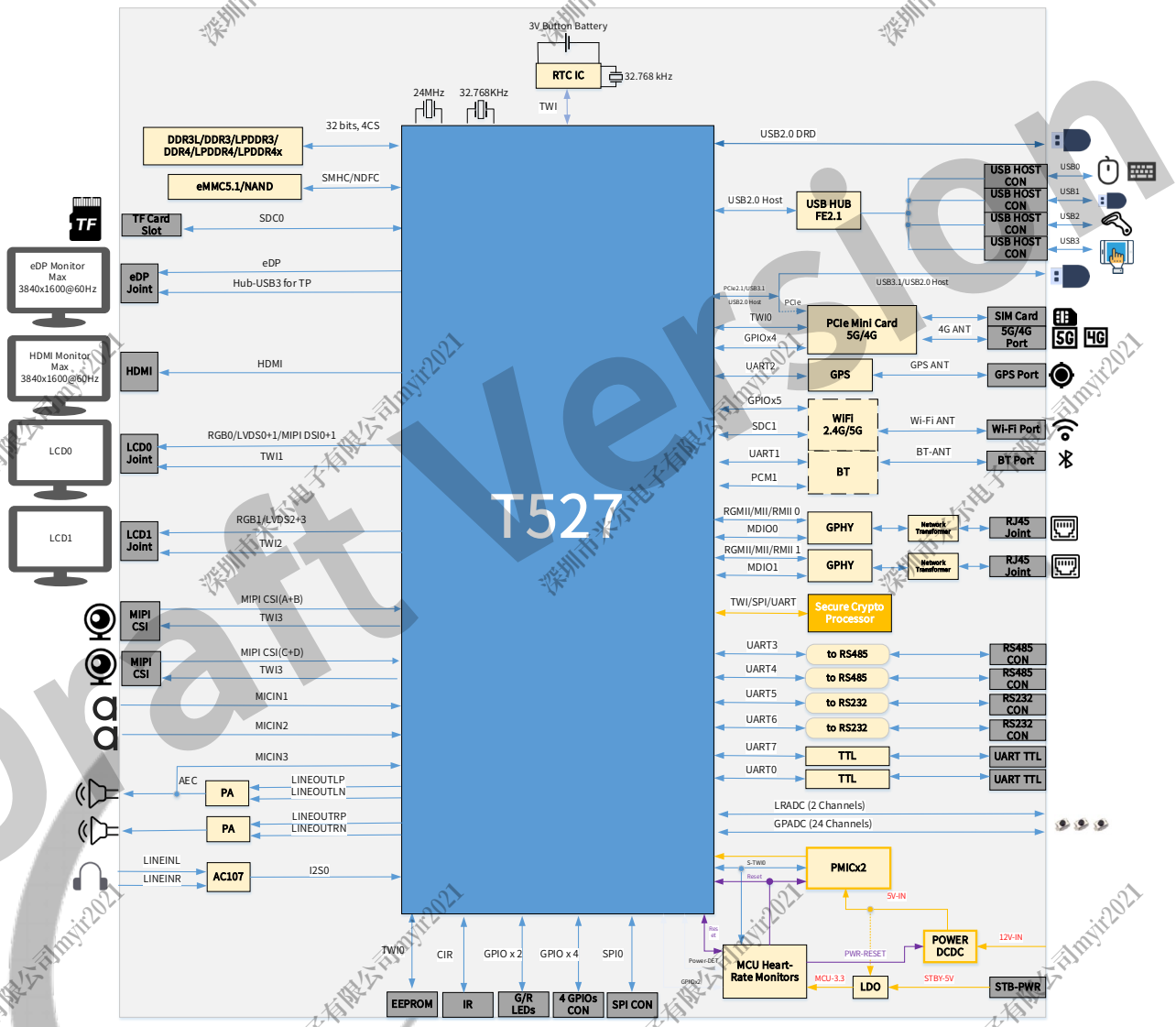
The following figure shows the typical application of the T527.

Figure 1-2 Typical Application



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2 System

2.1 Memory Mapping

Module	Address	Size(Bytes)
BROM & SRAM		
S_BROM	0x0000 0000---0x0000 AFFF	44 KB
M_BROM	0x0001 0000---0x0001 8FFF	36 KB
DSP0 SRAM	0x0002 0000---0x0002 FFFF	64 KB The local SRAM is switched to system boot.
DSP0 DRAM0	0x0003 0000---0x0003 7FFF	32 KB The local SRAM is switched to system boot.
DSP0 DRAM1	0x0003 8000---0x0003 FFFF	32 KB The local SRAM is switched to system boot.
SRAM A2	0x0004 0000---0x0006 3FFF	16 KB+128 KB
DSP0 IRAM（Local SRAM）	0x0040 0000---0x0040 FFFF	64 KB
DSP0 DRAM0（Local SRAM）	0x0042 0000---0x0042 7FFF	32 KB
DSP0 DRAM1（Local SRAM）	0x0044 0000---0x0044 7FFF	32 KB
GPU_SYS		
GPU	0x0180 0000---0x0183 FFFF	256 KB
VE_SYS		
VE	0x01C0 E000---0x01C0 EFFF	4 KB
SP0		
GPIO	0x0200 0000---0x0200 07FF	2 KB
SPC	0x0200 0800---0x0200 0BFF	1 KB
PWMCTRL0	0x0200 0C00---0x0200 0FFF	1 KB
CCU	0x0200 1000---0x0200 1FFF	4 KB
CIR_TX	0x0200 3000---0x0200 33FF	1 KB
CIR_RX	0x0200 5000---0x0200 53FF	1 KB
LEDC	0x0200 8000---0x0200 83FF	1 KB
GPADC_CTRL0	0x0200 9000---0x0200 93FF	1 KB
THS1	0x0200 9400---0x0200 97FF	1 KB
LRADC	0x0200 9800---0x0200 9BFF	1 KB
GPADC_CTRL1	0x0200 9C00---0x0200 9FFF	1 KB

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Module	Address	Size(Bytes)
THS0	0x0200 A000---0x0200 A3FF	1 KB
IOMMU	0x0201 0000---0x0201 FFFF	64 KB
NSI	0x0202 0000---0x0202 FFFF	64 KB
CPUX_WDT	0x0205 0000---0x0205 0FFF	4 KB
PWMCTRL1	0x0205 1000---0x0205 13FF	1 KB
NSI_CPU	0x0207 1000---0x0207 13FF	1 KB
SP1		
UART0	0x0250 0000---0x0250 03FF	1 KB
UART1	0x0250 0400---0x0250 07FF	1 KB
UART2	0x0250 0800---0x0250 0BFF	1 KB
UART3	0x0250 0C00---0x0250 0FFF	1 KB
UART4	0x0250 1000---0x0250 13FF	1 KB
UART5	0x0250 1400---0x0250 17FF	1 KB
UART6	0x0250 1800---0x0250 1BFF	1 KB
UART7	0x0250 1C00---0x0250 1FFF	1 KB
TWI0	0x0250 2000---0x0250 23FF	1 KB
TWI1	0x0250 2400---0x0250 27FF	1 KB
TWI2	0x0250 2800---0x0250 2BFF	1 KB
TWI3	0x0250 2C00---0x0250 2FFF	1 KB
TWI4	0x0250 3000---0x0250 33FF	1 KB
TWI5	0x0250 3400---0x0250 37FF	1 KB
SH0		
SYSCTRL	0x0300 0000---0x0300 0FFF	4 KB
CPUX_TIMER	0x0300 8000---0x0300 83FF	1 KB
DMAC	0x0300 2000---0x0300 2FFF	4 KB
CPUX_MSGBOX	0x0300 3000---0x0300 3FFF	4 KB
SPINLOCK	0x0300 5000---0x0300 5FFF	4 KB
SID	0x0300 6000---0x0300 6FFF	4 KB
CE_NS	0x0304 0000---0x0304 07FF	2 KB
CE_S	0x0304 0800---0x0304 0FFF	2 KB
MEMC	0x0310 2000---0x0330 1FFF	2 M
MEMC_SMC	0x0311 0000---0x0311 FFFF	64 KB
MEMC_COMMON	0x0312 0000---0x0312 FFFF	64 KB
MEMC_DDRC	0x0313 0000---0x0313 FFFF	64 KB
MEMC_PHY	0x0314 0000---0x0314 FFFF	64 KB
GIC	0x0340 0000---0x034E FFFF	15*64 KB
SH2		
NDFC	0x0401 1000---0x0401 1FFF	4 KB
SMHC0	0x0402 0000---0x0402 0FFF	4 KB

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Module	Address	Size(Bytes)
SMHC1	0x0402 1000---0x0402 1FFF	4 KB
SMHC2	0x0402 2000---0x0402 2FFF	4 KB
SPI0	0x0402 5000---0x0402 5FFF	4 KB
SPI1	0x0402 6000---0x0402 6FFF	4 KB
SPI2	0x0402 7000---0x0402 7FFF	4 KB
USB0	0x0410 0000---0x041F FFFF	1 MB
USB1	0x0420 0000---0x042F FFFF	1 MB
GMAC0	0x0450 0000---0x0450 FFFF	64 KB
GMAC1	0x0451 0000---0x0451 FFFF	64K
SPIFC	0x047F 0000---0x047F 0FFF	4 KB
PCIE	0x0480 0000---0x04CF FFFF	5 MB
USB3	0x04D0 0000---0x04EF FFFF	2 MB
PCIE_USB3_TOP_APP	0x04F0 0000---0x04F7 FFFF	512 KB
DE_SYS		
DE	0x0500 0000---0x053F FFFF	4 MB
DI	0x0540 0000---0x0543 FFFF	256 KB
G2D	0x0544 0000---0x0547 FFFF	256 KB
VIDEO0_OUT_SYS		
DISPLAY0_TOP	0x0550 0000---0x0550 0FFF	4 KB
TCON_LCD0	0x0550 1000---0x0550 1FFF	4 KB
TCON_LCD1	0x0550 2000---0x0550 2FFF	4 KB
TCON_TV0	0x0550 3000---0x0550 3FFF	4 KB
TCON_TV1	0x0550 4000---0x0550 4FFF	4 KB
COMBOPHY_DSI0	0x0550 6000---0x0550 7FFF	8 KB
COMBOPHY_DSI1	0x0550 8000---0x0550 9FFF	8 KB
HDMI	0x0552 0000---0x0561 FFFF	1 MB
EDP	0x0572 0000---0x0572 3FFF	16 KB
VIDEO1_OUT_SYS		
DISPLAY1_TOP	0x0573 0000---0x0573 0FFF	4 KB
TCON_LCD2	0x0573 1000---0x0573 1FFF	4 KB
VIDEO_IN_SYS		
CSI	0x0580 0000---0x058F FFFF	1 MB
ISP	0x0590 0000---0x05CF FFFF	4 MB
APBS0		
S_PPU1	0x0700 1400---0x0700 17FF	1 KB
S_SPC	0x0700 2000---0x0700 23FF	1 KB
STBY_PRCM	0x0701 0000---0x0701 FFFF	64 KB
CPUS_WDT	0x0702 0400---0x0702 07FF	1 KB
S_TWD	0x0702 0800---0x0702 0BFF	1 KB
S_PWMCTRL	0x0702 0C00---0x0702 0FFF	1 KB

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Module	Address	Size(Bytes)
S_INTC	0x0702 1000---0x0702 13FF	1 KB
S_GPIO	0x0702 2000---0x0702 27FF	2 KB
CPUS_CFG	0x0703 1000---0x0703 1FFF	4 KB
S_CIRRX	0x0704 0000---0x0704 03FF	1 KB
PCK600_CPU	0x0705 0000---0x0705 FFFF	64 KB
PCK600_QCHANNEL(S_PPU)	0x0706 0000---0x0706 7FFF	32 KB
APBS1		
S_UART0	0x0708 0000---0x0708 03FF	1 KB
S_UART1	0x0708 0400---0x0708 07FF	1 KB
S_TWI0	0x0708 1400---0x0708 17FF	1 KB
S_TWI1	0x0708 1800---0x0708 1BFF	1 KB
S_TWI2	0x0708 1C00---0x0708 1FFF	1 KB
AHBS		
RTC	0x0709 0000---0x0709 03FF	1 KB
CPUS_TIMER	0x0709 0400---0x0709 07FF	1 KB
S_SPI0	0x0709 2000---0x0709 2FFF	4 KB
S_SPINLOCK	0x0709 3000---0x0709 3FFF	4 KB
CPUS_MSGBOX	0x0709 4000---0x0709 4FFF	4 KB
DSP_APB0		
DSP_CFG	0x0710 0000---0x0710 03FF	1 KB
DSP_WDT	0x0710 0400---0x0710 07FF	1 KB
DSP_PRCM	0x0710 2000---0x0710 2FFF	4 KB
DSP_PWMCTRL	0x0710 3000---0x0710 33FF	1 KB
AUDIO CODEC	0x0711 0000---0x0711 0FFF	4 KB
DMIC	0x0711 1000---0x0711 13FF	1 KB
I2S0	0x0711 2000---0x0711 2FFF	4 KB
I2S1	0x0711 3000---0x0711 3FFF	4 KB
I2S2	0x0711 4000---0x0711 4FFF	4 KB
I2S3	0x0711 5000---0x0711 5FFF	4 KB
OWA	0x0711 6000---0x0711 63FF	1 KB
DSP_AHB		
DSP_MSGBOX	0x0712 0000---0x0712 0FFF	4 KB
DSP_DMAC	0x0712 1000---0x0712 1FFF	4 KB
NPU	0x0712 2000---0x0712 2FFF	4 KB
DSP_TIMER	0x0712 3000---0x0712 33FF	1 KB
RISCV_SYS		
RISCV_CFG	0x0713 0000---0x0713 0FFF	4 KB
RISCV_WDT	0x0713 2000---0x0713 2FFF	4 KB
RISCV_LCNT	0x0713 4000---0x0713 4FFF	4 KB
RISCV_MSGBOX	0x0713 6000---0x0713 6FFF	4 KB

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Module	Address	Size(Bytes)
DSP_SRAM		
SRAMA3_0	0x0728 0000---0x072B FFFF	256 KB (SRAMA3_0 can not be used cross 256 KB boundary)
SRAMA3_1	0x072C 0000---0x072F FFFF	256 KB (SRAMA3_1 can not be used cross 256 KB boundary)
NPU		
SRAMA3_2	0x0730 0000---0x0737 FFFF	512 KB
CPUX Related		
CPU_SUBSYS_CTRL	0x0800 0000---0x0800 0FFF	4 KB
TIMESTAMP_STA	0x0801 0000---0x0801 0FFF	4 KB
TIMESTAMP_CTRL	0x0802 0000---0x0802 0FFF	4 KB
APB_ROM1	0x0880 1000---0x0880 1FFF	4 KB
CTI	0x0880 3000---0x0880 3FFF	4 KB
CS_TS_CTRL	0x0880 5000---0x0880 5FFF	4 KB
CS_TS_READ	0x0880 7000---0x0880 7FFF	4 KB
TPIU	0x0880 9000---0x0880 9FFF	4 KB
ETB	0x0880 B000---0x0880 BFFF	4 KB
APB_ROM2	0x0881 1000---0x0881 1FFF	4 KB
ATB_FUNNEL	0x0881 3000---0x0881 3FFF	4 KB
CLUSTER_CFG	0x0881 5000---0x0881 5FFF	4 KB
CPU_PLL_CFG	0x0881 7000---0x0881 7FFF	4 KB
CLUSTER_DBUG	0x0980 0000---0x09BF FFFF	4 MB
PCIE		
PCIE_SLV	0x2000 0000---0x2FFF FFFF	256 MB
RISCV Related (Only RISC-V access)		
RISCV_CLINT	0xE000 0000---0xE000 FFFF	64 KB
RISCV_CLIC	0xE080 0000---0xE080 4FFF	20 KB
RISCV_SYSMAP	0xEFFF F000---0xEFFF FFFF	4 KB
DRAM Space		
DRAM SPACE	0x4000 0000---0x13FFF FFFF	4 GB RISC-V core accesses the DRAM address: 0x4004 0000---0x7FFF FFFF

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2.2 ARM Cortex™-A55 System(CPUX)

2.2.1 Overview

T527 CPU architecture adopts DynamIQ technology. The CPUX system includes DynamIQ Shared Unit (DSU), DynamIQ cluster, GIC600 distributor, coresight subsystem, and timestamp module. The features of the CPUX cores and DSU in DynamIQ cluster are as follows.

CPUX Cores

- Two sets of ARM Cortex™-A55 cores in a DynamIQ big. LITTLE configuration
- Memory subsystem features
  - 32 KB L1 I-cache and D-cache
  - Optional 64KB L2 cache for 'LITTLE' cores
  - Optional 128KB L2 cache for 'big' cores
  - Separate L1 instruction side memory subsystem with a Memory Management Unit (MMU)
- A64, A32, and T32 instruction sets running on ARMv8-A architecture ISA
- Both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3).
- In-order pipeline with direct and indirect branch prediction.
- Optional Data Engine Unit implementing the advanced Single Instruction Multiple Data (SIMD) and floating-point architecture
- Optional Cryptography extensions
- Separate L1 instruction side memory system with a Memory Management Unit (MMU)
- ARM TrustZone® technology
- Generic Interrupt Controller (GIC) interface connecting an external distributor
- Generic Timers interface supporting 64-bit count input from an external system counter
- Reliability, Availability, and Serviceability (RAS) extension
- Debug and trace capabilities

NOTE

Cryptography extensions are available only when Data Engine unit is present.

DSU

DSU comprises the L3 cache, the Snoop Control Unit (SCU), internal interfaces to the cores, and external interfaces to the SoC.

- Memory subsystem features
  - 1024 KB L3 cache

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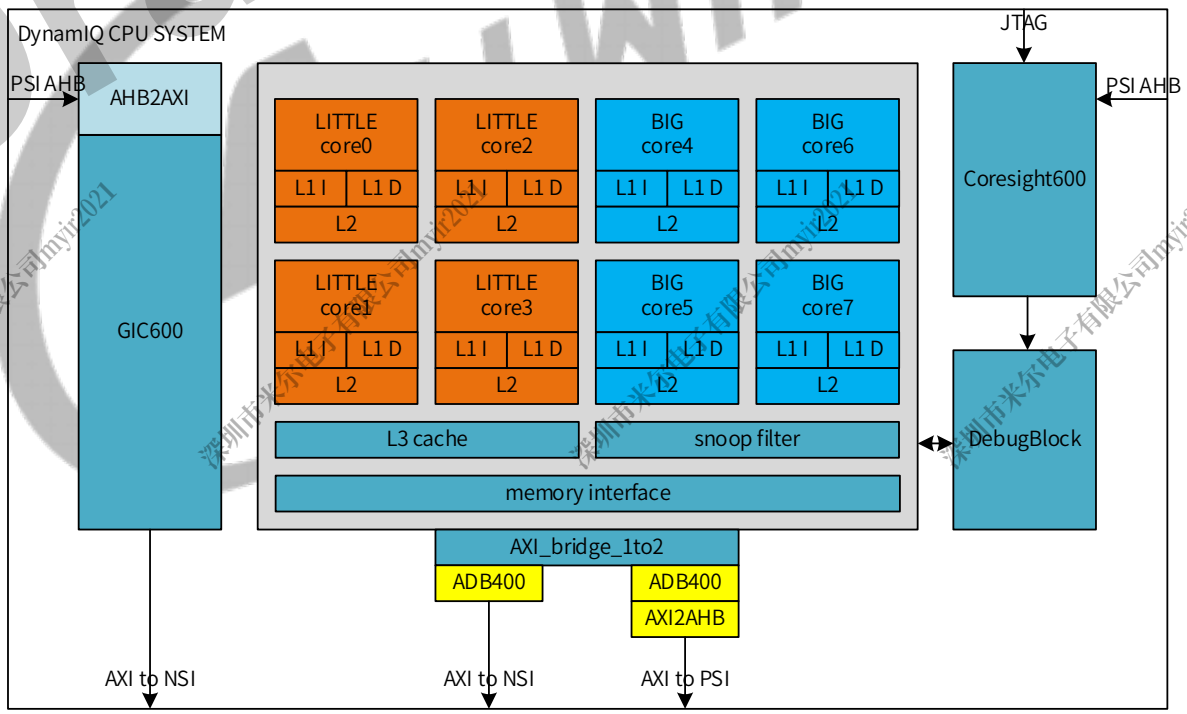
- Optional 16-way set-associative L3 cache, 64-byte cache line
- L3 memory system can be clocked at a rate synchronous to the external system interconnect or at integer multiples.
- L3 cache partial power down
- Optional cache protection in the form of Error Correcting Code (ECC) on L3 cache RAM instances
- 40-bit, 44-bit, and 48-bit physical addresses

- Main bus interface adopting AMBA 5 ACE protocol or AMBA 5 CHI protocol
- Optional 128-bit wide and I/O-coherent Accelerator Coherency Port (ACP)
- Optional 64-bit wide peripheral port
- ARMv8.2 debug logic
- Supports RAS

2.2.2 Block diagram

The following figure shows the block diagram of CPUX system.

Figure 2-1 CPUX System Block Diagram



The following table describes the components of T527 DynamIQ big. LITTLE cluster.

Table 2-1 CPUX DynamIQ Cluster Components

Components	Description
CPU bridges	For communication between cores and DSU buffers.

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Components	Description
SCU	The SCU maintains coherency and cache-to-cache transmission for all CPUX cores.
Debug and trace components	Each core allows tracing supported by Embedded Trace Macrocell (ETM). The trigger events from CPUX cores are transmitted through debug APB master/slave interface.
Clock and power management	The cluster supports low power mode and is controlled by a low power control module outside the cluster power-down domain. DSU and each CPUX core has independent P-channels. They could control the power mode through P-channels.
L3 memory interfaces	To access memory and peripherals.
DSU system control registers	Include information related to CPUX core configuration, such as: • Power management of the cluster • QOS and ID control of CHI bus • DSU hardware configuration information • L3 cache hit and miss count information

2.2.3 Functional Descriptions

2.2.3.1 Power Block System

Power Domain

The following table describes the power domain of the CPUX.

Table 2-2 CPUX Power domain

Power Domain	Power Switch	Description
VDD-CPUB	Yes	Power source of Core4-Core7. It is controlled by the PPU for each core.
VDD-CPUL	Yes	Power source of the cluster top and Core0-Core3. It is controlled by the PPU for the cluster top and each core.
VDD-SYS	No	Power source of CPUX system excluding the cluster top and CPUX cores. It is the same power supply of the SoC system.

Power Mode

CPUX cores support four power modes:

- Debug Recovery
- ON
- OFF (emulated)
- OFF

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DSU supports the following power modes

- ON: SFONLY_ON、1/4 ON、1/2 ON、3/4 ON、FULL ON
- Functional Retention: SFONLY FUNC_RET, ¼FUNC_RET, ½FUNC_RET, ¾FUNC_RET, FULL FUNC_RET
- OFF and OFF_EMU

2.2.3.2 CPU PLL Distribution and Clock Sources

The CPUX system contains three linear frequency modulation PLLs: CPU_L_PLL, CPU_DSU_PLL, and CPU_B_PLL. The following table shows the clock sources of CPUX cores and DSU.

Table 2-3 Clock Sources of CPUX Cores and DSU

CPUX Cores	Clock Sources	Description
Core0-Core3	CLK32K	• Generally, CPU_L_PLL is the main clock source of Core0-Core3. For all clock sources of Core0-Core3, refer to CPUA_CLK_REG register. • Generally, CPU_B_PLL is the main clock source of Core4-Core7. For all clock sources of Core4-Core7, refer to CPUB_CLK_REG register. • Generally, CPU_DSU_PLL is the main clock source of DSU. For all clock sources of DSU, refer to DSU_CLK_REG register.
	CLK16M_RC	
	HOSC	
	PERI0_600M	
	CPU_L_PLL	
Core4-Core7	CLK32K	
	CLK16M_RC	
	HOSC	
	PERI0_600M	
	CPU_PLL3CPU_B_PLL	
DSU	CLK32K	
	CLK16M_RC	
	HOSC	
	PERI0_600M	
	PLL_PERI0(2X)	
	CPU_DSU_PLL	

2.2.3.3 CPUX Reset System

The following table shows the input reset signal of the whole CPUX system.

Table 2-4 Reset signal description of CPUX System

Reset signal	Source	Description
DBGSYS_RST	CCU	For detailed information, please refer to the description of DBGSYS_RST in section 2.7.6.75 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000).
DSU_RSTN	PPU	Whether to reset is controlled by PPU according to the power mode.

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Reset signal	Source	Description
CORE_RSTN	PPU	Whether to reset is controlled by PPU according to the power mode.

2.2.4 Programming Guidelines

The following takes CPU_L_PLL as an example, CPU_DSU_PLL and CPU_B_PLL are the same.

NOTE

It is not suggested to enable or disable the PLLs during usage. When the clock is not required, it is recommended to configure the PLL_OUTPUT_EN bit of PLL control register as 0.

2.2.4.1 Enabling the Linear Frequency Modulation PLLs

Step 1 Write 1 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

Step 2 Configure the N, M, and P factors of the CPU_L_PLL_CTRL_REG register.

Step 3 Write 1 to the PLL_PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the CPU_L_PLL_CTRL_REG register.

Step 4 Write 1 to the LOCK_ENABLE bit (bit [29]) of the CPU_L_PLL_CTRL_REG register.

Step 5 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register.

Step 6 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 7 Wait for the status of the Lock to change to 1.

Step 8 Delay 10 ms.

Step 9 Write 0 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

2.2.4.2 Configuring the Frequency of Linear Frequency Modulation PLLs

Step 1 Configure the PLL_SSC_STEP bit (bit [3:0]) of the CPU_L_PLL_SSC_REG register to select required frequency modulation slope.

Step 2 Configure the PLL_SSC bit (bit [28:12]) of the CPU_L_PLL_SSC_REG register to set the SSC ampltitude.

Step 3 Write 1 to the PLL_SSC_MODE bit (bit [31]) of the CPU_L_PLL_SSC_REG register to enable linear frequency modulation.

Step 4 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register to update PLL configuration parameters.

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Step 5 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 6 Configure the N factor of the CPU_L_PLL_CTRL_REG register.

Step 7 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register to update PLL configuration parameters.

Step 8 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 9 Write 0 to the PLL_SSC_MODE bit (bit [31]) of the CPU_L_PLL_SSC_REG register to disable linear frequency modulation.

Step 10 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register to update PLL configuration parameters.

Step 11 Wait for the value of the PLL_UPDATE bit to change to 0.

2.2.4.3 Disabling the Linear Frequency Modulation PLLs

Follow the steps below to disable the PLL:

Step 1 Write 0 to the PLL_PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the CPU_L_PLL_CTRL_REG register.

Step 2 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register.

Step 3 Write 1 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

Step 4 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register.

Step 5 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 6 Write 0 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

2.2.5 Register list

Module Name	Base Address	Description
CPU_SUBSYS_CTRL	0x08000000	CPU Subsystem Control (4KB)
TIMESTAMP_STA	0x08010000	Timestamp Status Registers (4KB)
TIMESTAMP_CTRL	0x08020000	Timestamp Control Registers (4KB)
CPU_PLL_CFG	0x08817000	Cluster PLL configure (4KB)

2.2.5.1 CPU_SUBSYS_CTRL Register List

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GIC_JTAG_RST_CTRL	0x000C	GIC and JTAG reset control Register
DBG_STATE	0x001C	Debug State Register
CPU0_CTRL_REG	0x0020	CPU0 Control Register

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Register Name	Offset	Description
CPU1_CTRL_REG	0x0024	CPU1 Control Register
CPU2_CTRL_REG	0x0028	CPU2 Control Register
CPU3_CTRL_REG	0x002C	CPU3 Control Register
CPU4_CTRL_REG	0x0030	CPU4 Control Register
CPU5_CTRL_REG	0x0034	CPU5 Control Register
CPU6_CTRL_REG	0x0038	CPU6 Control Register
CPU7_CTRL_REG	0x003C	CPU7 Control Register
RVBARADDR0_L	0x0040	Reset Vector Base Address Register0_L
RVBARADDR0_H	0x0044	Reset Vector Base Address Register0_H
RVBARADDR1_L	0x0048	Reset Vector Base Address Register1_L
RVBARADDR1_H	0x004c	Reset Vector Base Address Register1_H
RVBARADDR2_L	0x0050	Reset Vector Base Address Register2_L
RVBARADDR2_H	0x0054	Reset Vector Base Address Register2_H
RVBARADDR3_L	0x0058	Reset Vector Base Address Register3_L
RVBARADDR3_H	0x005C	Reset Vector Base Address Register3_H
RVBARADDR4_L	0x0060	Reset Vector Base Address Register4_L
RVBARADDR4_H	0x0064	Reset Vector Base Address Register4_H
RVBARADDR5_L	0x0068	Reset Vector Base Address Register5_L
RVBARADDR5_H	0x006c	Reset Vector Base Address Register5_H
RVBARADDR6_L	0x0070	Reset Vector Base Address Register6_L
RVBARADDR6_H	0x0074	Reset Vector Base Address Register6_H
RVBARADDR7_L	0x0078	Reset Vector Base Address Register7_L
RVBARADDR7_H	0x007C	Reset Vector Base Address Register7_H
PLL_CTRL_REG0	0x0140	PLL control register 0
PLL_CTRL_REG1	0x0144	PLL control register 1

2.2.5.2 TIMESTAMP_STA Register List

Register Name	Offset	Description
CNTCVLREAD	0x0000	Current value of Counter[31:0]
CNTCVUREAD	0x0004	Current value of Counter[63:32]
PIDR4	0x0FD0	Peripheral Identification Register 4
PIDR5	0x0FD4	Peripheral Identification Register 5
PIDR6	0x0FD8	Peripheral Identification Register 6
PIDR7	0x0FDC	Peripheral Identification Register 7
PIDR0	0x0FE0	Peripheral Identification Register 0
PIDR1	0x0FE4	Peripheral Identification Register 1
PIDR2	0x0FE8	Peripheral Identification Register 2
PIDR3	0x0FEC	Peripheral Identification Register 3
CIDR0	0x0FF0	Component Identification Register 0
CIDR1	0x0FF4	Component Identification Register 1

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Register Name	Offset	Description
CIDR2	0x0FF8	Component Identification Register 2
CIDR3	0x0FFc	Component Identification Register 3

2.2.5.3 TIMESTAMP_CTRL Register List

Register Name	Offset	Description
CNTCR	0x0000	Counter Control Register
CNTSR	0x0004	Counter Status Register
CNTCVL	0x0008	Current value of Counter[31:0]
CNTCVU	0x000c	Current value of Counter[63:32]
CNTFID0	0x0020	Base Frequency ID register
ITSTAT	0x0EF8	Integration Test Status Register
ITCTRL	0x0F00	Integration Mode Control Register
PIDR4	0x0FD0	Peripheral Identification Register 4
PIDR5	0x0FD4	Peripheral Identification Register 5
PIDR6	0x0FD8	Peripheral Identification Register 6
PIDR7	0x0FDC	Peripheral Identification Register 7
PIDR0	0x0FE0	Peripheral Identification Register 0
PIDR1	0x0FE4	Peripheral Identification Register 1
PIDR2	0x0FE8	Peripheral Identification Register 2
PIDR3	0x0FEC	Peripheral Identification Register 3
CIDR0	0x0FF0	Component Identification Register 0
CIDR1	0x0FF4	Component Identification Register 1
CIDR2	0x0FF8	Component Identification Register 2
CIDR3	0x0FFc	Component Identification Register 3

2.2.5.4 CPU_PLL_CTRL Register List

Register Name	Offset	Description
CPU_L_PLL_CTRL_REG	0x0004	CPU_L_PLL Control Register
CPU_DSU_PLL_CTRL_REG	0x0008	CPU_DSU_PLL Control Register
CPU_B_PLL_CTRL_REG	0x000c	CPU_B_PLL Control Register
CPU_L_PLL__PAT0_CTRL_REG	0x0010	CPU_L_PLL Pattern0 Control Register
CPU_L_PLL__PAT1_CTRL_REG	0x0014	CPU_L_PLL Pattern1 Control Register
CPU_DSU_PLL__PAT0_CTRL_REG	0x0018	CPU_DSU_PLL Pattern0 Control Register
CPU_DSU_PLL__PAT1_CTRL_REG	0x001c	CPU_DSU_PLL Pattern1 Control Register
CPU_B_PLL__PAT0_CTRL_REG	0x0020	CPU_B_PLL Pattern0 Control Register
CPU_B_PLL__PAT1_CTRL_REG	0x0024	CPU_B_PLL Pattern1 Control Register
CPU_L_PLL_BIAS_REG	0x002c	CPU_L_PLL Bias Register
CPU_DSU_PLL_BIAS_REG	0x0030	CPU_DSU_PLL Bias Register
CPU_B_PLL_BIAS_REG	0x0034	CPU_B_PLL Bias Register

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Register Name	Offset	Description
CPU_L_PLL_TUN0_REG	0x003C	CPU_L_PLL Tuning0 Control Register
CPU_L_PLL_TUN1_REG	0x0040	CPU_L_PLL Tuning1 Control Register
CPU_DSU_PLL_TUN0_REG	0x0044	CPU_DSU_PLL Tuning0 Control Register
CPU_DSU_PLL_TUN1_REG	0x0048	CPU_DSU_PLL Tuning1 Control Register
CPU_B_PLL_TUN0_REG	0x004C	CPU_B_PLL Tuning0 Control Register
CPU_B_PLL_TUN1_REG	0x0050	CPU_B_PLL Tuning1 Control Register
CPU_L_PLL_SSC_REG	0x0054	CPU_L_PLL SSC Register
CPU_DSU_PLL_SSC_REG	0x0058	CPU_DSU_PLL SSC Register
CPU_B_PLL_SSC_REG	0x005c	CPU_B_PLL SSC Register
CPUA_CLK_REG	0x0060	CPUA Clock Register
CPUB_CLK_REG	0x0064	CPUB Clock Register
CPU_GATING_REG	0x0068	CPU Gating Configuration Register
DSU_CLK_REG	0x006c	DSU Clock Register
PLL_TEST_CLK_SEL	0x0070	PLL Test Clock Selection Register

2.2.6 CPU_SUBSYS_CTRL Register Description

2.2.6.1 0x0000 General Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GENER_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	GICCDISABLE DEBUGBLOCK Control
0	R/W	0x0	CDBGRSTACK Debug Reset ACK

2.2.6.2 0x000C GIC and JTAG Reset Control Register (Default Value: 0x0000_003F)

Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	EXM_CLR [3:0] Clear the status of interface, for debug
15:7	/	/	/
6	R/W	0x1	GIC_DBG_RSTN GIC OUTRE Reset 0: Assert 1: De-assert.

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Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	GIC_OUT_RSTN GIC OUTRE Reset 0: Assert 1: De-assert.
4	R/W	0x1	GIC_OUT_MBIST_RSTN GIC OUTER MBIST Reset 0: Assert 1: De-assert.
3	R/W	0x1	COREPLL_RST COREPLL Reset 0: Assert 1: De-assert.
2	R/W	0x1	CS_RST CoreSight Reset 0: Assert 1: De-assert.
1	R/W	0x1	PORTRST JTAG Portrst 0: Assert 1: De-assert.
0	R/W	0x1	TRST Jtag TRST 0: Assert 1: De-assert.

2.2.6.3 0x001C Debug State Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DBG_STATE
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CLU_PWRSW_STA
23:0	/	/	/

2.2.6.4 0x0020 CPU0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CPU0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0020			Register Name: CPU0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Cluster 0 CPU0 AA64NAA32 Register Width State 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.5 0x0024 CPU1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CPU1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU1 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

2.2.6.6 0x0028 CPU2 Control Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CPU2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU2 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.7 0x002C CPU3 Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CPU3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU3 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

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2.2.6.8 0x0030 CPU4 Control Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CPU4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU4 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.9 0x0034 CPU5 Control Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CPU5_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU5 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.10 0x0038 CPU6 Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CPU6_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU6 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.11 0x003C CPU7 Control Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x003C			Register Name: CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Cluster 0 CPU7 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.12 0x0040 Reset Vector Base Address Register0_L (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: RVBARADDR0_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU0.
1:0	/	/	/

2.2.6.13 0x0044 Reset Vector Base Address Register0_H (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: RVBARADDR0_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU0.

2.2.6.14 0x0048 Reset Vector Base Address Register1_L (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: RVBARADDR1_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU1.
1:0	/	/	/

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2.2.6.15 0x004C Reset Vector Base Address Register1_H (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: RVBARADDR1_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU1.

2.2.6.16 0x0050 Reset Vector Base Address Register2_L (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: RVBARADDR2_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU2.
1:0	/	/	/

2.2.6.17 0x0054 Reset Vector Base Address Register2_H (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: RVBARADDR2_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU2.

2.2.6.18 0x0058 Reset Vector Base Address Register3_L (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: RVBARADDR3_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU3.
1:0	/	/	/

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2.2.6.19 0x005C Reset Vector Base Address Register3_H (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: RVBARADDR3_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU3.

2.2.6.20 0x0060 Reset Vector Base Address Register4_L (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: RVBARADDR4_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU4.
1:0	/	/	/

2.2.6.21 0x0064 Reset Vector Base Address Register4_H (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: RVBARADDR4_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU4.

2.2.6.22 0x0068 Reset Vector Base Address Register5_L (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: RVBARADDR5_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU5.
1:0	/	/	/

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2.2.6.23 0x006C Reset Vector Base Address Register5_H (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: RVBARADDR5_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU5.

2.2.6.24 0x0070 Reset Vector Base Address Register6_L (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: RVBARADDR6_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU6.
1:0	/	/	/

2.2.6.25 0x0074 Reset Vector Base Address Register6_H (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: RVBARADDR6_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU6.

2.2.6.26 0x0078 Reset Vector Base Address Register7_L (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: RVBARADDR7_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU7.
1:0	/	/	/

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2.2.6.27 0x007C Reset Vector Base Address Register7_H (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: RVBARADDR7_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU7.

2.2.6.28 0x0140 PLL Control Register 0 (Default: 0x0000_0007)

Offset: 0x0140			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL Test Clock Selection 0: XTAL. 1: External Clock
23:3	/	/	/
2	R/W	0x1	GM1 XTAL Gain Control Bit1
1	R/W	0x1	GM0 XTAL Gain Control Bit0
0	R/W	0x1	PLL_BIAS_EN PLL Bias Enable 0: Disable 1: Enable.

2.2.6.29 0x0144 PLL Control Register 1 (Default: 0x00040005)

Offset: 0x0144			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD Key Field for LDO Enable bit If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/

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Offset: 0x0144			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
18:16	R/W	0x4	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control 000: 0.90 V 001: 0.94 V 010: 0.98 V 011: 1.02 V 100: 1.06 V 101: 1.10 V 110: 1.14 V 111: 1.18 V
15:5	/	/	/
4	R/W	0x0	MBIAS_EN Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias
3	R/W	0x0	PLLTEST_EN. PLLTEST pin enable For Verify (Back door clock PLLTEST enable). 0：Output clock is gated off. 1：Clock Output. The clock is the clock output to the PLL and the clock after frequency division through PLLTEST pin.
2:1	/	/	/
0	R/W	0x1	LDO_EN. PLL Power Enable (The power source is VCC_PLL) 0: Disable 1: Enable

2.2.7 TIMESTAMP_STA Register Description

2.2.7.1 0x0000 Current value of Counter [31:0] Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CNTCVLREAD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNTCVL32 The lower 32 bits of the current timestamp counter value.

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2.2.7.2 0x0004 Current value of Counter [63:32] Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CNTCVUREAD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNTCVU32 The upper 32 bits of the current timestamp counter value.

2.2.7.3 0x0FD0 Peripheral Identification Register 4 Register (Default Value:0x0000_0004)

Offset: 0x0FD0			Register Name: PIDR4
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	SIZE Indicates the memory size that is used by this component. Returns 0 indicating that the component uses an UNKNOWN number of 4KB blocks. Using the SIZE field to indicate the size of the component is deprecated.
3:0	R	0x4	DES_2 JEP106 continuation code. Together, with PIDR2.DES_1 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

2.2.7.4 0x0FD4 Peripheral Identification Register 5 Register (Default Value:0x0000_0000)

Offset: 0x0FD4			Register Name: PIDR5
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR5 Reserved

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2.2.7.5 0x0FD8 Peripheral Identification Register 6 Register (Default Value:0x0000_0000)

Offset: 0x0FD8			Register Name: PIDR6
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR6 Reserved

2.2.7.6 0x0FDC Peripheral Identification Register 7 Register (Default Value:0x0000_0000)

Offset: 0x0FDC			Register Name: PIDR7
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR7 Reserved

2.2.7.7 0x0FE0 Peripheral Identification Register 0 Register (Default Value:0x0000_0093)

Offset: 0x0FE0			Register Name: PIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x93	PART_0 Part number, bits [7:0]. Taken together with PIDR1.PART_1 it indicates the component. The Part Number is selected by the designer of the component.

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2.2.7.8 0x0FE4 Peripheral Identification Register 1 Register (Default Value:0x0000_00B1)

Offset: 0x0FE4			Register Name: PIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xB	DES_0 JEP106 identification code, bits [3:0]. Together, with PIDR4.DES_2 and PIDR2.DES_1, they indicate the designer of the component and not the implementer, except where the two are the same.
3:0	R	0x1	PART_1 Part number, bits [11:8]. Taken together with PIDR0.PART_0 it indicates the component. The Part Number is selected by the designer of the component.

2.2.7.9 0x0FE8 Peripheral Identification Register 2 Register (Default Value:0x0000_000B)

Offset: 0x0FE8			Register Name: PIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVISION Revision. It is an incremental value starting at 0x0 for the first design of a component. See the css600 Component list in Chapter 1 for information on the RTL revision of the component.
3	R	0x1	JEDEC 1 - Always set. Indicates that a JEDEC assigned value is used.
2:0	R	0x3	DES_1 JEP106 identification code, bits [6:4]. Together, with PIDR4.DES_2 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

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2.2.7.10 0x0FEC Peripheral Identification Register 3 Register (Default Value:0x0000_0000)

Offset: 0x0FEC			Register Name: PIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVAND This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is 0x0.
3:0	R	0x0	CMOD Customer Modified. Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is 0x0.

2.2.7.11 0x0FF0 Component Identification Register 0 Register (Default Value:0x0000_000D)

Offset: 0x0FF0			Register Name: CIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0D	PRMBL_0 Preamble. Returns 0x0D.

2.2.7.12 0x0FF4 Component Identification Register 1 Register (Default Value:0x0000_00F0)

Offset: 0x0FF4			Register Name: CIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xF	CLASS Component class. Returns 0xF, indicating CoreLink, PrimeCell, or system component.
3:0	R	0x0	PRMBL_1 Preamble. Returns 0x0.

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2.2.7.13 0x0FF8 Component Identification Register 2 Register (Default Value:0x0000_0005)

Offset: 0x0FF8			Register Name: CIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x05	PRMBL_2 Preamble. Returns 0x05.

2.2.7.14 0x0FFC Component Identification Register 3 Register (Default Value:0x0000_00B1)

Offset: 0x0FFC			Register Name: CIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0xB1	PRMBL_3 Preamble. Returns 0xB1.

2.2.8 TIMESTAMP_CTRL Register Description

2.2.8.1 0x0000 Counter Control Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CNTCR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	HDBG Halt On Debug 0 Do not halt on debug. The HALT_REQ signal into the counter has no effect. 1 Halt on debug. When the HALT_REQ pulse is received, the count value is held static.
0	R/W	0x0	EN Enable Bit 0 The counter is disabled. Count is not incrementing. 1 The counter is enabled. Count is incrementing.

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2.2.8.2 0x0004 Counter Status Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CNTSR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x0	DBGH Debug status. 0 Debug is halted 1 Debug is not halted.
0	/	/	/

2.2.8.3 0x0008 Current value of Counter [31:0] Register (Default Value:0x0000_0000)

Offset: 0x0008			Register Name: CNTCVL
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNTCVL32 Reads to this register return the lower 32 bits of the current timestamp counter value. To change the current timestamp value, write the lower 32 bits of the new value to this register before writing the upper 32 bits to CNTCVU. The timestamp value is not changed until the CNTCVU register is written to.

2.2.8.4 0x000C Current value of Counter [63:32] Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CNTCVU
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNTCVU32 Reads to this register return the upper 32 bits of the current timestamp counter value. To change the current timestamp value, write the lower 32 bits of the new value to CNTCVL before writing the upper 32 bits to this register. The 64-bit timestamp value is updated with the value from both writes when this register is written to.

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2.2.8.5 0x0020 Base Frequency ID Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name:CNTFID0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	Freq Frequency in number of ticks per second. Up to 4GHz can be specified.

2.2.8.6 0x0EF8 Integration Test Status Register (Default Value:0x0000_0000)

Offset: 0x0EF8			Register Name: ITSTAT
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x0	ITTRESTARTREQ Integration Test Restart Request status of the RESTART_REQ input. Integration testing mode:Behaves as a sticky bit and latches to 1 when TSGEN receives restart request. Cleared onreading this register. If RESTART_REQ is asserted in the same cycle as an APB read of this register, the read takes priority and the register is cleared as a result. Always returns 0 in normal functional mode.
0	R	0x0	ITHALTREQ Integration Test Halt Request status of the HALT_REQ input. Integration testing mode: Behaves as a sticky bit and latches to 1 when TSGEN receives halt request. Cleared on reading this register. If HALT_REQ is asserted in the same cycle as an APB read of this register, the read takes priority and the register is cleared as a result. Always returns 0 in normal functional mode.

2.2.8.7 0x0F00 Integration Mode Control Register (Default Value:0x0000_0000)

Offset: 0x0F00			Register Name: ITCTRL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0F00			Register Name: ITCTRL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	IME Integration Mode Enable. When set, the component enters integration mode, enabling topology detection or integration testing to be performed.

2.2.8.8 0x0FD0 Peripheral Identification Register 4 Register (Default Value:0x0000_0004)

Offset: 0x0FD0			Register Name:PIDR4
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	SIZE Indicates the memory size that is used by this component. Returns 0 indicating that the component uses an UNKNOWN number of 4KB blocks. Using the SIZE field to indicate the size of the component is deprecated.
3:0	R	0x4	DES_2 JEP106 continuation code. Together, with PIDR2.DES_1 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

2.2.8.9 0x0FD4 Peripheral Identification Register 5 Register (Default Value:0x0000_0000)

Offset: 0x0FD4			Register Name:PIDR5
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR5 Reserved

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2.2.8.10 0x0FD8 Peripheral Identification Register 6 Register (Default Value:0x0000_0000)

Offset: 0x0FD8			Register Name:PIDR6
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR6 Reserved

2.2.8.11 0x0FDC Peripheral Identification Register 7 Register (Default Value:0x0000_0000)

Offset: 0x0FDC			Register Name:PIDR7
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR7 Reserved

2.2.8.12 0x0FE0 Peripheral Identification Register 0 Register (Default Value:0x0000_0093)

Offset: 0x0FE0			Register Name:PIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x93	PART_0 Part number, bits [7:0]. Taken together with PIDR1.PART_1 it indicates the component. The Part Number is selected by the designer of the component.

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2.2.8.13 0x0FE4 Peripheral Identification Register 1 Register (Default Value:0x0000_00B1)

Offset: 0x0FE4			Register Name:PIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xB	DES_0 JEP106 identification code, bits [3:0]. Together, with PIDR4.DES_2 and PIDR2.DES_1, they indicate the designer of the component and not the implementer, except where the two are the same.
3:0	R	0x1	PART_1 Part number, bits [11:8]. Taken together with PIDR0.PART_0 it indicates the component. The Part Number is selected by the designer of the component.

2.2.8.14 0x0FE8 Peripheral Identification Register 2 Register (Default Value:0x0000_000B)

Offset: 0x0FE8			Register Name:PIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVISION Revision. It is an incremental value starting at 0x0 for the first design of a component. For information on the RTL revision of the component, see the css600 Component list in chapter 1 of *coresight_soc600_technical_reference_manual_100806_0300_00_en.pdf*
3	R	0x1	JEDEC 1: Always set. Indicates that a JEDEC assigned value is used.
2:0	R	0x3	DES_1 JEP106 identification code, bits [6:4]. Together, with PIDR4.DES_2 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

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2.2.8.15 0x0FEC Peripheral Identification Register 3 Register (Default Value:0x0000_0000)

Offset: 0x0FEC			Register Name:PIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVAND This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is 0x0.
3:0	R	0x0	CMOD Customer Modified. Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is 0x0.

2.2.8.16 0x0FF0 Component Identification Register 0 Register (Default Value:0x0000_000D)

Offset: 0x0FF0			Register Name:CIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0D	PRMBL_0 Preamble. Returns 0x0D.

2.2.8.17 0x0FF4 Component Identification Register 1 Register (Default Value:0x0000_00F0)

Offset: 0x0FF4			Register Name:CIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xF	CLASS Component class. Returns 0xF, indicating CoreLink, PrimeCell, or system component.
3:0	R	0x0	PRMBL_1 Preamble. Returns 0x0.

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2.2.8.18 0x0FF8 Component Identification Register 2 Register (Default Value:0x0000_0005)

Offset: 0x0FF8			Register Name:CIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x05	PRMBL_2 Preamble. Returns 0x05.

2.2.8.19 0x0FFC Component Identification Register 3 Register (Default Value:0x0000_00B1)

Offset: 0x0FFC			Register Name:CIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0xB1	PRMBL_3 Preamble. Returns 0xB1.

2.2.9 CPU_PLL_CFG Register Description

2.2.9.1 0x0004 CPU_L_PLL Control Register (Default Value: 0x4880_1400)

Offset: 0x0004			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable The CPU_L_PLL= InputFreq*N/P/(M0*M1). Note: The CPU_L_PLL output frequency must be in the range from 480 MHz to 2.6 GHz. And the default value of CPU_L_PLL is 480 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO Enable. 0: Disable 1: Enable

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Offset: 0x0004			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock INFO. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26	R/WAC	0x0	PLL_UPDATE Write q update the CFG to PLL, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R/W	0x0	PLL_P PLL PREDIV P P = PLL_P + 1
15:8	R/W	0x14	PLL_N PLL N N= PLL_N
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/

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Offset: 0x0004			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PLL_M1 PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

2.2.9.2 0x0008 CPU_DSU_PLL Control Register (Default Value: 0x4880_1400)

Offset: 0x0008			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The CPU_DSU_PLL= InputFreq*N/P/(M0*M1). Note: The CPU_DSU_PLL output frequency must be in the range from 200 MHz to 3 GHz. And the default value of CPU_DSU_PLL is 408 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26	R/WAC	0x0	PLL_UPDATE Write q update the CFG to PLL, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET

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Offset: 0x0008			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 15.
19:16	R/W	0x0	PLL_P PLL PREDIV P P = PLL_P + 1
15:8	R/W	0x14	PLL_N PLL N N= PLL_N
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

2.2.9.3 0x000C CPU_B_PLL Control Register (Default Value: 0x4880_1400)

Offset: 0x000C			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The CPU_B_PLL= InputFreq*N/P/(M0*M1). Note: The CPU_B_PLL output frequency must be in the range from 480 MHz to 2.6 GHz. And the default value of CPU_B_PLL is 480 MHz when the crystal oscillator is 24 MHz.

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Offset: 0x000C			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x1	PLL_LDO_EN. LDO Enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock INFO 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26	R/WAC	0x0	PLL_UPDATE Write q update the CFG to PLL, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 15.
19:16	R/W	0x0	PLL_P P = PLL_P + 1
15:8	R/W	0x14	PLL_N N= PLL_N
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/

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Offset: 0x000C			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15

2.2.9.4 0x0010 CPU_L_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CPU_L_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular (1bit) 11: Triangular (n bit)
28:17	R/W	0x0	WAVE_STEP Wave Step
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.2.9.5 0x0014 CPU_L_PLL Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CPU_L_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	SDM_CYCLE SDM Cycle SDM_CYCLE=SDM_FRE/CLK_SDM/2
21	/	/	/
20	R/W	0x0	SDM_DIRECTION SDM direction 0: UP 1: DOWM
19	/	/	/
18	R/W	0x0	DITHER_EN Dither Enable
17	R/W	0x0	FRAC_EN Fraction Enable

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Offset: 0x0014			Register Name: CPU_L_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	FRAC_IN Fraction In

2.2.9.6 0x0018 CPU_DSU_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CPU_DSU_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular (1bit) 11: Triangular (n bit)
28:17	R/W	0x0	WAVE_STEP Wave Step
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.2.9.7 0x001C CPU_DSU_PLL Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: CPU_DSU_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	SDM_CYCLE SDM Cycle SDM_CYCLE=SDM_FRE/CLK_SDM/2
21	/	/	/
20	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWM
19	/	/	/
18	R/W	0x0	DITHER_EN Dither Enable
17	R/W	0x0	FRAC_EN Fraction Enable
16:0	R/W	0x0	FRAC_IN Fraction In

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2.2.9.8 0x0020 CPU_B_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CPU_B_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular (1 bit) 11: Triangular (n bit)
28:17	R/W	0x0	WAVE_STEP Wave Step
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.2.9.9 0x0024 CPU_B_PLL Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CPU_B_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	SDM_CYCLE SDM Cycle SDM_CYCLE=SDM_FRE/CLK_SDM/2
21	/	/	/
20	R/W	0x0	SDM_DIRECTION SDM direction 0: UP 1: DOWM
19	/	/	/
18	R/W	0x0	DITHER_EN Dither Enable
17	R/W	0x0	FRAC_EN Fraction Enable
16:0	R/W	0x0	FRAC_IN Fraction In

2.2.9.10 0x002C CPU_L_PLL Bias Register (Default Value: 0x0010_0000)

Offset: 0x002C			Register Name: CPU_L_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

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Offset: 0x002C			Register Name: CPU_L_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
20:16	R/W	0x10	PLL_CP PLL Current Bias Control
15:0	/	/	/

2.2.9.11 0x0030 CPU_DSU_PLL Bias Register (Default Value: 0x0010_0000)

Offset: 0x0030			Register Name: CPU_DSU_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x10	PLL_CP PLL Current Bias Control
15:0	/	/	/

2.2.9.12 0x0034 CPU_B_PLL Bias Register (Default Value: 0x0010_0000)

Offset: 0x0034			Register Name: CPU_B_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x10	PLL_CP PLL Current Bias Control
15:0	/	/	/

2.2.9.13 0x003C CPU_L_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CPU_L_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR

2.2.9.14 0x0040 CPU_L_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x0040			Register Name: CPU_L_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN
30	R/W	0x0	PLL_FF_EN
29	R/W	0x0	PLL_SS_EN

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Offset: 0x0040			Register Name: CPU_L_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
28:20	R/W	0x0	PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC

2.2.9.15 0x0044 CPU_DSU_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CPU_DSU_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR

2.2.9.16 0x0048 CPU_DSU_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x0048			Register Name: CPU_DSU_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN
30	R/W	0x0	PLL_FF_EN.
29	R/W	0x0	PLL_SS_EN
28:20	R/W	0x0	PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC

2.2.9.17 0x004C CPU_B_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CPU_B_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR

2.2.9.18 0x0050 CPU_B_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x0050			Register Name: CPU_B_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN.

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Offset: 0x0050			Register Name: CPU_B_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	PLL_FF_EN
29	R/W	0x0	PLL_SS_EN
28:20	R/W	0x0	PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC

2.2.9.19 0x0054 CPU_L_PLL SSC Register (Default Value: 0x4CCC_A000)

Offset: 0x0054			Register Name: CPU_L_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SSC_MODE 0: Normal Mode 1:Continuously Frequency Scale
30	R/W	0x1	PLL_SSC_RSTN SSC RSTN Bake Up
29	R/W	0x0	PLL_SSC_CLK_SEL SSC CLK Selection 0: REF_CLK 1: PLL_CLK_SDM
28:12	R/W	0xCCCA	PLL_SSC SSC amplitude must be an integer multiple of 2^step. spread spectrum amplitude = (SSC amplitude + 2^step) *24/(2^17), unit: MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_PHASE_COMPENSATE The value of bit[6:4] is based on 24M clock, then the default PLL phase compensate is (3/24000000)s.

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Offset: 0x0054			Register Name: CPU_L_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PLL_SSC_STEP 0000:0.00439MHz/us (576/2^17) 0001:0.00879MHz/us (576/2^16) 0010:0.01758MHz/us (576/2^15) 0011:0.03516MHz/us (576/2^14) 0100:0.07031MHz/us (576/2^13) 0101:0.14062MHz/us (576/2^12) 0110:0.28125MHz/us (576/2^11) 0111:0.56250MHz/us (576/2^10) 1000:1.12500MHz/us (576/2^9) 1001:2.25000MHz/us (576/2^8) 1010:4.50000MHz/us (576/2^7) 1011:9.00000MHz/us (576/2^6) Others:0.00439MHz/us (576/2^17)

2.2.9.20 0x0058 CPU_DSU_PLL SSC Register (Default Value: 0x4CCC_A000)

Offset: 0x0058			Register Name: CPU_DSU_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SSC_MODE 0: Normal Mode 1:Continuously Frequency Scale
30	R/W	0x1	PLL_SSC_RSTN SSC RSTN Bake Up
29	R/W	0x0	PLL_SSC_CLK_SEL SSC CLK Selection 0: REF_CLK 1: PLL_CLK_SDM
28:12	R/W	0xCCCA	PLL_SSC SSC amplitude must be an integer multiple of 2^step. spread spectrum amplitude = (SSC amplitude + 2^step) *24/(2^17), unit: MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_PHASE_COMPENSATE The value of bit[6:4] is based on 24M clock, then the default PLL phase compensate is (3/24000000)s.

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Offset: 0x0058			Register Name: CPU_DSU_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PLL_SSC_STEP 0000:0.00439MHz/us (576/2^17) 0001:0.00879MHz/us (576/2^16) 0010:0.01758MHz/us (576/2^15) 0011:0.03516MHz/us (576/2^14) 0100:0.07031MHz/us (576/2^13) 0101:0.14062MHz/us (576/2^12) 0110:0.28125MHz/us (576/2^11) 0111:0.56250MHz/us (576/2^10) 1000:1.12500MHz/us (576/2^9) 1001:2.25000MHz/us (576/2^8) 1010:4.50000MHz/us (576/2^7) 1011:9.00000MHz/us (576/2^6) Others:0.00439MHz/us (576/2^17)

2.2.9.21 0x005C CPU_B_PLL SSC Register (Default Value: 0x4CCC_A000)

Offset: 0x005C			Register Name: CPU_B_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SSC_MODE 0: Normal Mode 1:Continuously Frequency Scale
30	R/W	0x1	PLL_SSC_RSTN SSC RSTN Bake Up
29	R/W	0x0	PLL_SSC_CLK_SEL SSC CLK Selection 0: REF_CLK 1: PLL_CLK_SDM
28:12	R/W	0xCCCA	PLL_SSC SSC amplitude must be an integer multiple of 2^step. spread spectrum amplitude = (SSC amplitude + 2^step) *24/(2^17), unit: MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_PHASE_COMPENSATE The value of bit[6:4] is based on 24M clock, then the default PLL phase compensate is (3/24000000)s.

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Offset: 0x005C			Register Name: CPU_B_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PLL_SSC_STEP 0000:0.00439MHz/us (576/2^17) 0001:0.00879MHz/us (576/2^16) 0010:0.01758MHz/us (576/2^15) 0011:0.03516MHz/us (576/2^14) 0100:0.07031MHz/us (576/2^13) 0101:0.14062MHz/us (576/2^12) 0110:0.28125MHz/us (576/2^11) 0111:0.56250MHz/us (576/2^10) 1000:1.12500MHz/us (576/2^9) 1001:2.25000MHz/us (576/2^8) 1010:4.50000MHz/us (576/2^7) 1011:9.00000MHz/us (576/2^6) Others:0.00439MHz/us (576/2^17)

2.2.9.22 0x0060 CPUA Clock Register (Default Value: 0x0000_0305)

Offset: 0x0060			Register Name: CPUA_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CPUA_CLK_SEL Clock Source Selection 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPU1PLL/P 100: PERI0_600M 101: CPU0PLL CPUA_CLK = Clock Source The clock MUX supports glitch-free switch and dynamic configuration.
23:18	/	/	/

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Offset: 0x0060			Register Name: CPUA_CLK_REG
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	CPU_L_PLL_OUT_EXT_DIVP Factor P 00: 1 01: 2 10: 4 11: \ When the output clock is less than 288 MHz, it can divide P to get the required clock frequency.
15:10	/	/	/
9:8	R/W	0x3	CPU_APB_DIV_CFG. Factor N. (N = FACTOR_N +1) FACTOR_N is 1 or 3. The clock division is no-burr switch, and supports dynamic configuration.
7:4	/	/	/
3:2	R/W	0x1	CPU_PERI_DIV_CFG. Factor M1:(M= FACTOR_M1 +1) FACTOR_M1 is 0, 1, or 3. The clock division is no-burr switch, and supports dynamic configuration.
1:0	R/W	0x1	CPU_AXI_DIV_CFG. Factor M:(M= FACTOR_M +1) FACTOR_M is from 1 to 3 The clock division is no-burr switch, and supports dynamic configuration.

2.2.9.23 0x0064 CPUB Clock Register (Default Value: 0x0000_0305)

Offset: 0x0064			Register Name: CPUB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

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Offset: 0x0064			Register Name: CPUB_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CPUB_CLK_SEL. Clock Source Selection. 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPU3PLL/P 100: PERI0_600M 101: CPU0PLL CPU_CLK = Clock Source. The clock MUX supports glitch-free switch and dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	CPU_B_PLL_OUT_EXT_DIVP. Factor P 00: 1 01: 2 10: 4 11: \ When the output clock is less than 288 MHz, it can divide P to get the required clock frequency.
15:0	/	/	/

2.2.9.24 0x0068 CPU Gating Configuration Register (Default Value: 0x0000_0007)

Offset: 0x0068			Register Name: CPU_GATING_REG:
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD CPU Gating Field If CPU_GATING_FIELD==16’h16AA，the bit [15:0] can be configured.
15:4	/	/	/
3	R/W	0x0	DSU_PPU_SW_GATE_EN DSU PPU Control Enable 0: Disable 1: Enable
2	R/W	0x1	DSU_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON

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Offset: 0x0068			Register Name: CPU_GATING_REG:
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	CPUB_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON
0	R/W	0x1	CPUA_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON

2.2.9.25 0x006C DSU Clock Register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: DSU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	DSU_CLK_SEL Clock Source Selection 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPU2PLL/P 100: PERI0PLL2X 101: PERI0_600M DSU_CLK = Clock Source. CPU_AXI Clock = DSU_CLK/M. CPU_APB Clock= DSU_CLK/N. CPU_GIC Clock=DSU_CLK/M1. The clock MUX supports glitch-free switch and dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	CPU_DSU_PLL_OUT_EXT_DIVP Factor P 00: 1 01: 2 10: 4 11: \ When the output clock is less than 288 MHz, it can divide P to get the required clock frequency.
15:0	/	/	/

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2.2.9.26 0x0070 PLL Test Clock Selection Register (Default Value: 0x0000_0300)

Offset: 0x0070			Register Name: PLL_TEST_CLK_SEL
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
9:8	R/W	0x3	PLL_CFG_CLK_DIV PLL Config Clock Div
7:1	/	/	/
0	R/W	0x0	CLK_SEL Clock Selection 0: COREPLLA 1: DSU_CLK

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2.3 RISC-V System (RISCV)

2.3.1 Overview

The RISC-V system includes RISC IP core and related peripheral devices (AHB_Decoder, AHB2APB, RISCV_CFG, RISC_TIMESTAMP, and so on), which is able to be interconnected to DSP system by DSP AHB Matrix.

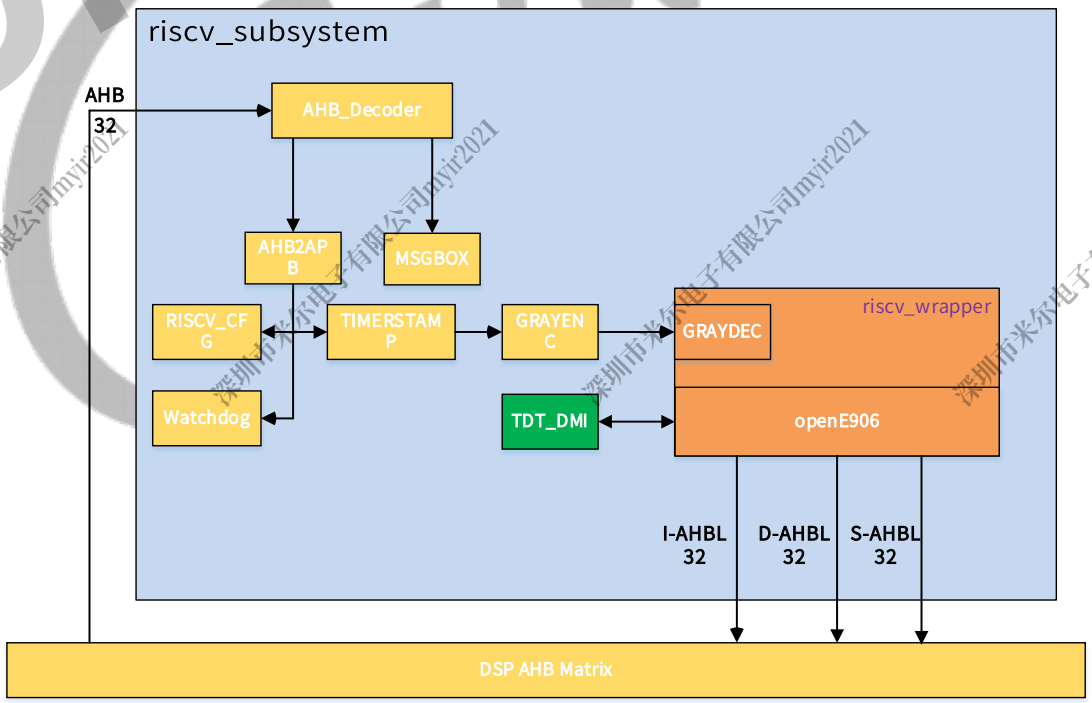
The RISC-V system has the following features:

- Configurable start address via software
- Combined with PPU module, supporting standby in low-power mode and wake-up through external interrupts
- Separate TIMERSTAMP supports timing immediately after reset is released
- Separate watchdog supports to reset the SoC system when the RISC-V system malfunctions
- Separate message box supports communicating with other modules
- Supports separate PMU check module

2.3.2 Block Diagram

The following figure shows the block diagram of RISC-V system.

Figure 2-2 RISC-V System Block Diagram



2.3.3 Register List

Module Name	Base Address
RISCV_CFG	0x0713_0000

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Register Name	Offset	Description
RF1P_CFG_REG	0x0010	RF1P Configuration Register
TS_TMODE_SEL_REG	0x0040	Timestamp Test Mode Selection Register
RISCV_STA_ADD_REG	0x0204	RISC-V Start Address Register
RISCV_WAKEUP_EN_REG	0x0220	RISC-V Wakeup Enable Register
RISCV_WAKEUP_MASK0_REG	0x0224	RISC-V Wakeup Mask0 Register
RISCV_WAKEUP_MASK1_REG	0x0228	RISC-V Wakeup Mask1 Register
RISCV_WAKEUP_MASK2_REG	0x022C	RISC-V Wakeup Mask2 Register
RISCV_WAKEUP_MASK3_REG	0x0230	RISC-V Wakeup Mask3 Register
RISCV_WORK_MODE_REG	0x0248	RISC-V Work Mode Register

2.3.4 Register Description

2.3.4.1 0x0010 RF1P Configuration Register (Default Value: 0x0000_0400)

Offset: 0x0010			Register Name: RF1P_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x400	RF1P_CFG RF1P Configuration

2.3.4.2 0x0040 Timestamp Test Mode Selection Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TS_TMODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	RISCV_TS_TEST_MODE_EN RISCV Timestamp Test Mode Enable 0: Normal Mode 1: Test Mode In Test Mode, this Counter Low/Hi registers will count simultaneously.
0	/	/	/

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2.3.4.3 0x0204 RISCV Start Address Register (Default Value: 0x3FFC_0000)

this register is the running PC address after RISCV releases reset. Before releasing reset, this register should be configured. This register does support dynamic configuration.

Offset: 0x0204			Register Name: RISCV_STA_ADD0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x3FFC0000	STA_ADD Start Address The bit 0 is fixed as 0 and could not be written.

2.3.4.4 0x0220 RISCV Wakeup Enable Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: RISCV_WAKEUP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WP_EN Wakeup Enable To wake up the enable bit of RISC-V, when RISC-V is in low power mode.

2.3.4.5 0x0224 RISCV Wakeup Mask0 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0230 registers corresponds to the wakeup enable bits of 128 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1. For detailed interrupt sources, please refer to section 2.10 Core-Local Interrupt Controller (CLIC)

Offset: 0x0224			Register Name: RISCV_WAKEUP_MASK0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK0 Wakeup Mask0

2.3.4.6 0x0228 RISCV Wakeup Mask1 Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: RISCV_WAKEUP_MASK1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK1 Wakeup Mask1

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2.3.4.7 0x022C RISCV Wakeup Mask2 Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: RISCV_WAKEUP_MASK2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK2 Wakeup Mask2

2.3.4.8 0x00230 RISCV Wakeup Mask3 Register (Default Value: 0x0000_0000)

Offset: 0x00230			Register Name: RISCV_WAKEUP_MASK3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK3 Wakeup Mask3

2.3.4.9 0x0248 RISCV Work Mode Register (Default Value: 0x0000_0003)

Offset: 0x0248			Register Name: RISCV_WORK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	LOCKUP_STA Lockup Status 0: Not Lockup 1: Lockup If CPU has a lockup, CPU will stop accessing data and fetching, and clear the pipeline. Reset processor unit and debug unit to unlock.
2	R	0x0	DM_STA Debug Mode Status 0: Normal Mode 1: Debug Mode
1:0	R	0x3	LP_STA Low Power Status 00: Deep Sleep Low Power Mode 01: Light Sleep Low Power Mode 10: Reserved 11: Normal Mode

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2.4 GPU

The GPU has the following features:

- ARM G57 MC01 GPU
- Supports OpenGL ES 3.2/2.0/1.1, Vulkan1.1/1.2/1.3, and OpenCL2.2
- Output and input format: 8-bit, 10-bit, and 16-bit YUV
- Anti-aliasing algorithm
- High memory bandwidth and low power consumption in 3D graphics processing
- AMBA4 AXI slave interface
- Latency tolerance
- Texture compression
- Configurable power management
- AFBC1.3
- Supports Digital Rights Management (DRM)

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2.5 NPU

The NPU has the following features:

- Up to 2 Tops NPU
- Embedded 512 KB internal buffer
- Supports deep learning frameworks:TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, and so on.
- Primary APIs
  - OpenVX 1.2
  - OpenVX 1.2 neural network extension
  - OpenCL 1.2/1.1
- Additional APIs
  - VivanteVX
  - Vivante extensions for OpenCL 1.2
  - Vivante extensions for OpenVX
  - Vivante extensions for convolutional neural networks
- Enhanced vision instructions: EVIS 1 and EVIS 2 instruction sets
- Drivers
  - OpenVX 1.2
  - OpenCL 1.2 / 1.1
- Primary operating system
  - Android 13.0/10.0 / 9.0 / 8.0 / 7.x / 6.0 / 5.1
- Parallel processing units
  - Programmable Scalable Ultra-threaded execution unit (SIMD4:transcendental,ctl-flow)
  - IEEE 32-bit floating-point pipeline supports long instructions
- Code and data memory location restrictions
  - Unrestricted; arbitrary memory reads and writes

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2.6 BROM System

2.6.1 Overview

The system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) that is considered the primary program-loader. On the startup process, the T527 starts to fetch the first instruction from address 0x0, where is the BROM located at.

The BROM system is divided into two parts: the firmware exchange launch (FEL) module and the Medium Boot module. FEL is responsible for writing the external data to the local NVM, and Medium Boot is responsible for loading an effective and legitimate BOOT0 from NVM and running.

The BROM system includes the following features:

- Supports CPU0 boot process
- Supports mandatory upgrade process through USB and SD card
- Supports GPADC0 pin and eFuse module to select the boot media type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Ensures that the secure boot is in a trusted environment

2.6.2 Functional Description

2.6.2.1 Selecting the Boot Medium

The BROM system supports the following boot media:

- SD Card
- eMMC
- RAW NAND Flash
- SPI NOR Flash (Quad Mode and Single Mode)
- SPI NAND Flash

There are two ways to select the boot medium: GPADC Pin Select and eFuse Select. The BROM will read the state of BOOT_MODE first, and then select the boot medium according to the state of BOOT_MODE. The BOOT_MODE is the BROM_Config in the eFuse mapping.

The following table shows the BOOT_MODE setting:

Table 2-5 BOOT_MODE Setting

BOOT_MODE[0]	Boot Select type
0	GPADC Selection
1	eFuse Selection

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NOTE

The BOOT_MODE BIT is bit [0] of the eFuse register 0x03006210.

GPADC Boot Selection

If the state of the BOOT_MODE is 0, choose the GPADC Boot Selection.

If BROM failed to boot from the selected medium, it will try other media with the following priority:

EMMC_USR -> EMMC_BOOT -> SLC_NAND -> MLC_NAND -> SPI_NOR -> SPI_NAND

And the medium selected by GPADC will be skipped.

For example, when BROM failed to boot from SPI NOR, it will try other media with the following priority:

SPI NOR (selected by GPADC) -> EMMC_USR -> EMMC_BOOT -> SLC_NAND -> MLC_NAND -> SPI_NOR (try at first, skipped) -> SPI_NAND

The following table shows GPADC Boot Select setting.

Table 2-6 GPADC Boot Select Setting

KEY_VALUE	Boot Select type
0x00-0xB6	SD Card->MLC NAND->SLC NAND->try (except SPI in PJ)
0xB7-0x22B	SD Card->SLC NAND->MLC NAND->try (except SPI in PJ)
0x22C-0x3AF	SD Card->EMMC_USER->EMMC_BOOT->try (except SPI in PJ)
0x3B0-0x57B	SD Card->EMMC_BOOT->EMMC_USER->try (except SPI in PJ)
0x57C-0x73C	SD Card->SPI NOR->try (except SPI in PJ)
0x73D-0x8CC	SD Card->SPI NAND->try (except SPI in PJ)
0x8CD-0xB49	SD Card->SPI NOR in PJ->try
0xB4A-0xE7C	SD Card->SPI NAND in PJ->try
0x8CD-0xFFF	Reserved

NOTE

When trying SPI NOR, BROM try 4 wire mode first, then 1 wire mode.

eFuse Boot Selection

If the state of the BOOT_MODE is 1, choose the eFuse Boot Selection.

The eFuse_Boot_Select_Cfg is divided into 3 groups and each group is 3-bit. The following table shows the groups of eFuse_Boot_Select.

Table 2-7 Groups of eFuse_Boot_Select

eFuse_Boot_Select_Cfg [11:0]	Description
eFuse_Boot_Select[3:0]	eFuse_Boot_Select_1

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eFuse_Boot_Select_Cfg [11:0]	Description
eFuse_Boot_Select[7:4]	eFuse_Boot_Select_2
eFuse_Boot_Select[11:8]	eFuse_Boot_Select_3

These three groups take effect with the following priority:

eFuse_Boot_Select_1 -> eFuse_Boot_Select_2 -> eFuse_Boot_Select_3

For example, eFuse_Boot_Select_2 will not take effect unless eFuse_Boot_Select_1 is set as 0b1111(skip), eFuse_Boot_Select_3 will not take effect unless eFuse_Boot_Select_2 is set as 0b1111(skip), etc. If all three groups are set to 0b1111, no other groups can be used for boot select, BROM assume "try" is selected.

In the Try mode, the BROM follows the order below to select the boot medium:

SD Card -> eMMC -> NAND FLASH -> SPI NOR -> SPI NAND

The following table shows the boot medium priority for the different values of eFuse_Boot_Select_n, where n = [4:1].

Table 2-8 eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot media
0000	Try (except SPI in PJ)
0001	SLC NAND -> MLC NAND
0010	EMMC_USER -> EMMC_BOOT
0011	SPI NOR
0100	SPI NAND
0101	MLC NAND -> SLC NAND
0110	MMC_BOOT -> EMMC_USER
1011	SPI NOR in PJ
1100	SPI NAND in PJ
1111	When n is 1 or 2: The boot medium is decided by the value of **eFuse_Boot_Select_(n + 1)**. When n is 4: Select the boot medium in Try mode.

NOTE

The status of the eFuse boot select pin is the bit [11:0] of the eFuse register 0x03006212.

2.6.2.2 Selecting the Boot Mode

For SoCs that have implemented and enabled the ARM TrustZone technology, there are two boot modes: Normal BROM Mode and Secure BROM Mode.

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Secure BROM Mode is designed to protect against attackers modifying the code or data areas in the programmable memory.

During the startup process, the BROM will select the boot mode according to the value of the Secure Enable bit. If the value of Secure Enable bit is 0, the system will boot in Normal BROM Mode. Otherwise, it will boot in Secure BROM Mode.

NOTE

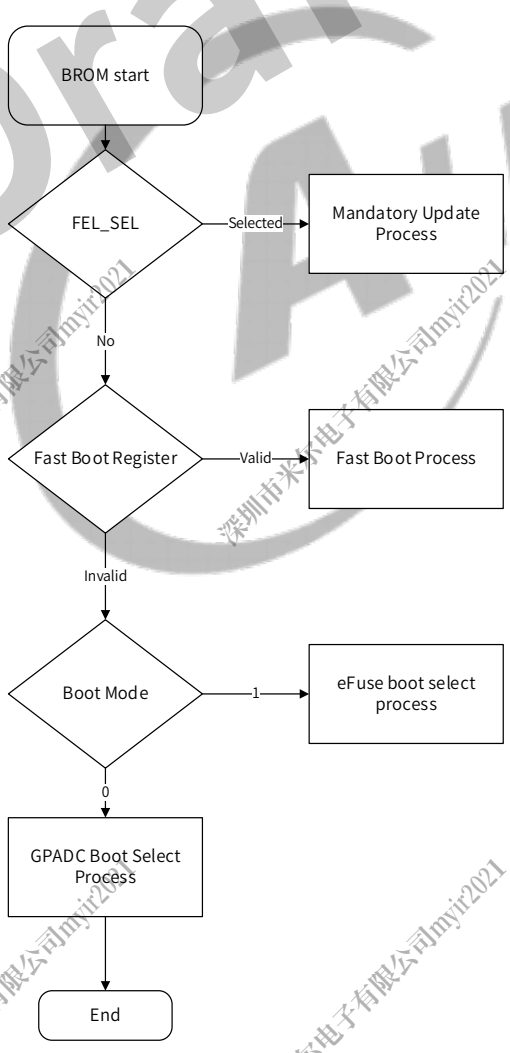
The System on Chip (SoC) supports the ARM TrustZone technology. If the Secure Enable Bit is enabled, the BROM will be safely booted based on this ARM TrustZone technology.

Normal BROM Mode

In Normal BROM Mode, the system boot starts from CPU0, and then the BROM will read the state of the FEL pin. If the FEL pin is high, the system will jump to the fast boot process. If it is low, the system will jump to the mandatory upgrade process.

The following figure shows the boot process in Normal BROM Mode.

Figure 2-3 Boot Process in Normal BROM Mode



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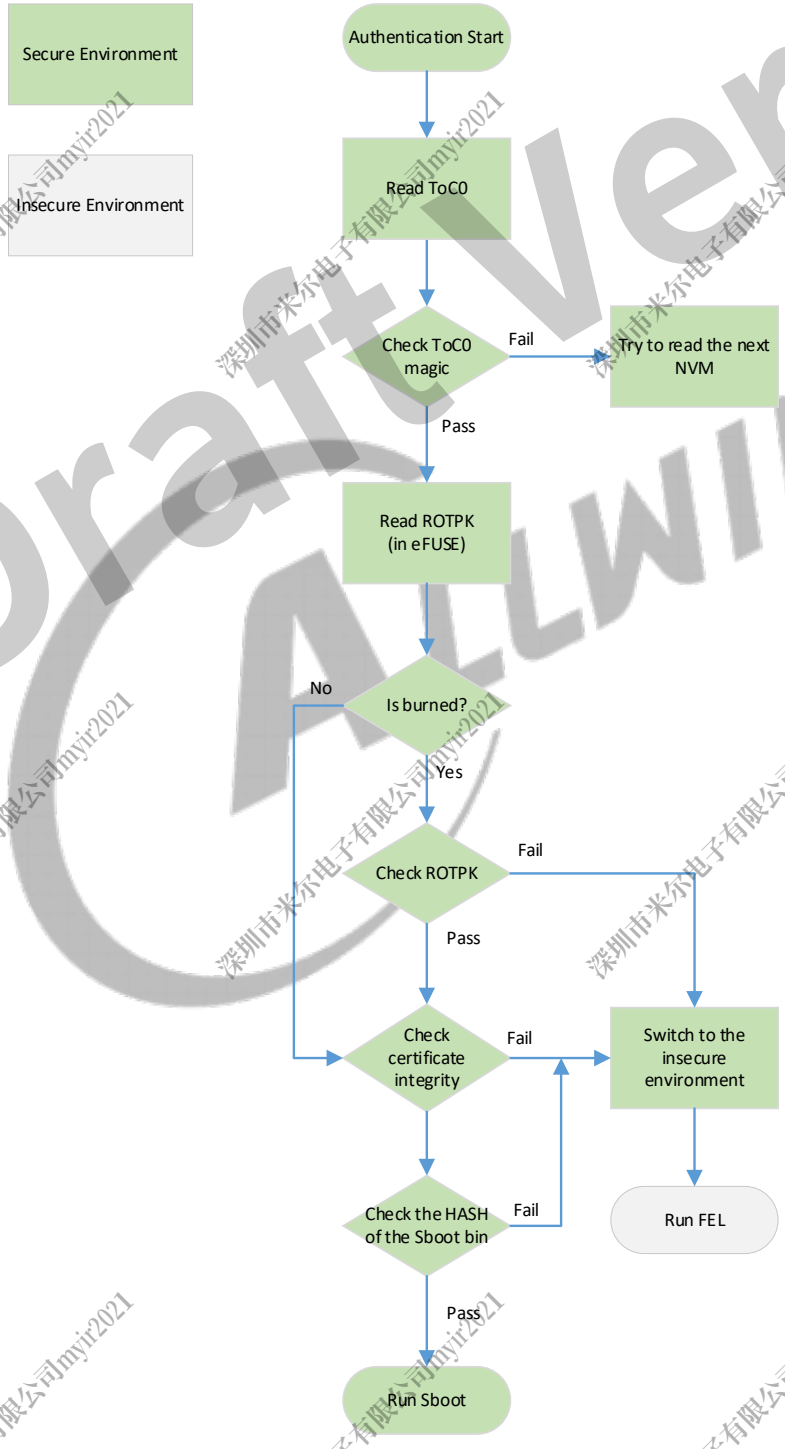
Secure BROM Mode

The process of selecting the boot medium in Secure Boot Mode is the same as that in Normal Boot Mode.

In Secure Boot Mode, after the boot medium is selected, the system additionally runs the Security Boot software to authenticate the Sboot bin file.

The following figure shows the authentication process.

Figure 2-4 Authentication Process in Secure BROM Mode



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Secure BROM Requirements

The Secure Boot has the following some requirement:

- Supports X509 certificate

  The certificate is used to check whether the Security Boot software is modified or replaced. Before running the Security Boot software, the system checks the integrity of the certificate make sure the software has not been modified or replaced.

- Supports cryptographic algorithms
  - AES-128
  - SHA-256
  - RSA-2048
  - AES, DES

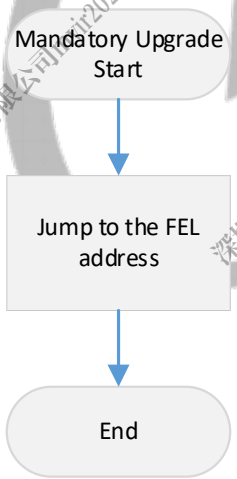
  The system uses the Crypto Engine (CE) hardware module to accelerate the speed of encryption and decryption. The standard cryptography ensures the reliability of the firmware images. The reliable firmware image ensures that the system security state can be as expected.

- Support OTP/eFuse

2.6.2.3 Mandatory Upgrade Process

If the FEL pin is detected to pull low, the system will jump to the mandatory upgrade process. The following figure shows the mandatory upgrade process.

Figure 2-5 Mandatory Upgrade Process



NOTE

The FEL address of the Normal BROM is 0x20.

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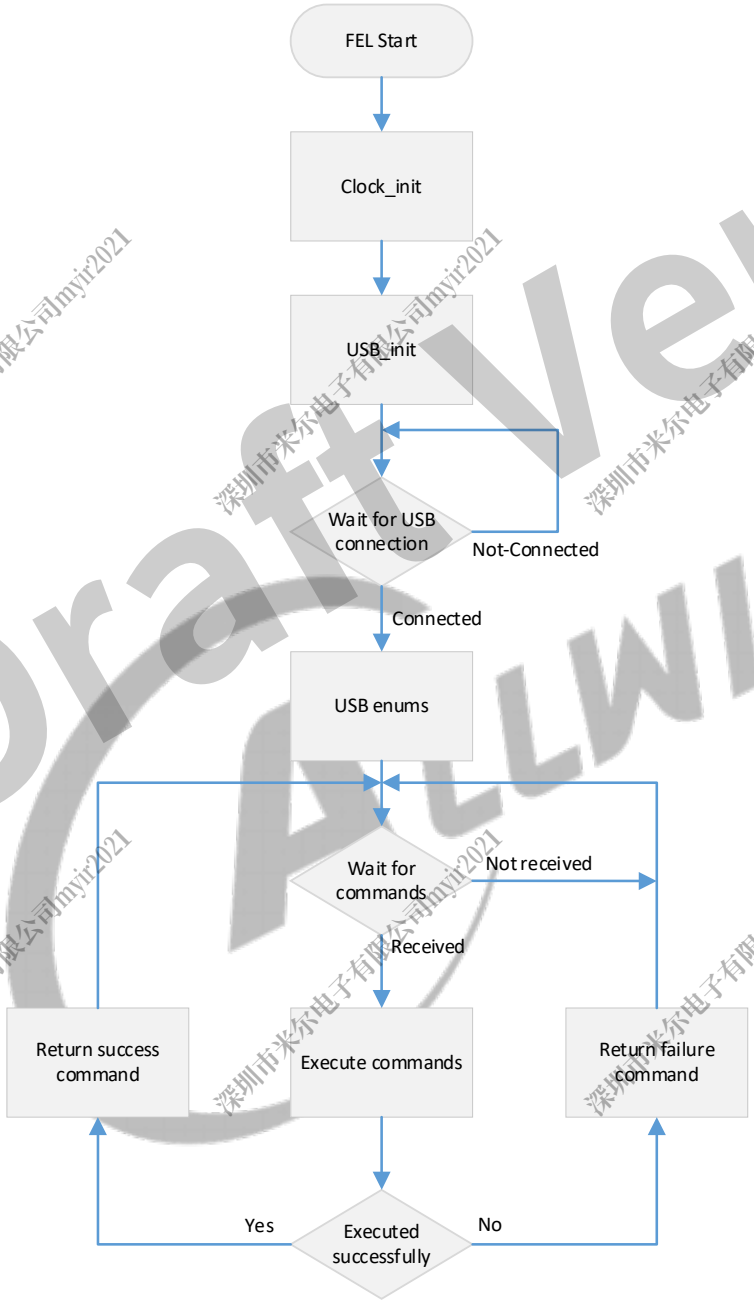
FEL Process

When the system enters mandatory upgrade process, it will jump to the FEL process.

The following figure shows the FEL upgrade process.

Figure 2-6 USB FEL Process



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2.6.2.4 Fast Boot Process

If the value of the Fast Boot register (0x07090120) in RTC module is not zero, the system will enter the fast boot process. The following table shows the boot medium priority for different values of the Fast Boot register.

Table 2-9 Fast Boot Select Setting

Reg_bit[31:28]	Boot Select type
1	SD Card->MLC NAND -> SLC NAND -> TRY
2	SD Card->EMMC_USER -> EMMC_BOOT -> TRY
3	SD Card->SPI NOR(1 wire)-> SPI NOR(4 wire)-> TRY
4	SD Card->SPI NAND -> TRY
5	SD Card->EMMC_BOOT -> EMMC_USER -> TRY
6	SD Card->SLC NAND -> MLC NAND -> TRY
7	Reserved
8	SD Card->SPI NOR(4 wire)-> SPI NOR(1 wire)-> TRY
10	SD Card->SPI NOR(4 wire) in PJ -> TRY
11	SD Card->SPI NAND in PJ-> TRY

NOTE

- The Fast Boot register bit [27:0] is used record the media information.
- Unused value like 7 regarded as “TRY”.

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2.7 Clock Controller Unit (CCU)

2.7.1 Overview

The clock controller unit (CCU) controls the PLL configurations and most of the clock generation, division, distribution, synchronization, and gating. The input signals of the CCU include the external clock for the reference frequency (24 MHz). The outputs from the CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 11 PLLs
- Bus source and divisions
- Clock output control
- Configuring modules clock
- Bus clock gating
- Bus software reset

NOTE

- There are 16 PLLs in T527. 11 PLLs in CCU, 4 PLLs in CPUX system, and 1 PLL in DSP_PRCM.
- CCU describes module clocks in CPUX domain excluding the clock of CPUX system.
- For clock description of CPUX system, please refer to section 2.2.3.2 CPU PLL Distribution and Clock Sources.
- For module clocks in CPUS domain, please refer to section 2.13 Power Reset Clock Management (PRCM).

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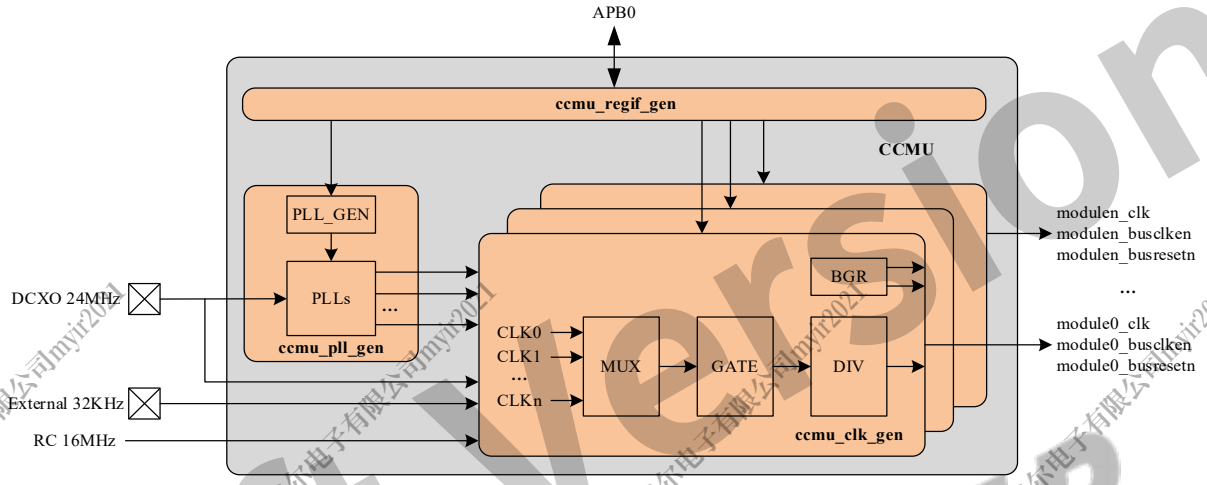
2.7.2 Block Diagram

The following figure shows the functional block diagram of the CCU.

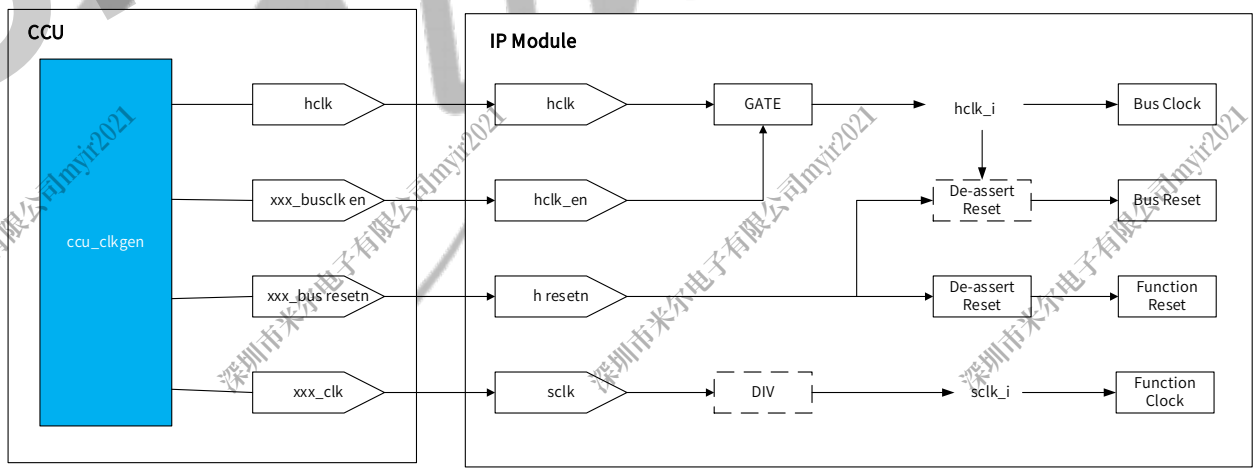
Figure 2-7 CCU Block Diagram



2.7.3 Functional Description

2.7.3.1 Typical Application

Figure 2-8 CCU Typical Application Diagram



CCU outputs bus clock, bus reset, function clock, and function reset to each IP module.

It is needed to enable the bus clock gating signal before using the bus clock. For some subsystems, CCU outputs special bus clock with clock gating added. You also need to enable the bus clock gating signal before using the special bus clock.

The IP reset sources from the synchronous release of the input reset signal. To ensure the synchronous release is implemented in every module, you need to release the reset signal before enabling the clock gating signal of the function clock.

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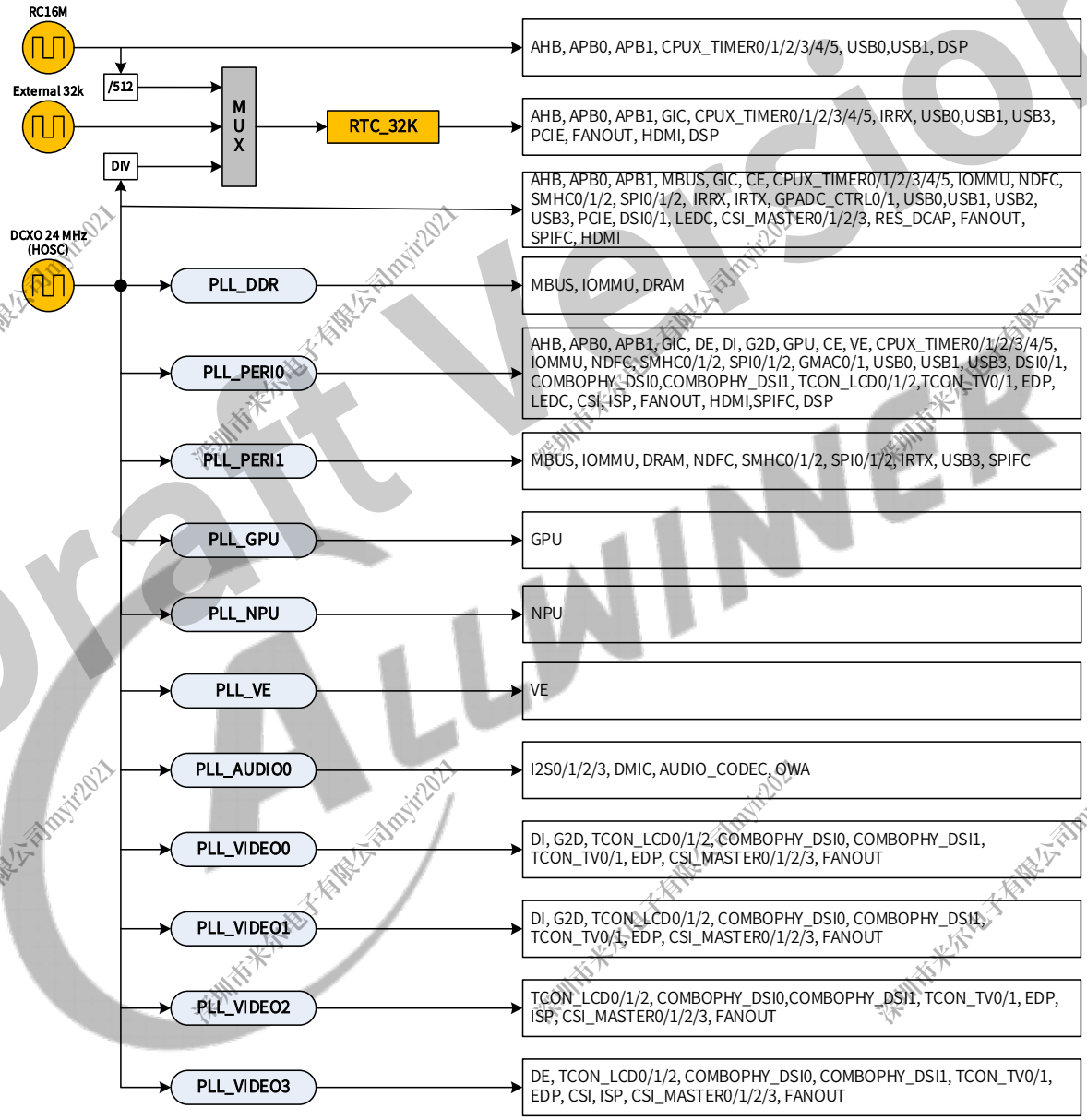
2.7.3.2 PLL Distribution

The following figure shows the block diagram of the PLL distribution.

Figure 2-9 PLL Distribution



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2.7.3.3 PLL Features

The following table shows the PLL features.

Table 2-10 PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Pk-Pk	Lock Time
PLL_DDR	1.26 GHz～2.52 GHz	< 2.5 GHz	Yes	No	< 200ps	500us
PLL_NPU	1.26 GHz～2.52 GHz	< 1.5 GHz	Yes	No	< 200ps	500us
PLL_GPU	1.26 GHz～2.52 GHz	< 1.5 GHz	Yes	No	< 200ps	500us
PLL_PERI0	1.26 GHz～2.52 GHz	2x：1.2 GHz 3x：800 MHz 5x：480 MHz	Yes	No	< 200ps	500us
PLL_PERI1	1.26 GHz～2.52 GHz	2x：1.248 GHz/1.2 GHz 3x：832 MHz/800 MHz 5x：499.2 MHz/480 MHz	Yes	No	< 200ps	500us
PLL_VE	1.26 GHz～2.52 GHz	< 1.5 GHz	Yes	No	< 200ps	500us
PLL_AUDIO0	1.26 GHz～2.52 GHz	1x：22.5792 MHz 4x：22.5792*4 MHz	Yes	No	< 200ps	500us
PLL_VIDEO	1.26 GHz～2.52 GHz	3x:792 MHz 4x:1188 MHz	Yes	No	< 200ps	500us

2.7.4 Programming Guidelines

NOTE

It is not suggested to enable or disable the PLLs frequently during usage. Because the enabling and disabling of PLL will cause a mutual interference between PLLs, which will affect system stability. When the clock is not required, it is recommended to configure the PLL_OUTPUT_GATE bit of PLL control register as 0 instead of writing 0 to the enable bit.

2.7.4.1 Enabling the PLL

Follow the steps below to enable the PLL:

Step 1 Configure the N, M, and P factors of the PLL control register.

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Step 2 Write 1 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register, write 0 to the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register.

Step 3 Write 1 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

Step 4 Wait for the status of the Lock to change to 1.

Step 5 Delay 20 us.

Step 6 Write the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register to 1 and then the PLL will be available.

2.7.4.2 Configuring the Frequency of General PLLs

Step 1 Make sure the PLL is enabled. If not, refer to section 2.7.4.1 Enabling the PLL to enable the PLL.

Step 2 Configure the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register as 0 to disable the output gate of the PLL. Because, general PLLs are unavailable in the process of frequency modulation.

Step 3 Configure the N and M factors. (It is not suggested to configure M1 factor)

Step 4 Write 0 and then write 1 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

Step 5 Wait for the LOCK bit (bit [28]) of the PLL control register to 1.

Step 6 Configure PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register to 1.

2.7.4.3 Configuring the Frequency of PLL_AUDIO0

The frequency configuration formula of PLL_AUDIO0:

PLL_AUDIO0 = 24 MHz*N/M0/M1/P

PLL_AUDIO0 does not support dynamic adjustment because changing any parameter of N, M0, M1, and P will affect the normal work of PLL, and the PLL will need to be relocked.

Generally, PLL_AUDIO0 only needs two frequency points: 24.576*4 MHz or 22.5792*4 MHz. For these two frequencies, there are usually special recommended matching factors. To implement the desired frequency point of PLL_AUDIO0, you need to use the decimal frequency-division function, so follow the steps below:

Step 1 Configure the N, M0, M1 and P factors.

Step 2 Write 1 to the PLL_SDM_EN bit (bit [24]) of PLL_AUDIO0_CTRL register.

Step 3 Configure PLL_AUDIO0_PAT0_CTRL register to enable the digital spread spectrum.

Step 4 Write 0 and then write 1 to the LOCK ENABLE bit (bit [29]) of PLL_AUDIO0_CTRL register.

Step 5 Write 1 to the LOCK bit (bit [28]) of PLL_AUDIO0_CTRL register.

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NOTE

- When the P factor of PLL_AUDIO0 is an odd number, the clock output is an unequal-duty-cycle signal.
- T527 includes PLL_AUDIO0 and PLL_AUDIO1. For detailed description of PLL_AUDIO1, please refer to section 2.13 Power Reset Clock Management (PRCM).

2.7.4.4 Disabling the PLL

Follow the steps below to disable the PLL:

Step 1 Write 0 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register.

Step 2 Write 0 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

2.7.4.5 Implementing Spread Spectrum

The spread spectrum technology is to convert a narrowband signal into a wideband signal. It helps to reduce the effect of electromagnetic interference (EMI) associated with the fundamental frequency of the signal.

For the general PLL frequency, the calculation formula is as follows:

$$f = \frac{N+1+X}{P\cdot(M0+1)\cdot(M1+1)}\cdot 24MHz,\ 0<X<1$$

Where,

P is the frequency division factor of module or PLL;

M0 is the post-frequency division factor of PLL;

M1 is the pre-frequency division factor of PLL;

N is the frequency doubling factor of PLL;

X is the amplitude coefficient of the spread spectrum.

The parameters N, P, M1, and M0 are for the frequency division.

When M1 = 0, M0 = 0, and P = 1 (no frequency division), the calculation formula of PLL frequency can be simplified as follows:

$$f = (N+1+X)\cdot 24MHz,\ 0<X<1$$

$$[f_1, f_2] = (N+1+[X_1, X_2])\cdot 24MHz$$

$$SDM_BOT = 2^{17}\cdot X_1$$

$$\text{WAVE_STEP} = 2^{17}\cdot(X_2 - X_1)/(24\ \text{MHz}/PREQ)\cdot 2$$

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Where, SDM_BOT and WAVE_STEP are bits of the PLL pattern control register, and PREQ is the frequency of the spread spectrum.

NOTE

Different PLLs have different calculate formulas, refer to the CTRL register of the corresponding PLL in section 2.7.6 Register Description.

Follow the steps below to implement the spread spectrum:

Step 1 Configure the control register of the corresponding PLL

a) Calculate the factor N and decimal value X according to the PLL frequency and PLL frequency formula. Refer to the control register of the corresponding PLL (named PLL_xxx_CTRL_REG, where xxx is the module name) in 2.7.6 Register Description for the corresponding PLL frequency formula.

b) Write M0, M1, N, and PLL frequency to the PLL control register.

c) Configure the PLL_SDM_EN bit (bit [24]) of the PLL control register to 1 to enable the spread spectrum function.

Step 2 Configure the pattern control register of the corresponding PLL

a) Calculate the SDM_BOT and WAVE_STEP of the pattern control register according to decimal value X and spread spectrum frequency (the bit [18:17] of the PLL pattern register)

b) Configure the spread spectrum mode (SPR_FREQ_MODE) to 2 or 3.

c) If the PLL_INPUT_DIV2 of the PLL control register is 1, configure the spread spectrum clock source select bit (SDM_CLK_SEL) of the PLL pattern control register to 1. Otherwise, configure SDM_CLK_SEL to the default value 0.

d) Write SDM_BOT, WAVE_STEP, PREQ, SPR_FREQ_MODE, and SDM_CLK_SEL to the PLL pattern control register, and configure the SIG_DELT_PAT_EN bit (bit [31]) of this register to 1.

Step 3 Delay 20 us

2.7.4.6 Configuring Bus Clock

The bus clock supports dynamic switching, but the process of switching needs to follow the following two rules.

- From a higher frequency to a lower frequency: switch the clock source first, and then set the frequency division factor;
- From a lower frequency to a higher frequency: configure the frequency division factor first, and then switch the clock source.

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The bus frequency for each bus is as follows:

- AXI: It is suggested to be configured as the CPU clock frequency divided by 3. when the CPU clock frequency is less than 1.2 GHz, AXI frequency could be configured as the CPU clock frequency divided by 2.
- AHB: Maximum 200 MHz
- APB0: Maximum 100 MHz
- APB1: Maximum 160 MHz
- MBUS: Maximum 700 MHz
- IOMMU: Maximum 600 MHz

2.7.4.7 Configuring Module Clock

For the Bus Gating Reset register of a module, the reset bit is de-asserted first, and then the clock gating bit is enabled to avoid potential problems caused by the asynchronous release of the reset signal.

For all module clocks except the DDR clock, configure the clock source and frequency division factor first, and then release the clock gating (that is, set to 1). For the configuration order of the clock source and frequency division factor, follow the rules below:

- With the increasing of the clock source frequency, configure the frequency division factor before the clock source;
- With the decreasing of the clock source frequency, configure the clock source before the frequency division factor.

2.7.5 Register List

NOTE

- Before switching the glitch-free MUX, ensure that
  - Every clock source is in use.
  - The switching time is longer than two clock periods of the slowest clock source.
- Before switching the normal MUX, ensure that the clock sources are closed.

Module Name	Base Address
CCU	0x0200 1000

Register Name	Offset	Description
PLL_DDR_CTRL_REG	0x0010	PLL_DDR Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register

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Register Name	Offset	Description
PLL_PERI1_CTRL_REG	0x0028	PLL_PERI1 Control Register
PLL_GPU_CTRL_REG	0x0030	PLL_GPU Control Register
PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_VIDEO1_CTRL_REG	0x0048	PLL_VIDEO1 Control Register
PLL_VIDEO2_CTRL_REG	0x0050	PLL_VIDEO2 Control Register
PLL_VE_CTRL_REG	0x0058	PLL_VE Control Register
PLL_VIDEO3_CTRL_REG	0x0068	PLL_VIDEO3 Control Register
PLL_AUDIO0_CTRL_REG	0x0078	PLL_AUDIO0 Control Register
PLL_NPU_CTRL_REG	0x0080	PLL_NPU Control Register
PLL_DDR_PAT0_CTRL_REG	0x0110	PLL_DDR Pattern0 Control Register
PLL_DDR_PAT1_CTRL_REG	0x0114	PLL_DDR Pattern1 Control Register
PLL_PERI0_PAT0_CTRL_REG	0x0120	PLL_PERI0 Pattern0 Control Register
PLL_PERI0_PAT1_CTRL_REG	0x0124	PLL_PERI0 Pattern1 Control Register
PLL_PERI1_PAT0_CTRL_REG	0x0128	PLL_PERI1 Pattern0 Control Register
PLL_PERI1_PAT1_CTRL_REG	0x012C	PLL_PERI1 Pattern1 Control Register
PLL_GPU_PAT0_CTRL_REG	0x0130	PLL_GPU Pattern0 Control Register
PLL_GPU_PAT1_CTRL_REG	0x0134	PLL_GPU Pattern1 Control Register
PLL_VIDEO0_PAT0_CTRL_REG	0x0140	PLL_VIDEO0 Pattern0 Control Register
PLL_VIDEO0_PAT1_CTRL_REG	0x0144	PLL_VIDEO0 Pattern1 Control Register
PLL_VIDEO1_PAT0_CTRL_REG	0x0148	PLL_VIDEO1 Pattern0 Control Register
PLL_VIDEO1_PAT1_CTRL_REG	0x014C	PLL_VIDEO1 Pattern1 Control Register
PLL_VIDEO2_PAT0_CTRL_REG	0x0150	PLL_VIDEO2 Pattern0 Control Register
PLL_VIDEO2_PAT1_CTRL_REG	0x0154	PLL_VIDEO2 Pattern1 Control Register
PLL_VE_PAT0_CTRL_REG	0x0158	PLL_VE Pattern0 Control Register
PLL_VE_PAT1_CTRL_REG	0x015C	PLL_VE Pattern1 Control Register
PLL_VIDEO3_PAT0_CTRL_REG	0x0168	PLL_VIDEO3 Pattern0 Control Register
PLL_VIDEO3_PAT1_CTRL_REG	0x016C	PLL_VIDEO3 Pattern1 Control Register
PLL_AUDIO0_PAT0_CTRL_REG	0x0178	PLL_AUDIO0 Pattern0 Control Register
PLL_AUDIO0_PAT1_CTRL_REG	0x017C	PLL_AUDIO0 Pattern1 Control Register
PLL_NPU_PAT0_CTRL_REG	0x0180	PLL_NPU Pattern0 Control Register
PLL_NPU_PAT1_CTRL_REG	0x0184	PLL_NPU Pattern1 Control Register
PLL_DDR_BIAS_REG	0x0310	PLL_DDR Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_PERI1_BIAS_REG	0x0328	PLL_PERI1 Bias Register
PLL_GPU_BIAS_REG	0x0330	PLL_GPU Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_VIDEO1_BIAS_REG	0x0348	PLL_VIDEO1 Bias Register
PLL_VIDEO2_BIAS_REG	0x0350	PLL_VIDEO2 Bias Register
PLL_VE_BIAS_REG	0x0358	PLL_VE Bias Register
PLL_VIDEO3_BIAS_REG	0x0368	PLL_VIDEO3 Bias Register
PLL_AUDIO0_BIAS_REG	0x0378	PLL_AUDIO0 Bias Register
PLL_NPU_BIAS_REG	0x0380	PLL_NPU Bias Register

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Register Name	Offset	Description
AHB_CLK_REG	0x0510	AHB Clock Register
APB0_CLK_REG	0x0520	APB0 Clock Register
APB1_CLK_REG	0x0524	APB1 Clock Register
MBUS_CLK_REG	0x0540	MBUS Clock Register
NSI_BGR_REG	0x054C	NSI Bus Gating Reset Register
GIC_CLK_REG	0x0550	GIC Clock Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
DI_CLK_REG	0x0620	DI Clock Register
DI_BGR_REG	0x062C	DI Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
DE_SYS_BGR_REG	0x064C	DE_SYS Bus Gating Reset Register
GPU_CLK_REG	0x0670	GPU Clock Register
GPU_GATING_REG	0x067C	GPU Gating Reset Configuration Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
NPU_CLK_REG	0x06E0	NPU Clock Register
DMAC_BGR_REG	0x070C	DMAC Bus Gating Reset Register
CPUX_MSGBOX_BGR_REG	0x071C	CPUX_MSGBOX Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	SPINLOCK Bus Gating Reset Register
CPUX_TIMER0_CLK_REG	0x0730	CPUX_TIMER0 Clock Register
CPUX_TIMER1_CLK_REG	0x0734	CPUX_TIMER1 Clock Register
CPUX_TIMER2_CLK_REG	0x0738	CPUX_TIMER2 Clock Register
CPUX_TIMER3_CLK_REG	0x073C	CPUX_TIMER3 Clock Register
CPUX_TIMER4_CLK_REG	0x0740	CPUX_TIMER4 Clock Register
CPUX_TIMER5_CLK_REG	0x0744	CPUX_TIMER5 Clock Register
CPUX_TIMER_BGR_REG	0x074C	CPUX_TIMER Bus Gating Reset Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PWMCTRL_BGR_REG	0x07AC	PWMCTRL Bus Gating Reset Register
IOMMU_CLK_REG	0x07B0	IOMMU Clock Register
IOMMU_BGR_REG	0x07BC	IOMMU Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MAT_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
NDFC_CLK0_CLK_REG	0x0810	NDFC CLK0 Clock Register
NDFC_CLK1_CLK_REG	0x0814	NDFC CLK1 Clock Register
NDFC_BGR_REG	0x082C	NDFC Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register

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Register Name	Offset	Description
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
SYSDAP_BGR_REG	0x088C	SYSDAP Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPIFC_CLK_REG	0x0950	SPIFC Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
GMAC0 _25M_CLK_REG	0x0970	GMAC0_25M Clock Register
GMAC1 _25M_CLK_REG	0x0974	GMAC1_25M Clock Register
GMAC0_BGR_REG	0x097C	GMAC0 Bus Gating Reset Register
GMAC1_BGR_REG	0x098C	GMAC1 Bus Gating Reset Register
IRRX_CLK_REG	0x0990	IRRX Clock Register
IRRX_BGR_REG	0x099C	IRRX Bus Gating Reset Register
IRTX_CLK_REG	0x09C0	IRTX Clock Register
IRTX_BGR_REG	0x09CC	IRTX Bus Gating Reset Register
GPADC_CTRL0_24M_CLK_REG	0x09E0	GPADC_CTRL0_24M Clock Register
GPADC_CTRL1_24M_CLK_REG	0x09E4	GPADC_CTRL1_24M Clock Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
USB0_CLK_REG	0x0A70	USB0 Clock Register
USB1_CLK_REG	0x0A74	USB1 Clock Register
USB2_REF_CLK_REG	0x0A80	USB2_REF Clock Register
USB3_PCIE_REF_CLK_REG	0x0A84	USB3_PCIE Reference Clock Register
USB3_SUSPEND_CLK_REG	0x0A88	USB3_SUSPEND Clock Register
USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
LRADC_BGR_REG	0x0A9C	LRADC Bus Gating Reset Register
PCIE_AUX_CLK_REG	0x0AA0	PCIE_AUX Clock Register
PCIE_BGR_REG	0x0AAC	PCIE Bus Gating Reset Register
DISPLAY0_TOP_BGR_REG	0x0ABC	DISPLAY0_TOP Bus Gating Reset Register
DISPLAY1_TOP_BGR_REG	0x0ACC	DISPLAY1_TOP Bus Gating Reset Register
HDMI_24M_CLK_REG	0x0B04	HDMI_24M Clock Register
HDMI_CEC_CLK_REG	0x0B10	HDMI CEC Clock Register
HDMI_BGR_REG	0x0B1C	HDMI Bus Gating Reset Register
DSI0_CLK_REG	0x0B24	DSI0 Clock Register
DSI1_CLK_REG	0x0B28	DSI1 Clock Register
DSI_BGR_REG	0x0B4C	DSI Bus Gating Reset Register
TCONLCD0_CLK_REG	0x0B60	TCONLCD0 Clock Register
TCONLCD1_CLK_REG	0x0B64	TCONLCD1 Clock Register
TCONLCD2_CLK_REG	0x0B68	TCONLCD2 Clock Register

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Register Name	Offset	Description
COMBOPHY_DSI0_CLK_REG	0x0B6C	COMBOPHY_DSI0 Clock Register
COMBOPHY_DSI1_CLK_REG	0x0B70	COMBOPHY_DSI1 Clock Register
TCONLCD_BGR_REG	0x0B7C	TCONLCD Bus Gating Reset Register
TCONTV0_CLK_REG	0x0B80	TCONTV0 Clock Register
TCONTV1_CLK_REG	0x0B84	TCONTV1 Clock Register
TCONTV_BGR_REG	0x0B9C	TCONTV Bus Gating Reset Register
LVDS_BGR_REG	0x0BAC	LVDS Bus Gating Reset Register
EDP_CLK_REG	0x0BB0	EDP Clock Register
EDP_BGR_REG	0x0BBC	EDP Bus Gating Reset Register
VIDEO_OUT_BGR_REG	0x0BCC	Video out Bus Gating Reset Register
LEDC_CLK_REG	0x0BF0	LEDC Clock Register
LEDC_BGR_REG	0x0BFC	LEDC Bus Gating Reset Register
CSI_CLK_REG	0x0C04	CSI Clock Register
CSI_MASTER0_CLK_REG	0x0C08	CSI Master0 Clock Register
CSI_MASTER1_CLK_REG	0x0C0C	CSI Master1 Clock Register
CSI_MASTER2_CLK_REG	0x0C10	CSI Master2 Clock Register
CSI_MASTER3_CLK_REG	0x0C14	CSI Master3 Clock Register
CSI_BGR_REG	0x0C1C	CSI Bus Gating Reset Register
ISP_CLK_REG	0x0C20	ISP Clock Register
DSP_CLK_REG	0x0C70	DSP Clock Register
AHB_GATE_EN_REG	0x0E04	AHB Gate Enable Register
PERI0PLL_GATE_EN_REG	0x0E08	PERI0PLL Gate Enable Register
CLK24M_GATE_EN_REG	0x0E0C	CLK24M Gate Enable Register
PERI1PLL_GATE_EN_REG	0x0E10	PERI1PLL Gate Enable Register
VIDEOPLL_GATE_EN_REG	0x0E14	VIDEOPLL Gate Enable Register
CM_GPU_CFG_REG	0x0E20	CM GPU Enable Configuration Register
CM_VE_CFG_REG	0x0E24	CM VE Enable Configuration Register
CM_DE_CFG_REG	0x0E28	CM DE Enable Configuration Register
CM_VI_CFG_REG	0x0E2C	CM VI Enable Configuration Register
CM_VO0_CFG_REG	0x0E30	CM VO0 Enable Configuration Register
CM_VO1_CFG_REG	0x0E34	CM VO1 Enable Configuration Register
CM_NDFC_CFG_REG	0x0E38	CM NDFC Enable Configuration Register
CM_PCIE_CFG_REG	0x0E3C	CM PCIE Enable Configuration Register
CCU_SEC_SWITCH_REG	0x0F00	CCU Security Switch Register
SYSDAP_REQ_CTRL_REG	0x0F08	SYSDAP REQ Control Register
CCU_FAN_GATE_REG	0x0F30	CCU FANOUT CLOCK GATE Register
CLK27M_FAN_REG	0x0F34	CLK27M FANOUT Register
CLK_FAN_REG	0x0F38	CLK FANOUT Register
CCU_FAN_REG	0x0F3C	CCU FANOUT Register
PLL_CFG0_REG	0x0F40	PLL Configuration0 Register
PLL_CFG1_REG	0x0F44	PLL Configuration1 Register
PLL_CFG2_REG	0x0F48	PLL Configuration2 Register

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2.7.6 Register Description

2.7.6.1 0x0010 PLL_DDR Control Register (Default Value: 0x4800_2301)

Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The DDRPLL= InputFreq*N/M1/M0 The default value of PLL_DDR is 432 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1:Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.

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Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

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2.7.6.2 0x0020 PLL_PERI0 Control Register (Default Value: 0x4821_6310)

Offset: 0x0020			Register Name: PLL_PERI0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable PERI0PLL2X = 24MHz*N/M1/P0 PERI0_800M = 24MHz*N/M1/P1 PERI0_480M = 24MHz*N/M1/P2 PERI0_600M = PERI0PLL2X/2 PERI0_400M = PERI0PLL2X/3 PERI0_300M = PERI0_600M/2 PERI0_200M = PERI0_400M/2 PERI0_160M = PERI0_480M/3 PERI0_150M = PERI0_300M/2 When the crystal oscillator is 24 MHz, the default frequency of PERI0PLL2X is 1.2 GHz, the default frequency of PERI0_800M is 800 MHz, and the default frequency of PERI0_480M is 480 MHz. The output clock of PERI0PLL2X is fixed to 1.2 GHz and is not suggested to change the parameter.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/

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Offset: 0x0020			Register Name: PLL_PERI0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x2	PLL_P1 PLL Output Div P1 P1=PLL_P1 + 1 PLL_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0 PLL Output Div P0 P0=PLL_P0 + 1 PLL_P0 is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_P2 PLL Output Div P2 P2=PLL_P2 + 1 PLL_P2 is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	/	/	/

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2.7.6.3 0x0028 PLL_PERI1 Control Register (Default Value: 0x4821_6310)

Offset: 0x0028			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable PERI1PLL2X = 24MHz*N/M1/P0 PERI1_800M = 24MHz*N/M1/P1 PERI1_480M = 24MHz*N/M1/P2 PERI1_600M = PERI1PLL2X/2 PERI1_400M = PERI1PLL2X/3 PERI1_300M = PERI1_600M/2 PERI1_200M = PERI1_400M/2 PERI1_160M = PERI1_480M/3 PERI1_150M = PERI1_300M/2 When the crystal oscillator is 24 MHz, the default frequency of PERI1PLL2X is 1.2 GHz, the default frequency of PERI1_800M is 800 MHz, and the default frequency of PERI1_480M is 480 MHz. The output clock of PERI1PLL2X is fixed to 1.2 GHz and not suggested to change the parameter.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/

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Offset: 0x0028			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x2	PLL_P1 PLL Output Div P1 P1=PLL_P1 + 1 PLL_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0 PLL Output Div P0 P0=PLL_P0 + 1 PLL_P0 is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_P2 PLL Output Div P2 P2=PLL_P2 + 1 PLL_P2 is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	/	/	/

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2.7.6.4 0x0030 PLL_GPU Control Register (Default Value: 0x4800_2301)

Offset: 0x0030			Register Name: PLL_GPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL_GPU = InputFreq*N/M1/M0 The default value of PLL_GPU is 432 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable. 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL Factor N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.

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Offset: 0x0030			Register Name: PLL_GPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1

2.7.6.5 0x0040 PLL_VIDEO0 Control Register (Default Value: 0x4800_6201)

Offset: 0x0040			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable For application, VIDEO0PLL4X = InputFreq *N/M1/M0 VIDEO0PLL3X = InputFreq *N/M1/3 The default value of VIDEO0PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable

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Offset: 0x0040			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.

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Offset: 0x0040			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.7.6.6 0x0048 PLL_VIDEO1 Control Register (Default Value: 0x4800_6201)

Offset: 0x0048			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable For application, VIDEO1PLL4X = InputFreq *N/M1/M0 VIDEO1PLL3X = InputFreq *N/M1/3 The default value of VIDEO1PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/

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Offset: 0x0048			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

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2.7.6.7 0x0050 PLL_VIDEO2 Control Register (Default Value: 0x4800_6201)

Offset: 0x0050			Register Name: PLL_VIDEO2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable For application, VIDEO2PLL4X = InputFreq *N/M1/M0. VIDEO2PLL3X = InputFreq *N/M1/3. The default value of VIDEO2PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.

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Offset: 0x0050			Register Name: PLL_VIDEO2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.7.6.8 0x0058 PLL_VE Control Register (Default Value: 0x4800_2301)

Offset: 0x0058			Register Name: PLL_VE_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL_VE = InputFreq*N/M1/M0 The default value of PLL_VE is 432 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

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Offset: 0x0058			Register Name: PLL_VE_CTRL_REG
Bit	Read/Write	Default/Hex	Description
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

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2.7.6.9 0x0068 PLL_VIDEO3 Control Register (Default Value: 0x4800_6201)

Offset: 0x0068			Register Name: PLL_VIDEO3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable For application, VIDEO3PLL4X = InputFreq *N/M1/M0 VIDEO3PLL3X = InputFreq *N/M1/3 The default value of VIDEO3PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.

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Offset: 0x0068			Register Name: PLL_VIDEO3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.7.6.10 0x0078 PLL_AUDIO0 Control Register (Default Value: 0x4814_5500)

Offset: 0x0078			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable AUDIO0PLL4X = 24MHz*N/M1/M0/P AUDIO0PLL2X = 24MHz*N/M1/M0/P/2 AUDIO0PLL1X = 24MHz*N/M1/M0/P/4 7.5≤N/M0/M1≤125 and 12≤N The working frequency range of 24MHz*N/M0/M1 is from 180 MHz to 3.0 GHz. The default frequency of PLL_AUDIO0PLL1X is 24.5714 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable

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Offset: 0x0078			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) The bit is only valid when the bit29 is set to 1.
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23:22	/	/	/
21:16	R/W	0x14	PLL_P PLL Post Div P P= PLL_POST_DIV_P +1 PLL_POST_DIV_P is from 0 to 63.
15:8	R/W	0x55	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/

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Offset: 0x0078			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.7.6.11 0x0080 PLL_NPU Control Register (Default Value: 0x4800_2903)

Offset: 0x0080			Register Name: PLL_NPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The NPUPLL4X = 24MHz*N/M1 The NPUPLL2X = 24MHz*N/M1/2 The NPUPLL1X = 24MHz*N/M1/4 The working frequency for NPUPLL4X is from 180 MHz to 3.0 GHz and the default value of NPUPLL4X is 504 MHz.
30	R/W	0x1	PLL_LDO_EN LDO enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0:Disable 1:Enable The bit is used to control the output enable of the PLL.

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Offset: 0x0080			Register Name: PLL_NPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x29	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div D D=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1 (This factor is only for test) For test, NPUPLL4X = 24MHz*N/M/D

2.7.6.12 0x0110 PLL_DDR Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable

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Offset: 0x0110			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.13 0x0114 PLL_DDR Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

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2.7.6.14 0x0120 PLL_PERI0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PLL_PERI0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom.

2.7.6.15 0x0124 PLL_PERI0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/

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Offset: 0x0124			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.16 0x0128 PLL_PERI1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PLL_PERI1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.17 0x012C PLL_PERI1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable

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Offset: 0x012C			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.18 0x0130 PLL_GPU Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PLL_GPU_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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2.7.6.19 0x0134 PLL_GPU Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: PLL_GPU_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.20 0x0140 PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz

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Offset: 0x0140			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.21 0x0144 PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.22 0x0148 PLL_VIDEO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_VIDEO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.

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Offset: 0x0148			Register Name: PLL_VIDEO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom.

2.7.6.23 0x014C PLL_VIDEO1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PLL_VIDEO1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.24 0x0150 PLL_VIDEO2 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PLL_VIDEO2_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step

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Offset: 0x0150			Register Name: PLL_VIDEO2_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.25 0x0154 PLL_VIDEO2 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: PLL_VIDEO2_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.26 0x0158 PLL_VE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PLL_VE_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable

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Offset: 0x0158			Register Name: PLL_VE_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.27 0x015C PLL_VE Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PLL_VE_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

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2.7.6.28 0x0168 PLL_VIDEO3 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PLL_VIDEO3_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.29 0x016C PLL_VIDEO3 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: PLL_VIDEO3_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/

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Offset: 0x016C			Register Name: PLL_VIDEO3_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.30 0x0178 PLL_AUDIO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, this bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.7.6.31 0x017C PLL_AUDIO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PLL_AUDIO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable

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Offset: 0x017C			Register Name: PLL_AUDIO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.32 0x0180 PLL_NPU Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PLL_NPU_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz When the PLL_INPUT_DIV_M1 is 1, this bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency. 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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2.7.6.33 0x0184 PLL_NPU Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: PLL_NPU_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.7.6.34 0x0310 PLL_DDR Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.35 0x0320 PLL_PERI0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.36 0x0328 PLL_PERI1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0328			Register Name: PLL_PERI1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

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2.7.6.37 0x0330 PLL_GPU Bias Register (Default Value: 0x0003_0000)

Offset: 0x0330			Register Name: PLL_GPU_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.38 0x0340 PLL_VIDEO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.39 0x0348 PLL_VIDEO1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0348			Register Name: PLL_VIDEO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL Bias Control
15:0	/	/	/

2.7.6.40 0x0350 PLL_VIDEO2 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0350			Register Name: PLL_VIDEO2_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL Bias Control
15:0	/	/	/

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2.7.6.41 0x0358 PLL_VE Bias Register (Default Value: 0x0003_0000)

Offset: 0x0358			Register Name: PLL_VE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.42 0x0368 PLL_VIDEO3 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0368			Register Name: PLL_VIDEO3_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.43 0x0378 PLL_AUDIO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.7.6.44 0x0380 PLL_NPU Bias Register (Default Value: 0x0003_0000)

Offset: 0x0380			Register Name: PLL_NPU_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

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2.7.6.45 0x0510 AHB Clock Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: AHB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI0_600M_BUS The clock MUX supports glitch-free switch and dynamic configuration. AHB_CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31 The clock DIV supports glitch-free switch and dynamic configuration.

2.7.6.46 0x0520 APB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI0_600M_BUS The clock MUX supports glitch-free switch and dynamic configuration. APB0_CLK = Clock Source/M
23:5	/	/	/

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Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.7.6.47 0x0524 APB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: APB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK32K 010: CLK16M_RC 011: PERI0_600M_BUS 100: PERI0_480M_BUS The clock MUX supports glitch-free switch and dynamic configuration. APB1_CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

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2.7.6.48 0x0540 MBUS Clock Register (Default Value: 0xC000_0000)

Offset: 0x0540			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MBUS_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS CLK = Clock Source/M
30	R/W	0x1	MBUS_RST MBUS Reset 0: Assert 1: De-assert
29	/	/	/
28	R/W	0x0	MBUS_DFS_EN MBUS Clock Dynamic Frequency Scaling Enable 0: Disable 1: Enable
27	R/WAC	0x0	MBUS_UPD MBUS Clock Configuration 0 update 0: Invalid 1: Valid Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This register supports DRAM REQ/ACK signal. When MBUS_UPD is set to 1, MBUS_CLK_SEL and MBUS_CLK1 will be updated.
26:24	R/W	0x0	MBUS_CLK_SEL Clock Source Select 000: DDRPLL 001: PERI1_600M 010: PERI1_480M 011: PERI1_400M 100: PERI1_150M 101: HOSC The clock MUX supports glitch-free switch and dynamic configuration.
23:5	/	/	/

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Offset: 0x0540			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	MBUS_DIV1 Factor M M= MBUS_DIV1 + 1 FACTOR M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.7.6.49 0x054C NSI Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x054C			Register Name: NSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	NSI_RST NSI Reset 0: Assert 1: De-assert
15:0	/	/	/

2.7.6.50 0x0550 GIC Clock Register (Default Value: 0x8000_0000)

Offset: 0x0550			Register Name: GIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	GIC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GIC_CLK = Clock Source/M
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK32K 010: PERI0_600M 011: PERI0_480M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.7.6.51 0x0600 DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DE_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DE_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO3PLL4X 011: VIDEO3PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.52 0x060C DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DE_RST DE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE_GATING Gating Clock for DE 0: Mask 1: Pass

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2.7.6.53 0x0620 DI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0620			Register Name: DI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DI_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DI_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO0PLL4X 011: VIDEO1PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.54 0x062C DI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x062C			Register Name: DI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DI_RST DI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DI_GATING Gating Clock for DI 0: Mask 1: Pass

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2.7.6.55 0x0630 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	G2D_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON G2D_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_400M 001: PERI0_300M 010: VIDEO0PLL4X 011: VIDEO1PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.56 0x063C G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	G2D_RST G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING Gating Clock for G2D 0: Mask 1: Pass

2.7.6.57 0x064C DE_SYS Bus Gating Reset Register (Default Value: 0x0001_0000)

Offset: 0x064C			Register Name: DE_SYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0x064C			Register Name: DE_SYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x1	DE_SYS_RST DE_SYS Reset 0: Assert 1: De-assert
15:0	/	/	/

2.7.6.58 0x0670 GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x0670			Register Name: GPU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPU_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GPU_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: GPUPLL 001: PERI0_800M 010: PERI0_600M 011: PERI0_400M 100: PERI0_300M 101: PERI0_200M The clock selection supports glitch-free switch.
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M 0000: not mask 0001: mask 1 cycle at 16 cycles 0010: mask 2 cycles at 16 cycles 0011: mask 3 cycles at 16 cycles ..... 1111: mask 15 cycles at 16 cycles

2.7.6.59 0x067C GPU Gating Reset Configuration Register (Default Value: 0x0000_0000)

Offset: 0x067C			Register Name: GPU_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0x067C			Register Name: GPU_GATING_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	GPU_RST GPU Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPU_GATING Gating Clock for GPU 0: Mask 1: Pass

2.7.6.60 0x0680 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CE_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CE_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_480M 010: PERI0_400M 011: PERI0_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.7.6.61 0x068C CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG:
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

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Offset: 0x068C			Register Name: CE_BGR_REG:
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	CE_SYS_RST CE_SYS Reset 0: Assert 1: De-assert
16	R/W	0x0	CE_RST CE Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	CE_SYS_GATING Gating Clock for CE_SYS 0: Mask 1: Pass
0	R/W	0x0	CE_GATING Gating Clock for CE 0: Mask 1: Pass

2.7.6.62 0x0690 VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VE_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON VE_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VEPLL 001: PERI0_480M 010: PERI0_400M 011: PERI0_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

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2.7.6.63 0x069C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	VE_RST VE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING Gating Clock for VE 0: Mask 1: Pass

2.7.6.64 0x06E0 NPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x06E0			Register Name: NPU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NPU_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON NPU_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_480M 001: PERI0_600M 010: PERI0_800M 011: NPUPLL2X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

2.7.6.65 0x070C DMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMAC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0x070C			Register Name: DMAC_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DMAC_RST DMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMAC_GATING Gating Clock for DMAC 0: Mask 1: Pass

2.7.6.66 0x071C CPUX_MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: CPUX_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUX_MSGBOX_RST CPUX_MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUX_MSGBOX_GATING Gating Clock for CPUX_MSGBOX 0: Mask 1: Pass

2.7.6.67 0x072C SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPINLOCK_RST SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING Gating Clock for SPINLOCK 0: Mask 1: Pass

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2.7.6.68 0x0730 CPUX_TIMER0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0730			Register Name: CPUX_TIMER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER0_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER0_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER0 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.7.6.69 0x0734 CPUX_TIMER1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0734			Register Name: CPUX_TIMER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER1_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER1_CLK=Clock Source/M
30:27	/	/	/

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Offset: 0x0734			Register Name: CPUX_TIMER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER1 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.7.6.70 0x0738 CPUX_TIMER2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0738			Register Name: CPUX_TIMER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER2_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER2_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER2 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.

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Offset: 0x0738			Register Name: CPUX_TIMER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.7.6.71 0x073C CPUX_TIMER3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: CPUX_TIMER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER3_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER3_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER3 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/

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Offset: 0x073C			Register Name: CPUX_TIMER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.7.6.72 0x0740 CPUX_TIMER4 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: CPUX_TIMER4_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER4_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER4_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER4 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/

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Offset: 0x0740			Register Name: CPUX_TIMER4_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.7.6.73 0x0744 CPUX_TIMER5 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0744			Register Name: CPUX_TIMER5_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER5_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER5_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER5 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/

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Offset: 0x0744			Register Name: CPUX_TIMER5_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.7.6.74 0x074C CPUX_TIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x074C			Register Name: CPUX_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUX_TIMER_RST. CPUX_TIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUX_TIMER_GATING. Gating Clock for CPUX_TIMER 0: Mask 1: Pass

2.7.6.75 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST DBGSYS Reset 0: Assert 1: De-assert
15:1	/	/	/

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Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DBGSYS_GATING Gating Clock for DBGSYS 0: Mask 1: Pass

2.7.6.76 0x07AC PWMCTRL Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	PWMCTRL1_RST PWMCTRL1 Reset 0: Assert 1: De-assert
16	R/W	0x0	PWMCTRL0_RST PWMCTRL0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	PWMCTRL1_GATING Gating Clock for PWMCTRL1 0: Mask 1: Pass
0	R/W	0x0	PWMCTRL0_GATING Gating Clock for PWMCTRL0 0: Mask 1: Pass

2.7.6.77 0x07B0 IOMMU Clock Register (Default Value: 0x8000_0000)

Offset: 0x07B0			Register Name: IOMMU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	IOMMU_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON IOMMU_CLK = Clock Source/M
30:29	/	/	/

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Offset: 0x07B0			Register Name: IOMMU_CLK_REG
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	IOMMU_DFS_EN IOMMU CLK Dynamic Frequency Scaling Enable 0: Disable 1: Enable
27	R/WAC	0x0	IOMMU_UPD IOMMU Clock Configuration 0 update 0: Invalid 1: Valid Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This register supports DRAM REQ/ACK signal. When IOMMU_UPD is set to 1. IOMMU_CLK_SEL and IOMMU_CLK1 will be updated.
26:24	R/W	0x0	IOMMU_CLK_SEL Clock Source Select 000: PERI0_600M 001: DDRPLL 010: PERI1_480M 011: PERI1_400M 100: PERI1_150M 101: HOSC The clock MUX supports glitch-free switch and dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	IOMMU_DIV1 Factor M M= IOMMU_DIV1 + 1 FACTOR M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.7.6.78 0x07BC IOMMU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07BC			Register Name: IOMMU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	IOMMU_GATING Gating Clock for IOMMU 0: Mask 1: Pass

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2.7.6.79 0x0800 DRAM Clock Register (Default Value: 0x8000_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	DRAM_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DRAM_CLK = Clock Source/M
30:28	/	/	/
27	R/WAC	0x0	DRAM_UPD SDRCLK Configuration 0 update 0: Invalid 1: Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This register supports DRAM REQ/ACK signal. When DRAM_UPD is set to 1. RAM_CLK_GATING, DRAM_CLK_SEL, and DRAM_DIV1 will be updated.
26:24	R/W	0x0	DRAM_CLK_SEL Clock Source Select 000: DDRPLL 001: PERI1_600M 010: PERI1_480M 011: PERI1_400M 100: PERI1_150M The clock MUX supports glitch-free switch and dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	DRAM_DIV1 Factor M M= DRAM_DIV1 + 1 FACTOR M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.7.6.80 0x0804 MBUS Master Clock Gating Register (Default Value: 0x03D7_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/

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Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x1	USB_SYS_MBUS_GATE_SW_CFG USB_SYS MBUS Clock Gate Enable 0: Disable 1:Enable
24	R/W	0x1	GPU_MBUS_GATE_SW_CFG GPU MBUS Clock Gate Enable 0: Disable 1:Enable
23	R/W	0x1	DE_SYS_MBUS_GATE_SW_CFG DE_SYS MBUS Clock Gate Enable 0: Disable 1:Enable
22	R/W	0x1	NDFC_MBUS_GATE_SW_CFG NDFC MBUS Clock Gate Enable 0: Disable 1:Enable
21	/	/	/
20	R/W	0x1	VID_IN_MBUS_GATE_SW_CFG VID_IN MBUS Clock Gate Enable 0: Disable 1:Enable
19	/	/	/
18	R/W	0x1	CE_MBUS_GATE_SW_CFG CE MBUS Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	VE_MBUS_GATE_SW_CFG VE MBUS Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	DMAC_MBUS_GATE_SW_CFG DMAC MBUS Clock Gate Enable 0: Disable 1:Enable
15:13	/	/	/
12	R/W	0x0	GMAC1_MCLK_EN. Gating MBUS Clock For GMAC1. 0: Mask 1: Pass
11:10	/	/	/

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Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	ISP_MCLK_EN Gating MBUS Clock for ISP 0: Mask 1: Pass
8	R/W	0x0	CSI_MCLK_EN Gating MBUS Clock for CSI 0: Mask 1: Pass
7	/	/	/
6	R/W	0x0	USB3_MCLK_EN Gating MBUS Clock for USB3 0: Mask 1: Pass
5	R/W	0x0	NDFC_MCLK_EN Gating MBUS Clock for NDFC 0: Mask 1: Pass
4:3	/	/	/
2	R/W	0x0	CE_MCLK_EN Gating MBUS Clock for CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_EN Gating MBUS Clock for VE 0: Mask 1: Pass
0	R/W	0x0	DMAC_MCLK_EN Gating MBUS Clock for DMAC 0: Mask 1: Pass

2.7.6.81 0x080C DRAM Bus Gating Reset Register (Default Value: 0x0000_0001)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DRAM_RST DRAM Reset 0: Assert 1: De-assert

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Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:1	/	/	/
0	R/W	0x1	DRAM_GATING Gating Clock for DRAM 0: Mask 1: Pass

2.7.6.82 0x0810 NDFC CLK0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0810			Register Name: NDFC_CLK0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NDFC_CLK0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON NDFC_CLK0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.7.6.83 0x0814 NDFC CLK1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: NDFC_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NDFC_CLK1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON NDFC_CLK1_CLK = Clock Source/M
30:27	/	/	/

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Offset: 0x0814			Register Name: NDFC_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.7.6.84 0x082C NDFC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: NDFC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	NDFC_RST NDFC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NDFC_GATING Gating Clock for NDFC 0: Mask 1: Pass

2.7.6.85 0x0830 SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SMHC0_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.86 0x0834 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SMHC1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/

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Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.87 0x0838 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SMHC2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_800M 010: PERI0_600M 011: PERI1_800M 100: PERI1_600M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.88 0x084C SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

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Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST SMHC1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST SMHC0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING Gating Clock for SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING Gating Clock for SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING Gating Clock for SMHC0 0: Mask 1: Pass

2.7.6.89 0x088C SYSDAP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x088C			Register Name: SYSDAP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SYSDAP_RST SYSDAP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SYSDAP_GATING Gating Clock for DRAM 0: Mask 1: Pass

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2.7.6.90 0x090C UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	UART7_RST UART7 Reset 0: Assert 1: De-assert
22	R/W	0x0	UART6_RST UART6 Reset 0: Assert 1: De-assert
21	R/W	0x0	UART5_RST UART5 Reset 0: Assert 1: De-assert
20	R/W	0x0	UART4_RST UART4 Reset 0: Assert 1: De-assert
19	R/W	0x0	UART3_RST UART3 Reset 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST UART2 Reset 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST UART0 Reset 0: Assert 1: De-assert
15:8	/	/	/
7	R/W	0x0	UART7_GATING Gating Clock for UART7 0: Mask 1: Pass

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Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	UART6_GATING Gating Clock for UART6 0: Mask 1: Pass
5	R/W	0x0	UART5_GATING Gating Clock for UART5 0: Mask 1: Pass
4	R/W	0x0	UART4_GATING Gating Clock for UART4 0: Mask 1: Pass
3	R/W	0x0	UART3_GATING Gating Clock for UART3 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING Gating Clock for UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING Gating Clock for UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING Gating Clock for UART0 0: Mask 1: Pass

2.7.6.91 0x091C TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	TWI5_RST TWI5 Reset 0: Assert 1: De-assert

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Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	TWI4_RST TWI4 Reset 0: Assert 1: De-assert
19	R/W	0x0	TWI3_RST TWI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST TWI0 Reset 0: Assert 1: De-assert
15:6	/	/	/
5	R/W	0x0	TWI5_GATING Gating Clock for TWI5 0: Mask 1: Pass
4	R/W	0x0	TWI4_GATING Gating Clock for TWI4 0: Mask 1: Pass
3	R/W	0x0	TWI3_GATING Gating Clock for TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING Gating Clock for TWI2 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING Gating Clock for TWI1 0: Mask 1: Pass

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Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TWI0_GATING Gating Clock for TWI0 0: Mask 1: Pass

2.7.6.92 0x0940 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPI0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100:PERI1_200M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.7.6.93 0x0944 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPI1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100:PERI1_200M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.94 0x0948 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPI2_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100:PERI1_200M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.95 0x0950 SPIFC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0950			Register Name: SPIFC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPIFC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPIFC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100:PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/

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Offset: 0x0950			Register Name: SPIFC_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.96 0x096C SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	SPIFC_RST SPIFC Reset 0: Assert 1: De-assert
18	R/W	0x0	SPI2_RST SPI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST SPI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST SPI0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	SPIFC_GATING Gating Clock for SPIFC 0: Mask 1: Pass
2	R/W	0x0	SPI2_GATING Gating Clock for SPI2 0: Mask 1: Pass
1	R/W	0x0	SPI1_GATING Gating Clock for SPI1 0: Mask 1: Pass

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Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SPI0_GATING Gating Clock for SPI0 0: Mask 1: Pass

2.7.6.97 0x0970 GMAC0_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970			Register Name: GMAC0_25M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GMAC0_25M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GMAC0_25M_CLK =PERI0_150M/6=25M
30	R/W	0x0	GMAC0_25M_CLK_SRC_GATING Gating the Source Clock for Low Power Design 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

2.7.6.98 0x0974 GMAC1_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0974			Register Name: GMAC1_25M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GMAC1_25M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GMAC1_25M_CLK =PERI0_150M/6=25M
30	R/W	0x0	GMAC1_25M_CLK_SRC_GATING Gating the Source Clock for Low Power Design 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

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2.7.6.99 0x097C GMAC0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: GMAC0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GMAC0_RST GMAC0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GMAC0_GATING Gating Clock for GMAC0 0: Mask 1: Pass

2.7.6.100 0x098C GMAC1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x098C			Register Name: GMAC1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	GMAC1_AXI_RST GMAC1 AXI Reset 0: Assert 1: De-assert
16	R/W	0x0	GMAC1_RST GMAC1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GMAC1_GATING Gating Clock for GMAC1 0: Mask 1: Pass

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2.7.6.101 0x0990 IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0990			Register Name: IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IRRX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON IRRX_CLK = Clock Source/M
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: CLK32K 1: HOSC
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.102 0x099C IRRX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x099C			Register Name: IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	IRRX_RST IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRRX_GATING Gating Clock for IRRX 0: Mask 1: Pass

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2.7.6.103 0x09C0 IRTX Clock Register (Default Value: 0x0000_0000)

Offset: 0x09C0			Register Name: IRTX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IRTX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON IRTX_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: HOSC 1: PERI1_600M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.104 0x09CC IRTX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09CC			Register Name: IRTX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	IRTX_RST IRTX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRTX_GATING Gating Clock for IRTX 0: Mask 1: Pass

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2.7.6.105 0x09E0 GPADC_CTRL0_24M Clock Register (Default Value: 0x0000_0000)

Offset: 0x09E0			Register Name: GPADC_CTRL0_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPADC_CTRL0_24M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GPADC_CTRL0_24M_CLK = HOSC
30:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.106 0x09E4 GPADC_CTRL1_24M Clock Register (Default Value: 0x0000_0000)

Offset: 0x09E4			Register Name: GPADC_CTRL1_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPADC_CTRL1_24M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GPADC_CTRL1_24M_CLK = HOSC
30:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.107 0x09EC GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	GPADC_CTRL1_RST GPADC_CTRL1 Reset 0: Assert 1: De-assert

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Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	GPADC_RST GPADC_CTRL0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	GPADC_CTRL1_GATING Gating Clock for GPADC_CTRL1 0: Mask 1: Pass
0	R/W	0x0	GPADC_CTRL1_GATING Gating Clock for GPADC_CTRL1 0: Mask 1: Pass

2.7.6.108 0x09FC THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			Register Name: THS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	THS_RST THS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING Gating Clock for THS 0: Mask 1: Pass

2.7.6.109 0x0A70 USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB0_CLKEN Gating Clock for OHCI0 0: Clock is OFF 1: Clock is ON

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Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	USBPHY0_RSTN USB PHY0 Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USB0_CLK12M_SEL OHCI0 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from HOSC 10: CLK32K 11: CLK16M_RC
23:0	/	/	/

2.7.6.110 0x0A74 USB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A74			Register Name: USB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB1_CLKEN Gating Clock for OHCI1 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY1_RSTN USB PHY1 Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USB1_CLK12M_SEL OHCI1 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from HOSC 10: CLK32K 11: CLK16M_RC
23:0	/	/	/

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2.7.6.111 0x0A80 USB2_REF Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A80			Register Name: USB2_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_REF_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON USB2_REF_CLK = HOSC
30:0	/	/	/

2.7.6.112 0x0A84 USB3_PCIE_REF Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A84			Register Name: USB3_PCIE_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB3_PCIE_REF_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON USB3_REF_CLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 01: PERI0_200M 10: PERI1_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.113 0x0A88 USB3_SUSPEND Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A88			Register Name: USB3_SUSPEND_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB3_SUSPEND_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON USB3_SUSPEND_CLK = Clock Source/M
30:25	/	/	/

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Offset: 0x0A88			Register Name: USB3_SUSPEND_CLK_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: CLK32K 1: HOSC
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.114 0x0A8C USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	USBDEVICE0_RST USBDEVICE0 Reset 0: Assert 1: De-assert
23:22	/	/	/
21	R/W	0x0	USBEHCI1_RST USBEHCI1 Reset 0: Assert 1: De-assert
20	R/W	0x0	USBEHCI0_RST USBEHCI0 Reset 0: Assert 1: De-assert
19:18	/	/	/
17	R/W	0x0	USBOHCI1_RST USBOHCI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	USBOHCI0_RST USBOHCI0 Reset 0: Assert 1: De-assert
15:9	/	/	/

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Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	USBDEVICE0_GATING Gating Clock for USBDEVICE0 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	USBEHCI1_GATING Gating Clock for USBEHCI1 0: Mask 1: Pass
4	R/W	0x0	USBEHCI0_GATING Gating Clock for USBEHCI0 0: Mask 1: Pass
3:2	/	/	/
1	R/W	0x0	USBOHCI1_GATING Gating Clock for USBOHCI1 0: Mask 1: Pass
0	R/W	0x0	USBOHCI0_GATING Gating Clock for USBOHCI0 0: Mask 1: Pass

2.7.6.115 0x0A9C LRADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A9C			Register Name: LRADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LRADC_RST LRADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LRADC_GATING Gating Clock for LRADC 0: Mask 1: Pass

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2.7.6.116 0x0AA0 PCIE_AUX Clock Register (Default Value: 0x8000_0000)

Offset: 0x0AA0			Register Name: PCIE_AUX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PCIE_AUX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON PCIE_REF_ALT_CLK = Clock Source/M
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: HOSC 1: CLK32K
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.117 0x0AAC PCIE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0AAC			Register Name:PCIE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PCIE_USB3_SYS_RST PCIE POWER_UP Reset 0: Assert 1: De-assert
15:0	/	/	/

2.7.6.118 0x0ABC DISPLAY0_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ABC			Register Name: DISPLAY0_TOP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DISPLAY0_TOP_RST DISPLAY0_TOP Reset 0: Assert 1: De-assert
15:1	/	/	/

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Offset: 0x0ABC			Register Name: DISPLAY0_TOP_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DISPLAY0_TOP_GATING Gating Clock for DISPLAY0_TOP 0: Mask 1: Pass

2.7.6.119 0x0ACC DISPLAY1_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ACC			Register Name: DPSS_TOP1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DISPLAY1_TOP_RST DISPLAY1_TOP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DISPLAY1_TOP_GATING Gating Clock For DISPLAY1_TOP 0: Mask 1: Pass

2.7.6.120 0x0B04 HDMI_24M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B04			Register Name: HDMI_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDMI_24M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON HDMI_24M_CLK = HOSC
30:0	/	/	/

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2.7.6.121 0x0B10 HDMI CEC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B10			Register Name: HDMI_CEC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDMI_CEC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON HDMI_CEC_CLK = Clock Source
30	R/W	0x0	PERI_GATING. Gating PERI0PLL2X Clock. 0: Clock is OFF 1: Clock is ON
29:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select. 0: CLK32K 1: HDMI_CEC_CLK32K, PERI0PLL2X/36621 = 32.768 kHz 1X:/
23:0	/	/	/

2.7.6.122 0x0B1C HDMI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B1C			Register Name: HDMI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	HDMI_SUB_RST HDMI_SUB Reset 0: Assert 1: De-assert
16	R/W	0x0	HDMI_MAIN_RST HDMI_MAIN Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HDMI_GATING Gating Clock For HDMI 0: Mask 1: Pass

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2.7.6.123 0x0B24 DSI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: DSI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DSI0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_200M 010: PERI0_150M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.124 0x0B28 DSI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B28			Register Name: DSI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DSI1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_200M 010: PERI0_150M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.7.6.125 0x0B4C DSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: DSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	DSI1_RST DSI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	DSI0_RST DSI0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	DSI1_GATING Gating Clock for DSI1 0: Mask 1: Pass
0	R/W	0x0	DSI0_GATING Gating Clock for DSI0 0: Mask 1: Pass

2.7.6.126 0x0B60 TCONLCD0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCONLCD0_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONLCD0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X

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Offset: 0x0B60			Register Name: TCONLCD0_CLK_REG:
Bit	Read/Write	Default/Hex	Description
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.127 0x0B64 TCONLCD1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B64			Register Name: TCONLCD1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONLCD1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.7.6.128 0x0B68 TCONLCD2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B68			Register Name: TCONLCD2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONLCD2_CLK = Clock Source/M

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Offset: 0x0B68			Register Name: TCONLCD2_CLK_REG
Bit	Read/Write	Default/Hex	Description
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.129 0x0B6C COMBOPHY_DSI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B6C			Register Name: COMBOPHY_DSI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMBOPHY_DSI0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON COMBOPHY_DSI0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110: VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.7.6.130 0x0B70 COMBOPHY_DSI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B70			Register Name: COMBOPHY_DSI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMBOPHY_DSI1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON COMBOPHY_DSI1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.131 0x0B7C TCONLCD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCONLCD_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	TCONLCD2_RST TCON LCD2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TCONLCD1_RST TCON LCD1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TCONLCD0_RST TCON LCD0 Reset 0: Assert 1: De-assert

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Offset: 0x0B7C			Register Name: TCONLCD_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:3	/	/	/
2	R/W	0x0	TCONLCD2_GATING Gating Clock for TCON LCD2 0: Mask 1: Pass
1	R/W	0x0	TCONLCD1_GATING Gating Clock for TCON LCD1 0: Mask 1: Pass
0	R/W	0x0	TCONLCD0_GATING Gating Clock for TCON LCD0 0: Mask 1: Pass

2.7.6.132 0x0B80 TCONTV0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B80			Register Name: TCONTV0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONTV0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONTV0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.7.6.133 0x0B84 TCONTV1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B84			Register Name: TCONTV1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONTV1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONTV1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.134 0x0B9C TCONTV Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B9C			Register Name: TCONTV_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	TCONTV1_RST TCONTV1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TCONTV0_RST TCONTV0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	TCONTV1_GATING Gating Clock for TCONTV1 0: Mask 1: Pass

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Offset: 0x0B9C			Register Name: TCONTV_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TCONTV0_GATING Gating Clock for TCONTV0 0: Mask 1: Pass

2.7.6.135 0x0BAC LVDS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BAC			Register Name: LVDS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	LVDS1_RST LVDS1 Reset 0: Assert 1: De-assert
16	R/W	0x0	LVDS0_RST LVDS0 Reset 0: Assert 1: De-assert
15:0	/	/	/

2.7.6.136 0x0BB0 EDP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BB0			Register Name: EDP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EDP_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON EDP_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X
23:5	/	/	/

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Offset: 0x0BB0			Register Name: EDP_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.137 0x0BBC EDP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BBC			Register Name: EDP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EDP_RST EDP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EDP_GATING Gating Clock for EDP 0: Mask 1: Pass

2.7.6.138 0x0BCC Video Out Bus Gating Reset Register (Default Value: 0x0003_0000)

Offset: 0x0BCC			Register Name: VIDEO_OUT_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	VIDEO_OUT1_RST VIDEO_OUT1 Reset 0: Assert 1: De-assert
16	R/W	0x1	VIDEO_OUT0_RST VIDEO_OUT0 Reset 0: Assert 1: De-assert
15:0	/	/	/

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2.7.6.139 0x0BF0 LEDC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BF0			Register Name: LEDC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LEDC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON LEDC_CLK = Clock Source/M/N
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_600M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.140 0x0BFC LEDC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BFC			Register Name: LEDC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LEDC_RST LEDC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LEDC_GATING Gating Clock for LEDC 0: Mask 1: Pass

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2.7.6.141 0x0C04 CSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: PERI0_480M 011: VIDEO3PLL4X 100: VIDEO3PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.142 0x0C08 CSI Master0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/

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Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.143 0x0C0C CSI Master1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI_MASTER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

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2.7.6.144 0x0C10 CSI Master2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C10			Register Name: CSI_MASTER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.145 0x0C14 CSI Master3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C14			Register Name: CSI_MASTER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER3_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER3_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x0C14			Register Name: CSI_MASTER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.146 0x0C1C CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C1C			Register Name: CSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CSI_RST CSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING Gating Clock for CSI 0: Mask 1: Pass

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2.7.6.147 0x0C20 ISP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C20			Register Name: ISP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ISP_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON ISP_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO2PLL4X 011: VIDEO3PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.7.6.148 0x0C70 DSP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C70			Register Name: DSP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSP_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DSP_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK32K 010: CLK16M_RC 011: PERI0PLL2X 100: PERI0_480M
23:5	/	/	/

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Offset: 0x0C70			Register Name: DSP_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

2.7.6.149 0x0E04 AHB Gate Enable Register (Default Value: 0x107F_0FFE)

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AHB_MONITOR_EN AHB bus auto clock gating function enable 1: enable auto clock gate 0: disable auto clock gate
30	/	/	/
29	R/W	0x0	SD_MONITOR_EN SD bus auto clock gating function enable 1: enable auto clock gate 0: disable auto clock gate
28	R/W	0x1	CPUS_HCLK_GATE_SW_CFG CPUS AHB Clock Gate Enable 0: Disable 1:Enable
27:23	/	/	/
22	R/W	0x1	SPIFC_MBUS_AHB_GATE_SW_CFG SPIFC MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
21	/	/	/
20	R/W	0x1	GMAC0_MBUS_AHB_GATE_SW_CFG GMAC0 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
19	R/W	0x1	SMHC2_MBUS_AHB_GATE_SW_CFG SMHC2 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
18	R/W	0x1	SMHC1_MBUS_AHB_GATE_SW_CFG SMHC1 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable

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Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x1	SMHC0_MBUS_AHB_GATE_SW_CFG SMHC0 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
16	R/W	0x1	USB_MBUS_AHB_GATE_SW_CFG USB MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
15:12	/	/	/
11	R/W	0x1	USB_SYS_AHB_GATE_SW_CFG USB_SYS AHB Clock Gate Enable 0: Disable 1: Enable
10	R/W	0x1	GPU_AHB_GATE_SW_CFG GPU AHB Clock Gate Enable 0: Disable 1: Enable
9	R/W	0x1	GMAC1_AHB_GATE_SW_CFG GMAC1 AHB Clock Gate Enable 0: Disable 1: Enable
8	R/W	0x1	GMAC_AHB_GATE_SW_CFG GMAC AHB Clock Gate Enable 0: Disable 1: Enable
7	R/W	0x1	SMHC2_AHB_GATE_SW_CFG SMHC2 AHB Clock Gate Enable 0: Disable 1: Enable
6	R/W	0x1	SMHC1_AHB_GATE_SW_CFG SMHC1 AHB Clock Gate Enable 0: Disable 1: Enable
5	R/W	0x1	SMHC0_AHB_GATE_SW_CFG SMHC0 AHB Clock Gate Enable 0: Disable 1: Enable
4	R/W	0x1	USB_AHB_GATE_SW_CFG USB AHB Clock Gate Enable 0: Disable 1: Enable

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Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x1	VID_OUT_AHB_GATE_SW_CFG Video Out AHB Clock Gate Enable 0: Disable 1: Enable
2	R/W	0x1	VID_IN_AHB_GATE_SW_CFG Video in AHB Clock Gate Enable 0: Disable 1: Enable
1	R/W	0x1	VE_AHB_GATE_SW_CFG VE AHB Clock Gate Enable 0: Disable 1: Enable
0	/	/	/

2.7.6.150 0x0E08 PERI0PLL Gate Enable Register (Default Value: 0x8FFF_0FFF)

Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PERI0_300M_DSP_GATE_EN. PERI0_300M For DSP Clock Gate Enable. 0:Disable 1:Enable
30:28	/	/	/
27	R/W	0x1	PERI0PLL2X_GATE_SW_CFG PERI0PLL2X Clock Gate Enable 0: Disable 1:Enable
26	R/W	0x1	PERI0_800M_GATE_SW_CFG PERI0 800M Clock Gate Enable 0: Disable 1:Enable
25	R/W	0x1	PERI0_600M_GATE_SW_CFG PERI0 600M Clock Gate Enable 0: Disable 1:Enable
24	R/W	0x1	PERI0_480M_GATE_ALL_CFG PERI0 480M Clock Gate Enable 0: Disable 1:Enable

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Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
23	R/W	0x1	PERI0_480M_GATE_SW_CFG PERI0 480M Clock Gate Enable 0: Disable 1:Enable
22	R/W	0x1	PERI0_160M_GATE_SW_CFG PERI0 160M Clock Gate Enable 0: Disable 1:Enable
21	R/W	0x1	PERI0_300M_GATE_ALL_CFG PERI0 300M Clock Gate Enable 0: Disable 1:Enable
20	R/W	0x1	PERI0_300M_GATE_SW_CFG PERI0 300M Clock Gate Enable 0: Disable 1:Enable
19	R/W	0x1	PERI0_150M_GATE_SW_CFG PERI0 150M Clock Gate Enable 0: Disable 1:Enable
18	R/W	0x1	PERI0_400M_GATE_ALL_CFG PERI0 400M Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	PERI0_400M_GATE_SW_CFG PERI0 400M Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	PERI0_200M_GATE_SW_CFG PERI0 200M Clock Gate Enable 0: Disable 1:Enable
15:12	/	/	/
11	R/W	0x1	PERI0PLL2X_AUTO_GATE_EN PERI0PLL2X Clock Auto Gate Enable 0: Auto 1:No-Auto
10	R/W	0x1	PERI0_800M_AUTO_GATE_EN PERI0 800M Clock Auto Gate Enable 0: Auto 1:No-Auto

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Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
9	R/W	0x1	PERI0_600M_AUTO_GATE_EN PERI0 600M Clock Auto Gate Enable 0: Auto 1:No-Auto
8	R/W	0x1	PERI0_480M_AUTO_GATE_EN_ALL PERI0 480M Clock Auto Gate Enable 0: Auto 1:No-Auto
7	R/W	0x1	PERI0_480M_AUTO_GATE_EN PERI0 480M Clock Auto Gate Enable 0: Auto 1:No-Auto
6	R/W	0x1	PERI0_160M_AUTO_GATE_EN PERI0 160M Clock Auto Gate Enable 0: Auto 1:No-Auto
5	R/W	0x1	PERI0_300M_AUTO_GATE_EN_ALL PERI0 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
4	R/W	0x1	PERI0_300M_AUTO_GATE_EN PERI0 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
3	R/W	0x1	PERI0_150M_AUTO_GATE_EN PERI0 150M Clock Auto Gate Enable 0: Auto 1:No-Auto
2	R/W	0x1	PERI0_400M_AUTO_GATE_EN_ALL PERI0 400M Clock Auto Gate Enable All 0: Auto 1:No-Auto
1	R/W	0x1	PERI0_400M_AUTO_GATE_EN PERI0 400M Clock Auto Gate Enable 0: Auto 1:No-Auto
0	R/W	0x1	PERI0_200M_AUTO_GATE_EN PERI0 200M Clock Auto Gate Enable 0: Auto 1:No-Auto

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2.7.6.151 0x0E0C CLK24M Gate Enable Register (Default Value: 0x0000_0009)

Offset: 0x0E0C			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x1	RES_DCAP_24M_GATE_EN RES_DCAP 24M Clock Gate Enable 0: Disable 1:Enable
2:1	/	/	/
0	R/W	0x1	USB_24M_GATE_EN USB 24M Clock Gate Enable 0: Disable 1:Enable

2.7.6.152 0x0E10 PERI1PLL Gate Enable Register (Default Value: 0x8EBF_0EBF)

Offset: 0x0E10			Register Name: PERI1PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PERI1_300M_DSP_GATE_EN. PERI1_300M For DSP Clock Gate Enable. 0:Disable 1:Enable
30:28	/	/	/
27	R/W	0x1	PERI1_800M_GATE_SW_CFG PERI1 800M Clock Gate Enable 0: Disable 1:Enable
26	R/W	0x1	PERI1_600M_GATE_ALL_CFG PERI1 600M Clock Gate Enable 0: Disable 1:Enable
25	R/W	0x1	PERI1_600M_GATE_SW_CFG PERI1 600M Clock Gate Enable 0: Disable 1:Enable
24	/	/	/
23	R/W	0x1	PERI1_480M_GATE_SW_CFG PERI1 480M Clock Gate Enable 0: Disable 1:Enable
22	/	/	/

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Offset: 0x0E10			Register Name: PERI1PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
21	R/W	0x1	PERI1_300M_GATE_ALL_CFG PERI1 300M Clock Gate Enable 0: Disable 1:Enable
20	R/W	0x1	PERI1_300M_GATE_SW_CFG PERI1 300M Clock Gate Enable 0: Disable 1:Enable
19	R/W	0x1	PERI1_150M_GATE_SW_CFG PERI1 150M Clock Gate Enable 0: Disable 1:Enable
18	R/W	0x1	PERI1_400M_GATE_ALL_CFG PERI1 400M Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	PERI1_400M_GATE_SW_CFG PERI1 400M Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	PERI1_200M_GATE_SW_CFG PERI1 200M Clock Gate Enable 0: Disable 1:Enable
15:12	/	/	/
11	R/W	0x1	PERI1_800M_AUTO_GATE_EN PERI1 800M Clock Auto Gate Enable 0: Auto 1:No-Auto
10	R/W	0x1	PERI1_600M_AUTO_GATE_EN_ALL PERI1 600M Clock Auto Gate Enable 0: Auto 1:No-Auto
9	R/W	0x1	PERI1_600M_AUTO_GATE_EN PERI1 600M Clock Auto Gate Enable 0: Auto 1:No-Auto
8	/	/	/

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Offset: 0x0E10			Register Name: PERI1PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	PERI1_480M_AUTO_GATE_EN PERI1 480M Clock Auto Gate Enable 0: Auto 1:No-Auto
6	/	/	/
5	R/W	0x1	PERI1_300M_AUTO_GATE_EN_ALL PERI1 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
4	R/W	0x1	PERI1_300M_AUTO_GATE_EN PERI1 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
3	R/W	0x1	PERI1_150M_AUTO_GATE_EN PERI1 150M Clock Auto Gate Enable 0: Auto 1:No-Auto
2	R/W	0x1	PERI1_400M_AUTO_GATE_EN_ALL PERI1 400M Clock Auto Gate Enable All 0: Auto 1:No-Auto
1	R/W	0x1	PERI1_400M_AUTO_GATE_EN PERI1 400M Clock Auto Gate Enable 0: Auto 1:No-Auto
0	R/W	0x1	PERI1_200M_AUTO_GATE_EN PERI1 200M Clock Auto Gate Enable 0: Auto 1:No-Auto

2.7.6.153 0x0E14 VIDEOPLL Gate Enable Register (Default Value: 0x00BF_00BF)

Offset: 0x0E14			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x1	VIDEO3PLL3X_GATE_SW_CFG VIDEO3PLL3X Clock Gate Enable 0: Disable 1:Enable
22	/	/	/

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Offset: 0x0E14			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
21	R/W	0x1	VIDEO1PLL3X_GATE_SW_CFG VIDEO1PLL3X Clock Gate Enable 0: Disable 1:Enable
20	R/W	0x1	VIDEO0PLL3X_GATE_SW_CFG VIDEO0PLL3X Clock Gate Enable 0: Disable 1:Enable
19	R/W	0x1	VIDEO3PLL4X_GATE_SW_CFG VIDEO3PLL4X Clock Gate Enable 0: Disable 1:Enable
18	R/W	0x1	VIDEO2PLL4X_GATE_SW_CFG VIDEO2PLL4X Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	VIDEO1PLL4X_GATE_SW_CFG VIDEO1PLL4X Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	VIDEO0PLL4X_GATE_SW_CFG VIDEO0PLL4X Clock Gate Enable 0: Disable 1:Enable
15:8	/	/	/
7	R/W	0x1	VIDEO3PLL3X_AUTO_GATE_EN VIDEO3PLL3X Clock Auto Gate Enable 0: Auto 1:No-Auto
6	/	/	/
5	R/W	0x1	VIDEO1PLL3X_AUTO_GATE_EN VIDEO1PLL3X Clock Auto Gate Enable 0: Auto 1:No-Auto
4	R/W	0x1	VIDEO0PLL3X_AUTO_GATE_EN VIDEO0PLL3X Clock Auto Gate Enable 0: Auto 1:No-Auto

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Offset: 0x0E14			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x1	VIDEO3PLL4X_AUTO_GATE_EN VIDEO3PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto
2	R/W	0x1	VIDEO2PLL4X_AUTO_GATE_EN VIDEO2PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto
1	R/W	0x1	VIDEO1PLL4X_AUTO_GATE_EN VIDEO1PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto
0	R/W	0x1	VIDEO0PLL4X_AUTO_GATE_EN VIDEO0PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto

2.7.6.154 0x0E20 CM GPU Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x0E20			Register Name: CM_GPU_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_GPU_STATUS CM GPU Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_GPU_MODULE_MODE CM GPU module mode 0: Disable 1: Enable

2.7.6.155 0x0E24 CM VE Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E24			Register Name: CM_VE_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/

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Offset: 0x0E24			Register Name: CM_VE_CFG_REG
Bit	R/W	Default/Hex	Description
17:16	R	0x2	CM_VE_STATUS CM VE Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VE_MODULE_MODE CM VE module mode 0: Disable 1: Enable

2.7.6.156 0x0E28 CM DE Enable Configuration Register(Default Value:0x0002_0000)

Offset: 0x0E28			Register Name:CM_DE_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_DE_STATUS CM DE Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_DE_MODULE_MODE CM DE module mode 0: Disable 1: Enable

2.7.6.157 0x0E2C CM VI Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E2C			Register Name: CM_VI_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VI_STATUS CM VI Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VI_MODULE_MODE CM VI module mode 0: Disable 1: Enable

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2.7.6.158 0x0E30 CM VO0 Enable Configuration Register(Default Value:0x0002_0000)

Offset:0x0E30			Register Name:CM_VO0_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VO0_STATUS CM VO0 Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VO0_MODULE_MODE CM VO0 module mode 0: Disable 1: Enable

2.7.6.159 0x0E34 CM VO1 Enable Configuration Register(Default Value:0x0002_0000)

Offset:0x0E34			Register Name:CM_VO1_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VO1_STATUS CM VO1 Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VO1_MODULE_MODE CM VO1 module mode 0: Disable 1: Enable

2.7.6.160 0x0E38 CM NDFC Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E38			Register Name: CM_NDFC_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_NDFC_STATUS CM NDFC Status 01: Power OFF 10: Power ON
15:1	/	/	/

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Offset: 0x0E38			Register Name: CM_NDFC_CFG_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	CM_NDFC_MODULE_MODE CM NDFC module mode 0: Disable 1: Enable

2.7.6.161 0x0E3C CM PCIE Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E3C			Register Name: CM_PCIE_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_PCIE_STATUS CM PCIE Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_PCIE_MODULE_MODE CM PCIE module mode 0: Disable 1: Enable

2.7.6.162 0x0F00 CCU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCU_SEC_SWITCH_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MBUS_SEC MBUS clock register security 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC Bus relevant registers security 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC PLL relevant registers security 0: Secure 1: Non-secure

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2.7.6.163 0x0F08 SYSDAP REQ Control Register (Default Value: 0x0000_0001)

Offset: 0x0F08			Register Name: SYSDAP_REQ_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	SYSDAP_REQ_ENABLE 0：Disable 1：Enable By configuring this bit, SYSDAP REQ signal could be set to control the clock and reset of CE and DAPSYS.

2.7.6.164 0x0F30 CCU FANOUT CLOCK GATE Register (Default Value:0x0000_0000)

Offset: 0x0F30			Register Name: CCU_FAN_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	CLK50M_EN Gating for CLK50M 0: Clock is OFF 1: Clock is ON
3	R/W	0x0	CLK25M_EN Gating for CLK25M 0: Clock is OFF 1: Clock is ON
2	R/W	0x0	CLK16M_EN Gating for CLK16M 0: Clock is OFF 1: Clock is ON
1	R/W	0x0	CLK12M_EN Gating for CLK12M 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	CLK24M_EN Gating for CLK24M 0: Clock is OFF 1: Clock is ON

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2.7.6.165 0x0F34 CLK27M FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F34			Register Name: CLK27M_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLK27M_EN Gating for CLK27M 0: Clock is OFF 1: Clock is ON SCLK=Clock Source/M/N
30:26	/	/	/
25:24	R/W	0x0	CLK27M_SCR_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X
23:13	/	/	/
12:8	R/W	0x0	CLK27M_DIV1 Factor N N= FACTOR_N +1 FACTOR_M is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	CLK27M_DIV0 Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.166 0x0F38 CLK FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F38			Register Name: CLK_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCLK_DIV_EN Gating for PCLK 0: Clock is OFF 1: Clock is ON PCLK = APB0_CLK/M/N
30:10	/	/	/
9:5	R/W	0x0	PCLK_DIV1 Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.

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Offset: 0x0F38			Register Name: CLK_FAN_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	PCLK_DIV Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.7.6.167 0x0F3C CCU FANOUT Register (Default Value:0x0000_0007)

Offset: 0x0F3C			Register Name: CCU_FAN_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	Reserved
23	R/W	0x0	CLK_FANOUT2_EN Gating for CLK_FANOUT2 0: Clock is OFF 1: Clock is ON
22	R/W	0x0	CLK_FANOUT1_EN Gating for CLK_FANOUT1 0: Clock is OFF 1: Clock is ON
21	R/W	0x0	CLK_FANOUT0_EN Gating for CLK_FANOUT0 0: Clock is OFF 1: Clock is ON
20:18	/	/	/
17:9	R/W	0x0	Reserved
8:6	R/W	0x0	CLK_FANOUT2_SEL Clock Fanout2 Select 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From DCXO/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From DCXO) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK 111: CLK50M (From PERI0_150M/3) CLK_FANOUT2 can be selected to output from the above seven sources.

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Offset: 0x0F3C			Register Name: CCU_FAN_REG
Bit	Read/Write	Default/Hex	Description
5:3	R/W	0x0	CLK_FANOUT1_SEL Clock Fanout1 Select 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From DCXO/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From DCXO) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK 111: CLK50M (From PERI0_150M/3) CLK_FANOUT1 can be selected to output from the above seven sources.
2:0	R/W	0x7	CLK_FANOUT0_SEL Clock Fanout0 Select 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From DCXO/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From DCXO) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK 111: CLK50M (From PERI0_150M/3) CLK_FANOUT0 can be selected to output from the above seven sources.

2.7.6.168 0x0F40 PLL Configuration0 Register (Default Value: 0x0000_0000)

Offset: 0x0F40			Register Name: PLL_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG0 PLL Control Reserved Register

2.7.6.169 0x0F44 PLL Configuration1 Register (Default Value: 0x0000_0000)

Offset: 0x0F44			Register Name: PLL_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG1 PLL Control Reserved Register

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2.7.6.170 0x0F48 PLL Configuration2 Register (Default Value: 0x0000_0000)

Offset: 0x0F48			Register Name: PLL_CFG2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG2 PLL Control Reserved Register

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2.8 DMA Controller (DMAC)

2.8.1 Overview

The Direct Memory Access (DMA) is a method of transferring data between peripherals and memories (including the SRAM and DRAM) without using the CPU. It is an efficient way to offload data transfer duties from the CPU. Without DMA, the CPU has to control all the data transfers. While with DMA, the DMAC directly transfers data between a peripheral and a memory, between peripherals, or between memories.

The DMAC has the following features:

- Up to 16-ch DMA in CPUX domain and 16-ch DMA in CPUS domain
- Provides 53 peripheral DMA requests for data reading and 53 peripheral DMA requests for data writing
- Transferring data with linked list
- Flexible data width: 8 bits, 16 bits, or, 32 bits
- Programmable DMA burst length
- DRQ response includes waiting mode and handshake mode
- Supports non-aligned transform for memory devices
- DMA channels that support the following:
  - Pausing DMA
  - BMODE and I/O speed mode
  - DMA timeout

NOTE

The following description focuses on the DMA of the CPUX domain.

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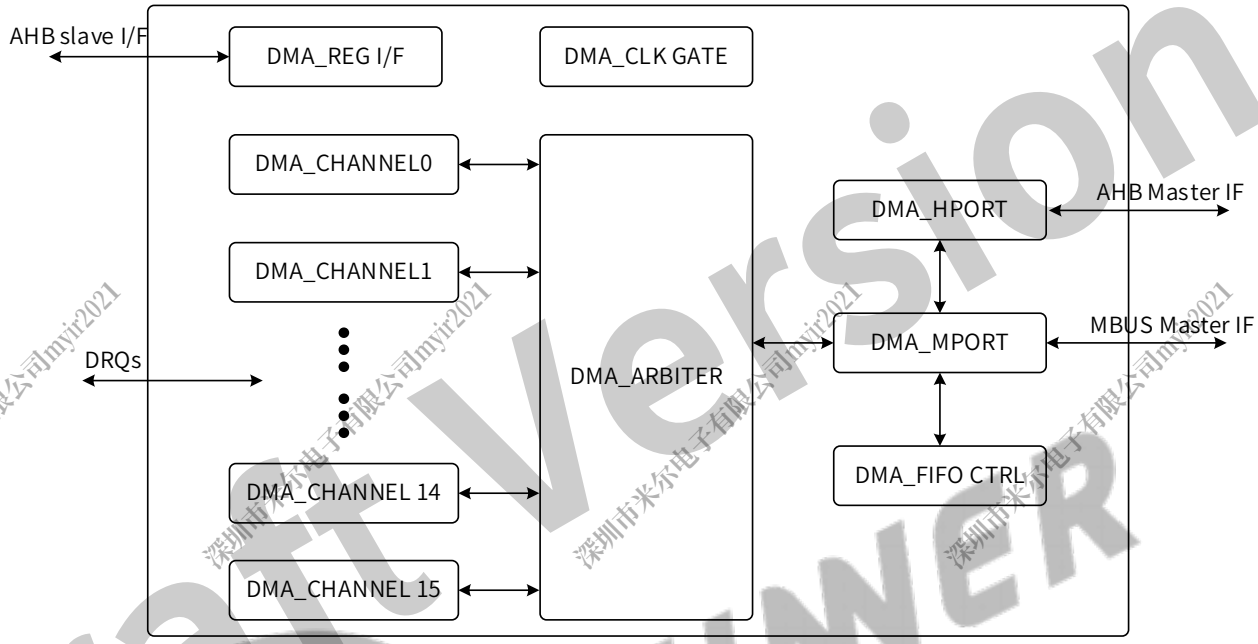
2.8.2 Block Diagram

The following figure shows a block diagram of DMAC.

Figure 2-10 DMAC Block Diagram



DMAC contains the following sub-blocks:

Table 2-11 DMAC Sub-blocks

Sub-block	Description
DMA_ARBITER	Arbitrates the DMA read/write requests from all channels, and converts the requests to the read/write requests of ports.
DMA_CHANNELs	DMA transfer engine. Each channel is independent. When the DMA requests from multiple peripherals are valid simultaneously, the channel with the highest priority starts data transfer first. The system uses the polling mechanism to decide the priorities of DMA channels. When DMA_ARBITER is idle, channel 0 has the highest priority, whereas channel 15 has the lowest priority. When DMA_ARBITER is busy processing the request from channel n, channel (n+1) has the highest priority. For n = 15, the channel (n + 1) should be channel 0.
DRQs	DMA requests. Peripherals use the DMA request signals to request a data transfer.
DMA_MPORT	Receives the read/write requests from DMA_ARBITER, and converts the requests to the corresponding MBUS access requests. It is mainly used for accessing the DRAM.
DMA_HPORT	The port for accessing the AHB Master. It is mainly used for accessing the SRAM and IO devices.
DMA_FIFO CTRL	Internal FIFO cell control module.
DMA_REG Interface	DMA_REG is the common register module that is mainly used to resolve AHB commands.

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Sub-block	Description
DMA_CLKGATE	The control module for hardware auto clock gating.

The DMAC integrates 16 independent DMA channels and each channel has an independent FIFO controller. When the DMA channel starts, the DMAC gets a DMA descriptor from the DMA_DESC_ADDR_REG and uses it as the configuration information for the data transfer of the current DMA package. Then the DMAC can transfer data between the specified devices. After transferring a DMA package, the DMAC judges if the current channel transfer is finished via the linked address in the descriptor. If the linked address shows all the packages are transferred, the DMAC will end the chain transmission and close the channel.

2.8.3 Functional Description

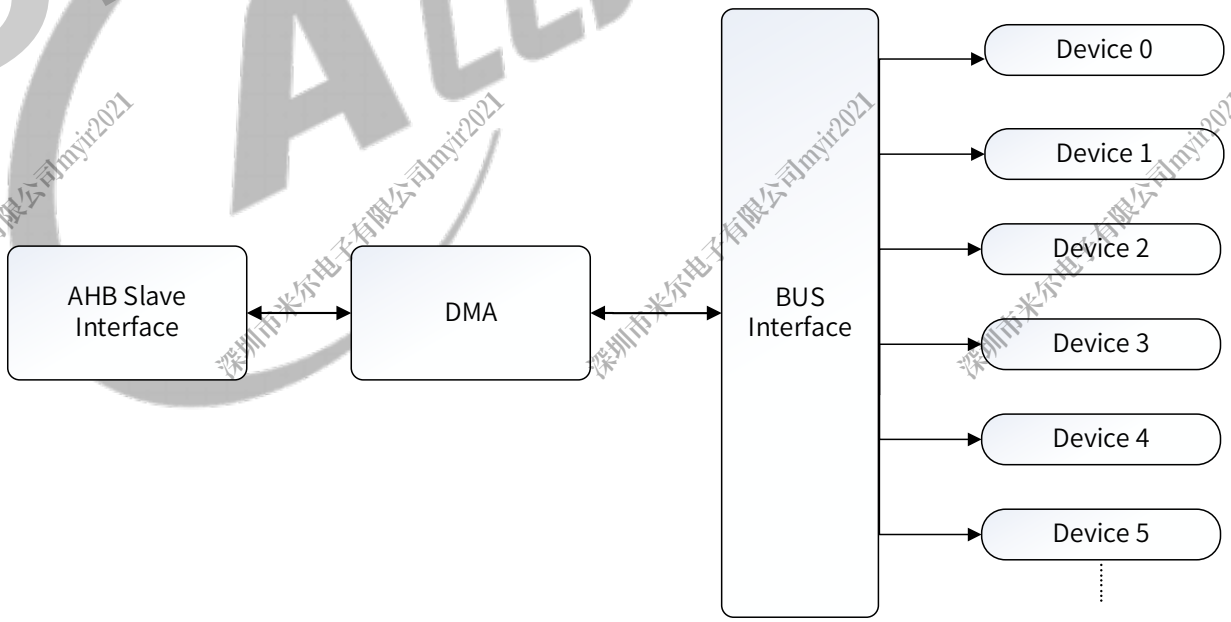
2.8.3.1 Clock

The DMAC is on AHB or MBUS. The clocks of AHB and MBUS influences the transfer efficiency of the DMAC.

2.8.3.2 Typical Application

The following figure shows a typical application of the DMAC.

Figure 2-11 DMAC Typical Application Diagram



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2.8.3.3 DRQ Port of Peripherals

The following tables show the source DRQ types and destination DRQ types of different ports.

Table 2-12 DMA DRQ Type

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2		port2	
port3		port3	
port4		port4	
port5		port5	
port6		port6	
port7		port7	
port8		port8	
port9		port9	
port10	NDFC	port10	NDFC
port11		port11	
port12	GPADC_CTRL0	Port12	
port13	GPADC_CTRL1	port13	CIR_TX
port14	UART0_RX	port14	UART0_TX
port15	UART1_RX	port15	UART1_TX
port16	UART2_RX	port16	UART2_TX
port17	UART3_RX	port17	UART3_TX
port18	UART4_RX	port18	UART4_TX
port19	UART5_RX	port19	UART5_TX
port20	UART6_RX	Port20	UART6_TX
port21	UART7_RX	port21	UART7_TX
port22	SPI0_RX	port22	SPI0_TX
port23	SPI1_RX	port23	SPI1_TX
port24	SPI2_RX	port24	SPI2_TX
port25		port25	
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	USB0_EP1	Port30	USB0_EP1
Port31	USB0_EP2	Port31	USB0_EP2
Port32	USB0_EP3	Port32	USB0_EP3
Port33	USB0_EP4	Port33	USB0_EP4
Port34	USB0_EP5	Port34	USB0_EP5
Port35		Port35	
Port36		Port36	

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Source DRQ Type		Destination DRQ Type	
Port37		Port37	
Port38		Port38	
Port39		Port39	
Port40		Port40	
Port41		Port41	
Port42		Port42	LEDC
Port43	TWI0	Port43	TWI0
Port44	TWI1	Port44	TWI1
Port45	TWI2	Port45	TWI2
Port46	TWI3	Port46	TWI3
Port47	TWI4	Port47	TWI4
Port48	TWI5	Port48	TWI5
Port49	S_TWI0	Port49	S_TWI0
Port50	S_TWI1	Port50	S_TWI1
Port51	S_UART0	Port51	S_UART0
Port52	S_UART1	Port52	S_UART1
Port53	S_SPI0	Port53	S_SPI0

Table 2-13 DMA DRQ Type of DSP_DMAC

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2	OWA	port2	OWA
port3	I2S0_RX	port3	I2S0_TX
port4	I2S1_RX	port4	I2S1_TX
port5	I2S2_RX	port5	I2S2_TX
port6	I2S3_RX	port6	I2S3_TX
port7	AUDIO_CODEC	port7	AUDIO_CODEC
port8	DMIC	port8	
port9	S_TWI0	port9	S_TWI0
port10	S_TWI1	port10	S_TWI1
port11	S_UART0	port11	S_UART0
port12	S_UART1	port12	S_UART1
Port13	S_SPI0	Port13	S_SPI0
Port14	S_TWI2	Port14	S_TWI2

2.8.3.4 DMA Descriptor

The DMAC descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words: Configuration, Source Address, Destination

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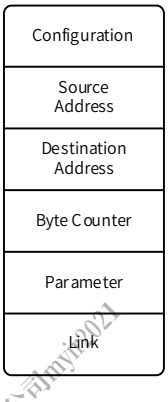
Address, Byte Counter, Parameter, and Link. The following figure shows the structure of the DMA descriptor.

Figure 2-12 DMA Descriptor



- **Configuration**: Configure the following information.
  - DRQ type: DRQ type of the source and destination devices.
  - Address counting mode: For both the source and destination devices, there are two address counting modes: the IO mode and linear mode. The IO mode is for IO devices whose address is fixed during the data transfer and the linear mode is for the memory whose address is increasing during the data transfer.
  - Transferred block length: How many times can non-memory peripherals transfer in a valid DRQ. The block length supports 1 time, 4 times, 8 times, and 16 times.
  - Transferred data width: The data width of operating the non-memory peripherals. The data width supports 8 bits, 16 bits, and 32 bits.

NOTE

The configuration supports BMODE mode. The BMODE is used in the following scenario: the source is an IO device, and the destination is a memory device. Setting the BMODE mode can limit the amount of block data transferred in DMA block transmission to the amount of data transferred when the DRQ threshold of the source IO device is 1.

- **Source Address**: Configure the address of the source device.
- **Destination Address**: Configure the address of the destination device.

  DMA reads data from the source address and then writes data to the destination address.

  Both the DMA source and destination addresses have 34 bits. In the descriptor, because there are only 32 bits in the Source/Destination Address field, another 2 bits are stored in the Parameter field.

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The following table shows the details of the related fields in the descriptor.

Table 2-14 Source/Destination Address Distribution

Descriptor Group	Bit	Description
Source Address	31:0	DMA transfers the lower 32 bits of the 34-bit source address
Destination Address	31:0	DMA transfers the lower 32 bits of the 34-bit destination address
Parameter	31	TIMEOUT Enable TIMEOUT only can be enabled in BMODE and IOspeed should be disabled when using this function.
	30:29	TIMEOUT Configuration 00: Not use sub-functions 01: Generate an interrupt and suspend the transmission after timeout. 10: Generate an interrupt and end the transmission after timeout. 11: Generate an interrupt and skip to the next descriptor after timeout.
	28:20	TIMEOUT Configuration Timer time of channels.
	19:18	DMA transfers the higher 2 bits of the 34-bit destination address
	17:16	DMA transfers the high 2 bits of the 34-bit source address
	15:9	Reserved
	8	I/O Speed Mode Enable If this bit is enabled, DMA will transmit the data of the I/O device from the source device or the destination device, or both of them at a faster speed. **Note: IOspeed and BMODE cannot be enabled at the same time.**
	7:0	Wait Clock Cycles Set the waiting time in DRQ mode
Link	31:2	The address of the next group descriptor, the lower 30 bits of the word address
	1:0	The address of the next group descriptor, the higher 2 bits of the word address

From the above table, you can get:

Real DMA source address (in byte mode) = {Parameter [17:16], Source Address [31:0]};

Real DMA destination address (in byte mode) = {Parameter [19:18], Destination Address [31:0]};

Real link address (in byte mode) = {Link [1:0], Link [31:2], 2'b00}.

- **Byte counter**: Configure the data amount of a package. The maximum value is (2^25-1) bytes. If the data amount of the package reaches the maximum value, even if DRQ is valid, the DMA will stop the current transfer.

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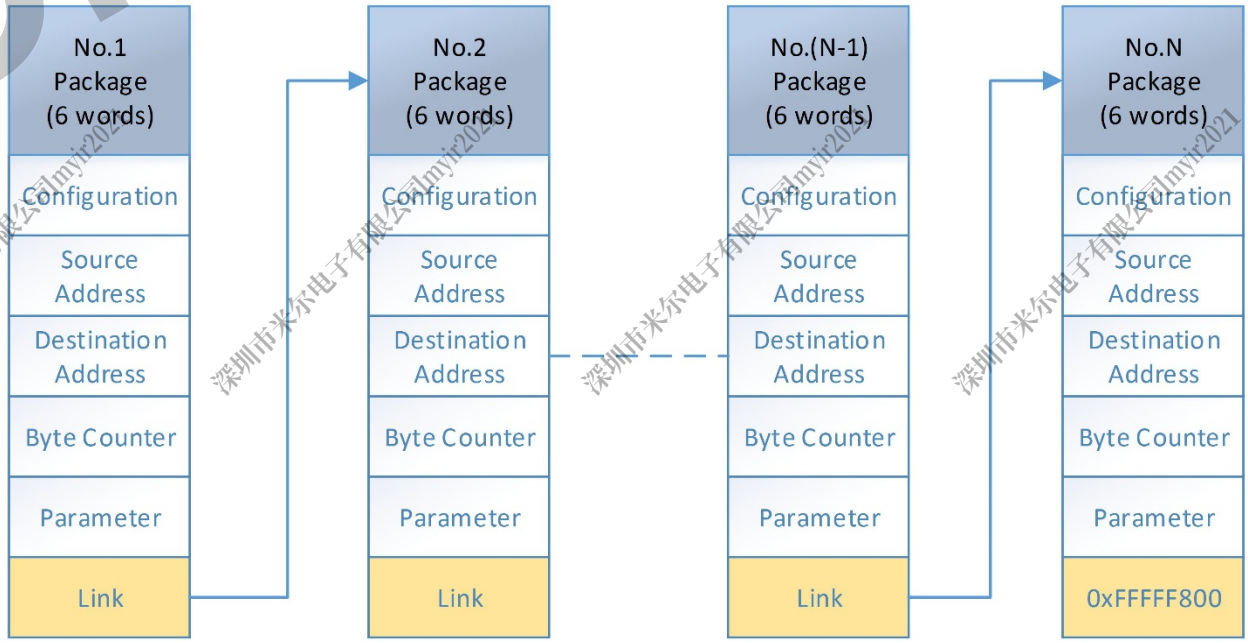
- **Parameter**: Configure the interval between the data block. The parameter is valid for non-memory peripherals. When DMA detects that the DRQ is high, the DMA transfers the data block and ignores the status changes of the DRQ until the data transfer finishes. After that, the DMA waits for certain clock cycles (WAIT_CYC) and executes the next DRQ detection. In addition, the Parameter is responsible for enabling and configuring TIMEOUT. In the case that the source device is an I/O device and the destination device is a memory device, the waiting time of a DRQ signal triggered by the source device can be set when TIMEOUT is enabled. When time is out, an interrupt signal of TIMEOUT will be generated by DMA. There are three sub-functions of TIMEOUT to be enabled (TIMEOUT will only generate interrupts if they are disabled): suspend the transmission of the current channel after an interrupt is generated; end the transmission of the current channel after an interrupt is generated; skip to the next descriptor for transmission after an interrupt is generated. (TIMEOUT only can be enabled in BMODE.)

  The Parameter also configures whether the IOspeed is enabled or not. If IOspeed is enabled, DMA will transmit the data of the I/O device from the source device or the destination device, or both of them at a faster speed. The larger block indicates a faster speed. However, when the block is 1, the speed won't change a lot even if the IO speed is enabled.

- **Link**: If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. The DMAC will stop the data transfer after transferring the package; otherwise, the value of the link is considered as the descriptor address of the next package.

Figure 2-13 DMA Chain Transfer



2.8.3.5 Interrupts

There are four kinds of DMA interrupts: the half package interrupt, package end interrupt, and queue end interrupt.

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- Half package interrupt

When enabled, the DMAC sends out a half package interrupt after transferring half of a package.

- Package end interrupt

When enabled, the DMAC sends out a package end interrupt after transferring a complete package.

- Queue end interrupt

When enabled, the DMAC sends out a queue end interrupt after transferring a complete queue.

- Timeout interrupt

When TIMEOUT is enabled, DMA will generate a timeout interrupt after timeout.

Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts are generated very closely, the later interrupt may override the former one. That is, from the perspective of the CPU, the DMAC has only a system interrupt source.

2.8.3.6 Clock Gating

The DMA_CLK_GATE module is a hardware module for controlling the clock gating automatically. It provides clock sources for sub-modules in DMAC and the module local circuits.

The DMA_CLK_GATE module consists of two parts: the channel clock gate and the common clock gate.

Channel clock gate: Controls the DMA clock of the DMA channels. When the system accesses the register of the current DMA channel and the DMA channel is enabled, the channel clock gate automatically opens the DMA clock. With a 16-HCLK-cycle delay after the system finishes accessing the register or the DMA data transfer is completed, the channel clock gate automatically closes the DMA clock. Also, the clock for the related circuits, such as for the channel control and FIFO control modules, will be closed.

Common clock gate: Controls the clocks of the DMA common circuits. The common circuits include the common circuit of the FIFO control module, MPORT module, and MBUS. When all the DMA channels are disabled, the common clock gate automatically closes the clocks for the above circuits.

The DMA clock gating can support all the functions stated above or not by software.

2.8.3.7 Transfer Mode

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC. After receiving the request signal, the DMAC converts it to the internal DRQ signal and controls the DMA data transfer.

The DMAC supports two data transfer modes: the waiting mode and handshake mode.

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The principle of waiting mode

- When the DMAC detects a valid external request signal, the DMAC starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ pulls low automatically.
- The internal DRQ holds low for certain clock cycles (WAIT_CYC), and then the DMAC restarts to detect the external requests. If the external request signal is valid, then the next transfer starts.

The principle of handshake mode

- When the DMAC detects a valid external request signal, the DMAC starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ will be pulled down automatically. For the last data transfer of the block, the DMAC sends a DMA Last signal with the DMA commands to the peripheral device. The DMA Last signal will be packed as part of the DMA commands and transmitted on the bus. It is used to inform the peripheral device that it is the end of the data transfer for the current DRQ.
- When the peripheral device receives the DMA Last signal, it can judge that the data transfer for the current DRQ is finished. To continue the data transfer, it sends a DMA Active signal to the DMAC.

NOTE

One DMA Active signal will be converted to one DRQ signal in the DMA module. To generate multiple DRQs, the peripheral device needs to send out multiple DMA Active signals via the bus protocol.

- When the DMAC received the DMA Active signal, it sends back a DMA ACK signal to the peripheral device.
- When the peripheral device receives the DMA ACK signal, it waits for all the operations on the local device completed, and both the FIFO and DRQ status refreshed. Then it invalidates the DMA Active signal.
- When the DMAC detects the falling edge of the DMA Active signal, it invalidates the corresponding DMA ACK signal, and restarts to detect the external request signals. If a valid request signal is detected, the next data transfer starts.

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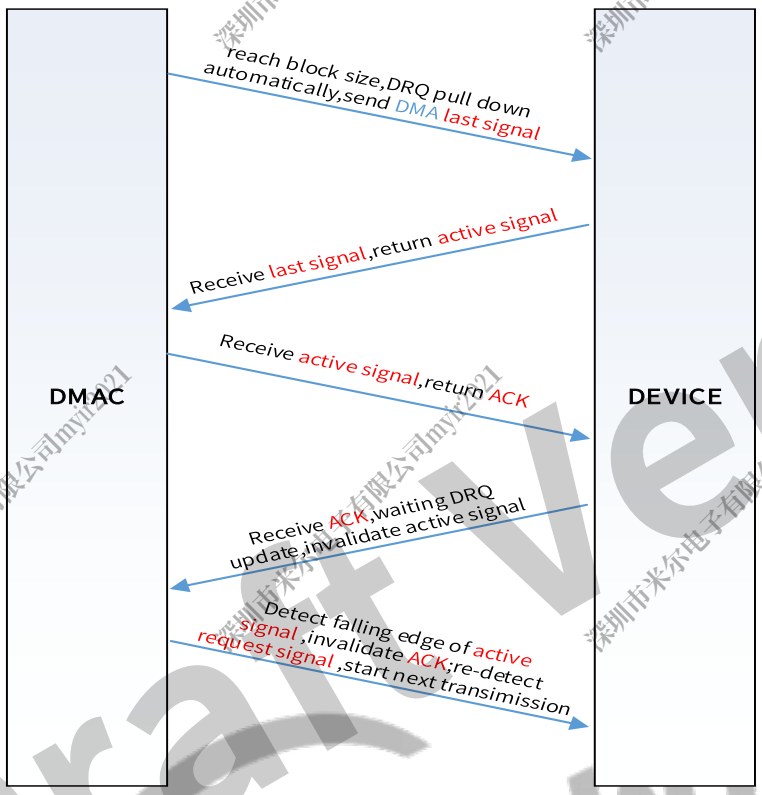
The following figure shows the workflow of the handshake mode.

Figure 2-14 Workflow of the DMAC Handshake Mode



2.8.3.8 Address Auto-Alignment

For the non-IO devices whose start address is not 32-byte-aligned, the DMAC will adjust the address to 32-byte-aligned through the burst transfer within 32 bytes. Adjusting address to 32-byte-aligned improves the DRAM access efficiency.

The following example shows how the DMAC adjusts the address: when the peripheral device of a DMA channel is a non-IO device whose start address is 0x86 (not 32-byte-aligned), the DMAC firstly uses a 26-byte burst transfer to align the address to 0xA0 (32-byte-aligned), and then transfers data by 64-byte burst (the maximum transfer amount that MBUS allows).

The IO devices do not support address alignment, so the bit width of IO devices must match the address offset; otherwise, the DMAC will ignore the inconsistency and directly transmit data of the corresponding bit width to the address.

The address of the DMA descriptor does not support the address auto-alignment. Make sure the address is word-aligned; otherwise the DMAC cannot identify the descriptor.

2.8.3.9 DMAC Clock Control

- The DMAC clock is synchronous with the AHB clock. Make sure that the DMAC gating bit of AHB clock is enabled before accessing the DMAC register.

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- The reset input signal of the DMAC is asynchronous with AHB and is low valid by default. Make sure that the reset signal of the DMAC is de-asserted before accessing the DMA register.
- To avoid the indefinite state within registers, de-assert the reset signal first, and then open the gating bit of AHB.
- The DMAC supports Clock Auto Gating function to reduce power consumption, the system will automatically disable the DMAC clock in the DMAC idle state. Clock Auto Gating is enabled by default.

2.8.4 Programming Guidelines

2.8.4.1 Using DMAC Transfer Process

The DMAC transfer process is as follows.

Step 1 Configure DMAC_IRQ_CPU_EN_REG register and DMAC_IRQ_DSP_EN_REG register to select whether the channel interrupt siganl is transferred to CPU field or DSP field. If both of the two registers are not configured, the IRQ will be transferred to both CPU field and DSP field by default.

Step 2 Request DMA channel, and check if the DMA channel is idle by checking if it is enabled. A disabled channel indicates it is idle, while an enabled channel indicates it is busy.

Step 3 Write the descriptor with 6 words into the memory. The descriptor must be word-aligned. For more details, refer to section 2.8.3.4 DMA Descriptor.

Step 4 Write the start address of the descriptor to DMAC_DESC_ADDR_REG.

Step 5 Enable the DMA channel, and write the corresponding channel to DMAC_EN_REG.

Step 6 The DMA obtains the descriptor information.

Step 7 Start to transmit a package. When half of the package is completed, the DMA sends a Half Package Transfer Interrupt; when a total package is completed, the DMA sends a Package End Transfer Interrupt. This interrupt status can be read by DMAC_IRQ_PEND_REG0.

Step 8 Set DMAC_PAU_REG to pause or resume the data transfer.

Step 9 After completing a total package transfer, the DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; otherwise, the next package starts to transmit. When the transfer ends, the DMA sends a Queue End Transfer Interrupt.

Step 10 Disable the DMA channel.

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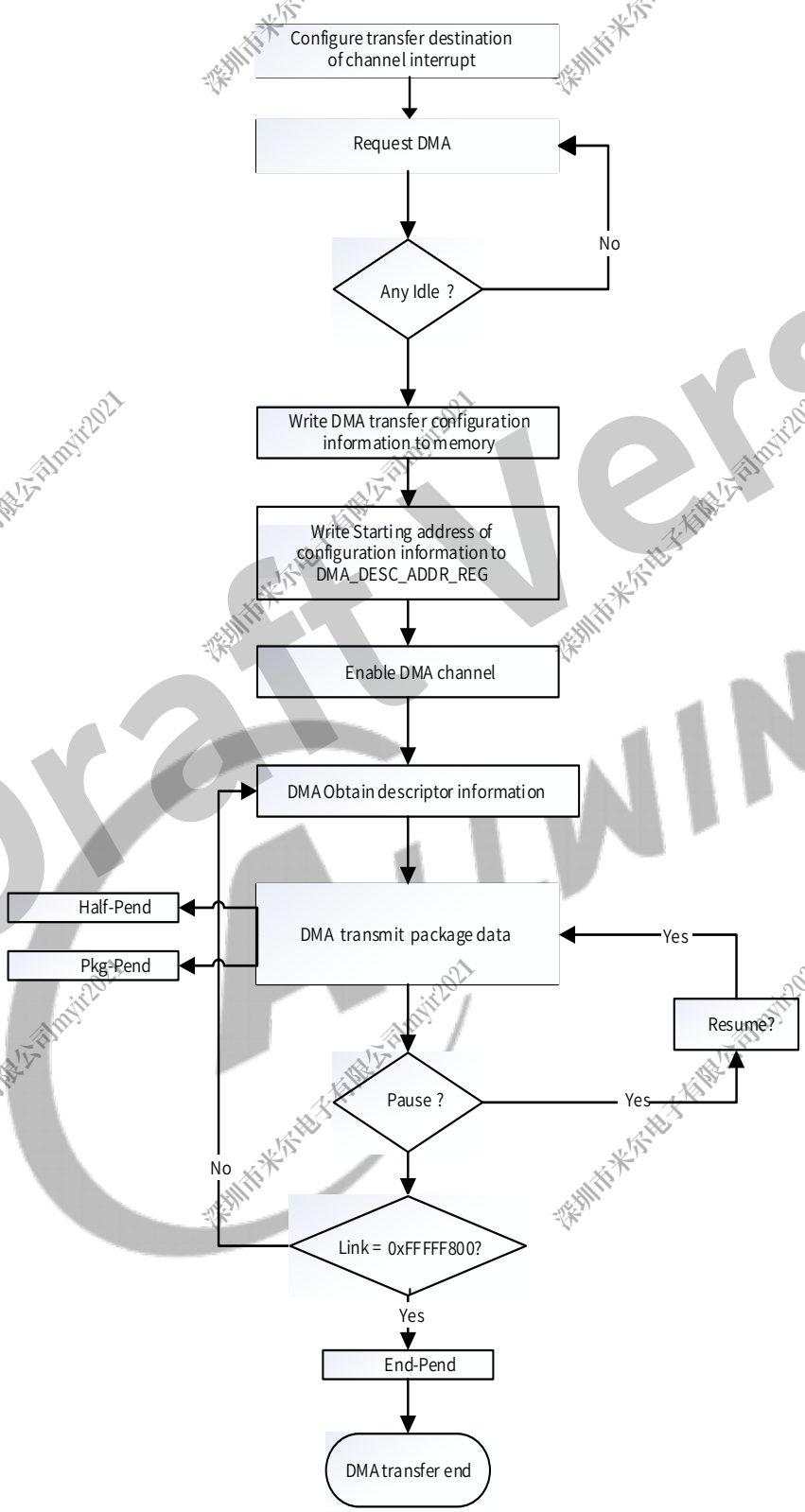
Figure 2-15 DMAC Transfer Process



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2.8.4.2 Processing DMAC Interrupt

Follow the steps below to process the DMAC interrupt:

Step 1 Enable interrupt: write the corresponding interrupt enable bit of DMAC_IRQ_EN_REG0. The system generates an interrupt when the corresponding condition is satisfied.

Step 2 After entering the interrupt process, write to clear the interrupt pending and execute the process of waiting for the interrupt.

Step 3 Resume the interrupt and continue to execute the interrupted process.

2.8.4.3 Configuring DMAC

To configure the DMAC, follow the guidelines below:

- Make sure the transfer bit width of IO devices is consistent with the offset of the start address.
- The MBUS protocol does not support the read operation of non-integer words. For the devices whose bit width is not word-aligned, after receiving the read command, they should resolve the read command according to their FIFO bit width instead of the command bit width, and ignore the redundant data caused by the inconsistency of the bit width.
- When the DMA transfer is paused, this is equivalent to invalid DRQ. Because there is a certain time delay between DMA transfer commands, the DMAC will not stop data transfer until the DMAC finishes processing the current command and the commands in Arbiter (at most 128 bytes' data).
- IOspeed and BMODE cannot be enabled at the same time.
- When IOspeed is enabled, the waiting cycle is recommended to be set to 1 in the waiting mode. (The waiting cycle cannot be larger than 32)
- As DMA will transmit interrupts to DMAC_IRQ_CPU_EN_REG and DMAC_IRQ_DSP_EN_REG by default simultaneously, it should be configured which one receives interrupts before transmission, and the other one ought to be disabled.
- Timeout Programming Instruction
  - Similar to the register configuration of other channels, configure by descriptors and read through registers.
  - Enable BMODE before using TIMEOUT functions.
  - The stop, pause, and jump functions of TIMEOUT cannot be enabled at the same time.
  - Before enabling TIMEOUT functions, if the source device configures the descriptor Config [7:6] as 0, set the DMAC_MODE_REG [4] as 1, and then start the DMA transfer.
  - After enabling the pause function of TIMEOUT, resume the data transfer by configuring the DMAC_PAU_REG.

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- After enabling the stop function of TIMEOUT, when TIMEOUT generates an interrupt, DMA will not generate the interrupt end signal of package and write-back. To restart the channel, configure the descriptors again.
- After enabling the jump function of TIMEOUT, when TIMEOUT generates an interrupt, DMA will not generate the interrupt end signal of package and write-back but skip to the next descriptor. Whether to start the TIMEOUT functions is decided by the descriptor being executed at that time. If there is no descriptor, transmission ends.
- The entered count number= the time to be counted * clock frequency (DMA clock frequency)/4096
- Take an example of 200MHz clock frequency for DMA. If the step size of timer is 20.48 us, and the maximum count is 511, the longest counting time will be the maximum count*step size=10.46 ms, and the shortest counting time will be 1*step size=20.48 us.

DMAC application example:

```
writel(0x00000000, mem_address + 0x00);  //Set configurations. The mem_address must be word-aligned.
writel (0x00001000, mem_address + 0x04);   // Set the start address for the source device.
writel (0x20000000, mem_address + 0x08);  //Set the start address for the destination device.
writel (0x00000020, mem_address + 0x0C);  // Set the data package size.
writel (0x00000000, mem_address + 0x10);  //Set the parameters.
writel (0xFFFFF800, mem_address + 0x14);  //Set the start address for the next descriptor.
writel (mem_address, 0x03002000+ 0x100 + 0x08); //Set the start address for the DMA channel0 descriptor.
do {
if (mem_address == readl (0x03002000+ 0x100 + 0x08));
break;
} while (1);            //Make sure that the writing operation is valid.
writel (0x000000001, 0x03002000+ 0x100 + 0x00);     // Enable DMA channel0 transfer.
```

The DMAC supports increasing data package in transfer, pay attention to the following points:

- The 0xFFFFF800 value of DMAC_FDESC_ADDR_REG indicates that the DMA channel has got back the descriptor of the last package. The DMA channel will automatically stop the data transfer after transferring the current package.
- To add a package during the data transfer, check if the DMA channel has got back the descriptor of the last package. If yes, you cannot add any package in the current queue. Request another DMA channel with a new DRQ to transfer the package. Otherwise, you can add the package by modifying the DMAC_FDESC_ADDR_REG of the last package from 0xFFFFF800 to the start address of the to-be-added package.

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To ensure that the modification is valid, read the value of DMAC_FDESC_ADDR_REG after the modification. The value 0xFFFFF800 indicates the modification fails and the other values indicate you have successfully added packages to the queue.

Another problem is, the system needs some time to process the modification, during which the DMA channel may get back the descriptor of the last package. You can read DMAC_CUR_SRC_REG and DMAC_CUR_DEST_REG and check if the increasing memory address accords with the information of the added package. If yes, the package is added successfully; otherwise, the modification failed.

To ensure a higher rate of success, it is suggested that you add the package before the half package interrupt of the penultimate package.

2.8.5 Register List

Module Name	Base Address	Comments
DMAC	0x0300 2000	
DSP_DMAC	0x0712 1000	DSP_DMAC register is the same with DMAC

Register Name	Offset	Description
DMAC_IRQ_EN_REG0	0x0000	DMAC IRQ Enable Register 0
DMAC_IRQ_EN_REG1	0x0004	DMAC IRQ Enable Register 1
DMAC_IRQ_PEND_REG0	0x0010	DMAC IRQ Pending Status Register 0
DMAC_IRQ_PEND_REG1	0x0014	DMAC IRQ Pending Status Register 1
DMAC_SEC_REG	0x0020	DMAC Security Register
DMAC_AUTO_GATE_REG	0x0028	DMAC Auto Gating Register
DMAC_STA_REG	0x0030	DMAC Status Register
DMAC_IRQ_CPU_EN_REG	0x0034	DMAC IRQ Transfer to CPU Field Enable Register
DMAC_IRQ_DSP_EN_REG	0x0038	DMAC IRQ Transfer to DSP Field Enable Register
DMAC_EN_REG	0x0100+N*0x0040 (N=0-15)	DMAC Channel Enable Register
DMAC_PAU_REG	0x0104+N*0x0040 (N=0-15)	DMAC Channel Pause Register
DMAC_DESC_ADDR_REG	0x0108+N*0x0040 (N=0-15)	DMAC Channel Descriptor Address Register
DMAC_CFG_REG	0x010C+N*0x0040 (N=0-15)	DMAC Channel Configuration Register
DMAC_CUR_SRC_REG	0x0110+N*0x0040 (N=0-15)	DMAC Channel Current Source Address Register
DMAC_CUR_DEST_REG	0x0114+N*0x0040 (N=0-15)	DMAC Channel Current Destination Address Register

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Register Name	Offset	Description
DMAC_BCNT_LEFT_REG	0x0118+N*0x0040 (N=0-15)	DMAC Channel Byte Counter Left Register
DMAC_PARA_REG	0x011C+N*0x0040 (N=0-15)	DMAC Channel Parameter Register
DMAC_MODE_REG	0x0128+N*0x0040 (N=0-15)	DMAC Mode Register
DMAC_FDESC_ADDR_REG	0x012C+N*0x0040 (N=0-15)	DMAC Former Descriptor Address Register
DMAC_PKG_NUM_REG	0x0130+N*0x0040 (N=0-15)	DMAC Package Number Register

2.8.6 Register Description

2.8.6.1 0x0000 DMAC IRQ Enable Register 0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA7_TIMEOUT_IRQ_EN DMA 7 Timeout Interrupt Enable. 0: Disable 1: Enable
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	R/W	0x0	DMA6_TIMEOUT_IRQ_EN DMA 6 Timeout Interrupt Enable. 0: Disable 1: Enable
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	R/W	0x0	DMA5_TIMEOUT_IRQ_EN DMA 5 Timeout Interrupt Enable. 0: Disable 1: Enable
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	R/W	0x0	DMA4_TIMEOUT_IRQ_EN DMA 4 Timeout Interrupt Enable. 0: Disable 1: Enable
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	DMA3_TIMEOUT_IRQ_EN DMA 3 Timeout Interrupt Enable. 0: Disable 1: Enable
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	R/W	0x0	DMA2_TIMEOUT_IRQ_EN DMA 2 Timeout Interrupt Enable. 0: Disable 1: Enable
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	R/W	0x0	DMA1_TIMEOUT_IRQ_EN DMA 1 Timeout Interrupt Enable. 0: Disable 1: Enable
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	R/W	0x0	DMA0_TIMEOUT_IRQ_EN DMA 0 Timeout Interrupt Enable. 0: Disable 1: Enable
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

2.8.6.2 0x0004 DMAC IRQ Enable Register 1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA15_TIMEOUT_IRQ_EN DMA 15 Timeout Interrupt Enable. 0: Disable 1: Enable
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	R/W	0x0	DMA14_TIMEOUT_IRQ_EN DMA 14 Timeout Interrupt Enable. 0: Disable 1: Enable
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	R/W	0x0	DMA13_TIMEOUT_IRQ_EN DMA 13 Timeout Interrupt Enable. 0: Disable 1: Enable
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	R/W	0x0	DMA12_TIMEOUT_IRQ_EN DMA 12 Timeout Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	DMA12_QUEUE_IRQ_EN DMA 12 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	R/W	0x0	DMA11_TIMEOUT_IRQ_EN DMA 11 Timeout Interrupt Enable. 0: Disable 1: Enable
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	R/W	0x0	DMA10_TIMEOUT_IRQ_EN DMA 10 Timeout Interrupt Enable. 0: Disable 1: Enable
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	R/W	0x0	DMA9_TIMEOUT_IRQ_EN DMA 9 Timeout Interrupt Enable. 0: Disable 1: Enable
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA9 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA9 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA9 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	R/W	0x0	DMA8_TIMEOUT_IRQ_EN DMA 8 Timeout Interrupt Enable. 0: Disable 1: Enable
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

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2.8.6.3 0x0010 DMAC IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMA7_TIMEOUT_IRQ_PEND DMA 7 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	R/W1C	0x0	DMA6_TIMEOUT_IRQ_PEND DMA 6 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	R/W1C	0x0	DMA5_TIMEOUT_IRQ_PEND DMA 5 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	R/W1C	0x0	DMA4_TIMEOUT_IRQ_PEND DMA 4 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	R/W1C	0x0	DMA3_TIMEOUT_IRQ_PEND DMA 3 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
11	R/W1C	0x0	DMA2_TIMEOUT_IRQ_PEND DMA 2 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	R/W1C	0x0	DMA1_TIMEOUT_IRQ_PEND DMA 1 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	R/W1C	0x0	DMA0_TIMEOUT_IRQ_PEND DMA 0 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

2.8.6.4 0x0014 DMAC IRQ Pending Status Register 1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMA15_TIMEOUT_IRQ_PEND DMA 15 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND. DMA 15 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_PEND DMA 15 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	R/W1C	0x0	DMA14_TIMEOUT_IRQ_PEND DMA 14 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_PEND DMA 14 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	R/W1C	0x0	DMA13_TIMEOUT_IRQ_PEND DMA 13 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA13_PKG_IRQ_PEND DMA 13 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND. DMA 13 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	R/W1C	0x0	DMA12_TIMEOUT_IRQ_PEND DMA 12 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_PEND DMA 12 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	R/W1C	0x0	DMA11_TIMEOUT_IRQ_PEND DMA 11 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
11	R/W1C	0x0	DMA10_TIMEOUT_IRQ_PEND DMA 10 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_PEND DMA 10 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	R/W1C	0x0	DMA9_TIMEOUT_IRQ_PEND DMA 9 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_PEND DMA 9 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	R/W1C	0x0	DMA8_TIMEOUT_IRQ_PEND DMA 8 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA8 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_PEND DMA 8 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA8 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

2.8.6.5 0x0020 DMAC Security Register (Default Value: 0x0000_FFFF)

Offset: 0x0020			Register Name: DMAC_SEC_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_SEC DMA channel 15 security. 0: Secure, 1: Non-secure.
14	R/W	0x1	DMA14_SEC DMA channel 14 security. 0: Secure, 1: Non-secure.
13	R/W	0x1	DMA13_SEC DMA channel 13 security. 0: Secure, 1: Non-secure.
12	R/W	0x1	DMA12_SEC DMA channel 12 security. 0: Secure, 1: Non-secure.

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Offset: 0x0020			Register Name: DMAC_SEC_REG
Bit	Read/Write	Default/Hex	Description
11	R/W	0x1	DMA11_SEC DMA channel 11 security. 0: Secure, 1: Non-secure.
10	R/W	0x1	DMA10_SEC DMA channel 10 security. 0: Secure, 1: Non-secure.
9	R/W	0x1	DMA9_SEC DMA channel 9 security. 0: Secure, 1: Non-secure.
8	R/W	0x1	DMA8_SEC DMA channel 8 security. 0: Secure, 1: Non-secure.
7	R/W	0x1	DMA7_SEC DMA channel 7 security. 0: Secure, 1: Non-secure.
6	R/W	0x1	DMA6_SEC DMA channel 6 security. 0: Secure, 1: Non-secure.
5	R/W	0x1	DMA5_SEC DMA channel 5 security. 0: Secure, 1: Non-secure.
4	R/W	0x1	DMA4_SEC DMA channel 4 security. 0: Secure, 1: Non-secure.
3	R/W	0x1	DMA3_SEC DMA channel 3 security. 0: Secure, 1: Non-secure.
2	R/W	0x1	DMA2_SEC DMA channel 2 security. 0: Secure, 1: Non-secure.

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Offset: 0x0020			Register Name: DMAC_SEC_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	DMA1_SEC DMA channel 1 security. 0: Secure, 1: Non-secure.
0	R/W	0x1	DMA0_SEC DMA channel 0 security. 0: Secure, 1: Non-secure.

2.8.6.6 0x0028 DMAC Auto Gating Register (Default Value: 0x00000000)

Offset: 0x0028			Register Name: DMAC_AUTO_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, bit-2 should be set up.

2.8.6.7 0x0030 DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: DMAC_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0	MBUS_FIFO_STATUS MBUS FIFO Status 0: Empty 1: Not Empty

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Offset: 0x0030			Register Name: DMAC_STA_REG
Bit	Read/Write	Default/Hex	Description
30:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy

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Offset: 0x0030			Register Name: DMAC_STA_REG
Bit	Read/Write	Default/Hex	Description
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle 1: Busy

2.8.6.8 0x0034 DMAC IRQ Transfer to CPU Field Enable Register (Default Value: 0x0000_FFFF)

Offset: 0x0034			Register Name: DMAC_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_IRQ_CPU_EN Control whether the DMA Channel 15 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
14	R/W	0x1	DMA14_IRQ_CPU_EN Control whether the DMA Channel 14 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field

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Offset: 0x0034			Register Name: DMAC_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
13	R/W	0x1	DMA13_IRQ_CPU_EN Control whether the DMA Channel 13 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
12	R/W	0x1	DMA12_IRQ_CPU_EN Control whether the DMA Channel 12 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
11	R/W	0x1	DMA11_IRQ_CPU_EN Control whether the DMA Channel 11 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
10	R/W	0x1	DMA10_IRQ_CPU_EN Control whether the DMA Channel 10 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
9	R/W	0x1	DMA9_IRQ_CPU_EN Control whether the DMA Channel 9 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
8	R/W	0x1	DMA8_IRQ_CPU_EN Control whether the DMA Channel 8 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
7	R/W	0x1	DMA7_IRQ_CPU_EN Control whether the DMA Channel 7 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
6	R/W	0x1	DMA6_IRQ_CPU_EN Control whether the DMA Channel 6 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field

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Offset: 0x0034			Register Name: DMAC_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	DMA5_IRQ_CPU_EN Control whether the DMA Channel 5 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
4	R/W	0x1	DMA4_IRQ_CPU_EN Control whether the DMA Channel 4 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
3	R/W	0x1	DMA3_IRQ_CPU_EN Control whether the DMA Channel 3 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
2	R/W	0x1	DMA2_IRQ_CPU_EN Control whether the DMA Channel 2 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
1	R/W	0x1	DMA1_IRQ_CPU_EN Control whether the DMA Channel 1 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
0	R/W	0x1	DMA0_IRQ_CPU_EN Control whether the DMA Channel 0 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field

2.8.6.9 0x0038 DMAC IRQ Transfer to DSP Field Enable Register (Default Value: 0x0000_FFFF)

Offset: 0x0038			Register Name: DMAC_IRQ_DSP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0038			Register Name: DMAC_IRQ_DSP_EN_REG
Bit	Read/Write	Default/Hex	Description
15	R/W	0x1	DMA15_IRQ_DSP_EN Control whether the DMA Channel 15 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
14	R/W	0x1	DMA14_IRQ_DSP_EN Control whether the DMA Channel 14 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
13	R/W	0x1	DMA13_IRQ_DSP_EN Control whether the DMA Channel 13 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
12	R/W	0x1	DMA12_IRQ_DSP_EN Control whether the DMA Channel 12 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
11	R/W	0x1	DMA11_IRQ_DSP_EN Control whether the DMA Channel 11 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
10	R/W	0x1	DMA10_IRQ_DSP_EN Control whether the DMA Channel 10 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
9	R/W	0x1	DMA9_IRQ_DSP_EN Control whether the DMA Channel 9 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
8	R/W	0x1	DMA8_IRQ_DSP_EN Control whether the DMA Channel 8 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field

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Offset: 0x0038			Register Name: DMAC_IRQ_DSP_EN_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	DMA7_IRQ_DSP_EN Control whether the DMA Channel 7 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
6	R/W	0x1	DMA6_IRQ_DSP_EN Control whether the DMA Channel 6 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
5	R/W	0x1	DMA5_IRQ_DSP_EN Control whether the DMA Channel 5 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
4	R/W	0x1	DMA4_IRQ_DSP_EN Control whether the DMA Channel 4 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
3	R/W	0x1	DMA3_IRQ_DSP_EN Control whether the DMA Channel 3 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
2	R/W	0x1	DMA2_IRQ_DSP_EN Control whether the DMA Channel 2 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
1	R/W	0x1	DMA1_IRQ_DSP_EN Control whether the DMA Channel 1 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field
0	R/W	0x1	DMA0_IRQ_DSP_EN Control whether the DMA Channel 0 IRQ signal can transfer to DSP field or not. 0: can not transfer to DSP field 1: can transfer to DSP field

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2.8.6.10 0x0100+N*0x0040 (N=0-15) DMAC Channel Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0040 (N=0-15)			Register Name: DMAC_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

2.8.6.11 0x0104+N*0x0040 (N=0-15) DMAC Channel Pause Register (Default Value: 0x0000_0000)

Offset: 0x0104+N*0x0040 (N=0-15)			Register Name: DMAC_PAU_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

2.8.6.12 0x0108+N*0x0040 (N=0-15) DMAC Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0108+N*0x0040 (N=0-15)			Register Name: DMAC_DESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	DMA_DESC_LOW_ADDR DMA Channel Descriptor Word Address, Low 30bits. The Descriptor Address must be word-aligned.
1:0	R/W	0x0	DMA_DESC_HIGH_ADDR DMA Channel Descriptor High Address, High 2bits The real address is as below: DMA Channel Descriptor Address = {bit[1:0],bit[31:2],2'b00};

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2.8.6.13 0x010C+N*0x0040 (N=0-15) DMAC Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x010C+N*0x0040 (N=0-15)			Register Name: DMAC_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R	0x0	BMODE_SEL Mode select 0: Normal Mode 1: BMODE
29:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: Reserved
24	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: Reserved
8	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode

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Offset: 0x010C+N*0x0040 (N=0-15)			Register Name: DMAC_CFG_REG
Bit	Read/Write	Default/Hex	Description
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

2.8.6.14 0x0110+N*0x0040 (N=0-15) DMAC Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x0040 (N=0-15)			Register Name: DMAC_CUR_SRC_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

2.8.6.15 0x0114+N*0x0040 (N=0-15) DMAC Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset: 0x0114+N*0x0040 (N=0-15)			Register Name: DMAC_CUR_DEST_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

2.8.6.16 0x0118+N*0x0040 (N=0-15) DMAC Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset: 0x0118+N*0x0040 (N=0-15)			Register Name: DMAC_BCNT_LEFT_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

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2.8.6.17 0x011C+N*0x0040 (N=0-15) DMAC Channel Parameter Register (Default Value: 0x0000_0000)

NOTE

- The entered count number (bit [28:20], this number needs to be integer) = the time to be counted * clock frequency (DMA clock frequency)/4096
- Take an example of 200MHz clock frequency for DMAC. If the step size of timer is 20.48 us, the longest counting time will be the maximum count*step size=10.46 ms.

Offset: 0x011C+N*0x0040 (N=0-15)			Register Name: DMAC_PARA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_TO_EN. Timeout Function Enable Bit 1: Enable 0: Disable
30:29	R	0x0	DMA_TO_FUN. Timeout Function Configuration 01: Enabling pause channel transfer function after timeout 10: Enabling stop channel transfer function after timeout 11: Enabling jump next opcode function after timeout
28:20	R	0x0	DMA_TO_WAIT_CYC. The time cycle of waiting the start device to restart transferring data.
19:18	R	0x0	DMA Channel Current Destination Address[33:32], Read only.
17:16	R	0x0	DMA Channel Current Source Address[33:32], read only.
15:9	/	/	/
8	R	0x0	DMA_IOSPEED_EN. Accelerating DMA speed when transferring the data of IO device 1: Enable 0: Disable
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

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2.8.6.18 0x0128+N*0x0040 (N=0-15) DMAC Mode Register (Default Value: 0x0000_0000)

Offset: 0x0128+N*0x0040 (N=0-15)			Register Name: DMAC_MODE_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	LAG_TIME_MODE In wait mode, enabling this bit, DMA will not timing wait cycle until DMA receive or transmit data successfully. It's recommend to enable this bit before using DMA when the DMA has enable more than one channel which access IO and memory equipment. 0: disable 1: enable
4	R/W	0x0	DMA_BLOCK_ZERO_EN Enable pre-read source DRQ when source block is configured 0. It needs to disable when opening timeout sub function (DMA Channel Parameter Register [30:29] =01, 10 or 11) and source block is configured 0. 0: enable 1: disable
3	R/W	0x0	DMA_DST_MODE. Destination communication Mode Select 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. Source communication Mode Select 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

2.8.6.19 0x012C+N*0x0040 (N=0-15) DMAC Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x012C+N*0x0040 (N=0-15)			Register Name: DMAC_FDESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to storing the former value of DMA Channel Descriptor Address Register.

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2.8.6.20 0x0130+N*0x0040 (N=0-15) DMAC Package Number Register (Default Value: 0x0000_0000)

Offset: 0x0130+N*0x0040 (N=0-15)			Register Name: DMAC_PKG_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

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2.9 Generic Interrupt Controller (GIC)

2.9.1 Overview

The GIC-600 is a generic interrupt controller that handles interrupts from peripherals to the cores and interrupts between cores. The GIC-600 supports a distributed microarchitecture containing several individual blocks that are used to provide a flexible GIC implementation.

All the GIC-600 blocks communicate through fully credited AXI4-Stream interface channels. This means that the interface exerts transient backpressure only on their ic<xy>tready signals, enabling packets to be routed over any free-flowing interconnect. Channels can be routed over dedicated AXI4-Stream buses, or over any available free-flowing transport layer in the system. A channel is described as free-flowing if all transactions on that channel complete without a non-transient dependency on any other transaction.

The GIC-600 includes build scripts that can create appropriate levels of hierarchy for any particular configuration. In small configurations, the distribution can be hidden and internally optimized.

the GIC has the following features:

- Interrupt services and masking:
  - Supports the following interrupt types:
    - Up to 56000 LPIs. A peripheral generates these interrupts by writing to a memory-mapped register in the GIC-600.
    - Up to 960 SPIs in groups of 32.
    - Up to 16 PPIs that are independent for each core and can be programmed to support either edge triggered or level-sensitive interrupts.
    - Up to 16 SGIs that are generated through the GIC CPU interface of a core.
  - Up to 16 ITS modules that provide device isolation and ID translation for message-based interrupts and enable virtual machines to program devices directly.
  - Interrupt masking and prioritization with 32 priority levels, five bits per interrupt.
- Registers and programming
  - Flexible affinity routing, using the Multiprocessor Identification Register (MPIDR) addresses, including support for all four affinity levels.
  - Single ACE-Lite slave port on each chip for programming of all GIC Distributor (GICD) registers, GIC Interrupt Translation Service (GITS) registers, and GIC Redistributor (GICR) registers. Each ITS has an optional ACE-Lite slave port for programming the GITS_TRANSLATER register.
  - Coherent view of SPI register data across multiple chips.
- Security
  - A global Disable Security (DS) bit. This bit enables support for systems without security.
  - The following interrupt groups allow interrupts to target different exception levels:

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- Group 0.
- Non-secure Group 1.
- Secure Group 1.

- Performance Monitoring Unit (PMU) counters with snapshot functionality.
- Error correction: ARMv8.2 Reliability Accessibility Serviceability (RAS) architecture-compliant error reporting for the following:
  - Software access errors
  - ITS command and translation errors
  - Error Correcting Code (ECC) errors

2.9.2 Functional Description

the following table describes the details of interrupt sources:

Table 2-15 Interrupt Source in CPUX Domain

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	CPUX_MSGBOX_R	0x0080	CPUX MSGBOX read IRQ for CPUX
33	CPUS _MSGBOX_W	0x0084	CPUS MSGBOX write IRQ for CPUX
34	UART0	0x0088	
35	UART1	0x008C	
36	UART2	0x0090	
37	UART3	0x0094	
38	UART4	0x0098	
39	UART5	0x009C	
40	UART6	0x00A0	
41	UART7	0x00A4	
42	TWI0	0x00A8	
43	TWI1	0x00AC	
44	TWI2	0x00B0	
45	TWI3	0x00B4	
46	TWI4	0x00B8	
47	TWI5	0x00BC	
48	SPI0	0x00C0	
49	SPI1	0x00C4	
50	SPI2	0x00C8	
51	PWMCTRL0	0x00CC	
52	SPIFC	0x00D0	
53		0x00D4	
54		0x00D8	
55		0x00DC	
56		0x00E0	
57		0x00E4	
58	CIR_TX	0x00E8	
59	CIR_RX	0x00EC	
60	LEDC	0x00F0	
61	USB0_DEVICE	0x00F4	
62	USB0_EHCI	0x00F8	
63	USB0_OHCI	0x00FC	
64	USB1_EHCI	0x0100	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
65	USB1_OHCI	0x0104	
66		0x0108	
67	USB2/USB3	0x010C	
68		0x0110	
69		0x0114	
70	NDFC	0x0118	
71	THS0	0x011C	
72	SMHC0	0x0120	
73	SMHC1	0x0124	
74	SMHC2	0x0128	
75	NSI	0x012C	
76	SMC	0x0130	
77		0x0134	
78	GMAC0	0x0138	
79	GMAC1	0x013C	
80	CCU_FERR	0x0140	
81	AHB_HREADY_TIME_OUT	0x0144	
82	DMAC_CPUX_NS	0x0148	DMAC channel 0-15 non-secure interrupt
83	DMAC_ CPUX_S	0x014C	DMAC channel 0-15 secure interrupt
84	CE_NS	0x0150	
85	CE_S	0x0154	
86	SPINLOCK	0x0158	
87	CPUX_TIMER0	0x015C	
88	CPUX_TIMER1	0x0160	
89	CPUX_TIMER2	0x0164	
90	CPUX_TIMER3	0x0168	
91	CPUX_TIMER4	0x016C	
92	CPUX_TIMER5	0x0170	
93	GPADC_CTRL0	0x0174	
94	THS1	0x0178	
95	CPUX_WDT	0x017C	
96	GPADC_CTRL1	0x0180	
97	IOMMU	0x0184	
98	LRADC	0x0188	
99	GPIOA_NS	0x018C	
100	GPIOA_S	0x0190	
101	GPIOB_NS	0x0194	
102	GPIOB_S	0x0198	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
103	GPIOC_NS	0x019C	
104	GPIOC_S	0x01A0	
105	GPIOD_NS	0x01A4	
106	GPIOD_S	0x01A8	
107	GPIOE_NS	0x01AC	
108	GPIOE_S	0x01B0	
109	GPIOF_NS	0x01B4	
110	GPIOF_S	0x01B8	
111	GPIOG_NS	0x01BC	
112	GPIOG_S	0x01C0	
113	GPIOH_NS	0x01C4	
114	GPIOH_S	0x01C8	
115	GPIOI_NS	0x01CC	
116	GPIOI_S	0x01D0	
117	GPIOJ_NS	0x01D4	
118	GPIOJ_S	0x01D8	
119	DE	0x01DC	
120	DI	0x01E0	
121	HDMI_PHY	0x01E4	
122	TCON_LCD0	0x01E8	
123	TCON_TV0	0x01EC	
124	TCON_LCD1	0x01F0	
125	HDMI	0x01F4	
126	DSI0	0x01F8	
127	DSI1	0x01FC	
128	TCON_TV1	0x0200	
129	TCON_LCD2	0x0204	
130	PCIE_EDMA[0]	0x0208	
131	PCIE_EDMA[1]	0x020C	
132	PCIE_EDMA[2]	0x0210	
133	PCIE_EDMA[0]	0x0214	
134	PCIE_EDMA[4]	0x0218	
135	PCIE_EDMA[5]	0x021C	
136	PCIE_EDMA[6]	0x0220	
137	PCIE_EDMA[7]	0x0224	
138	PCIE_SII	0x0228	
139	PCIE_MSI	0x022C	
140	PCIE_EDMA[8]	0x0230	
141	PCIE_EDMA[9]	0x0234	
142	PCIE_EDMA[10]	0x0238	
143	PCIE_EDMA[11]	0x023C	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
144	PCIE_EDMA[12]	0x0240	
145	PCIE_EDMA[13]	0x0244	
146	PCIE_EDMA[14]	0x0248	
147	PCIE_EDMA[15]	0x024C	
148	GPU_EVENT	0x0250	
149	GPU_JOB	0x0254	
150	GPU_MMU	0x0258	
151	GPU	0x025C	
152	VE3	0x0260	
153	MEMC_DFS	0x0264	
154	CSI_DMA0	0x0268	
155	CSI_DMA1	0x026C	
156	CSI_DMA2	0x0270	
157	CSI_DMA3	0x0274	
158	CSI_VIPP0	0x0278	
159	CSI_VIPP1	0x027C	
160	CSI_VIPP2	0x0280	
161	CSI_VIPP3	0x0284	
162	CSI_PARSER0	0x0288	
163	CSI_PARSER1	0x028C	
164	CSI_PARSER2	0x0290	
165	CSI_ISP0	0x0294	
166	CSI_ISP1	0x0298	
167	CSI_ISP2	0x029C	
168	CSI_ISP3	0x02A0	
169	CSI_CMB	0x02A4	
170	CSI_TDM	0x02A8	
171	CSI_TOP_PKT	0x02AC	
172	GPIOK_NS	0x02B0	
173	GPIOK_S	0x02B4	
174	PWMCTRL1	0x02B8	
175	G2D	0x02BC	
176	EDP	0x02C0	
177	CSI_DMA4	0x02C4	
178	CSI_DMA5	0x02C8	
179	CSI_PARSER3	0x02CC	
180	NMI	0x02D0	
181	S_PPU	0x02D4	
182	S_PPU1	0x02D8	
183	TWD	0x02DC	
184	CPUS_WDT	0x02E0	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
185	CPUS_TIMER0	0x02E4	
186	CPUS_TIMER1	0x02E8	
187	CPUS_TIMER2	0x02EC	
188	S_TWI2	0x02F0	
189	ALARM	0x02F4	
190	GPIOL_S	0x02F8	
191	GPIOL_NS	0x02FC	
192	GPIOM_S	0x0300	
193	GPIOM_NS	0x0304	
194	S_UART0	0x0308	
195	S_UART1	0x030C	
196	S_TWI0	0x0310	
197	S_TWI1	0x0314	
198		0x0318	
199	S_CIRRX	0x031C	
200	S_PWMCTRL	0x0320	
201		0x0324	
202	AHBS_HREADY_TIME_OUT	0x0328	
203	CPUIDLE(PCK600_CPU)	0x032C	
204	S_SPI	0x0330	
205	S_SPINLOCK	0x0334	
206	CPUS_MSGBOX_CPUX	0x0338	
207		0x033C	
208		0x0340	
209		0x0344	
210	DSP_DEE	0x0348	
211	DSP_PFE	0x034C	
212	S_TWD	0x0350	
213	DSP_MSGBOX_CPUX	0x0354	
214		0x0358	
215		0x035C	
216		0x0360	
217	DSP_TIMER0	0x0364	
218	DSP_TIMER1	0x0368	
219	DSP_TIMER2	0x036C	
220	DSP_AHB0_TO	0x0370	
221	DSP_AHB1_TO	0x0374	
222	AUDIO CODEC	0x0378	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
223	DMIC	0x037C	
224	I2S0	0x0380	
225	I2S1D	0x0384	
226	I2S2	0x0388	
227	I2S3	0x038C	
228	OWA	0x0390	
229	DSP_DMAC_NS	0x0394	
230	DSP_DMAC_S	0x0398	
231	DSP_NPU	0x039C	
232		0x03A0	
233	DSP_TIMER3	0x03A4	
234	DSP_TIMER4	0x03A8	
235	DSP_TIMER5	0x03AC	
236	DSP_MSGBOX_RV_CPUS	0x03B0	
237	DSP_MSGBOX_RV_CPUX	0x03B4	
238	DSP_RISCV_WDT	0x03B8	
239	DSP_PWMCTRL	0x03BC	
240		0x03C0	
241		0x03C4	
242		0x03C8	
243		0x03CC	
244		0x03D0	
245		0x03D4	
246		0x03D8	
247		0x03DC	
248		0x03E0	
249		0x03E4	
250		0x03E8	
251		0x03EC	
252		0x03F0	
253		0x03F4	
254		0x03F8	
255		0x03FC	
CPUX Related			
256	nERRIRQ[0]	0x0400	L3 ECC error that causes potential data corruption or loss of coherency

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
257	nERRIRQ[1]	0x0404	Core0 ECC error that causes potential data corruption or loss of coherency
258	nERRIRQ[2]	0x0408	Core1 ECC error that causes potential data corruption or loss of coherency
259	nERRIRQ[3]	0x040C	Core2 ECC error that causes potential data corruption or loss of coherency
260	nERRIRQ[4]	0x0410	Core3 ECC error that causes potential data corruption or loss of coherency
261	nERRIRQ[5]	0x0414	Core4 ECC error that causes potential data corruption or loss of coherency
262	nERRIRQ[6]	0x0418	Core5 ECC error that causes potential data corruption or loss of coherency
263	nERRIRQ[7]	0x041C	Core6 ECC error that causes potential data corruption or loss of coherency
264	nERRIRQ[8]	0x0220	Core7 ECC error that causes potential data corruption or loss of coherency
265	nFAULTIRQ[0]	0x0424	L3 detected 1-bit or 2-bit ECC or Parity error in the RAMs
266	nFAULTIRQ[1]	0x0428	Core0 detected 1-bit or 2-bit ECC or Parity error in the RAMs
267	nFAULTIRQ[2]	0x042C	Core1 detected 1-bit or 2-bit ECC or Parity error in the RAMs

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
268	nFAULTIRQ[3]	0x0430	Core2 detected 1-bit or 2-bit ECC or Parity error in the RAMs
269	nFAULTIRQ[4]	0x0434	Core3 detected 1-bit or 2-bit ECC or Parity error in the RAMs
270	nFAULTIRQ[5]	0x0438	Core4 detected 1-bit or 2-bit ECC or Parity error in the RAMs
271	nFAULTIRQ[6]	0x043C	Core5 detected 1-bit or 2-bit ECC or Parity error in the RAMs
272	nFAULTIRQ[7]	0x0440	Core6 detected 1-bit or 2-bit ECC or Parity error in the RAMs
273	nFAULTIRQ[8]	0x0444	Core7 detected 1-bit or 2-bit ECC or Parity error in the RAMs
274	nCLUSTERPMUIRQ	0x0448	Cluster PMU interrupt request
275	GIC_FAULT_INT	0x044C	
276	GIC_ERR_INT	0x0450	
277	GIC_PMU_INT	0x0454	
278		0x0458	
279		0x045C	
280		0x0460	
281		0x0464	
282		0x0468	
283		0x046C	
284		0x0470	
285		0x0474	
286		0x0478	
287		0x047C	

2.9.3 Register List

Module Name	Base Address	Comments
GIC		
GIC600_MON_4	0x03400000	General interrupt controller(23*64KB)
GITS_TRANSLATER	0x03450000	

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NOTE

Offsets that are not shown are reserved and RAZ/WI. Accessing these offsets might be reported in error record 0 as a SYN_ACE_BAD access.

Register Name	Offset	Description
GICD_CTLR	0x00000	Distributor Control Register
GICD_TYPER	0x00004	Interrupt Controller Type Register
GICD_IIDR	0x00008	Distributor Implementer Identification Register
GICD_FCTLR	0x00020	Function Control Register
GICD_SAC	0x00024	Secure Access Control
GICD_SETSPI_NSR	0x00040	Non-secure SPI Set Register
GICD_CLRSPI_NSR	0x00048	Non-secure SPI Clear Register
GICD_CLRSPI_NSR	0x00050	Secure SPI Set Register
GICD_CLRSPI_SR	0x00058	Secure SPI Clear Register
GICD_IGROUPRn	0x4*N +0x00080 (N=0-31)	Interrupt Group Registers
GICD_ISENABLERn	0x4*N +0x00100 (N=0-31)	Interrupt Set-Enable Registers 0-N
GICD_ICENABLERn	0x4*N +0x00180 (N=0-31)	Interrupt Clear-Enable Registers 0-N
GICD_ISPENDRn	0x4*N +0x00200 (N=0-31)	Interrupt Set-Pending Registers
GICD_ICPENDRn	0x4*N +0x00280 (N=0-31)	Interrupt Clear-Pending Registers
GICD_ISACTIVERn	0x4*N +0x00300 (N=0-31)	Interrupt Set-Active Registers
GICD_ICACTIVERn	0x4*N +0x00380 (N=0-31)	Interrupt Clear-Active Registers
GICD_IPRIORITYRn	0x4*N +0x00400 (N=0-255)	Interrupt Priority Registers
GICD_ICFGRn	0x4*N +0x00C00 (N=0-63)	Interrupt Configuration Registers
GICD_IGRPMODRn	0x4*N +0x00D00 (N=0-63)	Interrupt Group Modifier Registers
GICD_NSACRn	0x4*N +0x00E00 (N=0-63)	Non-secure Access Control Registers
GICD_IROUTERn	0x8*N +0x06000 (N=32-1019)	Interrupt Routing Registers
GICD_CHIPSR	0x0C000	Chip Status Register
GICD_DCHIPR	0x0C004	Default Chip Register

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Register Name	Offset	Description
GICD_CHIPRn	0x4*N +0x0C000 (N=2-32)	Chip Registers
GICD_ICLARn	0x4*N +0x0E000 (N=2-63)	Interrupt Class Registers
GICD_IERRRn	0x4*N +0x0E100 (N=2-31)	Interrupt Error Registers
GICD_CFGID	0x0F000	Configuration ID Register
GICD_PIDR4	0x0FFD0	Peripheral ID4 Register
GICD_PIDR5	0x0FFD4	Peripheral ID5 Register
GICD_PIDR6	0x0FFD8	Peripheral ID6 Register
GICD_PIDR7	0x0FFDC	Peripheral ID7 Register
GICD_PIDR0	0x0FFE0	Peripheral ID0 Register
GICD_PIDR1	0x0FFE4	Peripheral ID1 Register
GICD_PIDR2	0x0FFE8	Peripheral ID2 Register
GICD_PIDR3	0x0FFEC	Peripheral ID3 Register
GICD_CIDR0	0x0FFF0	Component ID 0 Register
GICD_CIDR1	0x0FFF4	Component ID 1 Register
GICD_CIDR2	0x0FFF8	Component ID 2 Register
GICD_CIDR3	0x0FFFC	Component ID 3 Register
GICA_SETSPI_NSR	0x10040	Aliased Non-secure SPI Set Register
GICA_CLRSPI_NSR	0x10048	Aliased Non-secure SPI Clear Register
GICA_SETSPI_SR	0x10050	Aliased Secure SPI Set Register
GICA_CLRSPI_SR	0x10058	Aliased Secure SPI Clear Register
GICT_ERR<n>FR	0x10*N +0x20000 (N=0-2)	Error Record Feature Register
GICT_ERR<n>CTLR	0x10*N +0x20008 (N=0-2)	Error Record Control Register,
GICT_ERR<n>STATUS	0x10*N +0x20010 (N=0-2)	Error Record Primary Status Register
GICT_ERR<n>ADDR	0x10*N +0x20018 (N=0-2)	Error Record Address Register
GICT_ERR<n>MISC0	0x10*N +0x20020 (N=0-2)	Error Record Miscellaneous Register 0
GICT_ERR<n>MISC1	0x10*N +0x20028 (N=0-2)	Error Record Miscellaneous Register 1

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Register Name	Offset	Description
GICT_ERRGSR	0x2E000	Error Group Status Register,
GICT_ERRIRQCR<n>	0x4*N +0x2E800 (N=0-2)	Error Interrupt Configuration Register
GICT_DEVARCH	0x2FFBC	Device Architecture register
GICT_ERRIDR	0x2FFC8	Error Record ID Register
GICT_PIDR4	0x2FFD0	Peripheral ID4 Register
GICT_PIDR5	0x2FFD4	Peripheral ID5 Register
GICT_PIDR6	0x2FFD8	Peripheral ID6 Register
GICT_PIDR7	0x2FFDC	Peripheral ID7 Register
GICT_PIDR0	0x2FFE0	Peripheral ID0 Register
GICT_PIDR1	0x2FFE4	Peripheral ID1 Register
GICT_PIDR2	0x2FFE8	Peripheral ID2 Register
GICT_PIDR3	0x2FFEC	Peripheral ID3 Register
GICT_CIDR0	0x2FFF0	Component ID 0 Register
GICT_CIDR1	0x2FFF4	Component ID 1 Register
GICT_CIDR2	0x2FFF8	Component ID 2 Register
GICT_CIDR3	0x2FFFC	Component ID 3 Register
GICP_EVCNTRn	0x4*N +0x30000 (N=0-2)	Event Counter Registers
GICP_EVTYPERn	0x4*N +0x30400 (N=0-2)	Event Type Configuration Register
GICP_SVRn	0x4*N +0x30600 (N=0-2)	Shadow Value Registers
GICP_FRn	0x4*N +0x30A00 (N=0-2)	Filter Registers
GICP_CNTENSET0	0x30C00	Counter Enable Set Register
GICP_CNTENCLR0	0x30C20	Counter Enable Clear Register 0,
GICP_INTENSET0	0x30C40	Interrupt Contribution Enable Set Register 0
GICP_INTENCLR0	0x30C60	Interrupt Contribution Enable Clear Register 0,
GICP_OVSCLR0	0x30C80	Overflow Status Clear Register 0,
GICP_OVSSET0	0x30CC0	Overflow Status Set Register 0,
GICP_CAPR	0x30D88	Counter Shadow Value Capture Register
GICP_CFGR	0x30E00	Configuration Information Register
GICP_CR	0x30E04	Control Register
GICP_IRQCR	0x30E50	Interrupt Configuration Register
GICP_PMAUTHSTATUS	0x30FB8	
GICP_PMDEVARCH	0x30FBC	
GICP_PMDEVTYPE	0x30FCC	
GICP_PIDR4	0x30FD0	Peripheral ID4 Register
GICP_PIDR5	0x30FD4	Peripheral ID5 Register
GICP_PIDR6	0x30FD8	Peripheral ID6 Register
GICP_PIDR7	0x30FDC	Peripheral ID7 Register

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Register Name	Offset	Description
GICP_PIDR0	0x30FE0	Peripheral ID0 Register
GICP_PIDR1	0x30FE4	Peripheral ID1 Register
GICP_PIDR2	0x30FE8	Peripheral ID2 Register
GICP_PIDR3	0x30FEC	Peripheral ID3 Register
GICP_CIDR0	0x30FF0	Component ID 0 Register
GICP_CIDR1	0x30FF4	Component ID 1 Register
GICP_CIDR2	0x30FF8	Component ID 2 Register
GICP_CIDR3	0x30FFC	Component ID 3 Register
GITS_CTLR	0x40000	ITS Control Register
GITS_IIDR	0x40004	ITS Implementer Identification Register
GITS_TYPER	0x40008	Interrupt Controller Type Register
GITS_FCTLR	0x40020	Function Control Register
GITS_OPR	0x40028	Operations Register
GITS_OPSR	0x40030	Operation Status Register
GITS_CBASER	0x40080	Command Queue Control Register
GITS_CWRITER	0x40088	Command Queue Write Pointer Register
GITS_CREADR	0x40090	Command Queue Read Pointer Register
GITS_BASER0	0x40100	ITS Translation Table Descriptor Register0
GITS_BASER1	0x40108	ITS Translation Table Descriptor Register1
GITS_CFGID	0x4F000	Configuration ID Register
GITS_PIDR4	0x4FFD0	Peripheral ID4 Register
GITS_PIDR5	0x4FFD4	Peripheral ID5 Register
GITS_PIDR6	0x4FFD8	Peripheral ID6 Register
GITS_PIDR7	0x4FFDC	Peripheral ID7 Register
GITS_PIDR0	0x4FFE0	Peripheral ID0 Register
GITS_PIDR1	0x4FFE4	Peripheral ID1 Register
GITS_PIDR2	0x4FFE8	Peripheral ID2 Register
GITS_PIDR3	0x4FFEC	Peripheral ID3 Register
GITS_CIDR0	0x4FFF0	Component ID 0 Register
GITS_CIDR1	0x4FFF4	Component ID 1 Register
GITS_CIDR2	0x4FFF8	Component ID 2 Register
GITS_CIDR3	0x4FFFC	Component ID 3 Register
GITS_TRANSLATER	0x50040	ITS Translation Register
GICR_CTLR_C0	0x60000	Redistributor Control Register
GICR_IIDR_C0	0x60004	Redistributor Implementation Identification Register
GICR_TYPER_C0	0x60008	Interrupt Controller Type Register
GICR_WAKER_C0	0x60014	Power Management Control Register
GICR_FCTLR_C0	0x60020	Function Control Register
GICR_PWRR_C0	0x60024	Power Register
GICR_CLASS_C0	0x60028	Class Register
GICR_SETLPIR_C0	0x60040	

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Register Name	Offset	Description
GICR_CLRLPIR_C0	0x60048	
GICR_PROPBASER_C0	0x60070	Redistributor Properties Base Address Register
GICR_PENDBASER_C0	0x60078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C0	0x600A0	
GICR_INVALLR_C0	0x600B0	
GICR_SYNCR_C0	0x600C0	
GICR_PIDR4_C0	0x6FFD0	Peripheral ID4 Register
GICR_PIDR5_C0	0x6FFD4	Peripheral ID5 Register
GICR_PIDR6_C0	0x6FFD8	Peripheral ID6 Register
GICR_PIDR7_C0	0x6FFDC	Peripheral ID7 Register
GICR_PIDR0_C0	0x6FFE0	Peripheral ID0 Register
GICR_PIDR1_C0	0x6FFE4	Peripheral ID1 Register
GICR_PIDR2_C0	0x6FFE8	Peripheral ID2 Register
GICR_PIDR3_C0	0x6FFEC	Peripheral ID3 Register
GICR_CIDR0_C0	0x6FFF0	Component ID 0 Register
GICR_CIDR1_C0	0x6FFF4	Component ID 1 Register
GICR_CIDR2_C0	0x6FFF8	Component ID 2 Register
GICR_CIDR3_C0	0x6FFFC	Component ID 3 Register
GICR_IGROUPR0_C0	0x70080	Interrupt Group Register
GICR_ISENABLER0_C0	0x70100	Interrupt Set-Enable Register
GICR_ICENABLER0_C0	0x70180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C0	0x70200	Interrupt Set-Pending Register
GICR_ICPENDR0_C0	0x70280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C0	0x70300	Interrupt Set-Active Register
GICR_ICACTIVER0_C0	0x70380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C0	0x4*N +0x70400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C0	0x4*N +0x70C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C0	0x70D00	Interrupt Group Modifier Register
GICR_NSACR_C0	0x70E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C0	0x7C000	Miscellaneous Status Register
GICR_IERRVR_C0	0x7C008	Interrupt Error Valid Register
GICR_SGIDR_C0	0x7C010	SGI Default Register
GICR_CFGID0_C0	0x7F000	Configuration ID0 Register
GICR_CFGID1_C0	0x7F004	Configuration ID1 Register
GICR_CTLR_C1	0x80000	Redistributor Control Register
GICR_IIDR_C1	0x80004	Redistributor Implementation Identification Register
GICR_TYPER_C1	0x80008	Interrupt Controller Type Register
GICR_WAKER_C1	0x80014	Power Management Control Register

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Register Name	Offset	Description
GICR_FCTLR_C1	0x80020	Function Control Register
GICR_PWRR_C1	0x80024	Power Register
GICR_CLASS_C1	0x80028	Class Register
GICR_SETLPIR_C1	0x80040	
GICR_CLRLPIR_C1	0x80048	
GICR_PROPBASER_C1	0x80070	Redistributor Properties Base Address Register
GICR_PENDBASER_C1	0x80078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C1	0x800A0	
GICR_INVALLR_C1	0x800B0	
GICR_SYNCR_C1	0x800C0	
GICR_PIDR4_C1	0x8FFD0	Peripheral ID4 Register
GICR_PIDR5_C1	0x8FFD4	Peripheral ID5 Register
GICR_PIDR6_C1	0x8FFD8	Peripheral ID6 Register
GICR_PIDR7_C1	0x8FFDC	Peripheral ID7 Register
GICR_PIDR0_C1	0x8FFE0	Peripheral ID0 Register
GICR_PIDR1_C1	0x8FFE4	Peripheral ID1 Register
GICR_PIDR2_C1	0x8FFE8	Peripheral ID2 Register
GICR_PIDR3_C1	0x8FFEC	Peripheral ID3 Register
GICR_CIDR0_C1	0x8FFF0	Component ID 0 Register
GICR_CIDR1_C1	0x8FFF4	Component ID 1 Register
GICR_CIDR2_C1	0x8FFF8	Component ID 2 Register
GICR_CIDR3_C1	0x8FFFC	Component ID 3 Register
GICR_IGROUPR0_C1	0x90080	Interrupt Group Register
GICR_ISENABLER0_C1	0x90100	Interrupt Set-Enable Register
GICR_ICENABLER0_C1	0x90180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C1	0x90200	Interrupt Set-Pending Register
GICR_ICPENDR0_C1	0x90280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C1	0x90300	Interrupt Set-Active Register
GICR_ICACTIVER0_C1	0x90380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C1	0x4*N +0x90400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C1	0x4*N +0x90C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C1	0x90D00	Interrupt Group Modifier Register
GICR_NSACR_C1	0x90E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C1	0x9C000	Miscellaneous Status Register
GICR_IERRVR_C1	0x9C008	Interrupt Error Valid Register
GICR_SGIDR_C1	0x9C010	SGI Default Register
GICR_CFGID0_C1	0x9F000	Configuration ID0 Register
GICR_CFGID1_C1	0x9F004	Configuration ID1 Register
GICR_CTLR_C2	0xA0000	Redistributor Control Register

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Register Name	Offset	Description
GICR_IIDR_C2	0xA0004	Redistributor Implementation Identification Register
GICR_TYPER_C2	0xA0008	Interrupt Controller Type Register
GICR_WAKER_C2	0xA0014	Power Management Control Register
GICR_FCTLR_C2	0xA0020	Function Control Register
GICR_PWRR_C2	0xA0024	Power Register
GICR_CLASS_C2	0xA0028	Class Register
GICR_SETLPIR_C2	0xA0040	
GICR_CLRLPIR_C2	0xA0048	
GICR_PROPBASER_C2	0xA0070	Redistributor Properties Base Address Register
GICR_PENDBASER_C2	0xA0078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C2	0xA00A0	
GICR_INVALLR_C2	0xA00B0	
GICR_SYNCR_C2	0xA00C0	
GICR_PIDR4_C2	0xAFFD0	Peripheral ID4 Register
GICR_PIDR5_C2	0xAFFD4	Peripheral ID5 Register
GICR_PIDR6_C2	0xAFFD8	Peripheral ID6 Register
GICR_PIDR7_C2	0xAFFDC	Peripheral ID7 Register
GICR_PIDR0_C2	0xAFFE0	Peripheral ID0 Register
GICR_PIDR1_C2	0xAFFE4	Peripheral ID1 Register
GICR_PIDR2_C2	0xAFFE8	Peripheral ID2 Register
GICR_PIDR3_C2	0xAFFEC	Peripheral ID3 Register
GICR_CIDR0_C2	0xAFFF0	Component ID 0 Register
GICR_CIDR1_C2	0xAFFF4	Component ID 1 Register
GICR_CIDR2_C2	0xAFFF8	Component ID 2 Register
GICR_CIDR3_C2	0xAFFFC	Component ID 3 Register
GICR_IGROUPR0_C2	0xB0080	Interrupt Group Register
GICR_ISENABLER0_C2	0xB0100	Interrupt Set-Enable Register
GICR_ICENABLER0_C2	0xB0180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C2	0xB0200	Interrupt Set-Pending Register
GICR_ICPENDR0_C2	0xB0280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C2	0xB0300	Interrupt Set-Active Register
GICR_ICACTIVER0_C2	0xB0380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C2	0x4*N +0xB0400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C2	0x4*N +0xB0C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C2	0xB0D00	Interrupt Group Modifier Register
GICR_NSACR_C2	0xB0E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C2	0xBC000	Miscellaneous Status Register
GICR_IERRVR_C2	0xBC008	Interrupt Error Valid Register

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Register Name	Offset	Description
GICR_SGIDR_C2	0xBC010	SGI Default Register
GICR_CFGID0_C2	0xBF000	Configuration ID0 Register
GICR_CFGID1_C2	0xBF004	Configuration ID1 Register
GICR_CTLR_C3	0xC0000	Redistributor Control Register
GICR_IIDR_C3	0xC0004	Redistributor Implementation Identification Register
GICR_TYPER_C3	0xC0008	Interrupt Controller Type Register
GICR_WAKER_C3	0xC0014	Power Management Control Register
GICR_FCTLR_C3	0xC0020	Function Control Register
GICR_PWRR_C3	0xC0024	Power Register
GICR_CLASS_C3	0xC0028	Class Register
GICR_SETLPIR_C3	0xC0040	
GICR_CLRLPIR_C3	0xC0048	
GICR_PROPBASER_C3	0xC0070	Redistributor Properties Base Address Register
GICR_PENDBASER_C3	0xC0078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C3	0xC00A0	
GICR_INVALLR_C3	0xC00B0	
GICR_SYNCR_C3	0xC00C0	
GICR_PIDR4_C3	0xCFFD0	Peripheral ID4 Register
GICR_PIDR5_C3	0xCFFD4	Peripheral ID5 Register
GICR_PIDR6_C3	0xCFFD8	Peripheral ID6 Register
GICR_PIDR7_C3	0xCFFDC	Peripheral ID7 Register
GICR_PIDR0_C3	0xCFFE0	Peripheral ID0 Register
GICR_PIDR1_C3	0xCFFE4	Peripheral ID1 Register
GICR_PIDR2_C3	0xCFFE8	Peripheral ID2 Register
GICR_PIDR3_C3	0xCFFEC	Peripheral ID3 Register
GICR_CIDR0_C3	0xCFFF0	Component ID 0 Register
GICR_CIDR1_C3	0xCFFF4	Component ID 1 Register
GICR_CIDR2_C3	0xCFFF8	Component ID 2 Register
GICR_CIDR3_C3	0xCFFFC	Component ID 3 Register
GICR_IGROUPR0	0xD0080	Interrupt Group Register
GICR_ISENABLER0_C3	0xD0100	Interrupt Set-Enable Register
GICR_ICENABLER0_C3	0xD0180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C3	0xD0200	Interrupt Set-Pending Register
GICR_ICPENDR0_C3	0xD0280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C3	0xD0300	Interrupt Set-Active Register
GICR_ICACTIVER0_C3	0xD0380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C3	0x4*N +0xD0400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C3	0x4*N +0xD0C00 (N=0-1)	Interrupt Configuration Registers

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Register Name	Offset	Description
GICR_IGRPMODR0_C3	0xD0D00	Interrupt Group Modifier Register
GICR_NSACR_C3	0xD0E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C3	0xDC000	Miscellaneous Status Register
GICR_IERRVR_C3	0xDC008	Interrupt Error Valid Register
GICR_SGIDR_C3	0xDC010	SGI Default Register
GICR_CFGID0_C3	0xDF000	Configuration ID0 Register
GICR_CFGID1_C3	0xDF004	Configuration ID1 Register
GICR_CTLR_C4	0xE0000	Redistributor Control Register
GICR_IIDR_C4	0xE0004	Redistributor Implementation Identification Register
GICR_TYPER_C4	0xE0008	Interrupt Controller Type Register
GICR_WAKER_C4	0xE0014	Power Management Control Register
GICR_FCTLR_C4	0xE0020	Function Control Register
GICR_PWRR_C4	0xE0024	Power Register
GICR_CLASS_C4	0xE0028	Class Register
GICR_SETLPIR_C4	0xE0040	
GICR_CLRLPIR_C4	0xE0048	
GICR_PROPBASER_C4	0xE0070	Redistributor Properties Base Address Register
GICR_PENDBASER_C4	0xE0078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C4	0xE00A0	
GICR_INVALLR_C4	0xE00B0	
GICR_SYNCR_C4	0xE00C0	
GICR_PIDR4_C4	0xEFFD0	Peripheral ID4 Register
GICR_PIDR5_C4	0xEFFD4	Peripheral ID5 Register
GICR_PIDR6_C4	0xEFFD8	Peripheral ID6 Register
GICR_PIDR7_C4	0xEFFDC	Peripheral ID7 Register
GICR_PIDR0_C4	0xEFFE0	Peripheral ID0 Register
GICR_PIDR1_C4	0xEFFE4	Peripheral ID1 Register
GICR_PIDR2_C4	0xEFFE8	Peripheral ID2 Register
GICR_PIDR3_C4	0xEFFEC	Peripheral ID3 Register
GICR_CIDR0_C4	0xEFFF0	Component ID 0 Register
GICR_CIDR1_C4	0xEFFF4	Component ID 1 Register
GICR_CIDR2_C4	0xEFFF8	Component ID 2 Register
GICR_CIDR3_C4	0xEFFFC	Component ID 3 Register
GICR_IGROUPR0	0xF0080	Interrupt Group Register
GICR_ISENABLER0_C4	0xF0100	Interrupt Set-Enable Register
GICR_ICENABLER0_C4	0xF0180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C4	0xF0200	Interrupt Set-Pending Register
GICR_ICPENDR0_C4	0xF0280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C4	0xF0300	Interrupt Set-Active Register
GICR_ICACTIVER0_C4	0xF0380	Interrupt Clear-Active Register

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Register Name	Offset	Description
GICR_IPRIORITYRn_C4	0x4*N +0xF0400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C4	0x4*N +0xF0C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C4	0xF0D00	Interrupt Group Modifier Register
GICR_NSACR_C4	0xF0E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C4	0xFC000	Miscellaneous Status Register
GICR_IERRVR_C4	0xFC008	Interrupt Error Valid Register
GICR_SGIDR_C4	0xFC010	SGI Default Register
GICR_CFGID0_C4	0xFF000	Configuration ID0 Register
GICR_CFGID1_C4	0xFF004	Configuration ID1 Register
GICR_CTLR_C5	0x100000	Redistributor Control Register
GICR_IIDR_C5	0x100004	Redistributor Implementation Identification Register
GICR_TYPER_C5	0x100008	Interrupt Controller Type Register
GICR_WAKER_C5	0x100014	Power Management Control Register
GICR_FCTLR_C5	0x100020	Function Control Register
GICR_PWRR_C5	0x100024	Power Register
GICR_CLASS_C5	0x100028	Class Register
GICR_SETLPIR_C5	0x100040	
GICR_CLRLPIR_C5	0x100048	
GICR_PROPBASER_C5	0x100070	Redistributor Properties Base Address Register
GICR_PENDBASER_C5	0x100078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C5	0x1000A0	
GICR_INVALLR_C5	0x1000B0	
GICR_SYNCR_C5	0x1000C0	
GICR_PIDR4_C5	0x10FFD0	Peripheral ID4 Register
GICR_PIDR5_C5	0x10FFD4	Peripheral ID5 Register
GICR_PIDR6_C5	0x10FFD8	Peripheral ID6 Register
GICR_PIDR7_C5	0x10FFDC	Peripheral ID7 Register
GICR_PIDR0_C5	0x10FFE0	Peripheral ID0 Register
GICR_PIDR1_C5	0x10FFE4	Peripheral ID1 Register
GICR_PIDR2_C5	0x10FFE8	Peripheral ID2 Register
GICR_PIDR3_C5	0x10FFEC	Peripheral ID3 Register
GICR_CIDR0_C5	0x10FFF0	Component ID 0 Register
GICR_CIDR1_C5	0x10FFF4	Component ID 1 Register
GICR_CIDR2_C5	0x10FFF8	Component ID 2 Register
GICR_CIDR3_C5	0x10FFFC	Component ID 3 Register
GICR_IGROUPR0	0x110080	Interrupt Group Register
GICR_ISENABLER0_C5	0x110100	Interrupt Set-Enable Register
GICR_ICENABLER0_C5	0x110180	Interrupt Clear-Enable Register

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Register Name	Offset	Description
GICR_ISPENDR0_C5	0x110200	Interrupt Set-Pending Register
GICR_ICPENDR0_C5	0x110280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C5	0x110300	Interrupt Set-Active Register
GICR_ICACTIVER0_C5	0x110380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C5	0x4*N +0x110400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C5	0x4*N +0x110C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C5	0x110D00	Interrupt Group Modifier Register
GICR_NSACR_C5	0x110E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C5	0x11C000	Miscellaneous Status Register
GICR_IERRVR_C5	0x11C008	Interrupt Error Valid Register
GICR_SGIDR_C5	0x11C010	SGI Default Register
GICR_CFGID0_C5	0x11F000	Configuration ID0 Register
GICR_CFGID1_C5	0x11F004	Configuration ID1 Register
GICR_CTLR_C6	0x120000	Redistributor Control Register
GICR_IIDR_C6	0x120004	Redistributor Implementation Identification Register
GICR_TYPER_C6	0x120008	Interrupt Controller Type Register
GICR_WAKER_C6	0x120014	Power Management Control Register
GICR_FCTLR_C6	0x120020	Function Control Register
GICR_PWRR_C6	0x120024	Power Register
GICR_CLASS_C6	0x120028	Class Register
GICR_SETLPIR_C6	0x120040	
GICR_CLRLPIR_C6	0x120048	
GICR_PROPBASER_C6	0x120070	Redistributor Properties Base Address Register
GICR_PENDBASER_C6	0x120078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C6	0x1200A0	
GICR_INVALLR_C6	0x1200B0	
GICR_SYNCR_C6	0x1200C0	
GICR_PIDR4_C6	0x12FFD0	Peripheral ID4 Register
GICR_PIDR5_C6	0x12FFD4	Peripheral ID5 Register
GICR_PIDR6_C6	0x12FFD8	Peripheral ID6 Register
GICR_PIDR7_C6	0x12FFDC	Peripheral ID7 Register
GICR_PIDR0_C6	0x12FFE0	Peripheral ID0 Register
GICR_PIDR1_C6	0x12FFE4	Peripheral ID1 Register
GICR_PIDR2_C6	0x12FFE8	Peripheral ID2 Register
GICR_PIDR3_C6	0x12FFEC	Peripheral ID3 Register
GICR_CIDR0_C6	0x12FFF0	Component ID 0 Register

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Register Name	Offset	Description
GICR_CIDR1_C6	0x12FFF4	Component ID 1 Register
GICR_CIDR2_C6	0x12FFF8	Component ID 2 Register
GICR_CIDR3_C6	0x12FFFC	Component ID 3 Register
GICR_IGROUPR0	0x130080	Interrupt Group Register
GICR_ISENABLER0_C6	0x130100	Interrupt Set-Enable Register
GICR_ICENABLER0_C6	0x130180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C6	0x130200	Interrupt Set-Pending Register
GICR_ICPENDR0_C6	0x130280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C6	0x130300	Interrupt Set-Active Register
GICR_ICACTIVER0_C6	0x130380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C6	0x4*N +0x130400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C6	0x4*N +0x130C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C6	0x130D00	Interrupt Group Modifier Register
GICR_NSACR_C6	0x130E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C6	0x13C000	Miscellaneous Status Register
GICR_IERRVR_C6	0x13C008	Interrupt Error Valid Register
GICR_SGIDR_C6	0x13C010	SGI Default Register
GICR_CFGID0_C6	0x13F000	Configuration ID0 Register
GICR_CFGID1_C6	0x13F004	Configuration ID1 Register
GICR_CTLR_C7	0x140000	Redistributor Control Register
GICR_IIDR_C7	0x140004	Redistributor Implementation Identification Register
GICR_TYPER_C7	0x140008	Interrupt Controller Type Register
GICR_WAKER_C7	0x140014	Power Management Control Register
GICR_FCTLR_C7	0x140020	Function Control Register
GICR_PWRR_C7	0x140024	Power Register
GICR_CLASS_C7	0x140028	Class Register
GICR_SETLPIR_C7	0x140040	
GICR_CLRLPIR_C7	0x140048	
GICR_PROPBASER_C7	0x140070	Redistributor Properties Base Address Register
GICR_PENDBASER_C7	0x140078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C7	0x1400A0	
GICR_INVALLR_C7	0x1400B0	
GICR_SYNCR_C7	0x1400C0	
GICR_PIDR4_C7	0x14FFD0	Peripheral ID4 Register
GICR_PIDR5_C7	0x14FFD4	Peripheral ID5 Register
GICR_PIDR6_C7	0x14FFD8	Peripheral ID6 Register

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Register Name	Offset	Description
GICR_PIDR7_C7	0x14FFDC	Peripheral ID7 Register
GICR_PIDR0_C7	0x14FFE0	Peripheral ID0 Register
GICR_PIDR1_C7	0x14FFE4	Peripheral ID1 Register
GICR_PIDR2_C7	0x14FFE8	Peripheral ID2 Register
GICR_PIDR3_C7	0x14FFEC	Peripheral ID3 Register
GICR_CIDR0_C7	0x14FFF0	Component ID 0 Register
GICR_CIDR1_C7	0x14FFF4	Component ID 1 Register
GICR_CIDR2_C7	0x14FFF8	Component ID 2 Register
GICR_CIDR3_C7	0x14FFFC	Component ID 3 Register
GICR_IGROUPR0	0x150080	Interrupt Group Register
GICR_ISENABLER0_C7	0x150100	Interrupt Set-Enable Register
GICR_ICENABLER0_C7	0x150180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C7	0x150200	Interrupt Set-Pending Register
GICR_ICPENDR0_C7	0x150280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C7	0x150300	Interrupt Set-Active Register
GICR_ICACTIVER0_C7	0x150380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C7	0x4*N +0x150400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C7	0x4*N +0x150C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C7	0x150D00	Interrupt Group Modifier Register
GICR_NSACR_C7	0x150E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C7	0x15C000	Miscellaneous Status Register
GICR_IERRVR_C7	0x15C008	Interrupt Error Valid Register
GICR_SGIDR_C7	0x15C010	SGI Default Register
GICR_CFGID0_C7	0x15F000	Configuration ID0 Register
GICR_CFGID1_C7	0x15F004	Configuration ID1 Register
GICDA_CTLR	0x160000	Distributor Control Register
GICDA_TYPER	0x160004	Interrupt Controller Type Register
GICDA_IIDR	0x160008	Distributor Implementer Identification Register
GICDA_FCTLR	0x160020	Function Control Register
GICDA_SAC	0x160024	Secure Access Control
GICDA_SETSPI_NSR	0x160040	Non-secure SPI Set Register
GICDA_CLRSPI_NSR	0x160048	Non-secure SPI Clear Register
GICDA_CLRSPI_NSR	0x160050	Secure SPI Set Register
GICDA_CLRSPI_SR	0x160058	Secure SPI Clear Register
GICDA_IGROUPRn	0x4*N +0x160080 (N=0-31)	Interrupt Group Registers

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Register Name	Offset	Description
GICDA_ISENABLERn	0x4*N +0x160100 (N=0-31)	Interrupt Set-Enable Registers 0-N
GICDA_ICENABLERn	0x4*N +0x160180 (N=0-31)	Interrupt Clear-Enable Registers 0-N
GICDA_ISPENDRn	0x4*N +0x160200 (N=0-31)	Interrupt Set-Pending Registers
GICDA_ICPENDRn	0x4*N +0x160280 (N=0-31)	Interrupt Clear-Pending Registers
GICDA_ISACTIVERn	0x4*N +0x160300 (N=0-31)	Interrupt Set-Active Registers
GICDA_ICACTIVERn	0x4*N +0x160380 (N=0-31)	Interrupt Clear-Active Registers
GICDA_IPRIORITYRn	0x4*N +0x160400 (N=0-255)	Interrupt Priority Registers
GICDA_ICFGRn	0x4*N +0x160C00 (N=0-63)	Interrupt Configuration Registers
GICDA_IGRPMODRn	0x4*N +0x160D00 (N=0-63)	Interrupt Group Modifier Registers
GICDA_NSACRn	0x4*N +0x160E00 (N=0-63)	Non-secure Access Control Registers
GICDA_IROUTERn	0x16*N +0x166000 (N=32-1019)	Interrupt Routing Registers
GICDA_CHIPSR	0x16C000	Chip Status Register
GICDA_DCHIPR	0x16C004	Default Chip Register
GICDA_CHIPRn	0x4*N +0x16C000 (N=2-32)	Chip Registers
GICDA_ICLARn	0x4*N +0x16E000 (N=2-63)	Interrupt Class Registers

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Register Name	Offset	Description
GICDA_IERRRn	0x4*N +0x16E100 (N=2-31)	Interrupt Error Registers
GICDA_CFGID	0x16F000	Configuration ID Register
GICDA_PIDR4	0x16FFD0	Peripheral ID4 Register
GICDA_PIDR5	0x16FFD4	Peripheral ID5 Register
GICDA_PIDR6	0x16FFD8	Peripheral ID6 Register
GICDA_PIDR7	0x16FFDC	Peripheral ID7 Register
GICDA_PIDR0	0x16FFE0	Peripheral ID0 Register
GICDA_PIDR1	0x16FFE4	Peripheral ID1 Register
GICDA_PIDR2	0x16FFE8	Peripheral ID2 Register
GICDA_PIDR3	0x16FFEC	Peripheral ID3 Register
GICDA_CIDR0	0x16FFF0	Component ID 0 Register
GICDA_CIDR1	0x16FFF4	Component ID 1 Register
GICDA_CIDR2	0x16FFF8	Component ID 2 Register
GICDA_CIDR3	0x16FFFC	Component ID 3 Register

2.9.4 Register Description

For detailed register description, please refer to *Arm® CoreLink™ GIC-600 Generic Interrupt Controller Technical Reference Manual* and *Arm® Generic Interrupt Controller Architecture Specification GIC architecture version 3 and version 4*.

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2.10 Core-Local Interrupt Controller (CLIC)

2.10.1 Overview

The Core-Local Interrupt Controller (CLIC) is only used for sampling, priority arbitration and distribution for external interrupt sources.

- supports RISC-V Core-Local Interrupt Controller Version 0.8 specification
- Up to 144 interrupt source sampling, supporting level interrupt and pulse interrupt
- 32 levels of interrupt priority
- 4 memory-mapped control registers for each interrupt
- Each attribute of this interrupt source can be configured by writing the control register of the corresponding interrupt source.

2.10.2 Functional Description

The following table describes the detail of interrupt sources.

Table 2-16 Interrupt Sources

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0-15	Reserved	0x0000-0x003C	Not Used
16	RISCV_WDT	0x0040	RISCV watchdog interrupt
17	RISCV_MSGBOX_RISCV	0x0044	RISCV MSGBOX read IRQ
18	DoubleExceptionError	0x0048	DSP_core DoubleExceptionError interrupt
19	PFatalError	0x004C	DSP_core PFatalError interrupt
20	DSP_WDT_IRQ	0x0050	
21	DSP_MSGBOX_IRQ_CPUX	0x0054	
22	DSP_MSGBOX_IRQ_CPUS	0x0058	
23	DSP_MSGBOX_IRQ_RISCV	0x005C	
24		0x0060	
25	DSP_TIMER0	0x0064	
26	DSP_TIMER1	0x0068	
27	DSP_TIMER2_	0x006C	
28	AHB0_HREADY_TIME_OUT	0x0070	DSP AHB decoder0 timer out interrupt
29	AHB1_HREADY_TIME_OUT	0x0074	DSP AHB decoder1 timer out interrupt
30	AUDIO CODEC	0x0078	Audio Codec IRQ
31	DMIC	0x007C	DMIC IRQ

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
32	I2S0	0x0080	I2S0 IRQ
33	I2S1	0x0084	I2S1 IRQ
34	I2S2	0x0088	I2S2 IRQ
35	I2S3	0x008C	I2S3 IRQ
36	OWA	0x0090	OWA IRQ
37	DSP_DMAC_NS	0x0094	DSP DMAC channel IRQ non-secure to DSP
38	DSP_DMAC_S	0x0098	DSP DMAC channel IRQ secure to DSP
39	NPU	0x009C	NPU interrupt
40		0x00A0	
41	DSP_TIMER3	0x00A4	
42	DSP_TIMER4	0x00A8	
43	DSP_TIMER5	0x00AC	
44	DSP_PWMCTRL	0x00B0	DSP PWMCTRL Interrupt
45		0x00B4	
46		0x00B8	
47		0x00BC	
48		0x00C0	
49		0x00C4	
50		0x00C8	
51		0x00CC	
52	NMI	0x00D0	STBY NMI interrupt
53	S_PPU	0x00D4	STBY PCK600 Q-channel Interrupt
54	S_PPU1	0x00D8	/
55	S_TWD	0x00DC	STBY TWD interrupt
56	CPUS_WDT	0x00E0	STBY WDT interrupt
57	CPUS_TIMER0	0x00E4	CPUS_TIMER0 interrupt
58	CPUS_TIMER1	0x00E8	CPUS_TIMER1 interrupt
59	CPUS_TIMER2	0x00EC	CPUS_TIMER2 interrupt
60	S_TWI2	0x00F0	
61	ALARM	0x00F4	RTC ALARM0 interrupt
62	GPIOL_S	0x00F8	
63	GPIOL_NS	0x00FC	
64	GPIOM_S	0x0100	
65	GPIOM_NS	0x0104	
66	S_UART0	0x0108	S_UART0 interrupt
67	S_UART1	0x010C	
68	S_TWI0	0x0110	
69	S_TWI1	0x0114	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
70		0x0118	
71	S_CIRRX	0x011C	S_CIRRX interrupt
72	S_PWMCTRL	0x0120	S_PWMCTRL interrupt
73		0x0124	
74	AHBS_HREADY_TOUT	0x0128	STBY AHBS TIMEOUT interrupt
75	PCK600_CPU	0x012C	CPUIDLE(PCK600_CPU) interrupt
76	S_SPI	0x0130	S_SPI interrupt
77	S_SPINLOCK	0x0134	S_SPINLOCK interrupt
78	CPUS_MSGBOX_CPUX	0x0138	CPUS MSGBOX write IRQ for CPUX
79		0x013C	
80		0x0140	
81	CPUS_MSGBOX_RISCV	0x0144	CPUS MSGBOX write IRQ for RISCV
82	CPUS_MSGBOX_DSP	0x0148	CPUS MSGBOX WRITE IRQ for DSP
83	INT_SCRI[0]	0x014C	CPUX_MSGBOX_IRQ_RISCV
84	INT_SCRI[1]	0x0150	CPUX_MSGBOX_IRQ_CPUS
85	INT_SCRI[2]	0x0154	SPLOCK_IRQ
86		0x0158	
87	INT_SCRI[4]	0x015C	
88	INT_SCRI[5]	0x0160	DMAC_IRQ1_NS
89	INT_SCRI[6]	0x0164	DMAC_IRQ1_S
90	INT_SCRI[7]	0x0168	GIC IRQ 32-39 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[7:0] in S_INTC. Group GIC IRQ bit [33:32] are fixed to be masked.
91	INT_SCRI[8]	0x016C	GIC IRQ 40-47 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[15:8] in S_INTC.

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
92	INT_SCRI[9]	0x0170	GIC IRQ 48-55 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[23:16] in S_INTC.
93	INT_SCRI[10]	0x0174	GIC IRQ 56-63 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[31:24] in S_INTC.
94	INT_SCRI[11]	0x0178	GIC IRQ 64-71 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[7:0] in S_INTC.
95	INT_SCRI[12]	0x017C	GIC IRQ 72-79 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[15:8] in S_INTC.
96	INT_SCRI[13]	0x0180	GIC IRQ 80-87 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[23:16] in S_INTC. Group GIC IRQ bit [83:82] are fixed to be masked.
97	INT_SCRI[14]	0x0184	GIC IRQ 88-95 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[31:24] in S_INTC.

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
98	INT_SCRI[15]	0x0188	GIC IRQ 96-103 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[7:0] in S_INTC.
99	INT_SCRI[16]	0x018C	GIC IRQ 104-111 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[15:8] in S_INTC.
100	INT_SCRI[17]	0x0190	GIC IRQ 112-119 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[23:16] in S_INTC.
101	INT_SCRI[18]	0x0194	GIC IRQ 120-127 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[31:24] in S_INTC.
102	INT_SCRI[19]	0x0198	GIC IRQ 128-135 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[7:0] in S_INTC.
103	INT_SCRI[20]	0x019C	GIC IRQ 136-143 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[15:8] in S_INTC.
104	INT_SCRI[21]	0x01A0	GIC IRQ 144-151 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[23:16] in S_INTC.

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
105	INT_SCRI[22]	0x01A4	GIC IRQ 152-159 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[31:24] in S_INTC.
106	INT_SCRI[23]	0x01A8	GIC IRQ 160-167 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG4[7:0] in S_INTC.
107	INT_SCRI[24]	0x01AC	GIC IRQ 168-175 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG4[15:8] in S_INTC.
108	INT_SCRI[25]	0x01B0	GIC IRQ 176-183 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG4[23:16] in S_INTC. Group GIC IRQ bit [183:180] are fixed to be masked.
109		0x01B4	
110		0x01B8	
111		0x01BC	
112		0x01C0	
113		0x01C4	
114		0x01C8	
115		0x01CC	
116		0x01D0	
117		0x01D4	
118		0x01D8	
119		0x01DC	
120		0x01E0	
121		0x01E4	
122		0x01E8	
123		0x01EC	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
124		0x01F0	
125		0x01F4	
126		0x01F8	
127		0x01FC	
128		0x0200	
129		0x0204	
130		0x0208	
131		0x020C	
132		0x0210	
133		0x0214	
134		0x0218	
135		0x021C	
136		0x0220	
137		0x0224	
138		0x0228	
139		0x022C	
140		0x0230	
141		0x0234	
142		0x0238	
143		0x023C	
144		0x0240	

2.10.3 Register List

2.10.3.1 CLIC Register List

Module Name	Base Address
RISCV CLIC	0xE080_0000

Register Name	Offset	Description
CLIC_CFG_REG	0x0000	CLIC Configuration Register
CLIC_MINTTHRESH_REG	0x0008	CLIC MINTTHRESH Register
CLIC_INT_REGn	0x1000+n*4	CLIC Interrupt Register n

2.10.3.2 S_INTC Register List

Module Name	Base Address
S_INTC	0x0702_1000

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Register Name	Offset	Description
GINTC_CONFIG_REG0	0x00C0	Group Interrupt Configuration Register 0
GINTC_CONFIG_REG1	0x00C4	Group Interrupt Configuration Register 1
GINTC_CONFIG_REG2	0x00C8	Group Interrupt Configuration Register 2
GINTC_CONFIG_REG3	0x00CC	Group Interrupt Configuration Register 3
GINTC_CONFIG_REG4	0x00D0	Group Interrupt Configuration Register 4

2.10.4 CLIC Register description

2.10.4.1 0x0000 CLIC Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CLICCFG_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:5	R/W	0x0	NM Indicates the effective number of bits in privilege mode. RISC-V only supports to process interrupt requests in machine mode whatever the value of CLICINTATTR MODE bit in CLIC_INT_REGn register is. The value of this bit is always 0.
4:1	R/W	0x0	NL Indicates the effective number of interrupt priority level bits. The number of bits is fixed at 8. You can fill the empty bits with 1.
0	R/W	0x1	NV Indicates the interrupt flag in hardware vector mode. This bit is fixed at 1 and this indicates that the CLIC controller supports hardware vector mode interrupt. RISC-V could perform a hardware two-stage jump to obtain the service program entry address of the hardware vector interrupt. RISC-V fetches the entry address from MTVT+ interrupt ID*4 after saving the processor field. Then RISC-V jumps to this address to process interrupt. The entry address of other mode interrupts is MTVEC[31:6]<<6.

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2.10.4.2 0x0008 CLIC_MINTTHRESH_REG (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CLIC_MINTTHRESH_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	MTH Machine Mode Threshold
23:0	/	/	/

2.10.4.3 0x1000+n*0x4 CLIC Interrupt Register n (Default Value: 0x07C0_0000)

Offset: 0x1000+n*0x4			Register Name: CLIC_INT_REGn
Bit	Read/Write	Default/Hex	Description
31:27	R/W	0x0	CLICINTCTL PRIO Interrupt Priority Level
26:24	/	0x3	/
23:22	R/W	0x3	CLICINTATTR MODE Interrupt Privilege Mode RISC-V only supports to process interrupt requests in machine mode. The value of this bit is always 2'b11.
21:19	/	/	/
18:17	R/W	0x0	CLICINTATTR TRIG Interrupt Trigger Used to distinguish interrupt trigger mode. CLICINTATTR TRIG [0] = 0: Level Interrupt CLICINTATTR TRIG [0] = 1: Pulse Interrupt CLICINTATTR TRIG [1] =0: Triggered on Rising Edge CLICINTATTR TRIG[1]=1: Triggered on Falling Edge
16	R/W	0x0	CLICINTATTR SHV Hardware Vector Interrupt Indicates whether the interrupt is in hardware vector mode.
15:9	/	/	/
8	R/W	0x0	CLICINTIE Interrupt Enable
7:1	/	/	/

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Offset: 0x1000+n*0x4			Register Name: CLIC_INT_REGn
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CLICINTIP Interrupt Pending **Level Interrupt Mode** the CLICINTIP bit is read-only. To modify the value of this bit, you could set the external interrupt source directly: If external interrupt source is high level, IP = 1. If external interrupt source is low level, IP =0. **Pulse Interrupt Mode** the CLICINTIP bit can be read or written. In hardware vector mode: The IP can be cleared automatically while RISC-V responds interrupt requests. In non-hardware vector mode: While RISC-V executes a CSR command, it is suggested to perform effective reading and writing operations on MNXTI register to obtain the waiting status of interrupt and the corresponding value of IP will be cleared automatically at the same time. If the interrupt request is transmitted to the RISC-V pipeline core directly, hardware is not able to clear the value of IP when RISC-V responds this interrupt. It needs to be cleared by software.

2.10.5 S_INTC Register Description

2.10.5.1 0x00C0 Group Interrupt Configuration Register 0 (Default Value:0x0000_0000)

Offset: 0x00C0			Register Name: GINTC_CONFIG_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG0. Group Interrupt [31:0] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

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2.10.5.2 0x00C4 Group Interrupt Configuration Register 1 (Default Value:0x0000_0000)

Offset: 0x00C4			Register Name: GINTC_CONFIG_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG1 Group Interrupt [63:32] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

2.10.5.3 0x00C8 Group Interrupt Configuration Register 2 (Default Value:0x0000_0000)

Offset: 0x00C8			Register Name: GINTC_CONFIG_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG2 Group Interrupt [95:64] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

2.10.5.4 0x00CC Group Interrupt Configuration Register 3 (Default Value:0x0000_0000)

Offset: 0x00CC			Register Name: GINTC_CONFIG_REG3
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG3. Group Interrupt [127:96] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

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2.10.5.5 0x00D0 Group Interrupt Configuration Register 4 (Default Value:0x0000_0000)

Offset: 0x00D0			Register Name: GINTC_CONFIG_REG4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG4. Group Interrupt [159:128] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

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2.11 I/O Memory Management Unit (IOMMU)

2.11.1 Overview

IOMMU (I/O Memory management unit) is designed for the specific memory requirements. It maps the virtual address (sent by the peripheral access memory) to the physical address. IOMMU allows multiple ways to manage the location of the physical address. It can use the physical address which has the potentially conflict mapping for different processes to allocate the memory space, and also allow application of non-continuous address mapping to the continuous virtual address space.

The IOMMU has the following features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1 , G2D, DE, and DI parallel address mapping
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI bypass function independently
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI pre-fetch independently
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.11.2 Block Diagram

The internal module of IOMMU mainly includes the following parts.

Micro TLB: Level1 TLB, 64 words. Each peripheral corresponds to a TLB, which caching the level2 page table for the peripheral.

Macro TLB: Level2 TLB, 4K words. Each peripheral shares a level2 TLB for caching the level2 page table.

Pre-fetch Logic: Each Micro TLB corresponds to a Pre-fetch Logic. By monitoring each master device to predict the bus access, the secondary page table corresponding to the address to be accessed can be read from the memory and stored in the secondary TLB to improve the hit ratio.

PTW Logic: Page Table Walk, mainly contains PTW Cache and PTW. The PTW Cache is used to store the level1 page table; when the virtual address is missed in the level1 and level2 TLB, it will trigger the PTW. PTW Cache can store 512 level1 page tables, that is, 512 words.

PMU: Performance Monitoring Unit, which is used to count the hit efficiency and the latency.

APB Interface: IOMMU register instantiation module. CPU reads and writes the IOMMU register by APB bus.

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The following figure shows the internal block diagram of IOMMU.

Figure IOMMU Block Diagram

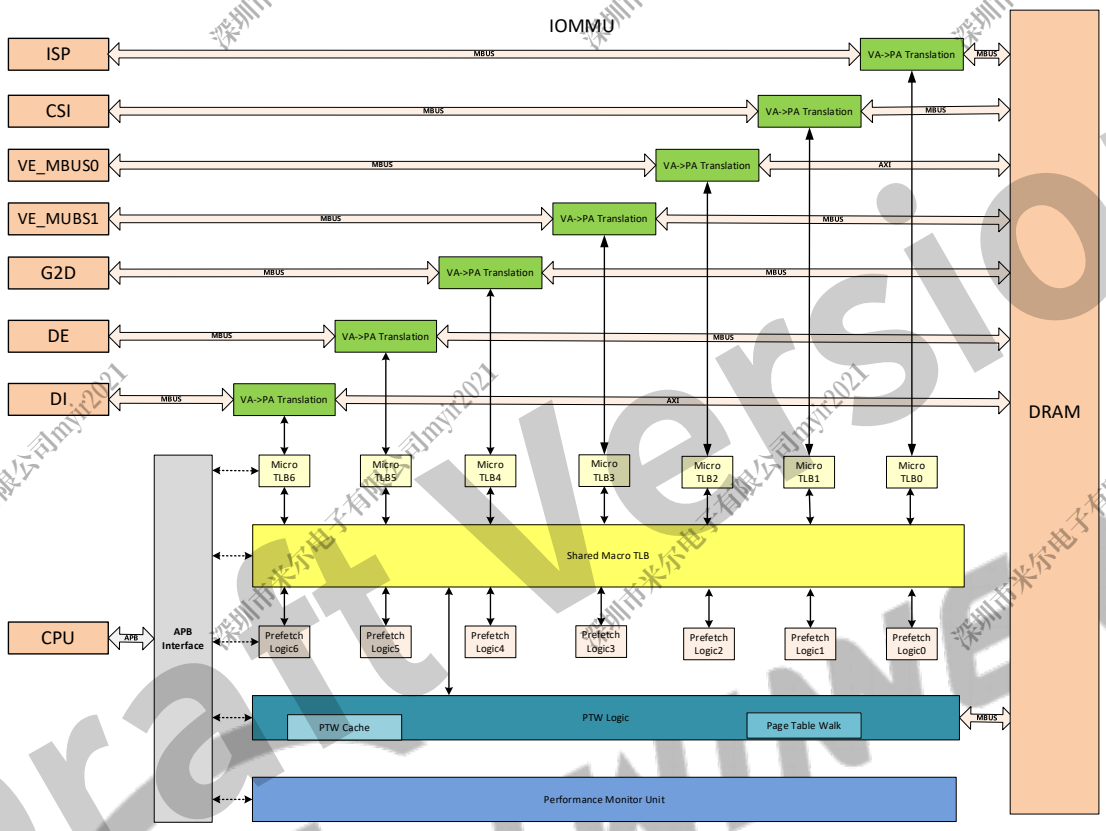

Table 2-17 Correspondence Relation between Master and Module

Master number	module
Master0	ISP
Master1	CSI
Master2	VE_MBUS0
Master3	VE_MBUS1
Master4	G2D
Master5	DE
Master6	DI

2.11.3 Function Descriptions

2.11.3.1 Initialization

- Release the IOMMU reset signal by writing 1 to the bit[31] of the IOMMU_RESET_REG (Offset: 0x0010);
- Write the base address of the first TLB to the IOMMU_TTB_REG (Offset: 0x0050);
- Set the IOMMU_INT_ENABLE_REG (Offset: 0x0100);
- Enable the IOMMU by configuring the IOMMU_ENABLE_REG (Offset: 0x0020) in the final.

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2.11.3.2 Address Translation

In the process of address mapping, the peripheral virtual address [31:12] are retrieved in the Level1 TLB. When TLB is hit, the mapping is finished. Otherwise, they are retrieved in the Level2 TLB in the same way. If TLB is hit, the hit mapping will be written to the Level1 TLB, and hit in Level1 TLB. If Level1 and Level2 TLB are retrieved fail, the PTW will be triggered. After opening the peripheral bypass function by setting IOMMU_BYPASS_REG (Offset: 0x0030), IOMMU will not map the address typed by this peripheral, and it will output the virtual address as the physical address. The typical applications are as follows.

Micro TLB hit

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is hit, it will return a Level2 page table containing the corresponding physical addresses and the permission Index;

Step 3 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB hit

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is missed, continue to search Macro TLB;

Step 3 If Macro TLB is hit, it will return the Level2 page table to Micro TLB;

Step 4 Micro TLB receives this page table, puts it in Micro TLB (If this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;

Step 5 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache hit

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is missed, continue to search Macro TLB;

Step 3 If Macro TLB is missed, send the request to the PTW to return the corresponding page table;

Step 4 PTW first accesses PTW Cache. If the required Level1 page table exists in the PTW Cache, send the page table to PTW logic;

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Step 5 PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;

Step 6 Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;

Step 7 Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;

Step 8 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache miss

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is missed, continue to search Macro TLB;

Step 3 If Macro TLB is missed, send the request to the PTW to return the corresponding page table;

Step 4 PTW accesses PTW Cache, there is no necessary Level1 page table;

Step 5 PTW accesses the memory, gets the corresponding Level1 page table and stores it in the PTW Cache (the replace activities may happen);

Step 6 PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;

Step 7 Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;

Step 8 Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;

Step 9 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Permission error

Step 1 The permission checking is always performed during the process of translating the address;

Step 2 Once the permission checking makes mistake, the new access of the master suspends, but the access before this checking can be continued;

Step 3 Set the error status register;

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Step 4 Trigger the interrupt.

Invalid Level1 page table

Step 1 The invalid Level1 page table is checked when PTW logic reads the new level page table from the memory;

Step 2 The PTW reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the PTW cache;

Step 3 If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.

NOTE

- Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in PTW Cache with target page table is found to be invalid after using;
- If a page table is invalid, invalidate the total cache line (that is two page tables).

Invalid Level2 page table

Step 1 The invalid Level2 page table is checked when Macro TLB reads the new level page table from the memory;

Step 2 The Macro TLB reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the Macro TLB;

Step 3 If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.

NOTE

- Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in Macro TLB with target page table is found to be invalid after using;
- If a page table is invalid, invalidate the total cache line (that is two page tables).

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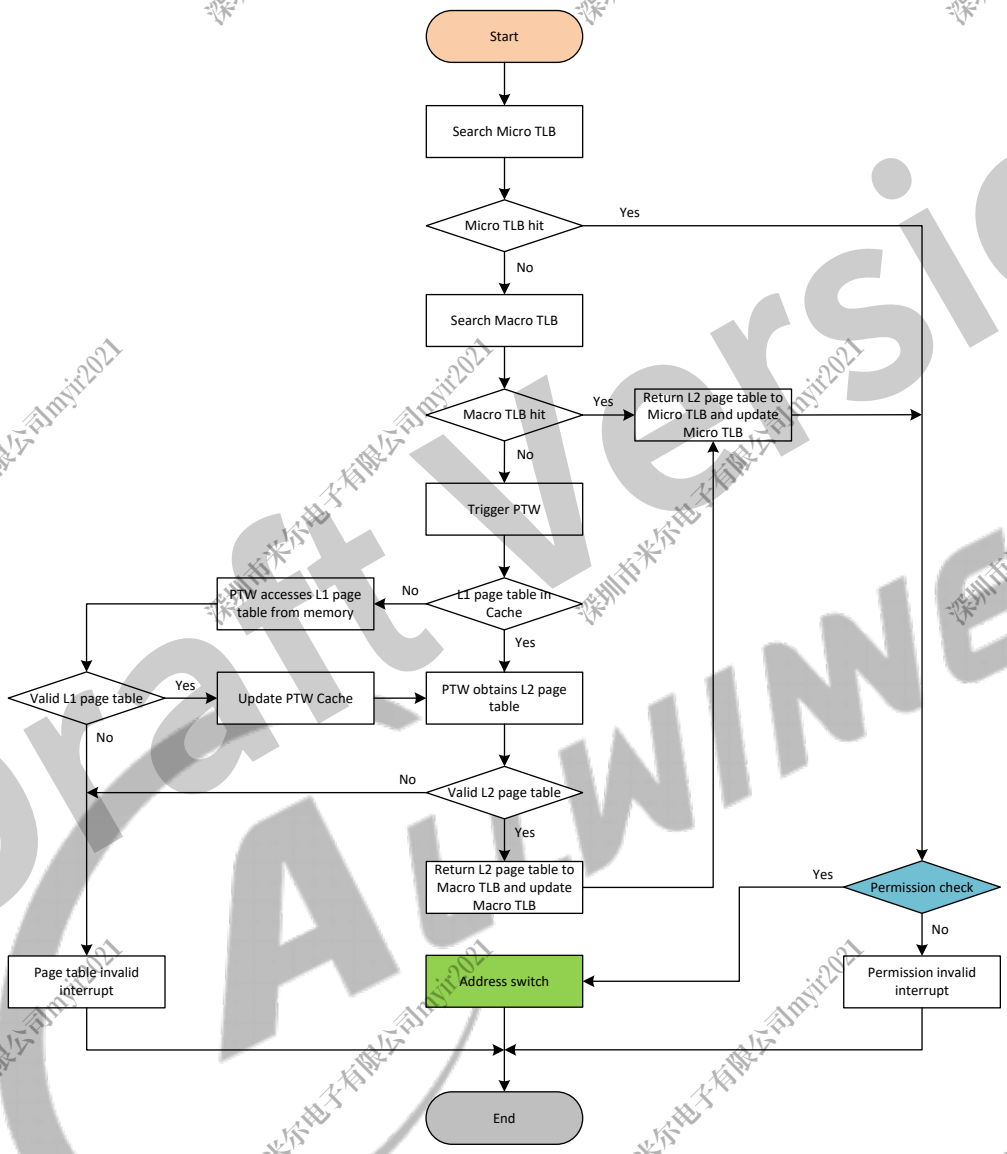
The internal address translation process is shown in the following figure.

Figure 2-16 Internal Switch Process



2.11.3.3 VA-PA Mapping

IOMMU page table is defined as the Level2 mapping. The first level is 1M address space mapping, the second level is 4K address space. This version does not support 1K, 16K and other page table sizes. IOMMU only supports a page table, the meaning is:

- All peripherals connected to IOMMU use the same virtual address space;
- The virtual address space of the peripherals can overlap;
- Different virtual addresses can map to the same physical address space;

Base address of this page table is defined by the software, and it needs 16 KB address alignment. The page table of the Level2 table item needs 1 KB address alignment. A complete VA-PA address translation process is shown in the following figure.

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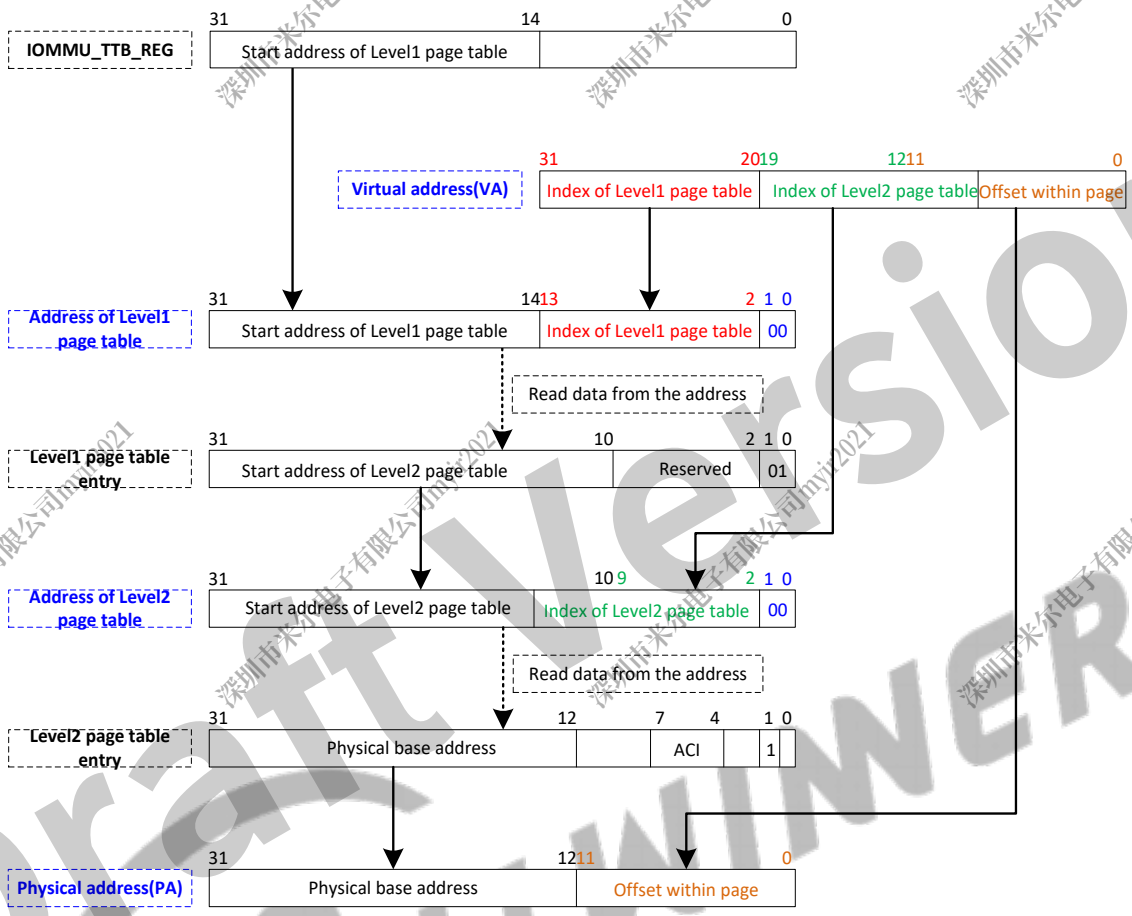
Figure 2-17 VA-PA Switch Process



2.11.3.4 Clearing and Invalidating TLB

When multi page table contents are refreshed or table address changes, all VA-PA mappings which have been cached in TLB will be invalid. You need to configure IOMMU_TLB_FLUSH_ENABLE_REG (Offset: 0x0080) to clear the TLB or PTW Cache according to the following steps:

Step 1 Suspend the access to TLB or Cache.

Step 2 Configure the corresponding Flush bit of IOMMU_TLB_FLUSH_ENABLE_REG (Offset: 0x0080).

Step 3 After the operation takes effect, the related peripherals can continue to send the new access memory operations.

When some page table is invalid or the mapping is incorrect, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. The invalid TLB supports the following two modes:

- Mode0

Step 1 Set IOMMU_TLB_IVLD_MODE_SEL_REG (Offset: 0x0084) to 0 and select mode0;

Step 2 Write the target address to IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090);

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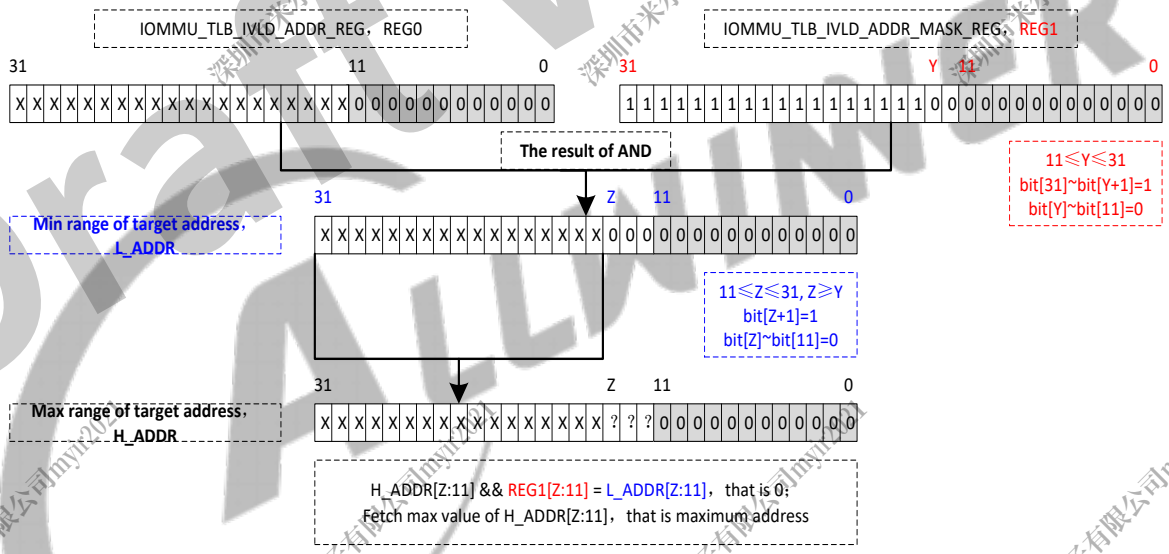
Step 3 Set the configuration values to IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094), the requirements are as follows:

- The value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) cannot be less than the IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090).
- The higher bit of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) must be continuous 1, the lower bit must be continuous 0. For example, 0xFFFFF000, 0xFFFFE000, 0xFFFFC000, 0xFFFF8000, and 0xFFFF0000 are legal values; while 0xFFFFD000, 0xFFFFB000, 0xFFFFA000, 0xFFFF9000, and 0xFFFF7000 are illegal values.

Step 4 Configure IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098) to enable the invalid operation. Among the way to determine the invalid address is to get the maximum valid bit and determine the target address range by the target address AND the mask address. The process is shown as follows.

Figure 2-18 Invalid TLB Address Range



The examples are shown below:

- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFF000 by default, the result of AND is target address. That is, only the target address is invalid.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFF0000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEEF000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFC000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEEB000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFF8000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEEC000, then target address range is from 0xEEEE8000 to 0xEEEEF000.

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- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFC000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEEE3000.

- Mode1

Step 1 Set IOMMU_TLB_IVLD_MODE_SEL_REG (Offset: 0x0084) to 1 and select mode1;

Step 2 Set the starting address and the ending address of the invalid TLB by IOMMU_TLB_IVLD_STA_ADDR_REG (Offset: 0x0088);

Step 3 Configure IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098) to enable the invalid operation, then the TLB invaliding operation can be completed.

2.11.3.5 Clearing and Invalidating PTW Cache

- Mode0

Step 1 Set IOMMU_PC_IVLD_MODE_SEL_REG (Offset: 0x009C) to 0 and select mode0.

Step 2 Invalid the IOMMU_PC_IVLD_ADDR_REG (Offset: 0x00A0), 1MB aligned.

Step 3 Configure IOMMU_PC_IVLD_ENABLE_REG (Offset: 0x00A8) to enable the invalid operation, then you can invalid one piece of CacheLine.

- Mode1

Step 1 Set IOMMU_PC_IVLD_MODE_SEL_REG (Offset: 0x009C) to 1 and select mode1.

Step 2 Set the starting address and the ending address of the invalid TLB by IOMMU_PC_IVLD_STA_ADDR_REG (Offset: 0x00A4).

Step 3 Configure IOMMU_PC_IVLD_ENABLE_REG (Offset: 0x00A8) to enable the invalid operation, then you can invalid a period of sections.

2.11.3.6 Level1 Page Table

The format of Level1 page table is as follows.

Figure 2-19 Level1 Page Table Format

31 10	9 2	1 0
Start address of Level2 page table	Reserved	01

Bit [31:10]: Base address of Level2 page table;

Bit [9:2]: Reserved;

Bit [1:0]: 01 is a valid page table; other values are fault;

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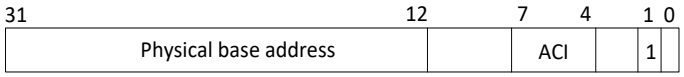
2.11.3.7 Level2 Page Table

The format of Level2 page table is as follows.

Figure 2-20 Level2 Page Table Format



Bit [31:12]: Physical address of 4K address;

Bit [11:8]: Reserved;

Bit [7:4]: ACI, permission control index; correspond to permission control bit of IOMMU Domain Authority Control Register;

Bit [3:2]: Reserved;

Bit [1]: 1 is a valid page table; 0 is fault;

Bit [0]: Reserved

2.11.4 Programming Guidelines

2.11.4.1 Resetting IOMMU

Before the IOMMU module software reset operation, make sure IOMMU is never opened, or all bus operations are completed, or DRAM and peripherals already open the corresponding switch, to shield the influence of IOMMU reset.

2.11.4.2 Enabling IOMMU

Before opening the IOMMU address mapping function, IOMMU_TTB_REG (Offset: 0x0050) should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

2.11.4.3 Configuring TTB

Operating the register must close IOMMU address mapping function, namely IOMMU_ENABLE_REG (Offset: 0x0020) is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

2.11.4.4 Clearing TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

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2.11.4.5 Reading/Writing VA Data

For the virtual address, read and write the corresponding physical address data to make sure whether IOMMU module address mapping function is normal. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after the operation is finished, check if the results are as expected.

2.11.4.6 PMU Statistics

When PMU function is used for the first time, set IOMMU_PMU_ENABLE_REG (Offset: 0x0200) to enable statistics function; when reading the relevant Register, clear the enable bit of IOMMU_PMU_ENABLE_REG (Offset: 0x0200); when PMU function is used next time, first IOMMU_PMU_CLR_REG (Offset: 0x0210) is set, after counter is cleared, set the enable bit of IOMMU_PMU_ENABLE_REG (Offset: 0x0200).

Given a Level2 page table administers continuous 4KB address, if Micro TLB misses in continuous virtual address, a Level2 page table needs to be returned from Macro TLB to hit; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So the true hit rate calculation is as follows:

Hit Rate = N1/M1 + (1-N1/M1)*N2/M2

N1: Micro TLB hit number
M1: Micro TLB access number
N2: Macro TLB hit number
M2: Macro TLB access number

2.11.5 Register List

Module Name	Base Address
IOMMU	0x0201_0000

Register Name	Offset	Description
IOMMU_RESET_REG	0x0010	IOMMU Reset Register
IOMMU_ENABLE_REG	0x0020	IOMMU Enable Register
IOMMU_BYPASS_REG	0x0030	IOMMU Bypass Register
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto Gating Register
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table Base Register
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB Enable Register
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB Prefetch Register

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Register Name	Offset	Description
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_MODE_SEL_REG	0x0084	IOMMU TLB Invalidation Mode Select Register
IOMMU_TLB_IVLD_STA_ADDR_REG	0x0088	IOMMU TLB Invalidation Start Address Register
IOMMU_TLB_IVLD_END_ADDR_REG	0x008C	IOMMU TLB Invalidation End Address Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register
IOMMU_PC_IVLD_MODE_SEL_REG	0x009C	IOMMU PC Invalidation Mode Select Register
IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register
IOMMU_PC_IVLD_STA_ADDR_REG	0x00A4	IOMMU PC Invalidation Start Address Register
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_PC_IVLD_END_ADDR_REG	0x00AC	IOMMU PC Invalidation End Address Register
IOMMU_INT_ENABLE_REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR_REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA_REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR0_REG	0x0110	IOMMU Interrupt Error Address 0 Register
IOMMU_INT_ERR_ADDR1_REG	0x0114	IOMMU Interrupt Error Address 1 Register
IOMMU_INT_ERR_ADDR2_REG	0x0118	IOMMU Interrupt Error Address 2 Register
IOMMU_INT_ERR_ADDR3_REG	0x011C	IOMMU Interrupt Error Address 3 Register
IOMMU_INT_ERR_ADDR4_REG	0x0120	IOMMU Interrupt Error Address 4 Register
IOMMU_INT_ERR_ADDR5_REG	0x0124	IOMMU Interrupt Error Address 5 Register
IOMMU_INT_ERR_ADDR6_REG	0x0128	IOMMU Interrupt Error Address 6 Register
IOMMU_INT_ERR_ADDR7_REG	0x0130	IOMMU Interrupt Error Address 7 Register
IOMMU_INT_ERR_ADDR8_REG	0x0134	IOMMU Interrupt Error Address 8 Register
IOMMU_INT_ERR_DATA0_REG	0x0150	IOMMU Interrupt Error Data 0 Register
IOMMU_INT_ERR_DATA1_REG	0x0154	IOMMU Interrupt Error Data 1 Register
IOMMU_INT_ERR_DATA2_REG	0x0158	IOMMU Interrupt Error Data 2 Register
IOMMU_INT_ERR_DATA3_REG	0x015C	IOMMU Interrupt Error Data 3 Register
IOMMU_INT_ERR_DATA4_REG	0x0160	IOMMU Interrupt Error Data 4 Register
IOMMU_INT_ERR_DATA5_REG	0x0164	IOMMU Interrupt Error Data 5 Register
IOMMU_INT_ERR_DATA6_REG	0x0168	IOMMU Interrupt Error Data 6 Register
IOMMU_INT_ERR_DATA7_REG	0x0170	IOMMU Interrupt Error Data 7 Register
IOMMU_INT_ERR_DATA8_REG	0x0174	IOMMU Interrupt Error Data 8 Register
IOMMU_L1PG_INT_REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT_REG	0x0184	IOMMU L2 Page Table Interrupt Register

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Register Name	Offset	Description
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE_REG	0x0200	IOMMU PMU Enable Register
IOMMU_PMU_CLR_REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW0_REG	0x0230	IOMMU PMU Access Low 0 Register
IOMMU_PMU_ACCESS_HIGH0_REG	0x0234	IOMMU PMU Access High 0 Register
IOMMU_PMU_HIT_LOW0_REG	0x0238	IOMMU PMU Hit Low 0 Register
IOMMU_PMU_HIT_HIGH0_REG	0x023C	IOMMU PMU Hit High 0 Register
IOMMU_PMU_ACCESS_LOW1_REG	0x0240	IOMMU PMU Access Low 1 Register
IOMMU_PMU_ACCESS_HIGH1_REG	0x0244	IOMMU PMU Access High 1 Register
IOMMU_PMU_HIT_LOW1_REG	0x0248	IOMMU PMU Hit Low 1 Register
IOMMU_PMU_HIT_HIGH1_REG	0x024C	IOMMU PMU Hit High 1 Register
IOMMU_PMU_ACCESS_LOW2_REG	0x0250	IOMMU PMU Access Low 2 Register
IOMMU_PMU_ACCESS_HIGH2_REG	0x0254	IOMMU PMU Access High 2 Register
IOMMU_PMU_HIT_LOW2_REG	0x0258	IOMMU PMU Hit Low 2 Register
IOMMU_PMU_HIT_HIGH2_REG	0x025C	IOMMU PMU Hit High 2 Register
IOMMU_PMU_ACCESS_LOW3_REG	0x0260	IOMMU PMU Access Low 3 Register
IOMMU_PMU_ACCESS_HIGH3_REG	0x0264	IOMMU PMU Access High 3 Register
IOMMU_PMU_HIT_LOW3_REG	0x0268	IOMMU PMU Hit Low 3 Register
IOMMU_PMU_HIT_HIGH3_REG	0x026C	IOMMU PMU Hit High 3 Register
IOMMU_PMU_ACCESS_LOW4_REG	0x0270	IOMMU PMU Access Low 4 Register
IOMMU_PMU_ACCESS_HIGH4_REG	0x0274	IOMMU PMU Access High 4 Register
IOMMU_PMU_HIT_LOW4_REG	0x0278	IOMMU PMU Hit Low 4 Register
IOMMU_PMU_HIT_HIGH4_REG	0x027C	IOMMU PMU Hit High 4 Register
IOMMU_PMU_ACCESS_LOW5_REG	0x0280	IOMMU PMU Access Low 5 Register
IOMMU_PMU_ACCESS_HIGH5_REG	0x0284	IOMMU PMU Access High 5 Register
IOMMU_PMU_HIT_LOW5_REG	0x0288	IOMMU PMU Hit Low 5 Register
IOMMU_PMU_HIT_HIGH5_REG	0x028C	IOMMU PMU Hit High 5 Register
IOMMU_PMU_ACCESS_LOW6_REG	0x0290	IOMMU PMU Access Low 6 Register
IOMMU_PMU_ACCESS_HIGH6_REG	0x0294	IOMMU PMU Access High 6 Register
IOMMU_PMU_HIT_LOW6_REG	0x0298	IOMMU PMU Hit Low 6 Register
IOMMU_PMU_HIT_HIGH6_REG	0x029C	IOMMU PMU Hit High 6 Register
IOMMU_PMU_ACCESS_LOW7_REG	0x02D0	IOMMU PMU Access Low 7 Register
IOMMU_PMU_ACCESS_HIGH7_REG	0x02D4	IOMMU PMU Access High 7 Register
IOMMU_PMU_HIT_LOW7_REG	0x02D8	IOMMU PMU Hit Low 7 Register
IOMMU_PMU_HIT_HIGH7_REG	0x02DC	IOMMU PMU Hit High 7 Register
IOMMU_PMU_ACCESS_LOW8_REG	0x02E0	IOMMU PMU Access Low 8 Register
IOMMU_PMU_ACCESS_HIGH8_REG	0x02E4	IOMMU PMU Access High 8 Register
IOMMU_PMU_HIT_LOW8_REG	0x02E8	IOMMU PMU Hit Low 8 Register
IOMMU_PMU_HIT_HIGH8_REG	0x02EC	IOMMU PMU Hit High 8 Register

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Register Name	Offset	Description
IOMMU_PMU_TL_LOW0_REG	0x0300	IOMMU Total Latency Low 0 Register
IOMMU_PMU_TL_HIGH0_REG	0x0304	IOMMU Total Latency High 0 Register
IOMMU_PMU_ML0_REG	0x0308	IOMMU Max Latency 0 Register
IOMMU_PMU_TL_LOW1_REG	0x0310	IOMMU Total Latency Low 1 Register
IOMMU_PMU_TL_HIGH1_REG	0x0314	IOMMU Total Latency High 1 Register
IOMMU_PMU_ML1_REG	0x0318	IOMMU Max Latency 1 Register
IOMMU_PMU_TL_LOW2_REG	0x0320	IOMMU Total Latency Low 2 Register
IOMMU_PMU_TL_HIGH2_REG	0x0324	IOMMU Total Latency High 2 Register
IOMMU_PMU_ML2_REG	0x0328	IOMMU Max Latency 2 Register
IOMMU_PMU_TL_LOW3_REG	0x0330	IOMMU Total Latency Low 3 Register
IOMMU_PMU_TL_HIGH3_REG	0x0334	IOMMU Total Latency High 3 Register
IOMMU_PMU_ML3_REG	0x0338	IOMMU Max Latency 3 Register
IOMMU_PMU_TL_LOW4_REG	0x0340	IOMMU Total Latency Low 4 Register
IOMMU_PMU_TL_HIGH4_REG	0x0344	IOMMU Total Latency High 4 Register
IOMMU_PMU_ML4_REG	0x0348	IOMMU Max Latency 4 Register
IOMMU_PMU_TL_LOW5_REG	0x0350	IOMMU Total Latency Low 5 Register
IOMMU_PMU_TL_HIGH5_REG	0x0354	IOMMU Total Latency High 5 Register
IOMMU_PMU_ML5_REG	0x0358	IOMMU Max Latency 5 Register
IOMMU_PMU_TL_LOW6_REG	0x0360	IOMMU Total Latency Low 6 Register
IOMMU_PMU_TL_HIGH6_REG	0x0364	IOMMU Total Latency High 6 Register
IOMMU_PMU_ML6_REG	0x0368	IOMMU Max Latency 6 Register

2.11.6 Register Description

2.11.6.1 0x0010 IOMMU Reset Register (Default Value: 0x8003_007F)

Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	IOMMU_RST IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; or all bus operations are completed; or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset.
30:18	/	/	/

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Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x1	PC_RST PTW Cache address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, this bit is used to reset PTW Cache individually.
16	R/W	0x1	MTLB_RST Macro TLB address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Macro TLB occurs abnormal, this bit is used to reset Macro TLB individually.
15:7	/	/	/
6	R/W	0x1	M6_RST Master6 address convert lane software reset switch 0: Set reset signal 1: Release reset signal When Master6 occurs abnormal, this bit is used to reset Master6 individually.
5	R/W	0x1	M5_RST Master5 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, this bit is used to reset Master5 individually.
4	R/W	0x1	M4_RST Master4 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, this bit is used to reset Master4 individually.
3	R/W	0x1	M3_RST Master3 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, this bit is used to reset Master3 individually.

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Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x1	M2_RST Master2 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, this bit is used to reset Master2 individually.
1	R/W	0x1	M1_RST Master1 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master1 occurs abnormal, this bit is used to reset Master1 individually.
0	R/W	0x1	M0_RST Master0 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, this bit is used to reset Master0 individually.

2.11.6.2 0x0020 IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	I ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU Before IOMMU address mapping function opens, configure the Translation Table Base register; or ensure all masters are in bypass status or no the status of sending bus demand(such as reset)

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2.11.6.3 0x0030 IOMMU Bypass Register (Default Value: 0x0000_007f)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	M6_BP Master6 bypass switch After bypass function is opened, IOMMU can not map the address of Master6 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
5	R/W	0x1	M5_BP Master5 bypass switch After bypass function is opened, IOMMU can not map the address of Master5 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
4	R/W	0x1	M4_BP Master4 bypass switch After bypass function is opened, IOMMU can not map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
3	R/W	0x1	M3_BP Master3 bypass switch After bypass function is opened, IOMMU can not map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
2	R/W	0x1	M2_BP Master2 bypass switch After bypass function is opened, IOMMU can not map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

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Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	M1_BP Master1 bypass switch After bypass function is opened, IOMMU can not map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
0	R/W	0x1	M0_BP Master0 bypass switch After bypass function is opened, IOMMU can not map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

NOTE

- Operating the register belongs to non-accurate timing sequence control function. That is, before the function is valid, master operation will complete address mapping function, and any subsequent operation will not perform address mapping.
- It is suggested that master is in reset state or in no any bus operation before operating the register.

2.11.6.4 0x0040 IOMMU Auto Gating Register (Default Value: 0x0000_0001)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	IOMMU_AUTO_GATING IOMMU circuit auto gating control The purpose is to decrease power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

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2.11.6.5 0x0044 IOMMU Write Buffer Control Register (Default Value: 0x0000_007f)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	Reserved
5	R/W	0x1	Reserved
4	R/W	0x1	Reserved
3	R/W	0x1	Reserved
2	R/W	0x1	Reserved
1	R/W	0x1	Reserved
0	R/W	0x1	Reserved

2.11.6.6 0x0048 IOMMU Out of Order Control Register (Default Value: 0x0000_007F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	M6_OOO_CTRL. Master6 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
5	R/W	0x1	M5_OOO_CTRL. Master5 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
4	R/W	0x1	M4_OOO_CTRL. Master4 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
3	R/W	0x1	M3_OOO_CTRL. Master3 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
2	R/W	0x1	M2_OOO_CTRL. Master2 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
1	R/W	0x1	M1_OOO_CTRL. Master1 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order

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Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	M0_OOO_CTRL. Master0 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order

2.11.6.7 0x004C IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_007F)

NOTE

When the virtual address sent by master is over the 4 KB boundary, 4 KB protection unit will split it into two serial access.

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	M6_4KB_BDY_PRT_CTRL Master6 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
5	R/W	0x1	M5_4KB_BDY_PRT_CTRL Master4 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
4	R/W	0x1	M4_4KB_BDY_PRT_CTRL Master4 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
3	R/W	0x1	M3_4KB_BDY_PRT_CTRL Master3 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
2	R/W	0x1	M2_4KB_BDY_PRT_CTRL Master2 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
1	R/W	0x1	M1_4KB_BDY_PRT_CTRL Master1 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect

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Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	M0_4KB_BDY_PRT_CTRL Master0 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect

2.11.6.8 0x0050 IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: IOMMU_TTB_REG
Bit	Read/Write	Default/Hex	Description
31:14	R/W	0x0	TTB Translation Table Base Level1 page table starting address, aligned to 16 KB. When operating the register, IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0; Or Bypass function of all main equipment is set to 1, or no the state of transfer bus commands (such as setting).
13:0	/	/	/

2.11.6.9 0x0060 IOMMU TLB Enable Register (Default Value: 0x0003_007F)

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	PC_EN PTW Cache Enable 0: Disable 1: Enbale
16	R/W	0x1	MICRO_TLB_ENABLE Micro TLB enable bit 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	MICRO_TLB6_ENABLE Micro TLB6 enable bit 0: Disable 1: Enable

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Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable
5	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable
4	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
3	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO1_TLB0_ENABLE Micro TLB01 enable bit 0: Disable 1: Enable
1	R/W	0x1	MACRO0_TLB_ENABLE Macro TLB0 enable bit 0: Disable 1: Enable
0	R/W	0x1	PC_EN PTW Cache Enable 0: Disable 1: Enbale

2.11.6.10 0x0070 IOMMU TLB PreFetch Register (Default Value: 0x0003_0000)

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	PF_VL_PT_TO_PC Prefetch Value Page Table to PTW Cache 0: Disable 1: Enable If the function is enabled, the prefetch function will not update the invalid Level1 page table to PTW cache.

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Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x1	PF_VL_PT_TO_MT Prefetch Value Page Table to Macro TLB 0: Disable 1: Enable If the function is enabled, the prefetch function will not update the invalid Level2 page table to Macro TLB.
15:7	/	/	/
6	R/W	0x0	MI_TLB6_PF Micro TLB6 Prefetch Enable 0: Disable 1: Enable
5	R/W	0x0	MI_TLB5_PF Micro TLB5 Prefetch Enable 0: Disable 1: Enable
4	R/W	0x0	MI_TLB4_PF Micro TLB4 Prefetch Enable 0: Disable 1: Enable
3	R/W	0x0	MI_TLB3_PF Micro TLB3 Prefetch Enable 0: Disable 1: Enable If G2D accesses DDR, it is suggested to disable the prefetch function.
2	R/W	0x0	MI_TLB2_PF Micro TLB2 Prefetch Enable 0: Disable 1: Enable
1	R/W	0x0	MI_TLB1_PF Micro TLB1 Prefetch Enable 0: Disable 1: Enable
0	R/W	0x0	MI_TLB0_PF Micro TLB0 Prefetch Enable 0: Disable 1: Enable

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2.11.6.11 0x0080 IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

When performing flush operations, all TLB/Cache access will be paused.

Before flush starts, the operation that has entered will continue until it finishes.

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PC_FS PTW Cache Flush Clear PTW Cache 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
16	R/WAC	0x0	MA_TLB_FS Macro TLB Flush Clear Macro TLB 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
15:7	/	/	/
6	R/WAC	0x0	MI_TLB6_FS Micro TLB6 Flush Clear Micro TLB6 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
5	R/WAC	0x0	MI_TLB5_FS Micro TLB5 Flush Clear Micro TLB5 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.

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Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
4	R/WAC	0x0	MI_TLB4_FS Micro TLB4 Flush Clear Micro TLB4 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
3	R/WAC	0x0	MI_TLB3_FS Micro TLB3 Flush Clear Micro TLB3 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
2	R/WAC	0x0	MI_TLB2_FS Micro TLB2 Flush Clear Micro TLB2 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
1	R/WAC	0x0	MI_TLB1_FS Micro TLB1 Flush Clear Micro TLB1 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
0	R/WAC	0x0	MI_TLB0_FS Micro TLB0 Flush Clear Micro TLB0 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.

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2.11.6.12 0x0084 IOMMU TLB Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TLB_IVLD_MODE_SEL 0: Invalidate TLB by using the Mask mode 1: Invalidate TLB by using the Start and End mode

2.11.6.13 0x0088 IOMMU TLB Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: IOMMU_TLB_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_SA TLB Invalid Start Address TLB invalid start address, 4 KB aligned.
11:0	/	/	/

2.11.6.14 0x008C IOMMU TLB Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: IOMMU_TLB_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_EA TLB Invalid End Address TLB invalid end address, 4 KB aligned.
11:0	/	/	/

2.11.6.15 0x0090 IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_ADDR TLB Invalid Address TLB invalid address, 4 KB aligned
11:0	/	/	/

Operation:

- Set the virtual address that needs to be operated in IOMMU_TLB_IVLD_ADDR_REG.
- Set the mask of virtual address that needs to be operated in IOMMU_TLB_IVLD_ADDR_MASK_REG.

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- Write '1' to IOMMU_TLB_IVLD_ENABLE_REG [0].
- Read IOMMU_TLB_IVLD_ENABLE_REG [0], when it is '0', it indicates that invalidation behavior is finished.

NOTE

- When performing invalidation operation, TLB/Cache operation has not affected.
- After or before invalidation operation starts, there is no absolute relationship between the same address switch operation and invalidation operation.

2.11.6.16 0x0094 IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB Invalid Address Mask TLB invalid address mask register, 4 KB aligned
11:0	/	/	/

2.11.6.17 0x0098 IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	TLB_IVLD_ENABLE: Enable TLB invalidation operation 0: No operation or operation is completed 1: Enable invalidation operation After invalidation operation is completed, the bit can clear automatically. When operating invalidation operation, TLB/Cache operation has not affected. After or before invalidation operation starts, there is no absolute relationship between the same address switch operation and invalidation operation.

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2.11.6.18 0x009C IOMMU PC Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: IOMMU_PC_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PC_IVLD_MS. PTW Cache Invalid Mode Select. 0: Invalidate PTW by using the Mask mode 1: Invalidate PTW by using the Start and End mode

2.11.6.19 0x00A0 IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_ADDR. PTW Cache Invalid Address, 1 MB aligned.
19:0	/	/	/

2.11.6.20 0x00A4 IOMMU PC Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: IOMMU_PC_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_SA. PTW Cache Invalid Start Address, 1M aligned.
19:0	/	/	/

2.11.6.21 0x00A8 IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: IOMMU_PC_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PC_IVLD_EN. Enable PTW Cache invalidation operation 0: No operation or operation is completed 1: Enable invalidation operation After invalidation operation is completed, the bit can clear automatically. After or before invalidation operation starts, there is no absolute relationship between the same address switch operation and invalidation operation.

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2.11.6.22 0x00AC IOMMU PC Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: IOMMU_PC_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_EA. PTW Cache invalid end address, 1 MB aligned.
19:0	/	/	/

2.11.6.23 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Invalid page table and permission error can not make one device or multi-devices in system work normally.

Permission error usually happens in MicroTLB. The error generates interrupt and waits for processing through software.

Invalid page table usually happens in Macro TLB. The error can not influence the access of other devices. So the error page table needs go back the way it comes, but the error should not be written in each level TLB.

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	DBG_PF_L2_IV_PT_EN. Debug or Prefetch Invalid Page Table Enable 0: Mask interrupt 1: Enable interrupt
19	R/W	0x0	DBG_PF_PC_IV_L1_PT_EN. Debug or Prefetch PTW Cache Invalid Level1 Page Table Enable 0: Mask interrupt 1: Enable interrupt
18	R/W	0x0	DBG_PF_DRAM_IV_L1_PT_EN. Debug or Prefetch DRAM Invalid Level1 Page Table Enable 0: Mask interrupt 1: Enable interrupt
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

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Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN Micro TLB6 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

2.11.6.24 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

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Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt **Note: The bit is not used.**
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt

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2.11.6.25 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens **Note: The bit is not used.**
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

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2.11.6.26 0x0110 IOMMU Interrupt Error Address 0 Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR0. Interrupt Error Address0. Virtual address that caused Micro TLB0 to interrupt

2.11.6.27 0x0114 IOMMU Interrupt Error Address 1 Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR1. Interrupt Error Address1. Virtual address that caused Micro TLB1 to interrupt

2.11.6.28 0x0118 IOMMU Interrupt Error Address 2 Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR2. Interrupt Error Address2. Virtual address that caused Micro TLB2 to interrupt

2.11.6.29 0x011C IOMMU Interrupt Error Address 3 Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR3. Interrupt Error Address3. Virtual address that caused Micro TLB3 to interrupt

2.11.6.30 0x0120 IOMMU Interrupt Error Address 4 Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR4. Interrupt Error Address4. Virtual address that caused Micro TLB4 to interrupt

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2.11.6.31 0x0124 IOMMU Interrupt Error Address 5 Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR5. Interrupt Error Address5. Virtual address that caused Micro TLB5 to interrupt

2.11.6.32 0x0128 IOMMU Interrupt Error Address 6 Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR6. Interrupt Error Address6. Virtual address that caused Micro TLB6 to interrupt

2.11.6.33 0x0130 IOMMU Interrupt Error Address 7 Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR7. Interrupt Error Address7. Virtual address that caused L1 page table to interrupt

2.11.6.34 0x0134 IOMMU Interrupt Error Address 8 Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR8. Interrupt Error Address8. Virtual address that caused L2 page table to interrupt

2.11.6.35 0x0150 IOMMU Interrupt Error Data 0 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA0. Interrupt Error Data0. Corresponding page table of virtual address that caused Micro TLB0 to interrupt

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2.11.6.36 0x0154 IOMMU Interrupt Error Data 1 Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA1. Interrupt Error Data1. Corresponding page table of virtual address that caused Micro TLB1 to interrupt

2.11.6.37 0x0158 IOMMU Interrupt Error Data 2 Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA2. Interrupt Error Data2. Corresponding page table of virtual address that caused Micro TLB2 to interrupt

2.11.6.38 0x015C IOMMU Interrupt Error Data 3 Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA3. Interrupt Error Data3. Corresponding page table of virtual address that caused Micro TLB3 to interrupt

2.11.6.39 0x0160 IOMMU Interrupt Error Data 4 Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA4. Interrupt Error Data4. Corresponding page table of virtual address that caused Micro TLB4 to interrupt

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2.11.6.40 0x0164 IOMMU Interrupt Error Data 5 Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA5. Interrupt Error Data5. Corresponding page table of virtual address that caused Micro TLB5 to interrupt

2.11.6.41 0x0168 IOMMU Interrupt Error Data 6 Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA6. Interrupt Error Data6. Corresponding page table of virtual address that caused Micro TLB6 to interrupt

2.11.6.42 0x0170 IOMMU Interrupt Error Data 7 Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA7. Interrupt Error Data7. Corresponding page table of virtual address that caused L1 page table to interrupt

2.11.6.43 0x0174 IOMMU Interrupt Error Data 8 Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA8. Interrupt Error Data8. Corresponding page table of virtual address that caused L2 page table to interrupt

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2.11.6.44 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L1PG_INT Debug mode address switch causes L1 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT Master6 address switch causes L1 page table to occur interrupt.
5	R	0x0	MASTER5_L1PG_INT Master5 address switch causes L1 page table to occur interrupt.
4	R	0x0	MASTER4_L1PG_INT Master4 address switch causes L1 page table to occur interrupt.
3	R	0x0	MASTER3_L1PG_INT Master3 address switch causes L1 page table to occur interrupt.
2	R	0x0	MASTER2_L1PG_INT Master2 address switch causes L1 page table to occur interrupt.
1	R	0x0	MASTER1_L1PG_INT Master1 address switch causes L1 page table to occur interrupt.
0	R	0x0	MASTER0_L1PG_INT Master0 address switch causes L1 page table to occur interrupt.

2.11.6.45 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L2PG_INT Debug mode address switch causes L2 page table to occur interrupt.
30:7	/	/	/

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Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
6	R	0x0	MASTER6_L2PG_INT Master6 address switch causes L2 page table to occur interrupt. **Note: The bit is not used.**
5	R	0x0	MASTER5_L2PG_INT Master5 address switch causes L2 page table to occur interrupt.
4	R	0x0	MASTER4_L2PG_INT Master4 address switch causes L2 page table to occur interrupt.
3	R	0x0	MASTER3_L2PG_INT Master3 address switch causes L2 page table to occur interrupt.
2	R	0x0	MASTER2_L2PG_INT Master2 address switch causes L2 page table to occur interrupt.
1	R	0x0	MASTER1_L2PG_INT Master1 address switch causes L2 page table to occur interrupt.
0	R	0x0	MASTER0_L2PG_INT Master0 address switch causes L2 page table to occur interrupt.

2.11.6.46 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA Virtual address of read/write

2.11.6.47 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA_DATA Data corresponding to read/write virtual address

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2.11.6.48 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MODE_SEL 0: Prefetch 1: Debug Mode It is used to choose prefetch mode or Debug mode.
30:9	/	/	/
8	R/W	0x0	VA_CONFIG Virtual Address Configuration 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation is completed 1: Start After the operation is completed, the bit can clear automatically.

Read operation process:

- Write IOMMU_VA_REG [31:0];
- Write IOMMU_VA_CONFIG_REG [8] to 0;
- Write IOMMU_VA_CONFIG_REG [0] to 1 to start read-process;
- Query IOMMU_VA_CONFIG_REG [0] until it is 0;
- Read IOMMU_VA_DATA_REG [31:0].

Write operation process:

- Write IOMMU_VA_REG [31:0];
- Write IOMMU_VA_DATA_REG [31:0];
- Write IOMMU_VA_CONFIG_REG [8] to 1;
- Write IOMMU_VA_CONFIG_REG [0] to 1 to start write-process;
- Query IOMMU_VA_CONFIG_REG [0] until it is 0.

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2.11.6.49 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disable statistical function 1: Enable statistical function

2.11.6.50 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation is completed 1: Clear counter data After the operation is completed, the bit can clear automatically.

2.11.6.51 0x0230 IOMMU PMU Access Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW0 Record total number of Micro TLB0 access, lower 32-bit register.

2.11.6.52 0x0234 IOMMU PMU Access High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record total number of Micro TLB0 access, higher 32-bit register

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2.11.6.53 0x0238 IOMMU PMU Hit Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW0 Record total number of Micro TLB0 hit, lower 32-bit register.

2.11.6.54 0x023C IOMMU PMU Hit High 0 Register (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record total number of Micro TLB0 hit, higher 32-bit register.

2.11.6.55 0x0240 IOMMU PMU Access Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW1 Record total number of Micro TLB1 access, lower 32-bit register.

2.11.6.56 0x0244 IOMMU PMU Access High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH1 Record total number of Micro TLB1 access, higher 32-bit register.

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2.11.6.57 0x0248 IOMMU PMU Hit Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW1 Record total number of Micro TLB1 hit, lower 32-bit register.

2.11.6.58 0x024C IOMMU PMU Hit High 1 Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record total number of Micro TLB1 hit, higher 11-bit register.

2.11.6.59 0x0250 IOMMU PMU Access Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW2 Record total number of Micro TLB2 access, lower 32-bit register.

2.11.6.60 0x0254 IOMMU PMU Access High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record total number of Micro TLB2 access, higher 11-bit register.

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2.11.6.61 0x0258 IOMMU PMU Hit Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW2 Record total number of Micro TLB2 hit，lower 32-bit register.

2.11.6.62 0x025C IOMMU PMU Hit High 2 Register (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record total number of Micro TLB2 hit，higher 11-bit register.

2.11.6.63 0x0260 IOMMU PMU Access Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW3 Record total number of Micro TLB3 access, lower 32-bit register.

2.11.6.64 0x0264 IOMMU PMU Access High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record total number of Micro TLB3 access, higher 11-bit register.

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2.11.6.65 0x0268 IOMMU PMU Hit Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW3 Record total number of Micro TLB3 hit，lower 32-bit register.

2.11.6.66 0x026C IOMMU PMU Hit High 3 Register (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record total number of Micro TLB3 hit，higher 11-bit register.

2.11.6.67 0x0270 IOMMU PMU Access Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW4 Record total number of Micro TLB4 access, lower 32-bit register.

2.11.6.68 0x0274 IOMMU PMU Access High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record total number of Micro TLB4 access, higher 11-bit register.

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2.11.6.69 0x0278 IOMMU PMU Hit Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW4 Record total number of Micro TLB4 hit，lower 32-bit register.

2.11.6.70 0x027C IOMMU PMU Hit High 4 Register (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record total number of Micro TLB4 hit，higher 11-bit register.

2.11.6.71 0x0280 IOMMU PMU Access Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW5 Record total number of Micro TLB5 access, lower 32-bit register.

2.11.6.72 0x0284 IOMMU PMU Access High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record total number of Micro TLB5 access, higher 11-bit register.

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2.11.6.73 0x0288 IOMMU PMU Hit Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW5 Record total number of Micro TLB5 hit，lower 32-bit register.

2.11.6.74 0x028C IOMMU PMU Hit High 5 Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record total number of Micro TLB5 hit，higher 11-bit register.

2.11.6.75 0x0290 IOMMU PMU Access Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW6 Record total number of Micro TLB6 access, lower 32-bit register.

2.11.6.76 0x0294 IOMMU PMU Access High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record total number of Micro TLB6 access, higher 11-bit register.

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2.11.6.77 0x0298 IOMMU PMU Hit Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW6 Record total number of Micro TLB6 hit，lower 32-bit register.

2.11.6.78 0x029C IOMMU PMU Hit High 6 Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record total number of Micro TLB6 hit，higher 11-bit register.

2.11.6.79 0x02D0 IOMMU PMU Access Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW7 Record total number of Macro TLB access, lower 32-bit register.

2.11.6.80 0x02D4 IOMMU PMU Access High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record total number of Macro TLB access, higher 11-bit register.

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2.11.6.81 0x02D8 IOMMU PMU Hit Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW7 Record total number of Macro TLB hit，lower 32-bit register.

2.11.6.82 0x02DC IOMMU PMU Hit High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record total number of Macro TLB hit，higher 11-bit register.

2.11.6.83 0x02E0 IOMMU PMU Access Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW8 Record total number of PTW Cache access, lower 32-bit register.

2.11.6.84 0x02E4 IOMMU PMU Access High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH8 Record total number of PTW Cache access, higher 11-bit register.

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2.11.6.85 0x02E8 IOMMU PMU Hit Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW8 Record total number of PTW Cache hit，lower 32-bit register.

2.11.6.86 0x02EC IOMMU PMU Hit High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record total number of PTW Cache hit，higher 11-bit register.

2.11.6.87 0x0300 IOMMU Total Latency Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW0 Record total latency of Master0, lower 32-bit register.

2.11.6.88 0x0304 IOMMU Total Latency High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record total latency of Master0, higher 18-bit register.

2.11.6.89 0x0308 IOMMU Max Latency 0 Register (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML0 Record the max latency of Master0.

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2.11.6.90 0x0310 IOMMU Total Latency Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW1 Record total latency of Master1, lower 32-bit register.

2.11.6.91 0x0314 IOMMU Total Latency High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record total latency of Master1, higher 18-bit register.

2.11.6.92 0x0318 IOMMU Max Latency 1 Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML1 Record the max latency of Master1.

2.11.6.93 0x0320 IOMMU Total Latency Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW2 Record total latency of Master2, lower 32-bit register.

2.11.6.94 0x0324 IOMMU Total Latency High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record total latency of Master2, higher 18-bit register.

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2.11.6.95 0x0328 IOMMU Max Latency 2 Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML2 Record the max latency of Master2.

2.11.6.96 0x0330 IOMMU Total Latency Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW3 Record total latency of Master3, lower 32-bit register.

2.11.6.97 0x0334 IOMMU Total Latency High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record total latency of Master3, higher 18-bit register.

2.11.6.98 0x0338 IOMMU Max Latency 3 Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML3 Record the max latency of Master3.

2.11.6.99 0x0340 IOMMU Total Latency Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW4 Record total latency of Master4, lower 32-bit register.

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2.11.6.1000x0344 IOMMU Total Latency High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record total latency of Master4, higher 18-bit register.

2.11.6.1010x0348 IOMMU Max Latency 4 Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML4 Record the max latency of Master4.

2.11.6.1020x0350 IOMMU Total Latency Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW5 Record total latency of Master5, lower 32-bit register.

2.11.6.1030x0354 IOMMU Total Latency High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH5 Record total latency of Master5, higher 18-bit register.

2.11.6.1040x0358 IOMMU Max Latency 5 Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML5 Record the max latency of Master5.

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2.11.6.1050x0360 IOMMU Total Latency Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW6 Record total latency of Master6, lower 32-bit register.

2.11.6.1060x0364 IOMMU Total Latency High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record total latency of Master6, higher 18-bit register.

2.11.6.1070x0368 IOMMU Max Latency 6 Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: IOMMU_PMU_ML6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML6 Record the max latency of Master6.

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2.12 Message Box (MSGBOX)

2.12.1 Overview

The Message Box (MSGBOX) provides interrupt communication mechanism for on-chip processor.

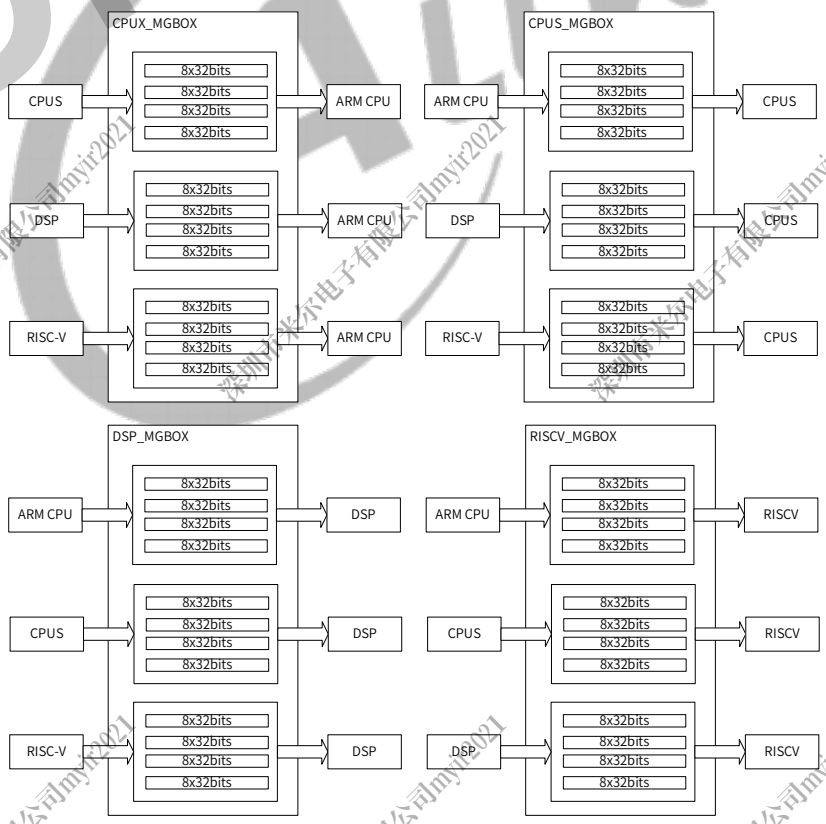
The MSGBOX has the following features:

- Supports communication between two CPUs through one way channels. Each CPU has one MSGBOX and can only read or write in one communication
  - CPUX_MSGBOX: CPUS/DSP/RISC-V write; ARM CPU read
  - CPUS_MSGBOX: ARM CPU/DSP/RISC-V write; CPUS read
  - DSP_MSGBOX: ARM CPU/CPUS/RISC-V write; DSP read
  - RISCV_MSGBOX: ARM CPU/DSP/CPUS write; RISC-V read
- The channel between two CPU has 4 channels, and the FIFO depth of a channel is 8 x 32 bits
- Supports interrupts

2.12.2 Block Diagram

The following figure shows the block diagram of the message box.

Figure 2-21 Message Box Block Diagram



For CPUX_MSGBOX: CPUS/DSP/RISC-V: Write; ARM CPU: Read.
For CPUS_MSGBOX: ARM CPU/DSP/RISC-V: Write; CPUS: Read.
For DSP_MSGBOX: ARM CPU/CPUS/RISC-V: Write; DSP Read
For RISCV_MSGBOX: ARM CPU/CPUS/DSP: Write; RISC-V: Read.

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Each CPU has 4 channels. The two channels can be configured to be secure by software, the other two channels can be configured to be non-secure by software. The two secure channels or two non-secure channels can be configured as one synchronous box (Sending a message requires a response) or one asynchronous box (Sending a message does not require a response).

2.12.3 Functional Description

2.12.3.1 Clock and Reset

The MSGBOX is mounted on AHB. Before accessing the MSGBOX registers, you need to de-assert the MSGBOX reset signal on AHB bus and then open the MSGBOX gating signal on AHB bus.

2.12.3.2 Transmitter/Receiver Mode

At the same channel, user1 is fixed as transmitter, user0 is fixed as receiver.

2.12.3.3 Typical Application

Several masters can build communication by configuring the MSGBOX. The communication parties have 4 channels. In a channel, the user1 is fixed as the transmitter and the user0 is fixed as the receiver. During the communication process, the current status can be judged through the interrupt or FIFO status.

2.12.3.4 Interrupt

Each channel can configure indepedently the interrupt enable bit, a read interrupt will be generated when the channel is empty, a write interrupt will be generated when the channel is non-full. For each CPU, all channels generate a read interrupt together, that is, if only a channel is non-full, the read interrupt will be generated, this channel can be obtained by quering the interrupt status register.

2.12.3.5 FIFO Status

When channel FIFO is non-full, the FIFO_NOT_AVA_FLAG is 0, at the moment the FIFO can be written.

When channel FIFO is full, the FIFO_NOT_AVA_FLAG is 1, at the moment if FIFO is written again, the first data of FIFO can be covered.

See MSGBOX_FIFO_STATUS_REG for FIFO status.

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2.12.4 Programming Guidelines

2.12.4.1 Checking the Transfer Status via the Interrupt

Follow the steps below to check the transfer status:

Step 1 Enable the interrupt for the channel: Configure the interrupt enable bits of transmitter/receiver through MSGBOX_WR_IRQ_EN_REG/MSGBOX_RD_IRQ_EN_REG. (user0: RX interrupt enable; user1: TX interrupt enable)

Step 2 Check the IRQ status of the corresponding queue through MSGBOX_WR_IRQ_STATUS_REG/MSGBOX_RD_IRQ_STATUS_REG.

- If the FIFO is not full, the channel generates a transmission interrupt to remind the transmitter to transmit data. Write data to the FIFO in the interrupt handler, then clear the pending bit of the transmitter in MSGBOX_WR_IRQ_STATUS_REG and the enable bit of the transmitter in MSGBOX_WR_IRQ_EN_REG.
- If the FIFO has new data, the channel generates a reception interrupt to remind the receiver to receive data. Read data from the FIFO in interrupt handler, then clear the pending bit of the receiver in MSGBOX_RD_IRQ_STATUS_REG and the enable bit of the receiver in MSGBOX_RD_IRQ_EN_REG.

2.12.4.2 Checking the Transfer Status via the FIFO

Follow the steps below to check the FIFO status of the corresponding queue:

- If the FIFO is not full, the transmitter fills the FIFO to 8*32 bits.
- If the FIFO is full, the receiver reads the FIFO data, and reads MSGBOX_FIFO_STATUS_REG to acquire the current FIFO data amount and the FIFO data amount before reading, which means no data is dropped.

2.12.4.3 Transmitting/Receiving Message

The following figure shows the communication process between CPUX_MSGBOX and CPUS_MSGBOX.

CPUX_MSGBOX: Receiving message

CPUS_MSGBOX: Transmitting message

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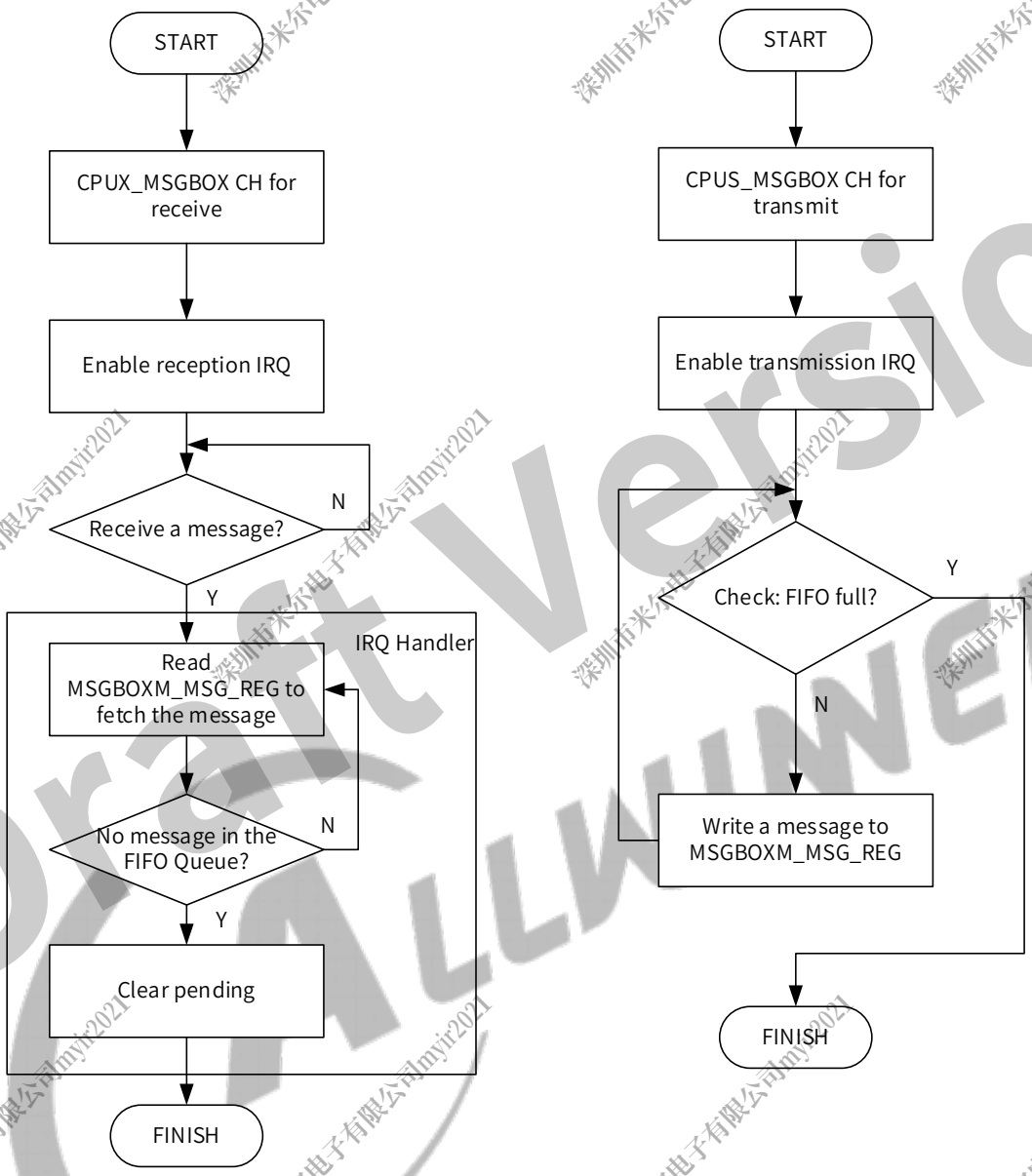
Figure 2-22 The Communication Process between CPUX_MSGBOX and CPUS_MSGBOX



2.12.5 Register List

Module Name	Base Address
CPUX_MSGBOX	0x0300 3000
CPUS_MSGBOX	0x0709 4000
DSP_MSGBOX	0x0712 0000
RISCV_MSGBOX	0x0713 6000

Parameter	Description	Value
N	The CPU numbers that communicates with the current CPU	0-2
P	The channel numbers between two communication CPU	0-3

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MSGBOX	CPU	The Value of N
CPUX_MSGBOX	CPUS->CPUX	N=0
CPUX_MSGBOX	DSP->CPUX	N=1
CPUX_MSGBOX	RISCV->CPUX	N=2
CPUS_MSGBOX	CPUX->CPUS	N=0
CPUS_MSGBOX	DSP->CPUS	N=1
CPUS_MSGBOX	RISCV->CPUS	N=2
DSP_MSGBOX	CPUX->DSP	N=0
DSP_MSGBOX	CPUS->DSP	N=1
DSP_MSGBOX	RISCV->DSP	N=2
RISCV_MSGBOX	CPUS->RISCV	N=0
RISCV_MSGBOX	DSP->RISCV	N=1
RISCV_MSGBOX	CPUX->RISCV	N=2

Register Name	Offset	Description
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100(N=0-2)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100(N=0-2)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100(N=0-2)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100(N=0-2)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100(N=0-2)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004(N=0-2)(P=0--3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004(N=0-2)(P=0-3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004(N=0-2)(P=0-3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESHOLD_REG	0x0080+N*0x0100+P*0x0004(N=0-2)(P=0-3)	MSGBOX Write IRQ Threshold Register

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2.12.6 Register Description

2.12.6.1 0x0020+N*0x0100(N=0-2) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020+N*0x0100(N=0-2)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN Reception Channel3 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 3 has received a new message.)
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN Reception Channel2 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 2 has received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN Reception Channel1 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 1 has received a new message.)
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN Reception Channel0 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

2.12.6.2 0x0024+N*0x0100(N=0-2) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0024+N*0x0100(N=0-2)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/

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Offset: 0x0024+N*0x0100(N=0-2)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND Reception Channel3 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Set one to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. Reception Channel2 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Set one to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND Reception Channel1 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Set one to this bit will clear it.
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND Reception Channel0 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Set one to this bit will clear it.

2.12.6.3 0x0030+N*0x0100(N=0-2) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x0100(N=0-2)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN Transmit Channel3 Interrupt Enable. 0: Disable 1: Enable (It will notify user 1 by interrupt when Message Queue 3 empty level reach the configured threshold.)
6	/	/	/

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Offset: 0x0030+N*0x0100(N=0-2)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN Transmit Channel2 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 2 empty level reach the configured threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN Transmit Channel1 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 1 empty level reach the configured threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN Transmit Channel0 Interrupt Enable 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 0 empty level reach the configured threshold.)
0	/	/	/

2.12.6.4 0x0034+N*0x0100(N=0-2) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0034+N*0x0100(N=0-2)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND Transmit Channel3 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configured threshold. Set one to this bit will clear it.
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND Transmit Channel2 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configured threshold. Set one to this bit will clear it.
4	/	/	/

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Offset: 0x0034+N*0x0100(N=0-2)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND Transmit Channel1 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configured threshold. Set one to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND Transmit Channel0 Interrupt Pending 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configured threshold. Set one to this bit will clear it.
0	/	/	/

2.12.6.5 0x0040+N*0x0100(N=0-2) MSGBOX Debug Register (Default Value: 0x0000_0000)

Offset: 0x0040+N*0x0100(N=0-2)			Register Name: MSGBOX_DEBUG_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0x0	FIFO_CTRL FIFO Control MQ [7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE Debug Mode In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

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2.12.6.6 0x0050+N*0x0100+P*0x0004(N=0-2) (P=0-3) MSGBOX FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050+N*0x0100+P*0x0004(N=0-2)(P=0-3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	R/W	Default/Hex	Description
31: 1	/	/	/
0	R	0x0	FIFO_NOT_AVA_FLAG FIFO is not available flag 0: The Message FIFO queue empty level is not reached the configured threshold. 1: The Message FIFO queue empty level reached the configured threshold. This FIFO status register has the status related to the message queue.

2.12.6.7 0x0060+N*0x0100+P*0x0004(N=0-2) (P=0--3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset: 0x0060+N*0x0100+P*0x0004(N=0-2)(P=0--3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0060+N*0x0100+P*0x0004(N=0-2)(P=0--3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
3:0	R	0x0	MSG_NUM Message Number Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001-1111:/

2.12.6.8 0x0070+N*0x0100+P*0x0004(N=0-2) (P=0-3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset: 0x0070+N*0x0100+P*0x0004(N=0-2)(P=0-3)			Register Name: MSGBOX_MSG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	MSG_QUE The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

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2.12.6.9 0x0080+N*0x0100+P*0x0004(N=0-2) (P=0-3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0080+N*0x0100+P*0x0004(N=0-2)(P=0-3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Configure the FIFO empty level to trigger the write interrupt for user1. 00: 1 01: 2 10: 4 11: 8

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2.13 Power Reset Clock Management (PRCM)

2.13.1 Overview

The Power Reset Clock Management (PRCM) module is one of the most import design aspects in this system. It provides a versatile supporting multiple power-management techniques. And it also manages the gating and enabling of the clocks to the device modules.

The system-level reset management provides correct reset routing and sequencing when one or more devices are stacked together in the same package. The device-level reset management provides reset routing to relevant devices, such as CPUS_TIMER, S_UART and so on.

The PRCM has the following features:

- Two PRCMs in CPUS domain: STBY_PRCM and DSP_PRCM
- 1 PLL
- CPUS Clock Configuration
- APBS Clock Configuration
- CPUS Module Clock Configuration
- CPUS Module BUS Gating and Reset
- RAM configure Control for STBY_PRCM

NOTE

- There are 15 PLLs in T527. 10 PLLs in CCU, 4 PLLs in CPUX system, and 1 PLL in DSP_PRCM.
- PRCM describes module clocks in CPUS domain.
- For clock description of CPUX system, please refer to section 2.2.3.2 CPU PLL Distribution and Clock Sources.
- For module clocks in CPUX domain (excluding the clocks of CPUX system.), please refer to section 2.7 Clock Controller Unit (CCU).

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2.13.2 Functional Description

2.13.2.1 System Bus Tree

The following figures show the diagram of the System Bus Tree.

Figure 2-23 System Bus Tree of STBY_PRCM

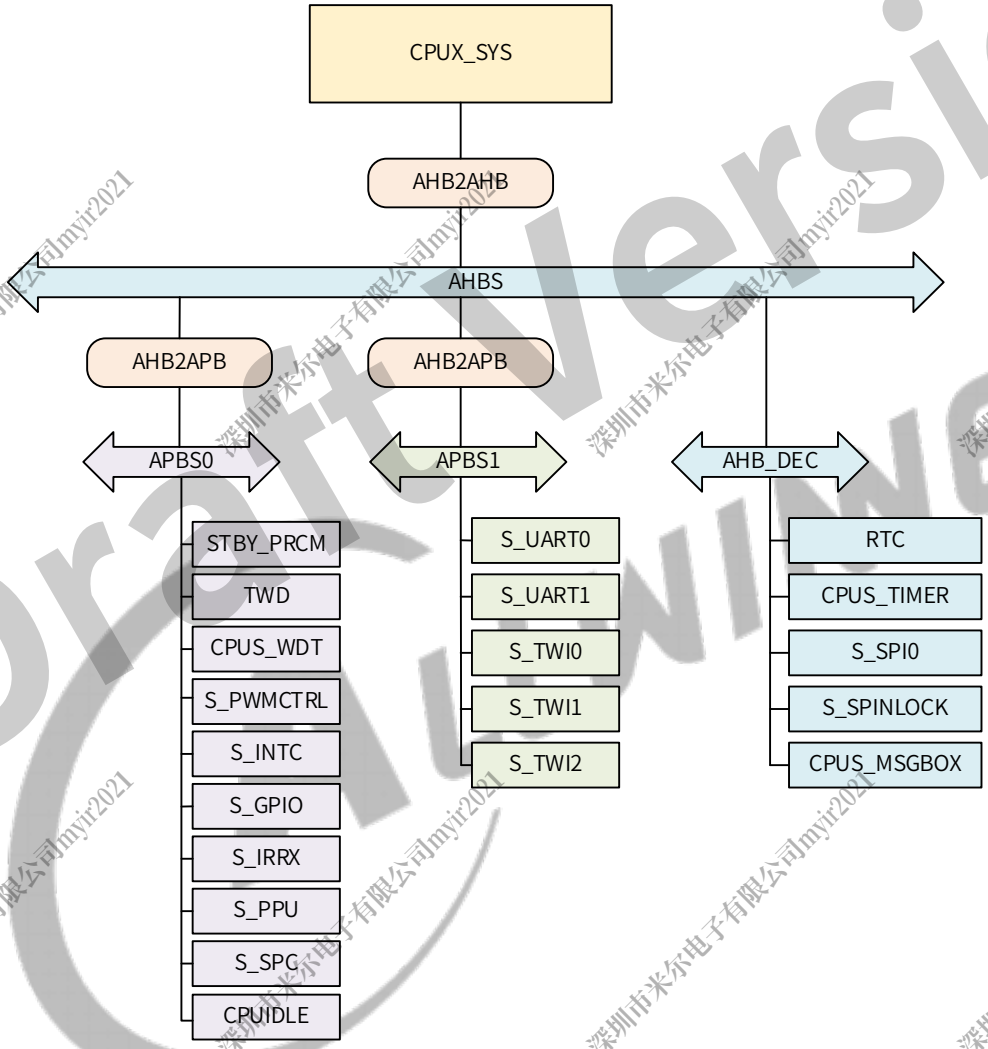

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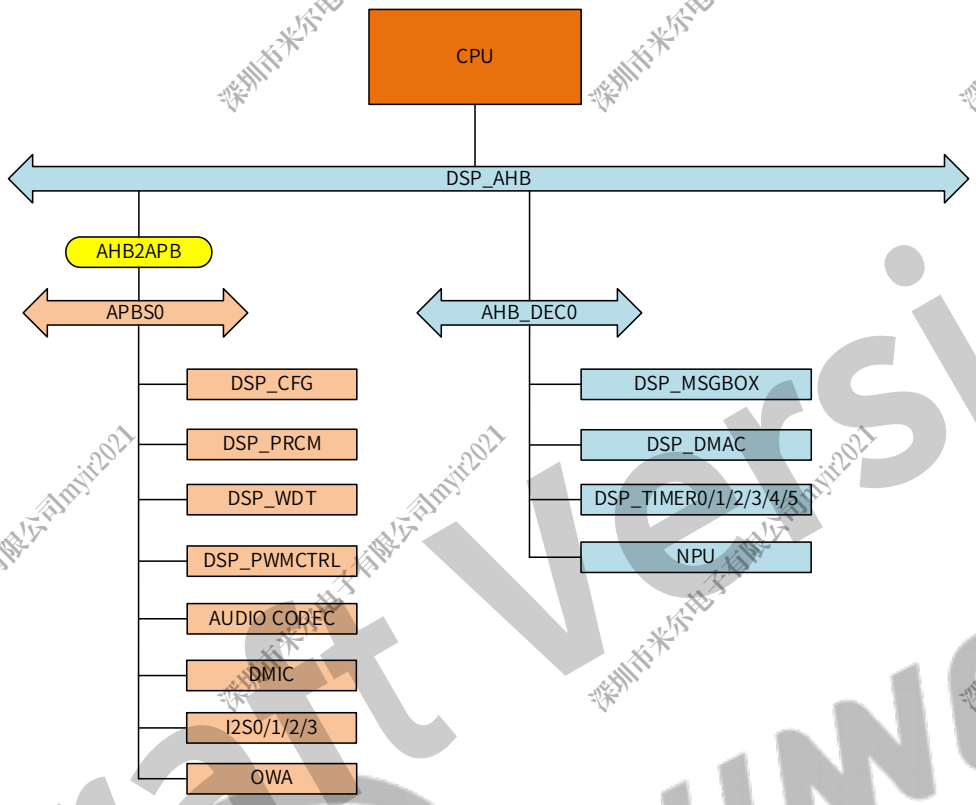
Figure 2-24 System Bus Tree of DSP_PRCM



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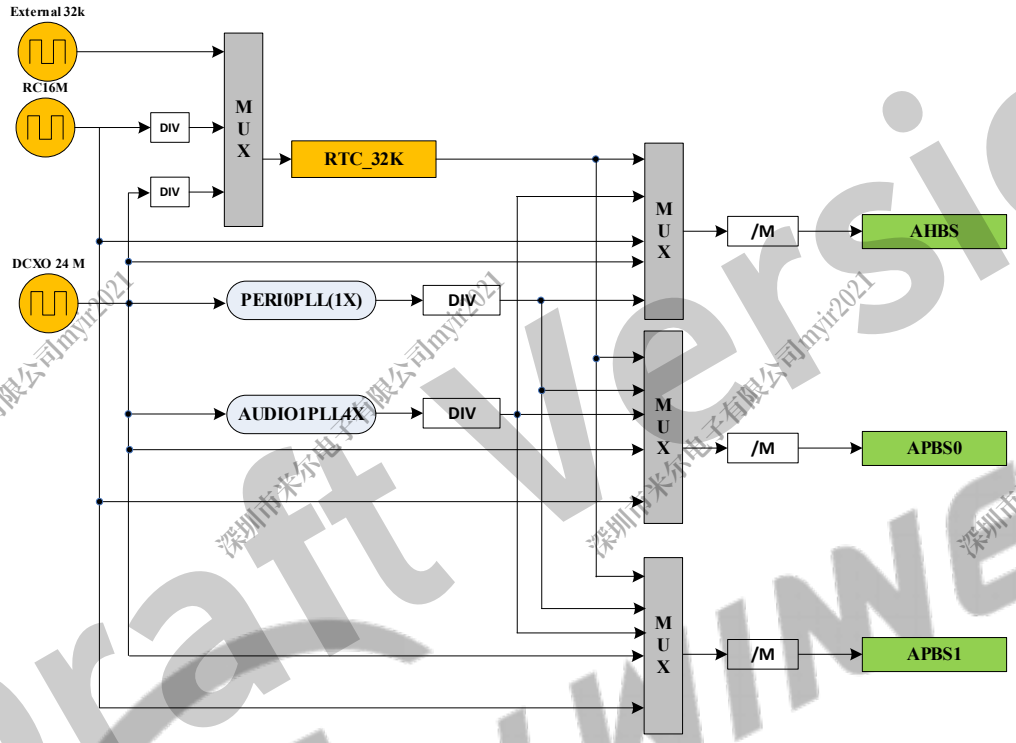
2.13.2.2 Bus Clock Tree

The following figures show a block diagram of the clock tree Diagram in CPUS domain.

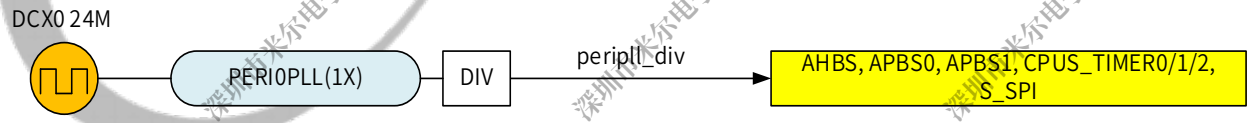
Figure 2-25 Bus Clock Tree



2.13.2.3 PLL Distribution

The following figures show the block diagram of the PLL distribution.

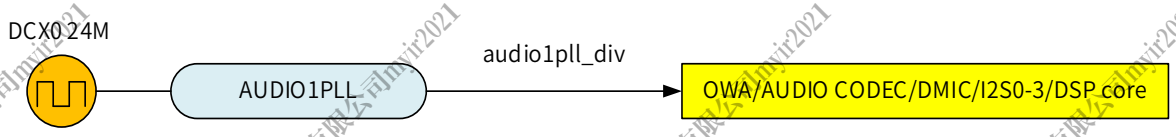
Figure 2-26 PLL Distribution of STBY_PRCM



NOTE

PERI0PLL(1X) is PERI0_600M = PERI0PLL2X/2. For detailed information of PLL_PERI0, see section 2.7.3.3 PLL Features.

Figure 2-27 PLL Distribution of DSP_PRCM



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2.13.2.4 PLL Features

The following table shows the PLL features.

Table 2-18 PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Pk-Pk	Lock Time
PLL_AUDIO1	1.52 GHz-3.1GHz	Integer mode: 1/2x: 1.536 GHz 1/5x: 614.4 MHz Decimal mode: 1/2x: 1.1179648 GHz 1/5x: 471.8592 MHz	Yes	No	< 200ps	500us

2.13.3 Programming Guidelines

2.13.3.1 Enabling the PLL

Follow the steps below to enable the PLL:

Step 1 Configure the N, M, and P factors of the PLL control register.

Step 2 Write 1 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register, write 0 to the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register.

Step 3 Write 1 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

Step 4 Wait for the status of the Lock to change to 1.

Step 5 Delay 20 us.

Step 6 Write the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register to 1 and then the PLL will be available.

2.13.3.2 Configuring the Frequency of PLL_AUDIO1

The frequency configuration formula of PLL_AUDIO1:

PLL_AUDIO1 = 24 MHz*N/M0/M1/P

PLL_AUDIO1 does not support dynamic adjustment because changing any parameter of N, M0, M1, and P will affect the normal work of PLL, and the PLL will need to be relocked.

Generally, PLL_AUDIO1 only needs two frequency points: 24.576*4 MHz or 22.5792*4 MHz. For these two frequencies, there are usually special recommended matching factors. To implement the desired frequency point of PLL_AUDIO1, you need to use the decimal frequency-division function, so follow the steps below:

Step 1 Configure the N, M0, M1 and P factors.

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Step 2 Write 1 to the PLL_SDM_EN bit (bit [24]) of PLL_AUDIO1_CTRL register.

Step 3 Configure PLL_AUDIO1_PAT0_CTRL register to enable the digital spread spectrum.

Step 4 Write 0 and then write 1 to the LOCK ENABLE bit (bit [29]) of PLL_AUDIO1_CTRL register.

Step 5 Write 1 to the LOCK bit (bit [28]) of PLL_ AUDIO1_CTRL register.

NOTE

When the P factor of PLL_AUDIO1 is an odd number, the clock output is an unequal-duty-cycle signal.

2.13.3.3 Disabling the PLL

Follow the steps below to disable the PLL:

Step 1 Write 0 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register.

Step 2 Write 0 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

2.13.3.4 Implementing Spread Spectrum

The spread spectrum technology is to convert a narrowband signal into a wideband signal. It helps to reduce the effect of electromagnetic interference (EMI) associated with the fundamental frequency of the signal.

For the general PLL frequency, the calculation formula is as follows:

$$f = \frac{N+1+X}{P\cdot(M0+1)\cdot(M1+1)}\cdot 24MHz,\ 0<X<1$$

Where,

P is the frequency division factor of module or PLL;

M0 is the post-frequzency division factor of PLL;

M1 is the pre-frequency division factor of PLL;

N is the frequency doubling factor of PLL;

X is the amplitude coefficient of the spread spectrum.

The parameters N, P, M1, and M0 are for the frequency division.

When M1 = 0, M0 = 0, and P = 1 (no frequency division), the calculation formula of PLL frequency can be simplified as follows:

$$f = (N+1+X)\cdot 24MHz,\ 0<X<1$$

$$[f_1, f_2] = (N+1+[X_1, X_2])\cdot 24MHz$$

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$$SDM_BOT = 2^{17} \cdot X_1$$

$$\text{WAVE_STEP} = 2^{17} \cdot (X_2 - X_1)/(24\,\text{MHz}/PREQ) \cdot 2$$

Where, SDM_BOT and WAVE_STEP are bits of the PLL pattern control register, and PREQ is the frequency of the spread spectrum.

Follow the steps below to implement the spread spectrum:

Step 1 Configure the control register of the corresponding PLL

a) Calculate the factor N and decimal value X according to the PLL frequency and PLL frequency formula. Refer to the control register of the corresponding PLL (named PLL_xxx_CTRL_REG, where xxx is the module name) in 3.3.6 Register Description for the corresponding PLL frequency formula.

b) Write M0, M1, N, and PLL frequency to the PLL control register.

c) Configure the PLL_SDM_EN bit (bit [24]) of the PLL control register to 1 to enable the spread spectrum function.

Step 2 Configure the pattern control register of the corresponding PLL

a) Calculate the SDM_BOT and WAVE_STEP of the pattern control register according to decimal value X and spread spectrum frequency (the bit [18:17] of the PLL pattern register)

b) Configure the spread spectrum mode (SPR_FREQ_MODE) to 2 or 3.

c) If the PLL_INPUT_DIV2 of the PLL control register is 1, configure the spread spectrum clock source select bit (SDM_CLK_SEL) of the PLL pattern control register to 1. Otherwise, configure SDM_CLK_SEL to the default value 0.

d) Write SDM_BOT, WAVE_STEP, PREQ, SPR_FREQ_MODE, and SDM_CLK_SEL to the PLL pattern control register, and configure the SIG_DELT_PAT_EN bit (bit[31]) of this register to 1.

Step 3 Delay 20 us

2.13.3.5 Configuring Bus Clock

The bus clock supports dynamic switching, but the process of switching needs to follow the following two rules.

- From a higher frequency to a lower frequency: switch the clock source first, and then set the frequency division factor;
- From a lower frequency to a higher frequency: configure the frequency division factor first, and then switch the clock source.

The typical bus frequency for each bus in STBY_PRCM and DSP_PRCM is as follows:

- AHBS: 200 MHz
- APBS0: 100 MHz

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- APBS1: 24 MHz

2.13.3.6 Configuring Module Clock

For the Bus Gating Reset register of a module, the reset bit is de-asserted first, and then the clock gating bit is enabled to avoid potential problems caused by the asynchronous release of the reset signal.

For all module clocks except the DDR clock, configure the clock source and frequency division factor first, and then release the clock gating (that is, set to 1). For the configuration order of the clock source and frequency division factor, follow the rules below:

- With the increasing of the clock source frequency, configure the frequency division factor before the clock source.
- With the decreasing of the clock source frequency, configure the clock source before the frequency division factor.

2.13.4 Register List

PRCM module includes two groups of registers:

Module Name	Base Address
STBY_PRCM	0x0701 0000
DSP_PRCM	0x0710 2000

2.13.4.1 STBY_PRCM Register List

Module Name	Base Address
STBY_PRCM	0x0701 0000

Register Name	Offset	Description
AHBS_CFG_REG	0x0000	AHBS Configuration Register
APBS0_CFG_REG	0x000C	APBS0 Configuration Register
APBS1_CFG_REG	0x0010	APBS1 Configuration Register
CPUS_TIMER0_CLK_REG	0x0100	CPUS_TIMER0 Clock Register
CPUS_TIMER1_CLK_REG	0x0104	CPUS_TIMER1 Clock Register
CPUS_TIMER2_CLK_REG	0x0108	CPUS_TIMER2 Clock Register
CPUS_TIMER_BGR_REG	0x011C	CPUS_TIMER Bus Gating Reset Register
S_TWD_BGR_REG	0x012C	S_TWD Bus Gating Reset Register
S_PWMCTRL_CLK_REG	0x0130	S_PWMCTRL Clock Register
S_PWMCTRL_BGR_REG	0x013C	S_PWMCTRL Bus Gating Reset Register
S_SPI_CLK_REG	0x0150	S_SPI Clock Register
S_SPI_BGR_REG	0x015C	S_SPI Bus Gating Reset Register
S_SPINLOCK_BGR_REG	0x016C	S_SPINLOCK Bus Gating Reset Register

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Register Name	Offset	Description
CPUS_MSGBOX_BGR_REG	0x017C	CPUS_MSGBOX Bus Gating Reset Register
S_UART_BGR_REG	0x018C	S_UART Bus Gating Reset Register
S_TWI_BGR_REG	0x019C	S_TWI Bus Gating Reset Register
S_PPU_BGR_REG	0x01AC	S_PPU Bus Gating Reset Register
S_CPUS_BIST_BGR_REG	0x01BC	S_CPUS_BIST Bus Gating Reset Register
S_IRRX_CLK_REG	0x01C0	S_IRRX Clock Register
S_IRRX_BGR_REG	0x01CC	S_IRRX Bus Gating Reset Register
DMA_ADB400_CLKEN_REG	0x01DC	DMA ADB400 Gating Register
RTC_BGR_REG	0x020C	RTC Bus Gating Reset Register
S_CPUCFG_BGR_REG	0x022C	S_CPUCFG Bus Gating Reset Register
PLL_CTRL_REG0	0x0240	PLL Control Register 0
PLL_CTRL_REG1	0x0244	PLL Control Register 1
VDD_SYS_PWROFF_GATING_REG	0x0250	VDD_SYS Power Off Gating Register
ANA_PWR_RST_REG	0x0254	Analog Power Off Gating Register
VDD_SYS_PWR_RST_REG	0x0260	VDD_SYS Power Domain Reset Register
DSP_SYS_PWR_RST_REG	0x0264	DSP_SYS Power Domain Reset Register
RAM1P_CFG_REG	0x0270	RAM1P Configuration Register
RAM2P_CFG_REG	0x0274	RAM2P Configuration Register
RAMSP_CFG_REG	0x0278	RAMSP Configuration Register
ROM_CFG_REG	0x027C	ROM Configuration Register
NMI_INT_CTRL_REG	0x0320	NMI Interrupt Control Register
NMI_INT_EN_REG	0x0324	NMI Interrupt Enable Register
NMI_INT_PEND_REG	0x0328	NMI Interrupt Pending Register
DEV_BUS_AUTOG_CTRL_REG	0x0338	DEV_BUS_AUTOG_CTRL_REG Register
BUS_ACG_REG	0x033C	Bus Auto Clock Gating Register
MSRAMOC_CTRL_REG	0x0360	MSRAMOC Control Register
REMAP_CTRL_REG	0x0364	REMAP Control Register
AHBS_RDY_TOUT_CTRL_REG	0x0368	AHBS Ready Timeout Control Register
CPUS_DEV_DMA_SEL_REG	0x0370	CPUS Device DMA Configuration Register
CRY_CONFIG_REG	0x03E0	Crypt Configuration Register
CRY_KEY_REG	0x03E4	Crypt Key Register
CRY_EN_REG	0x03E8	Crypt Enable Register

2.13.4.2 DSP_PRCM Register List

Module Name	Base Address
DSP_PRCM	0x0710 2000

Register Name	Offset	Description
PLL_CTRL_REG0	0x0000	PLL Control Register0

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Register Name	Offset	Description
PLL_CTRL_REG1	0x0004	PLL Control Register 1
PLL_AUDIO1_CTRL_REG	0x000C	PLL_AUDIO1 Control Register
PLL_AUDIO1_PAT0_CTRL_REG	0x0010	PLL_AUDIO1 Pattern0 Control Register
PLL_AUDIO1_PAT1_CTRL_REG	0x0014	PLL_AUDIO1 Pattern1 Control Register
PLL_AUDIO1_BIAS_REG	0x0018	PLL_AUDIO1 Bias Register
AUD_CLK_REG	0x001C	Audio Out Clock Register
DSP_CLK_REG	0x0020	DSP Clock Register
I2S0_CLK_REG	0x002C	I2S0 Clock Register
I2S1_CLK_REG	0x0030	I2S1 Clock Register
I2S2_CLK_REG	0x0034	I2S2 Clock Register
I2S3_CLK_REG	0x0038	I2S3 Clock Register
I2S3_ASRC_CLK_REG	0x003C	I2S3_ASRC Clock Register
I2S_BGR_REG	0x0040	I2S Bus Gating Reset Register
OWA_TX_CLK_REG	0x0044	OWA_TX Clock Register
OWA_RX_CLK_REG	0x0048	OWA_RX Clock Register
OWA_BGR_REG	0x004C	OWA Bus Gating Reset Register
DMIC_CLK_REG	0x0050	DMIC Clock Register
DMIC_BGR_REG	0x0054	DMIC Bus Gating Reset Register
AUDIO_CODEC_DAC_CLK_REG	0x0058	AUDIO_CODEC_DAC Clock Register
AUDIO_CODEC_ADC_CLK_REG	0x005C	AUDIO_CODEC_ADC Clock Register
AUDIO_CODEC_BGR_REG	0x0060	AUDIO_CODEC Bus Gating Reset Register
AHBS_RDY_TOUT_CTRL_REG	0x0064	AHBS Ready Timeout Control Register
DSP_MSGBOX_BGR_REG	0x0068	DSP MSGBOX Bus Gating Reset Register
DSP_CFG_BGR_REG	0x006C	DSP CFG Bus Gating Reset Gating Register
NPU_BGR_REG	0x0070	NPU Gating Reset Register
DSP_TIMER0_CLK_REG	0x0074	DSP_TIMER0 Clock Register
DSP_TIMER1_CLK_REG	0x0078	DSP_TIMER1 Clock Register
DSP_TIMER2_CLK_REG	0x007C	DSP_TIMER2 Clock Register
DSP_TIMER3_CLK_REG	0x0080	DSP_TIMER3 Clock Register
DSP_TIMER4_CLK_REG	0x0084	DSP_TIMER4 Clock Register
DSP_TIMER5_CLK_REG	0x0088	DSP_TIMER5 Clock Register
DSP_TIMER_BUS_BGR_REG	0x008C	DSP_TIMER Bus Gating Reset Register
DSP_DBG_BGR_REG	0x0100	DSP Debug Bus Gating Reset Register
DSP_DMAC_BGR_REG	0x0104	DSP_DMAC Bus Gating Reset Register
PUBSRAM_BGR_REG	0x0114	PUBSRAM Bus Gating Reset Register
AHBS1_RDY_TOUT_CTRL_REG	0x0118	AHBS1 Ready Timeout Control Register
MCLK_GATING_CFG_REG	0x011C	MCLK Gating Configuration Register
RISCV_CLK_REG	0x0120	RISCV Clock Register
RISCV_CFG_BGR_REG	0x0124	RISCV Configuration Bus Gating Reset Register

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Register Name	Offset	Description
RISCV_MSGBOX_BGR_REG	0x0128	RISCV MSGBOX Bus Gating Reset Register
DSP_PWMCTRL_CLK_REG	0x0130	DSP_PWMCTRL Clock Register
DSP_PWMCTRL_BGR_REG	0x0134	DSP_PWMCTRL Bus Gating Reset Register
PLL_BACKDOOR_OUTPUT_EN_REG	0x0160	PLL Backdoor Output Enable Register
TEST_DBG_REG	0x0164	Test Debug Register

2.13.5 STBY_PRCM Register Description

2.13.5.1 0x0000 AHBS Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AHBS_CFG_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	AHBS_CLK_SRC_SEL AHBS Clock Source Selection 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV = PERI0PLL1X/3 100: AUDIO1PLL4X Others: / CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.5.2 0x000C APBS0 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: APBS0_CFG_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/

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Offset: 0x000C			Register Name: APBS0_CFG_REG
Bit	R/W	Default/Hex	Description
26:24	R/W	0x0	APBS0_CLK_SRC_SEL APBS0 Clock Source Selection 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X Others: / CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.13.5.3 0x0010 APBS1 Configuration Register (Default: 0x0000_0000)

Offset: 0x0010			Register Name: APBS1_CFG_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	APBS1_CLK_SRC_SEL APBS1 Clock Source Selection 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV = PERI0PLL1X/3 100: AUDIO1PLL4X Others:/ CLK = Clock Source/ M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M (M= FACTOR_M +1) FACTOR_M is from 0 to 31.

2.13.5.4 0x0100 CPUS_TIMER0 Clock Register (Default: 0x0000_0000)

Offset: 0x0100			Register Name: CPUS_TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/

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Offset: 0x0100			Register Name: CPUS_TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
6:4	R/W	0x0	CLK_SRC_SEL. CPUS_TIMER0 Clock Source Selection. 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X CPUS_TIMER0_CLK = Clock Source / N.
3:1	R/W	0x0	CPUS_TIMER0_CLK_DIVN. Select the pre-scale of CPUS_TIMER0 clock source. Factor N 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	CPUS_TIMER0_CLK_GATING 0: Disable 1: Enable

2.13.5.5 0x0104 CPUS_TIMER1 Clock Register (Default: 0x0000_0000)

Offset: 0x0104			Register Name: CPUS_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL CPUS_TIMER1 Clock Source Selection 000: CLK24M 001: CLK32K 010:CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X CPUS_TIMER1_CLK = Clock Source/N

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Offset: 0x0104			Register Name: CPUS_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
3:1	R/W	0x0	CPUS_TIMER1_CLK_DIVN Select the pre-scale of CPUS_TIMER1 clock source. Factor N 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	CPUS_TIMER1_CLK_GATING 0: Disable 1: Enable

2.13.5.6 0x0108 CPUS_TIMER2 Clock Register (Default: 0x0000_0000)

Offset: 0x0108			Register Name: CPUS_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL CPUS_TIMER2 Clock Source Selection 000: CLK24M 001: CLK32K 010:CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X CPUS_TIMER2_CLK = Clock Source/N
3:1	R/W	0x0	CPUS_TIMER2_CLK_DIVN Select the pre-scale of CPUS_TIMER2 clock source. Factor N 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128

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Offset: 0x0108			Register Name: CPUS_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	CPUS_TIMER2_CLK_GATING 0: Disable 1: Enable

2.13.5.7 0x011C CPUS_TIMER BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: CPUS_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUS_TIMER_RST CPUS_TIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUS_TIMER_GATING Gating Clock for CPUS_TIMER 0: Mask 1: Pass

2.13.5.8 0x012C S_TWD BUS GATING RESET Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: S_TWD_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	S_TWD_GATING Gating Clock for S_TWD 0: Mask 1: Pass

2.13.5.9 0x0130 S_PWMCTRL Clock Register (Default: 0x0000_0000)

Offset: 0x0130			Register Name: S_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	S_PWMCTRL_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON S_PWMCTRL_CLK = Clock Source
30:26	/	/	/

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Offset: 0x0130			Register Name: S_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 00: CLK24M 01: CLK32K 10: CLK_RC 11:/ CLK32K is generated by calibrated CLK_RC or external low speed crystal. For more information, please refer to section 2.14 RTC.
23:0	/	/	/

2.13.5.10 0x013C S_PWMCTRL BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x013C			Register Name: S_PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_ PWMCTRL _RST S_ PWMCTRL Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_ PWMCTRL _GATING Gating bus Clock for S_ PWMCTRL 0: Mask 1: Pass

2.13.5.11 0x0150 S_SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: S_SPI0_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON R_SPI_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x0150			Register Name: S_SPI0_CLK_REG
Bit	R/W	Default/Hex	Description
26:24	R/W	0x0	SPI_CLK_SRC_SEL SPI Clock Source Selection 000: CLK24M 001: PERIPLL_DIV=PERI0PLL1X/3 010: PERI0_300M 011: PERI1_300M 100: AUDIO1PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.13.5.12 0x015C S_SPI0 BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x015C			Register Name: S_SPI0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_SPI0_RST S_SPI0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_SPI0_GATING Gating Clock for S_SPI0 0: Mask 1: Pass

2.13.5.13 0x016C S_SPINLOCK BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x016C			Register Name: S_SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0x016C			Register Name: S_SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	S_SPINLOCK_RST S_SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_SPINLOCK_GATING Gating Clock for S_SPINLOCK 0: Mask 1: Pass

2.13.5.14 0x017C CPUS_MSGBOX BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x017C			Register Name: CPUS_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUS_MSGBOX_RST CPUS_MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUS_MSGBOX_GATING Gating Clock for CPUS_MSGBOX 0: Mask 1: Pass

2.13.5.15 0x018C S_UART BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x018C			Register Name: S_UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_UART1_RST S_UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	S_UART0_RST S_UART0 Reset 0: Assert 1: De-assert
15:2	/	/	/

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Offset: 0x018C			Register Name: S_UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	S_UART1_GATING Gating Clock for S_UART1 0: Mask 1: Pass
0	R/W	0x0	S_UART0_GATING Gating Clock for S_UART0 0: Mask 1: Pass

2.13.5.16 0x019C S_TWI BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x019C			Register Name: S_TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	S_TWI2_RST S_TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	S_TWI1_RST R_TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	S_TWI0_RST R_TWI0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	S_TWI2_GATING Gating Clock for S_TWI2 0: Mask 1: Pass
1	R/W	0x0	S_TWI1_GATING Gating Clock for S_TWI1 0: Mask 1: Pass
0	R/W	0x0	S_TWI0_GATING Gating Clock for S_TWI0 0: Mask 1: Pass

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2.13.5.17 0x01AC S_PPU BUS GATING RESET Register (Default Value: 0x0001_0001)

Offset: 0x01AC			Register Name: S_PPU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_PPU1_RST S_PPU1 Reset 0: Assert 1: De-assert
16	R/W	0x1	Reserved
15:2	/	/	/
1	R/W	0x0	S_PPU1_GATING Gating Clock for S_PPU1 0: Mask 1: Pass
0	R/W	0x1	S_PPU_GATING Gating Clock for S_PPU(PCK600) 0: Mask 1: Pass

2.13.5.18 0x01BC S_CPUS_BIST BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: S_CPUS_BIST_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	S_CPUS_BIST_GATING Gating Clock for S_CPUS_BIST 0: Mask 1: Pass

2.13.5.19 0x01C0 S_IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: S_IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON S_IRRX_CLK = Clock Source/M
30:26	/	/	/

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Offset: 0x01C0			Register Name: S_IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 00: CLK32K 01: CLK24M 10:/ 11:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.13.5.20 0x01CC S_IRRX BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01CC			Register Name: S_IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_IRRX_RST S_IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_IRRX_GATING Gating Clock for S_IRRX 0: Mask 1: Pass

2.13.5.21 0x01DC DMA ADB400 GATING Register (Default Value: 0x0000_0001)

Offset: 0x01DC			Register Name: DMA_ADB400_CLKEN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	DMA_CLKEN_SW Gating Clock for DMA ADB400 MST 0: Mask 1: Pass

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2.13.5.22 0x020C RTC Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: RTC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	RTC_RST RTC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	RTC_GATING Gating Clock for RTC 0: Mask 1: Pass

2.13.5.23 0x022C S_CPUCFG Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x022C			Register Name: S_CPUCFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	S_CPUCFG_RST S_CPUCFG Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	S_CPUCFG_GATING Gating Clock for S_CPUCFG 0: Mask 1: Pass

2.13.5.24 0x0240 PLL Control Register 0 (Default Value: 0x0000_0007)

Offset: 0x0240			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL PLL Reference Clock Selection 0: DCXO 1: External Test Clock
23:3	/	/	/
2	R/W	0x1	GM1 XTAL Gain Control Bit1

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Offset: 0x0240			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
1	R/W	0x1	GM0 XTAL Gain Control Bit0
0	R/W	0x1	Reserved

2.13.5.25 0x0244 PLL Control Register 1 (Default Value: 0x0004_0005)

Offset: 0x0244			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD Key Field for LDO Enable bit If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/
18:16	R/W	0x4	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control 000: 0.82 V 001: 0.86 V 010: 0.9 V 011: 0.94v 100: 0.98v 101: 1.02v 110: 1.06v 111: 1.10v
15:5	/	/	/
4	R/W	0x0	MBIAS_EN Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias
3	R/W	0x0	PLLTEST_EN For Verify (Back door clock PLLTEST enable) 0：Output clock is gated off. 1：Clock Output. The clock is the clock output to the PLL and the clock after frequency division through pins.
2:1	R/W	0x2	Reserved
0	R/W	0x1	LDO_EN LDO Enable 0: Disable 1: Enable Note: PLL Power enable (power source from VCC_PLL).

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2.13.5.26 0X0250 VDD_SYS Power Off Gating Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	R/W	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	VDD_USB2CPUS_GATING 0: Invalid 1: Valid To gate off the signal output to VDD-CPUS from USB module, set this bit to 1.
7:6	/	/	/
5	R/W	0x0	VDD_SYS2DSP_GATING Gating the corresponding modules to the DSP module when VDD-SYS powers off. 0: Invalid 1: Valid This bit should be set to 1 before VDD-SYS power off while it should be set to 0 after the VDD-SYS power on. DSP CLK Source should switch to Internal OSC or AUDIO1PLL before VDD-SYS Power Off Gating.
4	R/W	0x0	VDD_DSP2CPUS_GATING Gating the corresponding modules to the CPUS module when DSP_SYS powers off. 0: Invalid 1: Valid This bit should be set to 1 before DSP_SYS powers off while it should be set to 0 after the DSP_SYS power on.
3	R/W	0x0	VDD_SYS2USB_GATING Gating the corresponding modules to the USB module when VDD_SYS power off. 0: Invalid 1: Valid This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on. USB CLK Source should switch to Internal OSC before VDD_SYS Power Off Gating.

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Offset: 0x0250			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	R/W	Default/Hex	Description
2	R/W	0x0	VDD_SYS2CPUS_GATING Gating the corresponding modules to the CPUS Power Domain when VDD_SYS power off. 0: Invalid 1: Valid This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on. CPUS CLK Source should switch to Internal OSC before VDD_SYS Power Off Gating.
1	/	/	/
0	R/W	0x0	VDD_DDR_GATING 0: valid (gate valid) 1: Inalid (gate invalid) When DDR entrys into power-down (low voltage) self-refresh mode, this signal will fix CLKE to 0.

2.13.5.27 0x0254 ANALOG Power Off Gating Register (Default Value: 0x0000_0005)

Offset: 0x0254			Register Name: ANA_PWR_RST_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	PWROFF_ANA_EN_CPU Gating The CPU PLL ANA Module Input When CPU_SYS Is Power Off. 0: Invalid, not gating 1: Valid, gating When system is cold start, this bit is default not gating, before using the relate ANA module, must set this bit to 0. Relate ANA module: PLL
2	R/W	0x1	PWROFF_ANA_EN_DSP Gating The DSP SYS PLL ANA Module Input When DSP_SYS Is Power Off. 0: Invalid, not gating 1: Valid, gating Note: When system is cold start, this bit is default gating, before using the related ANA module, must set this bit to 0. Related ANA module: PLL/AUDIO CODEC

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Offset: 0x0254			Register Name: ANA_PWR_RST_REG
Bit	R/W	Default/Hex	Description
1	R/W	0x0	PWROFF_ANA_EN Gating The PLL ANA Module Input When VDD Is Power Off. 0: Invalid, not gating 1: Valid, gating Note: When system is cold start, this bit is default not gating, before using the relate ANA module, must set this bit to 0. Relate ANA module: PLL
0	R/W	0x1	SYS_ANA_VDDON_CTRL Gating The System Domain ANA Module Input When VDD Is Power Off. 0: Invalid, not gating 1: Valid, gating Note: When system is cold start, this bit is default gating, before using the relate ANA module, must set this bit to 0. Relate ANA module: RES/RES_CAL_DCAP/GPADC/DSI/LVDS/LRADC/USB/CSI

2.13.5.28 0x0260 VDD_SYS Power Domain Reset Register (Default: 0x0000_0001)

Offset: 0x0260			Register Name: VDD_SYS_PWR_RST_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	MODULE_RST VDD_SYS Power Domain Modules should be reset before VDD_SYS power on 0: Assert 1: De-assert

2.13.5.29 0x0264 DSP_SYS Power Domain Reset Register (Default: 0x0000_0001)

Offset: 0x0264			Register Name: DSP_SYS_PWR_RST_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0264			Register Name: DSP_SYS_PWR_RST_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x1	DSP_SYS_RSTN DSP_SYS Power Domain Modules should be reset before DSP_SYS power on. 0: Assert 1: De-assert

2.13.5.30 0x0270 RAM1P Configuration Register (Default Value: 0x0000_0413)

Offset: 0x0270			Register Name: RAM1P_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x413	RF1P_MEM RF1P Configuration Information

2.13.5.31 0x0274 RAM2P Configuration Register (Default Value: 0x0000_8421)

Offset: 0x0274			Register Name: RAM2P_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x8421	RF2P_MEM RF2P Configuration Information

2.13.5.32 0x0278 RAMSP Configuration Register (Default Value: 0x0000_0403)

Offset: 0x0278			Register Name: RAMSP_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x403	SRAM_MEM SRAM Configuration Information

2.13.5.33 0x027C ROM Configuration Register (Default Value: 0x0000_0015)

Offset: 0x027C			Register Name: ROM_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x15	ROM_MEM ROM Configuration Information

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2.13.5.34 0x0320 NMI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: NMI_INT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	NMI_SRC_TYPE External NMI Interrupt Source Type 00: Low level sensitive 01: Negative edge trigged 10: High level sensitive 11: Positive edge sensitive

2.13.5.35 0x0324 NMI Interrupt Enable Register (Default Value: 0x8000_0000)

Offset: 0x0324			Register Name: NMI_INT_EN_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x1	NMI_INPUT_DET_EN NMI Input Detect Enable 0: Disable 1:Enable
30:1	/	/	/
0	R/W	0x0	NMIIRQ_SYS_EN Interrupt NMI for CPUX Enable Bits 0: Interrupt is disabled. 1: Interrupt is enabled.

2.13.5.36 0x0328 NMI Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: NMI_INT_PEND_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	NMI_IRQ_PEND NMI IRQ Pending Interrupt NMI Pending/Clear Bit. Set 1 to the bit will clear it. (after first enabling NMI IRQ function, must set this bit to 1 to clear the unexpected pending once) 0: Corresponding interrupt is not pending 1: Corresponding interrupt is pending

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2.13.5.37 0x0338 DEV_BUS_AUTOG_CTRL Register（Default Value：0x0000_0000

Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	CPUCLK_REC_DLY_TIME This bit indicates the delay time needed to respond to CPUS clock after respinding to peripherals and bus clocks, when exiting LP mode. The unit is PRCM clock. 0=256 cycle 1=1 cycle …… 255=255 cycle
23:21	/	/	/
20	R/W	0x0	LPI_OUT_SYNC_EN LPI Interface from CPUS to PRCM Enable 0: CPUS clock is synchronous with PRCM clock. 1: CPUS clock is asynchronous with PRCM clock.
18:12	/	/	/
11	R/W	0x0	LPI_IF_EN LPI Interfece Between CPUS and PRCM Enable 0: Disable 1: Enable When LPI is disabled, CPUS status will not be routed to PRCM.
10	R/W	0x0	LPI_IN_SYNC_EN LPI Interface from PRCM to CPUS Enable 0: CPUS clock is synchronous with PRCM clock. 1: CPUS clock is asynchronous with PRCM clock.
9	R/W	0x0	TT_AUTOGATE_EN CPUS Ticktimer Auto Gating Enbale When this bit is enabled and PM_TT_O is high, the ticktimer clock will be gated on automatically.
8	R/W	0x0	CPU_ICACHE_AUTOGATE_EN Clock (excludes ticktimer clock) Auto Gating Enable 0: Auto gating is disabled. 1: Auto gating is enabled. When this bit is enabled and both of PM_CPU_O and PM_ICACHE_O are high simultaneously, the clocks of CPUS, ICACHE, QMEM, and PM will be gated on automatically.

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Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL
Bit	R/W	Default/Hex	Description
7	R	0x0	PM_TT_STAT CPUS LP Interface Status 0: CPUS is in normal mode and the ticktimer clock is disable to be gated off 1: The ticktimer clock is able to be gated off.
6	R	0x0	PM_ICACHE_STAT CPUS LP Interface Status 0: CPUS is in normal mode and the ICACHE clock is disable to be gated off 1: The ICACHE clock is able to be gated off.
5	R	0x0	PM_CPU_STAT CPUS LP Interface Status 0: CPUS is in normal mode and the CPU clock is disable to be gated off. 1: The CPU clock is able to be gated off.
4	R	0x1	CACTIVE_STAT LPI CACTIVE Status 0: CPUS is in low power mode. 1: CPUS is in normal mode.
3:1	/	/	/
0	R/W	0x0	CPUS_CLKAUTG_EN 0: Auto gating is disabled. 1: Auto gating is enabled. When DSP gets into sleep mode, auto gating signal will be generated and then every modul bus and work clock will be gated on automatically.

2.13.5.38 0x033C Bus Auto Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: BUS_ACG_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	AHBS_AUTO_CLK_GATE_EN AHBS Bus Auto Clock Gating Function Enable 1: Enable auto clock gate 0: Disable auto clock gate
23:7	/	/	/

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Offset: 0x033C			Register Name: BUS_ACG_REG
Bit	R/W	Default/Hex	Description
6	R/W	0x0	CPUS_MSGBOX_ACG_MODE_EN CPUS_MSGBOX Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, CPUS_MSGBOX HCLK will also be closed when AHBS bus clock is closed.
5	R/W	0x0	S_SPINLOCK_ACG_MODE_EN S_SPINLOCK Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, S_SPINLOCK HCLK will also be closed when AHBS bus clock is closed.
4	R/W	0x0	Reserved
3	R/W	0x0	CPUS_TIMER_ACG_MODE_EN CPUS_TIMER Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, CPUS_ TIMER HCLK will also be closed when AHBS bus clock is closed.
2	R/W	0x0	MSRAM_ACG_MODE_EN MSRAMOC Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto AW1890clock gating function is enable, MSRAMOC HCLK will close when AHBS bus clock close.
1	R/W	0x0	RTC_ACG_MODE_EN RTC Auto Clock Gating Mode Enable SYSRTC module auto clock gating mode enable, if this bit is 1 and AHBS auto clock gating function is enable, SYSRTC module hclk will close when AHBS bus clock close.
0	R/W	0x0	BM_ACG_MODE_EN AHBS Bus Matrix Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, AHBS bus matrix HCLK will also be closed when AHBS bus clock is closed.

2.13.5.39 0x360 MSRAMOC Control Register (Default: 0x0000_0000)

Offset: 0x360			Register Name: MSRAMOC_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/

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Offset: 0x360			Register Name: MSRAMOC_CTRL_REG
Bit	R/W	Default/Hex	Description
1	R/W	0x0	MSRAMOC_PORT_HOLD_EN MSRAMOC Port Hold Enable 0: Disable 1: Enable
0	R/W	0x0	MSRAMOC_ACG_EN MSRAMOC Auto Clock Gating Enable 0: Disable 1: Enable

2.13.5.40 0x364 REMAP Control Register (Default: 0x0000_0001)

Offset: 0x364			Register Name: REMAP_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	SRAMA3_2_RAM_REMAP 0: SRAMA3_2 does not share for DSP_SYS 1: SRAMA3_2 shares for DSP_SYS
0	R/W	0x1	DSP_RAM_REMAP 0: DSP local memory only for DSP_SYS. 1: DSP local memory share for system.

2.13.5.41 0x0368 AHBS Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS_RDY_TIMEOUT_IRQ_PEND AHBS Hready Time Out IRQ Pending Write 1 Clear
23:9	/	/	/
8	R/W	0x0	AHBS_RDY_TIMEOUT_IRQ_EN AHBS Hready Time Out IRQ Enable 1: IRQ Enable 0: IRQ Disable
7	R/W	0x0	AHBS_TIMEOUT_INT_VAL_SEL AHBS Time Out Interval Value Selection 0: interal_value* 2^10 + 2^10 -1 1: interal_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS_TIMEOUT_CNT_INT_VAL AHBS Time Out Counter Interval Value

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Offset: 0x0368			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	AHBS_RDY_TIMEOUT_EN AHBS Hready Time Out Enable

2.13.5.42 0x0370 CPUS Device DMA Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0370			Register Name: CPUS_DEV_DMA_SEL_REG
Bit	R/W	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	DMA_SPI_SEL SPI DMA Selection 0: DSP DMA 1: SYS DMA
3	R/W	0x0	DMA_UART1_SEL UART1 DMA Selection 0: DSP DMA 1: SYS DMA
2	R/W	0x0	DMA_UART0_SEL UART0 DMA Selection 0: DSP DMA 1: SYS DMA
1	R/W	0x0	DMA_TWI1_SEL TWI1 DMA Selection 0: DSP DMA 1: SYS DMA
0	R/W	0x0	DMA_TWI0_SEL TWI0 DMA Selection 0: DSP DMA 1: SYS DMA

2.13.5.43 0x0374 I2S0 PAD Selection Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0374			Register Name: I2S0_PAD_SEL_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	I2S0_PAD_SEL I2S0 PAD Selection 0: Use CPUS PAD 1: Use SYS PAD

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2.13.5.44 0x0378 DMIC PAD Selection Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0378			Register Name: DMIC_PAD_SEL_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMIC_PAD_SEL DMIC PAD Selection 0: Use CPUS PAD 1: Use SYS PAD

2.13.5.45 0x03E0 Crypt Configuration Register (Default Value: 0x0000_0000)

Offset: 0x03E0			Register Name: CRY_CONFIG_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field If you want to read or write Crypt Key Register/Crypt Enable Register, you should write 0x1689 in these bits.

2.13.5.46 0x03E4 Crypt Key Register (Default Value: 0x0000_0000)

Offset: 0x03E4			Register Name: CRY_KEY_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	CRY_KEY Crypt Key

2.13.5.47 0x03E8 Crypt Enable Register (Default Value: 0x0000_0000)

Offset: 0x03E8			Register Name: CRY_EN_REG
Bit	R/	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypt Enable

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2.13.6 DSP_PRCM Register Description

2.13.6.1 0x0000 PLL Control Register0 (Default Value: 0x0000_0007)

Offset: 0x0000			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL PLL Reference Clock Selection 0: DCXO. 1: External Test Clock.
23:3	/	/	/
2	R/W	0x1	GM1 XTAL Gain Control Bit1
1	R/W	0x1	GM0. XTAL Gain Control Bit0
0	R/W	0x1	Reserved

2.13.6.2 0x0004 PLL Control Register 1 (Default Value: 0x0004_0005)

Offset: 0x0004			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD Key Field for LDO Enable If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/
18:16	R/W	0x4	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control 000: 0.90 V 001: 0.94 V 010: 0.98 V 011: 1.02 V 100: 1.06 V 101: 1.10 V 110: 1.14 V 111: 1.18 V
15:5	/	/	/
4	R/W	0x0	MBIAS_EN Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias

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Offset: 0x0004			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
3	R/W	0x0	PLLTEST_EN For Verify (Back door clock PLLTEST enable) 0：Output clock is gated off. 1：Clock Output. The clock is the clock output to the PLL and the clock after frequency division through pins.
2:1	R/W	0x2	Reserved
0	R/W	0x1	LDO_EN LDO Enable 0: Disable 1: Enable Note: PLL Power enable (power source from VCC_PLL).

2.13.6.3 0x000C PLL_AUDIO1 Control Register (Default Value: 0x4841_7F00)

Offset: 0x000C			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL_AUDIO1 = 24 MHz*N/M The PLL_AUDIO1 (DIV2) = 24 MHz*N/M /P0 The PLL_AUDIO1 (DIV5) = 24 MHz*N/M /P1 The working frequency range of 24 MHz/M*N is from 180 MHz to 3.5 GHz. The default frequency of PLL_AUDIO1 is 3072 MHz. The default frequency of PLL_AUDIO1 (DIV2) is 1536 MHz. The default frequency of PLL_AUDIO1 (DIV5) is 614.4MHz(24.576 MHz*25).
30	R/W	0x1	PLL_LDO_EN LDO enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

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Offset: 0x000C			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) This bit is only valid when the bit[29] is set to 1.
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable This bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x4	PLL_P1 PLL Output Div P1 P1=PLL_OUTPUT_DIV_P1 + 1 PLL_OUTPUT_DIV_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0 PLL Output Div P0 P0=PLL_OUTPUT_DIV_P0 + 1 PLL_OUTPUT_DIV_P0 is from 0 to 7.
15:8	R/W	0x7F	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254 In application, PLL_FACTOR_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

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Offset: 0x000C			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M M=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	/	/	/

2.13.6.4 0x0010 PLL_AUDIO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PLL_AUDIO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Selection 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1=1, this bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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2.13.6.5 0x0014 PLL_AUDIO1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: PLL_AUDIO1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.13.6.6 0x0018 PLL_AUDIO1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0018			Register Name: PLL_AUDIO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL Bias Control
15:0	/	/	/

2.13.6.7 0x001C Audio Out Clock Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: AUD_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUD_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON AUD_CLK = PLL_AUDIO1 (DIV2)/M
30:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

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2.13.6.8 0x0020 DSP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DSP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSP_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DSP_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: CLK24M 001: CLK32K 010: CLK_RC 011: AUDIO1PLL_DIV2 (low power clk from DSP_PRCM audio_sys) 100: AUDIO1PLL_DIV5 (DSP_PRCM audio_sys) 101: DSP_SYS_CLK (from ccu)
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.9 0x002C I2S0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)

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Offset: 0x002C			Register Name: I2S0_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.10 0x0030 I2S1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.13.6.11 0x0034 I2S2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.12 0x0038 I2S3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: I2S3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S3_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S3_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x0038			Register Name: I2S3_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.13 0x003C I2S3_ASRC Clock Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: I2S3_ASRC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S3_ASRC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S3_ASRC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: PERI0_300M 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31

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Offset: 0x003C			Register Name: I2S3_ASRC_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.14 0x0040 I2S Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: I2S_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
19	R/W	0x0	I2S3_RST I2S3 Reset 0: Assert 1: De-assert
18	R/W	0x0	I2S2_RST I2S2 Reset 0: Assert 1: De-assert
17	R/W	0x0	I2S1_RST I2S1 Reset 0: Assert 1: De-assert
16	R/W	0x0	I2S0_RST I2S0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	I2S3_GATING Gating Clock for I2S3 0: Mask 1: Pass
2	R/W	0x0	I2S2_GATING Gating Clock for I2S2 0: Mask 1: Pass
1	R/W	0x0	I2S1_GATING Gating Clock for I2S1 0: Mask 1: Pass

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Offset: 0x0040			Register Name: I2S_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	I2S0_GATING Gating Clock for I2S0 0: Mask 1: Pass

2.13.6.15 0x0044 OWA_TX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: OWA_TX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	OWA_TX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON OWA_TX_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N N= FACTOR_N +1
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.16 0x0048 OWA_RX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: OWA_RX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	OWA_RX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON OWA_RX_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x0048			Register Name: OWA_RX_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: PERI0_300M 001: AUDIO1PLL_DIV2(low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.17 0x004C OWA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: OWA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	OWA_RST OWA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	OWA_GATING Gating Clock for OWA 0: Mask 1: Pass

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2.13.6.18 0x0050 DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: DMIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMIC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DMIC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_M +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.19 0x0054 DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: DMIC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMIC_RST DMIC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING Gating Clock for DMIC 0: Mask 1: Pass

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2.13.6.20 0x0058 AUDIO_CODEC_DAC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: AUDIO_CODEC_DAC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUDIO_CODEC_DAC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_DAC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.21 0x005C AUDIO_CODEC_ADC Clock Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: AUDIO_CODEC_ADC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUDIO_CODEC_ADC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_ADC_CLK = Clock Source/M/N
30:27	/	/	/

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Offset: 0x005C			Register Name: AUDIO_CODEC_ADC_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from DSP_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from DSP_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.13.6.22 0x0060 AUDIO_CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: AUDIO_CODEC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST AUDIO_CODEC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING Gating Clock for AUDIO_CODEC 0: Mask 1: Pass

2.13.6.23 0x0064 AHBS Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS_RDY_TIMEOUT_IRQ_PEND AHBS Hready Time Out IRQ Pending Write 1 Clear

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Offset: 0x0064			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
23:9	/	/	/
8	R/W	0x0	AHBS_RDY_TIMEOUT_IRQ_EN AHBS Hready Time Out IRQ Enable 1: IRQ Enable 0: IRQ Disable
7	R/W	0x0	AHBS_TIMEOUT_INT_VAL_SEL AHBS Time Out Interval Value Selection 0: interal_value* 2^10 + 2^10 -1 1: interal_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS_TIMEOUT_CNT_INT_VAL AHBS Time Out Counter Interval Value
0	R/W	0x0	AHBS_RDY_TIMEOUT_EN AHBS Hready Time Out Enable

2.13.6.24 0x0068 DSP_MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: DSP_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSP_MSG_RST DSP MSG Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DSP_MSG_GATING Gating Clock For DSP_MSG 0: Mask 1: Pass

2.13.6.25 0x006C DSP CFG Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: DSP_CFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSP_CFG_RST DSP CFG Reset 0: Assert 1: De-assert
15:1	/	/	/

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Offset: 0x006C			Register Name: DSP_CFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DSP_CFG_GATING Gating Clock For DSP_CFG 0: Mask 1: Pass

2.13.6.26 0x0070 NPU Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: NPU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	NPU_RST NPU Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	NPU_ACLK_GATING. Gating Clock For NPU_ACLK 0: Mask 1: Pass
1	R/W	0x0	NPU_HCLK_GATING Gating Clock For NPU_HCLK 0: Mask 1: Pass
0	/	/	/

2.13.6.27 0x0074 DSP_TIMER0 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, DSP_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in DSP_PRCM.

Offset: 0x0074			Register Name: TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/

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Offset: 0x0074			Register Name: TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
5:4	R/W	0x0	CLK_SRC_SEL DSP_TIMER0 Clock Source Selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz) DSP_TIMER0 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	DSP_TIMER0_CLK_DIVN Select the pre-scale of DSP_TIMER0 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	DSP_TIMER0_CLK_GATING 0: Disable 1: Enable

2.13.6.28 0x0078 DSP_TIMER1 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, DSP_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in DSP_PRCM.

Offset: 0x0078			Register Name: DSP_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL DSP_TIMER1 clock source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) DSP_TIMER1 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.

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Offset: 0x0078			Register Name: DSP_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
3:1	R/W	0x0	DSP_TIMER1_CLK_DIVN Select the pre-scale of DSP_TIMER1 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	DSP_TIMER1_CLK_GATING 0: Disable 1: Enable

2.13.6.29 0x007C DSP_TIMER2 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, DSP_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in DSP_PRCM.

Offset: 0x007C			Register Name: DSP_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL DSP_TIMER2 clock source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) DSP_TIMER2 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.

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Offset: 0x007C			Register Name: DSP_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
3:1	R/W	0x0	DSP_TIMER2_CLK_DIVN Select the pre-scale of DSP_TIMER2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	DSP_TIMER2_CLK_GATING 0: Disable 1: Enable

2.13.6.30 0x0080 DSP_TIMER3 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, DSP_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in DSP_PRCM.

Offset: 0x0080			Register Name: DSP_TIMER3_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL DSP_TIMER3 Clock Source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) DSP_TIMER3 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.

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Offset: 0x0080			Register Name: DSP_TIMER3_CLK_REG
Bit	R/W	Default/Hex	Description
3:1	R/W	0x0	DSP_TIMER3_CLK_DIVN Select the pre-scale of DSP_TIMER2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	DSP_TIMER3_CLK_GATING 0: Disable 1: Enable

2.13.6.31 0x0084 DSP_TIMER4 Clock Register (Default: 0x0000_0000)

Offset: 0x0084			Register Name: DSP_TIMER4_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL DSP_TIMER4 clock source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) DSP_TIMER4 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	DSP_TIMER4_CLK_DIVN Select the pre-scale of DSP_TIMER4 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	DSP_TIMER4_CLK_GATING 0: Disable 1: Enable

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2.13.6.32 0x0088 DSP_TIMER5 Clock Register (Default: 0x0000_0000)

Offset: 0x0088			Register Name: DSP_TIMER5_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL DSP_TIMER5 Clock Source Selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) DSP_TIMER5 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	DSP_TIMER5_CLK_DIVN Select the pre-scale of DSP_TIMER5 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	DSP_TIMER5_CLK_GATING 0: Disable 1: Enable

2.13.6.33 0x008C DSP_TIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: DSP_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSP_TIMER_RST DSP_TIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DSP_TIMER_GATING Gating Clock for DSP_TIMER AHB_CLK 0: Mask 1: Pass

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2.13.6.34 0x0104 DSP_DMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: DSP_DMA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSP_DMAC_RST DSP DMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DSP_DMAC_GATING Gating Clock for DSP_DMAC 0: Mask 1: Pass

2.13.6.35 0x0114 PUBSRAM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PUBSRAM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PUBSRAM_RST PUBSRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PUBSRAM_GATING Gating Clock for PUBSRAM 0: Mask 1: Pass

2.13.6.36 0x0118 AHBS1 Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: AHBS1_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS1_RDY_TIMEOUT_IRQ_PEND AHBS Hready Time Out IRQ Pending Write 1 Clear
23:9	/	/	/

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Offset: 0x0118			Register Name: AHBS1_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
8	R/W	0x0	AHBS1_RDY_TIMEOUT_IRQ_EN AHBS Hready Time Out IRQ Enable 1: IRQ Enable 0: IRQ Disable
7	R/W	0x0	AHBS1_TIMEOUT_INT_VAL_SEL AHBS Time Out Interval Value Selection 0: interal_value* 2^10 + 2^10 -1 1: interal_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS1_TIMEOUT_CNT_INT_VAL AHBS Time Out Counter Interval Value
0	R/W	0x0	AHBS1_RDY_TIMEOUT_EN AHBS Hready Time Out Enable

2.13.6.37 0x011C MCLK Gating Configuration Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: MCLK_GATING_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	DSPSYS_MCLK_EN Gating Clock for DSPSYS_MCLK 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_EN Gating Clock for DMA_MCLK 0: Mask 1: Pass

2.13.6.38 0x0120 RISCV Clock Register (Default Value: 0x0000_0020)

Offset: 0x0120			Register Name: RISCV_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RISCV_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON RISCV_CLK = Clock Source/M/N
30	/	/	/

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Offset: 0x0120			Register Name: RISCV_CLK_REG
Bit	Read/Write	Default/Hex	Description
29:27	R/W	0x0	RSICVCLK_24M_SRC_SEL Clock Source Selection 000: CLK24M（from CCU) 001: CLK32K（from CCU) 010: CLK_RC（from CCU 16M)
26:0	/	/	/

2.13.6.39 0x0124 RISCV CFG Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: RISCV_CFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	RISCV_CORE_RST RISCV CORE Reset 0: Assert 1: De-assert
17	R/W	0x0	RISCV_APB_DB_RST RISCV APB Debug Reset 0: Assert 1: De-assert
16	R/W	0x0	RISCV_CFG_RST RISCV CFG Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	RISCV_CFG_GATING Gating Clock for RISCV_CFG 0: Mask 1: Pass

2.13.6.40 0x0128 RISCV_MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: RISCV_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	RISCV_MSGBOX_RST RISCV_MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/

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Offset: 0x0128			Register Name: RISCV_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	RISCV_MSGBOX_GATING Gating Clock for RISCV_MSGBOX 0: Mask 1: Pass

2.13.6.41 0x0130 DSP_PWMCTRL Clock Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: DSP_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PWMCTRL_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON
30	/	/	/
26:24	R/W	0x0	PWMCTRL_CLK_SRC_SEL Clock Source Selection 000: CLK24M 001: CLK32K 010:CLK_RC
23:0	/	/	/

2.13.6.42 0x0134 DSP_PWMCTRL Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: DSP_PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSP_PWMCTRL_RST DSP_PWMCTRL Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DSP_PWMCTRL_GATING Gating Clock for DSP_PWMCTRL PCLK 0: Mask 1: Pass

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2.13.6.43 0x0160 PLL Backdoor Output Enable Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PLL_BACKDOOR_OUTPUT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PLL_AUDIO1_ENABLE PLL AUDIO1 Enable 0: Disable 1: Enable

2.13.6.44 0x0164 Test Debug Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: TEST_DBG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_OUT_TEST_EN PLL Clock Output to PLLTEST pin Enable PLLTEST = PLL CLK Source/PLL_TEST_P_DIV 0: disable, 1: PLL Clock Output to PLLTEST
30:25	/	/	/
24	R/W	0x0	PLL_CLK_SOURCE AUDIOPLL Clock output selection on 0: AudioPLL output clock 1:AudioPLL reference clock
23:22	/	/	/
21:20	R/W	0x0	PLL_TEST_P_DIV PLL TEST Post Divider 00: /1 01: /2 10: /4 11: /8
19:0	/	/	/

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2.14 RTC

2.14.1 Overview

The Real Time Clock (RTC) is used to implement the time counter and the timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing the power-off information
- Multiple special registers for recording the BROM information

NOTE

The register configuration of RTC is AHB bus, it only can support word operation, not byte operation and half-word operation.

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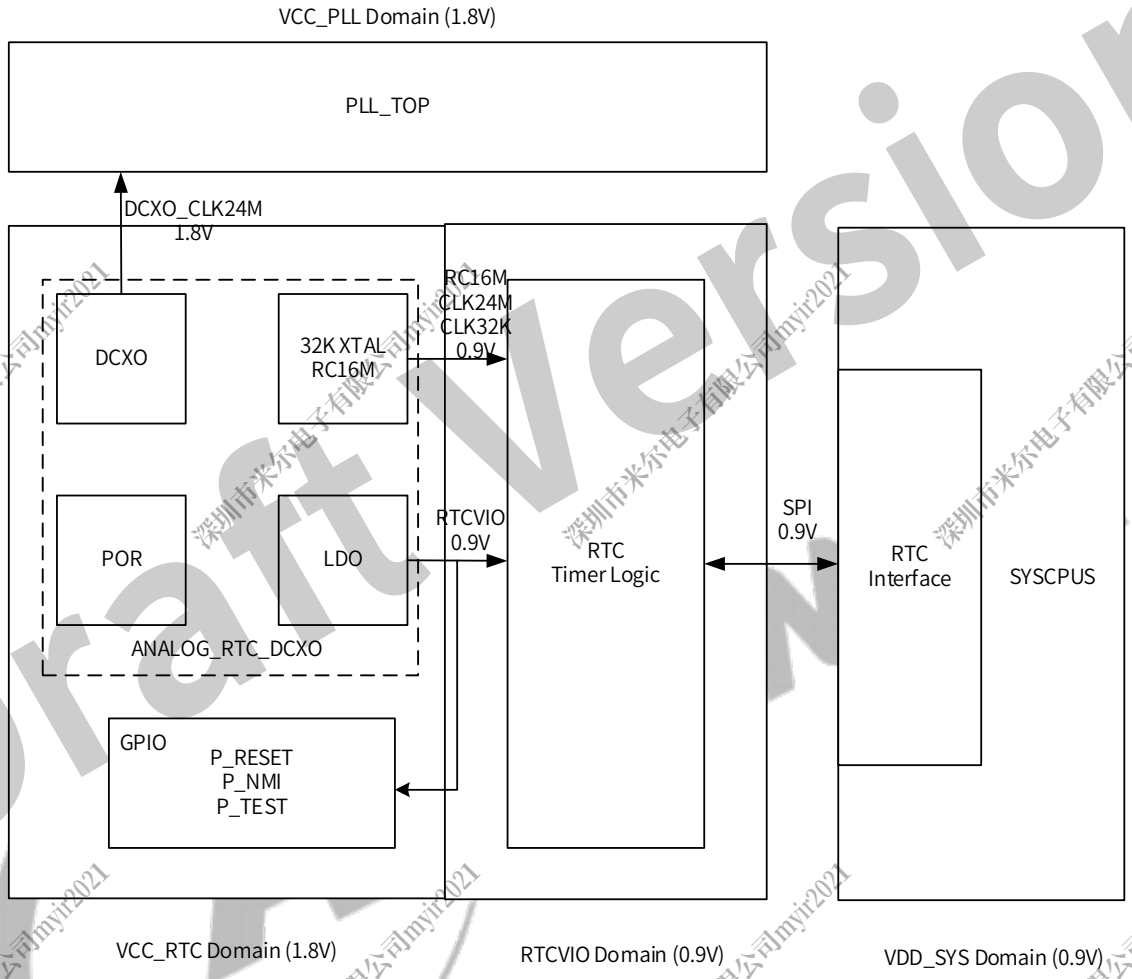
2.14.2 Block Diagram

The following figure shows the block diagram of the RTC.

Figure 2-28 RTC Block Diagram



2.14.3 Functional Descriptions

2.14.3.1 External Signals

Table 2-19 RTC External Signals

Signal Name	Description	Type
X32KFOUT	32.768 kHz clock Fanout Provides low frequency clock for external devices	AO,OD
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO

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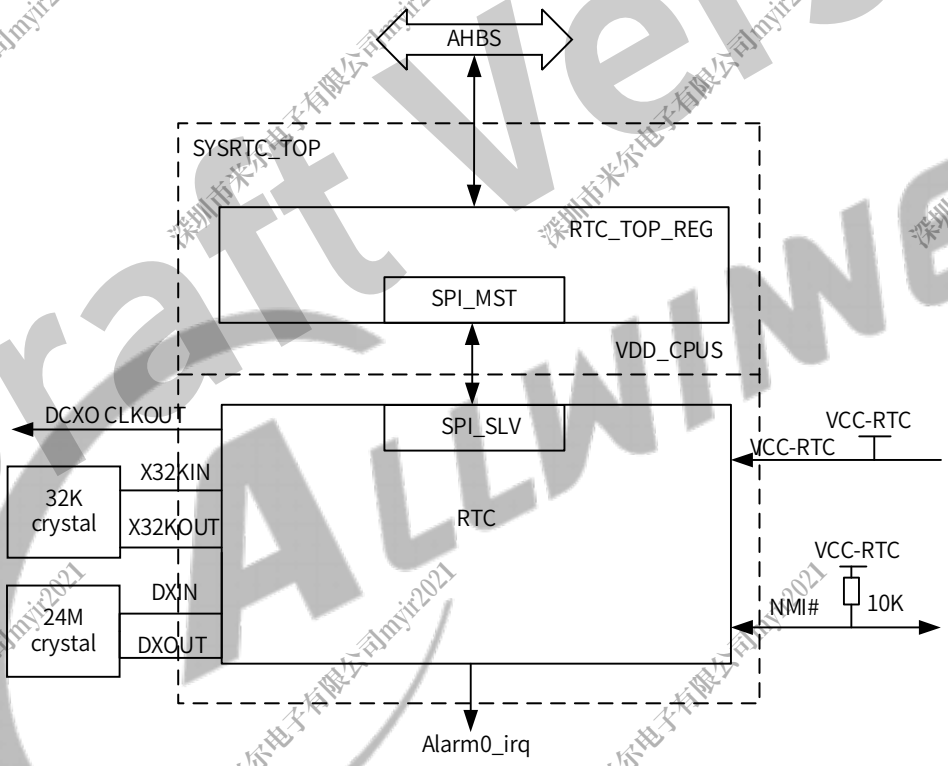
Signal Name	Description	Type
WREQIN	Request signal of REFCLK_OUT	AI
NMI	Non-Maskable Interrupt	I/O, OD
RESET	Reset Signal (Low Active)	I/O, OD
VCC-DCXO	Digital Compensated Crystal Oscillator Power Supply	P
VCC-RTC	RTC Power	P

2.14.3.2 Typical Application

Figure 2-29 RTC Application Diagram



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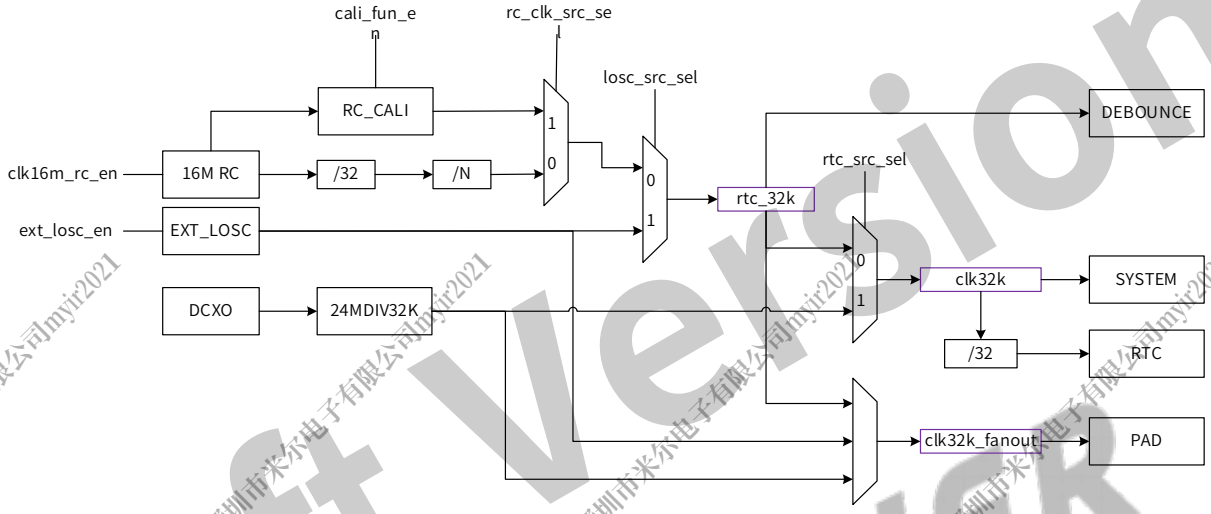
2.14.3.3 Clock Tree

The following figure shows the clock tree of the RTC.

Figure 2-30 RTC Clock Tree



RTC

The RTC has three clock sources:

- 32K divided by internal 16 MHz RC
- 32K divided by external DCXO
- external 32.768 kHz crystal

The RTC selects the internal RC by default, when the system starts, the RTC can select the external low frequency crystal to provide much accurate clock by software. The clock accuracy of the RTC is related to the accuracy of the external low frequency crystal. Usually 32.768 kHz crystal with ±50 ppm frequency tolerance is selected as the clock source. When using internal RC, the clock can be changed by changing division ratio. When using external clock, the clock cannot be changed.

System 32K

The system32K has three clock sources:

- 32K divided by the internal 16 MHz RC
- 32K divided by external DCXO
- external 32.768 kHz crystal

RTC_32K_FANOUT

The RTC_32K_FANOUT has three clock sources:

- 32K divided by the internal 16 MHz RC
- 32K divided by external DCXO
- external 32.768 kHz crystal

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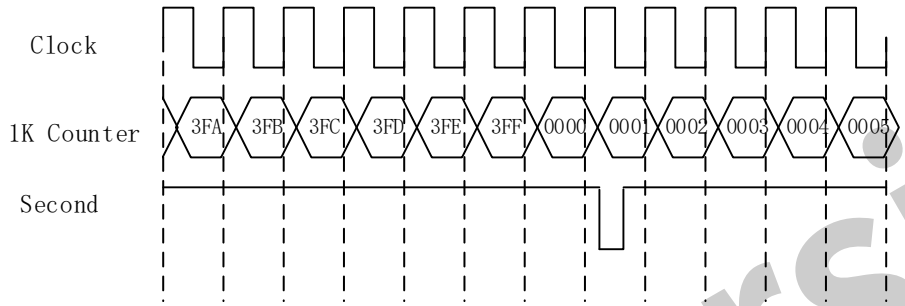
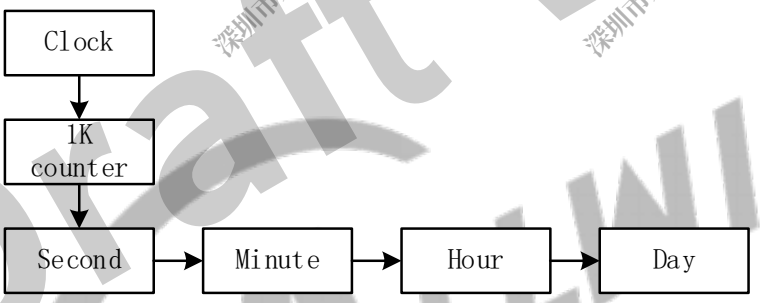
2.14.3.4 Real Time Clock

Figure 2-31 RTC Counter



The 1 kHz counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1 kHz counter starts to count again from 0, and the second counter adds 1. The step structure of 1 kHz counter is as follows.

Figure 2-32 RTC 1 kHz Counter Step Structure



According to above implementation, the changing range of each counter is as follows.

Table 2-20 RTC Counter Changing Range

Counter	Range
Second	0 to 59
Minute	0 to 59
Hour	0 to 23
Day	0 to 65535 (The year, month, day need be transformed by software according to day counter)

CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

2.14.3.5 Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

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The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC need set a new scheduled time, the next interrupt can be generated.

2.14.3.6 RTC-VIO

The RTC module has a LDO, the input source of the LDO is VCC-RTC, the output of the LDO is RTC-VIO, the value of RTC-VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

2.14.3.7 RC Calibration

Figure 2-33 Calibration Circuit

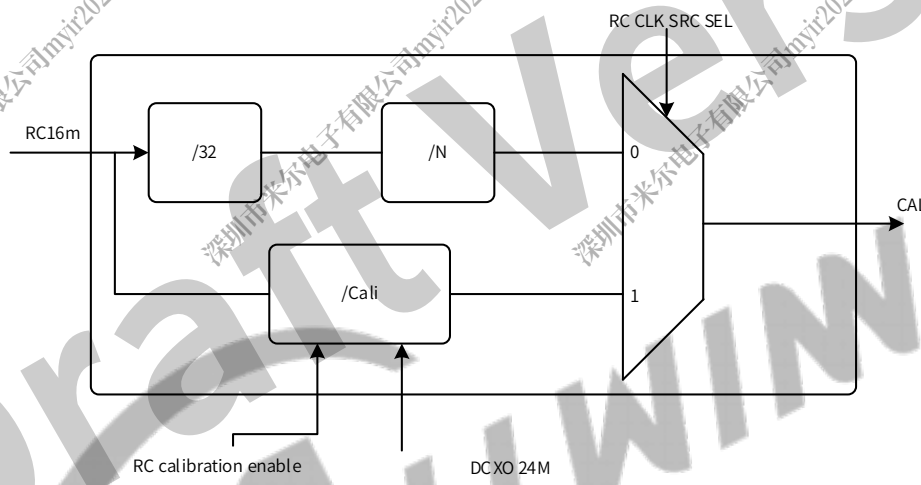
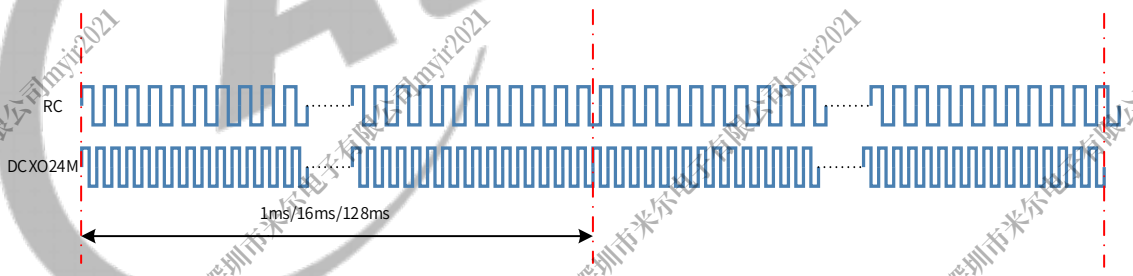


Figure 2-34 RC Waveform



The basic circuit of RC calibration is shown in Figure 2-33. Whether to output the calibrated RC clock can be selected by the RC_Cali_SEL control bit, the calibration principle is as follows:

Step 1 As shown in Figure 2-34, with DCXO 24M as the reference clock, calculate the counter number M of RC clock within 1 ms/16 ms/128 ms to obtain the accurate frequency of internal RC.

Step 2 Divide the accurate frequency by 32.768 kHz and the frequency divider(K) from RC clock to 32.768 kHz is obtained.

Step 3 Divide RC16M by the frequency divider(K) to obtain 32.768 kHz frequency.

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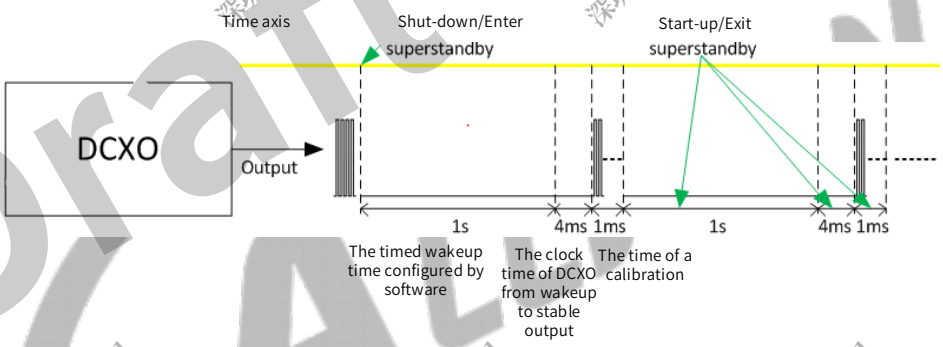
NOTE

The calibration principle is to output 32.768 kHz, not to input 16 MHz.

2.14.3.8 DCXO Timed Wakeup

The logic of DCXO timed wakeup circuit includes two controls: timed wakeup hardware automatic enable and timed wakeup time length (software configuration). The timed wakeup means that DCXO circuit is required to wakeup the output clock once every second (1s-60s, usually the ambient temperature changes little in a few seconds) for 32K calibration in the super standby or shutdown scenario, after calibration, DCXO circuit is closed, the closed time is timed wakeup time length (software configuration). The time of DCXO circuit from wakeup starting to stable output is 3 ms-4 ms. Although the timed wakeup function is closed, DCXO circuit always had worked. The process of timed wakeup is shown in the following figure.

Figure 2-35 DCXO Timed Wakeup Waveform



The time of a calibration in shutdown or super standby:

the timed wakeup time configured by software + the clock time of DCXO from wakeup to stable output + the time of a calibration.

The timed wakeup time configured by the software in the figure is 1 s, and can be configured by software in application. It is the theoretical maximum value for DCXO from wakeup to stable output clock in 4 ms, the specific value is subject to IC measured results. In the any time of these three periods, the startup or exit of the super standby action will not cause DCXO abnormal.

The enable signal of DCXO and the enable signal of timed wakeup DCXO is “OR” logic, and they do not contradict each other.

The interval between continuous DCXO enable operation and disable operation is at least greater than 4 ms.

2.14.3.9 RC Calibration Usage Scenario

Power-on: Select non-accurate 32K divided by internal RC.

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Normal scenario: Select external accurate 32K, or external calibrated 32K.

Standby or power-off scenario: Select external accurate 32K, or external calibrated 32K.

2.14.4 Programming Guidelines

2.14.4.1 RTC Clock Control

Step 1 Select clock source: Select clock source by the bit0 of LOSC_CTRL_REG, the clock source is the internal RC oscillator by default. When the system starts, the clock source can be switched to the external 32K oscillator by software.

Step 2 Auto switch: After enabled the bit [15:14] of LOSC_CTRL_REG, the RTC automatically switches clock source to the internal oscillator when the external crystal could not output waveform, the switch status can query by the bit [1] of LOSC_AUTO_SWT_STA_REG.

NOTE

If only configuring the bit [15] of LOSC_CTRL_REG, the clock source status bit cannot be changed after the auto switch is valid, because the two functions are independent.

Here are the basic code samples.

Write (0x16aa4000, LOSC_Ctrl); //Write key field

Write (0x16aa4001, LOSC_Ctrl); //Select the external 32K clock

2.14.4.2 RTC Calendar

Step 1 Write time initial value: Write the current time to RTC_DAY_REG and RTC_HH_MM_SS_SET_REG.

Step 2 After updated time, the RTC restarts to count again. The software can read the current time anytime.

NOTE

- The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.
- Ensure the bit [8:7] of LOSC_CTRL_REG is 0 before the next time configuration is performed.

Here are the basic code samples.

For example: set time to 21st, 07:08:09 and read it.

RTC_DAY_REG = 0x00000015;

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RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)

Read (RTC_DAY_REG);

Read (RTC_HH_MM_SS_REG);

2.14.4.3 Alarm0

Step 1 Enable alram0 interrupt by writing ALARM0_IRQ_EN.

Step 2 Set the counter comparator, write the count-down day, hour, minute, second number to ALARM0_DAY_SET_REG and ALARM0_CUR_VLU_REG.

Step 3 Enable alarm0 function by writing ALARM0_ENABLE_REG, then the software can query alarm count value in real time by ALARM0_DAY_SET_REG and ALARM0_CUR_VLU_REG. When the setting time reaches, ALARM0_IRQ_STA_REG is set to 1 to generate interrupt.

Step 4 After enter the interrupt process, write ALARM0_IRQ_STA_REG to clear the interrupt pending, and execute the interrupt process.

Step 5 Resume the interrupt and continue to execute the interrupted process.

Step 6 The power-off wakeup is generated via SoC hardware and PMIC, the software only needs to set the pending condition of alarm0, and set ALARM0_CONFIG_REG to 1.

2.14.4.4 Fanout

CLK32K Fanout

Set the LOSC_OUT_GATING bit (bit [0]) of CLK32K_FOUT_CTRL_GATING_REG register to 1, and ensure external pull-up resistor, voltage, and clock source are normal, then 32.768kHz square wave can be output.

CLK24M Fanout

To fanout CLK24M clock though REFCLK-OUT pin, configure the CLK_REQ_ENB bit (bit [31]) of DCXO_CTRL_REG register.

2.14.5 Register List

Module Name	Base Address
RTC	0x0709 0000

Register Name	Offset	Description
VDD_RTC Power Domain		
LOSC_CTRL_REG	0x0000	LOSC Control Register

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Register Name	Offset	Description
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
INTOSC_CLK_AUTO_CALI_REG	0x000C	Internal OSC Clock Auto Calibration Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_SET_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_DAY_SET_REG	0x0020	Alarm 0 Day Set Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM0_CONFIG_REG	0x0050	Alarm 0 Configuration Register
CLK32K_FOUT_CTRL_GATING_REG	0x0060	CLK32K Fanout Control register
GP_DATA_REGn	0x0100+N*0x0004 (N=0-7)	General Purpose Register
FBOOT_INFO_REG0	0x0120	Fast Boot Info Register0
FBOOT_INFO_REG1	0x0124	Fast Boot Info Register1
DCXO_CTRL_WP_REG	0x015C	DCXO Control Write Protect Register
DCXO_CTRL_REG	0x0160	DCXO Control Register
CALI_CTRL_REG	0x0164	Calibration Control Register
VDD_RTC_REG	0x0190	VDD_RTC Regulation Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_OFF_GATING_CTRL_REG	0x01F4	VDD Off Gating Control Register
EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
VDD_SYS Power Domain		
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

2.14.6 Register Description

2.14.6.1 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD KEY Field. This field should be filled with 0x16AA, and then the bit 0 and bit 1 can be written with the new value.

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Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable. 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K CLK source selection enable. 0: Disable. When the LOSC losts, 32k CLK source will not change to RC 1: Enable. When LOSC losts, 32k CLK source will change to RC (LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/
8	R	0x0	RTC_HHMMSS_ACCE RTC Hour Minute Second access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS register, the HH-MM-SS register will be refreshed for at most one second. Note: Make sure that the bit is 0 for time configuration.
7	R	0x0	RTC_DAY_ACCE RTC DAY access. After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second. Note: Make sure that the bit is 0 for time configuration.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32768Hz Crystal Enable. 0: disable 1: enable

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Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x0	EXT_LOSC_GSM External 32768Hz Crystal GSM. 00: Low 01: Reserved 10: Reserved 11: High When GSM is changed, the 32K oscillation circuit will arise transient instability. If the auto switch function (bit 15) is enabled, 32K changes to RC16M with certain probability. The GSM can influence the time of 32K starting oscillation, the more the GSM, the shorter the time of starting oscillation. So modifying GSM is not recommended. If you need to modify the GSM, firstly disable the auto switch function (bit 15), with a delay of 50 us, then change the GSM, the 32K clock source is changed to external clock.
1	R/W	0x0	RTC_SRC_SEL RTC_TIMER Clock Source Select. 0: LOSC_SRC 1: 24MDIV32K Before switching the bit, make sure that the 24MDIV32K function is enabled, that is, the bit16 of the 32K Fanout Control Register is 1.
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock Source Select. 'N' is the value of Internal OSC Clock Prescalar register. 0: Low Frequency Clock from 16M RC 1: External 32.768 kHz OSC.

2.14.6.2 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when auto switch function is enable. 0: External 32.768 kHz OSC work normally. 1: External 32.768 kHz OSC work abnormally.

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Offset: 0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending. 0: No effect 1: Auto switches pending, means LOSC_SRC_SEL is changed from 1 to 0.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar register. 0: Low Frequency Clock from 16M RC 1: External 32.768 kHz OSC

2.14.6.3 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset: 0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescalar value N The clock output = Internal RC/32 / N 00000: 1 00001: 2 00002: 3 ..... 11111: 32

2.14.6.4 0x000C Internal OSC Clock Auto Calibration Register (Default Value: 0x01E8_0000)

Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	Read/Write	Default/Hex	Description
31:22	R	0x1E8	32k calibration integer divide factor.
21:5	R	0x0	32k calibration decimal divide factor.
4	R/W	0x0	Calibration function Clk16M_RC_enable 0: Auto gating 1: Soft bypass
3:2	R/W	0x0	RC Calibration Precise Selection 00: 1ms calibration precise 01: 16ms calibration precise 10: 128ms calibration precise

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Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	RC calibration enable 0: Close Calibration circuit 1: Open Calibration circuit
0	R/W	0x0	RC CLK SRC SEL Select the RTC 32k clock source from normal RC or Calibrated RC： 0: Normal RC 1: Calibrated RC

2.14.6.5 0x0010 RTC Year-Month-DAY Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: RTC_DAY_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	UDF	DAY Set DAY. Range from 0-65535.

2.14.6.6 0x0014 RTC Hour-Minute-Second Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: RTC_HH_MM_SS_SET_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Set Hour. Range from 0-23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Set Minute. Range from 0-59
7:6	/	/	/
5:0	R/W	UDF	SECOND Set second. Range from 0-59

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2.14.6.7 0x0020 Alarm 0 Day Set Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is Based on Day.

2.14.6.8 0x0024 Alarm 0 Counter Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: ALARM0_CUR_VLU_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Current hour. Range from 0-23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Current minute. Range from 0-59
7:6	/	/	/
5:0	R/W	UDF	SECOND Current second. Range from 0-59

2.14.6.9 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: ALARM0_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. 0: Disable 1: Enable

2.14.6.10 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: ALARM0_IRQ_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x002C			Register Name: ALARM0_IRQ_EN
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable. 0: Disable 1: Enable

2.14.6.11 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit. 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 IRQ enable is set to 1, the pending bit will be sent to the interrupt controller.

2.14.6.12 0x0050 Alarm 0 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ALARM0_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

2.14.6.13 0x0060 CLK32K Fanout Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: CLK32K_FOUT_CTRL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DCXO_TO_32K_DIVIDER_ENABLE DCXO to 32k divider enable. 1: Enable the DCXO 24M to 32K divider circuit 0: Disable the DCXO 24M to 32K divider circuit
15:3	/	/	/

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Offset: 0x0060			Register Name: CLK32K_FOUT_CTRL_GATING_REG
Bit	Read/Write	Default/Hex	Description
2:1	R/W	0x0	LOSC_OUT_SRC_SEL LOSC Output Source Select. 00: RTC_32K (select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: LOSC 10: DCXO divided 32K
0	R/W	0x0	LOSC_OUT_GATING LOSC Output Gating Enable. Configuration of LOSC output, and no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

2.14.6.14 0x0100+N*0x0004 (N=0-7) General Purpose Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0004 (N=0-7)			Register Name: GP_DATA_REGn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA Data.

NOTE

General purpose register 0 to 7 value can be stored if the RTC-VI O is larger than 0.7 V.

2.14.6.15 0x0120 Fast Boot Info Register0 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: FBOOT_INFO_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO0. Fast Boot info. Fast Boot Information, refer to BROM spec.

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2.14.6.16 0x0124 Fast Boot Info Register1 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: FBOOT_INFO_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO1. Fast boot info. Fast Boot Information, refer to BROM spec.

2.14.6.17 0x015C DCXO Control Write Protect Register (Default Value:0x0000_0000)

Offset: 0x015C			Register Name: DCXO_CTRL_WP_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	Key Filed. Write protection for XO_CTRL_REG(0x0160). Write this field as 0x16AA before configuring XO_CTRL_REG(0x0160) and this field will be automatically cleared to 0 after XO_CTRL_REG is configured.

2.14.6.18 0x0160 DCXO Control Register (Default Value: 0x983F_10F7)

Offset: 0x0160			Register Name: DCXO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CLK_REQ_ENB CLK REQ Enable 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:29	/	/	/
28	R	0x1	DCXO_STABLE_STS DCXO Stable Status 0: no stable 1: stable
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value.
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value. cap cell is 55fF
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage.

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Offset: 0x0160			Register Name: DCXO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal active high.
6	R/W	0x1	XTAL_MODE XTAL mode enable signal active high. 0x0 for external CLK input mode. 0x1 for normal mode.
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO RFCLK Enhance. Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for 10pF, 0x2 for 15pF, 0x3 for 20pF
3	/	/	/
2	R/W	0x1	RSTO_DLY_SEL RSTO delay select. For Debug Use Only It cannot configure to 0 in normal state.
1	R/W	0x1	DCXO_EN DCXO Enable. 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN Clock RC16M Enable. 1: Enable 0: Disable The related register configuration is necessary to ensure the reset debounce circuit has a stable clock source. The first time SoC starts up, by default, the reset debounce circuit of SoC uses 32K divided by RC16M. In power-off, software reads the related bit to ensure whether EXT32K is working normally, if it is normal, first switch the clock source of debounce circuit to EXT32K, then close RC16M. Without EXT32K scenario or external RTC scenario, software confirms firstly whether EXT32K is working normally before switching, or software does not close RC16M.

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2.14.6.19 0x0164 Calibration Control Register (Default Value: 0x0000_0043)

Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WAKEUP_DCXO_EN Wake up DCXO circuit enable.
30:17	/	/	/
16	R/W	0x0	WAKEUP_READY_SLEEP_MODE Calibration wake up ready sleep mode, it must be set before 0x164 bit31 WAKEUP_DCXO_EN is set to 1. 0: Disable 1: Enable
15:12	R/W	0x0	TIMER FOR READY SLEEP Total timer for ready sleep 0x00: 15s 0x01: 30s 0x02: 45s 0x03: 60s 0x04: 90s 0x05: 120s 0x06: 150s Others: /
11:8	R/W	0x0	WAKEUP_CNT FOR READY SLEEP Wake up counter for ready sleep 0x00: 250ms 0x01: 500ms 0x02: 750ms 0x03: 1s 0x04: 1.25s 0x05: 1.5s 0x06: 1.75s 0x07: 2s 0x08: 2.25s 0x09: 2.5s 0x0A: 2.75s 0x0B: 3s 0x0C: 3.25s 0x0D: 3.5s 0x0E: 3.75s 0x0F: 4s

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Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x4	WAKEUP_CNT FOR SLEEP Wake up counter for sleep 0x00: 250ms 0x01: 500ms 0x02: 1s 0x03: 10s 0x04: 60s 0x05: 120s 0x06: 180s 0x07: 240s 0x08: 300s 0x09: 360s 0x0A: 420s 0x0B: 480s 0x0C: 540s 0x0D: 600s 0x0E: 1200s 0x0F: 1800s
3:0	R/W	0x3	WAIT DCXO SEL Select for DCXO active after DCXO enable 0x0: 1ms 0x1:2ms 0x2:3ms 0x3:4ms ... 0xF: 16ms

2.14.6.20 0x0190 VDD RTC Regulation Register (Default Value: 0x0000_0004)

Offset: 0x0190			Register Name: VDD_RTC_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	V_SEL VDD Select 0: Resistance divider 1: Band gap
3	/	/	/

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Offset: 0x0190			Register Name: VDD_RTC_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x4	VDD_RTC_REGU RTC VIO voltage select The RTC-VIO is provided power for RTC digital part. These bits are useful for regulating the RTC_VIO from 0.65 V to 1.3 V: 0x0: 1.0 V 0x1: 0.65 V 0x2: 0.7 V 0x3: 0.8 V 0x4: 0.9 V 0x5: 1.1 V 0x6: 1.2 V 0x7: 1.3 V

2.14.6.21 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: IC_CHARA_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	KEY_FIELD Write protect. Should be written at value 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA IC_CHARA. Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

2.14.6.22 0x01F4 VDD Off Gating Control Register (Default Value: 0x0000_0021)

Offset: 0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Write protect. This field should be filled with 0x16AA, and then the bit 15 can be configured.

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Offset: 0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
15	WAC	0x0	PWROFF_GAT_RTC_CFG. Power off gating control signal. When use VDD-SYS to RTC isolation software control, write this bit 1, it will only be clear by RESETB release. (For Debug Use Only)
14:12	/	/	/
11:4	R/W	0x2	VCCIO_DET_SPARE VCCIO detect spare. Bit [7:5]: Reserved Bit [4]: Bypass debounce circuit 0: bypass 1: no bypass Bit [3]: Enable control 0: Disable VCC-IO detecter 1: Force the detection output Bit [2:0]: Gear adjustment 000: Detection threshold is 2.5 V 001: Detection threshold is 2.6 V 010: Detection threshold is 2.7 V 011: Detection threshold is 2.8 V 100: Detection threshold is 2.9 V 101: Detection threshold is 3 V 110-111: N/A
3:1	/	/	/
0	R/W	0x1	VCCIO_DET_BYPASS_EN VCCIO detect bypass enable. 0: not bypass 1: bypass

2.14.6.23 0x0204 eFuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EFUSE_1P8V_POWER_SWITCH_CONTROL EFUSE power switch control 1: open power switch 0: close power switch

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2.14.6.24 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0009)

Offset: 0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RTC_SPI_GATE_EN RTC Reg CFG SPI Clock Gating. 0: Gating 1: Not Gating Before configurating RTC register, the clock divider of SPI needs be configured firstly, then clock gating needs be enabled. Note: Frequency division and clock gating can not be set at the same time.
30:5	/	/	/
4:0	R/W	0x9	RTC_SPI_DIV RTC Reg CFG SPI Clock Divider M. Actual SPI Clock = AHBS1/(M+1), (0 to 15) The default frequency of AHBS1 is 200 MHz, and the default frequency of SPI Clock is 20 MHz. **Note: The SPI clock can not exceed 50 MHz, or else the RTC register may be abnormal.**

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2.15 Spinlock

2.15.1 Overview

The spinlock provides hardware synchronization mechanism in multi-core systems. With the lock operation, the spinlock prevents multiple processors from handling the sharing data simultaneously and thus ensure the coherence of data.

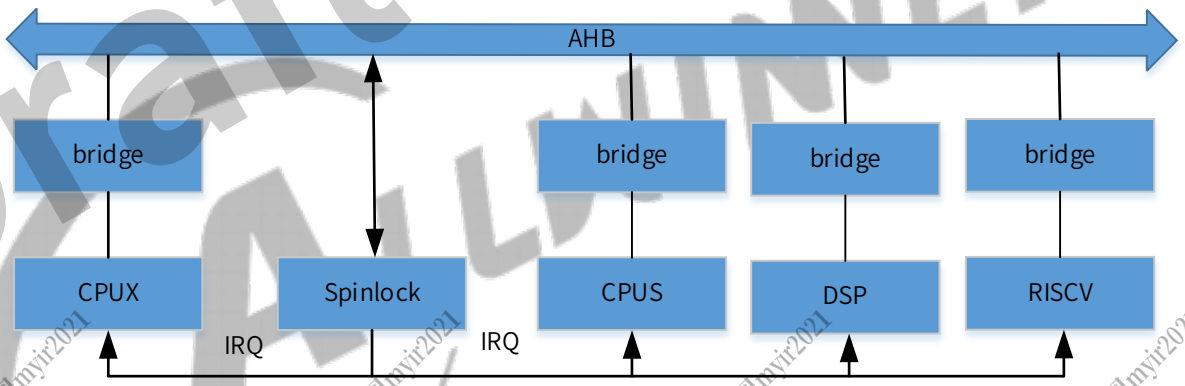
The spinlock has the following features:

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

2.15.2 Block Diagram

The following figure shows the block diagram of the spinlock.

Figure 2-36 Spinlock Block Diagram



2.15.3 Functional Description

2.15.3.1 Clock and Reset

The spinlock is mounted on AHB. Before accessing the spinlock registers, you need to de-assert the reset signal on AHB bus and then open the corresponding gating signal on AHB bus.

2.15.3.2 Typical Application

The following figure shows a typical application of the spinlock. A processor locks spinlock0 before executing specific codes, and then unlocks the codes. After the lock is freed, other processors can read or write the data.

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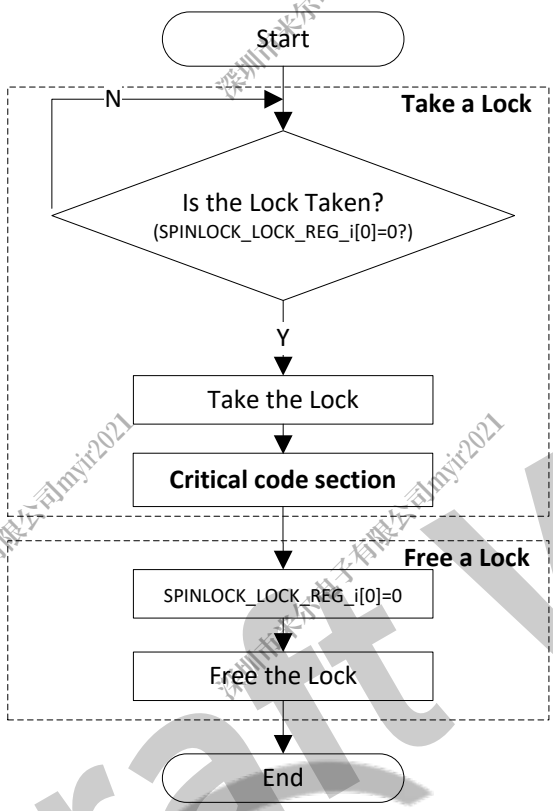
Figure 2-37 Spinlock Typical Application Diagram



2.15.3.3 Spinlock State Machine

When a processor uses spinlock, it needs to acquire the spinlock status through SPINLOCK_STATUS_REG.

Reading operation

when the return value is 0, it indicates that the spinlock enters the locked status; reading this status bit again can return 1, it indicates that the spinlock is the locked status.

Writing operation

when the spinlock is in the locked status, writing 0 can convert the spinlock to the unlocked status, the writing operation for other status is invalid.

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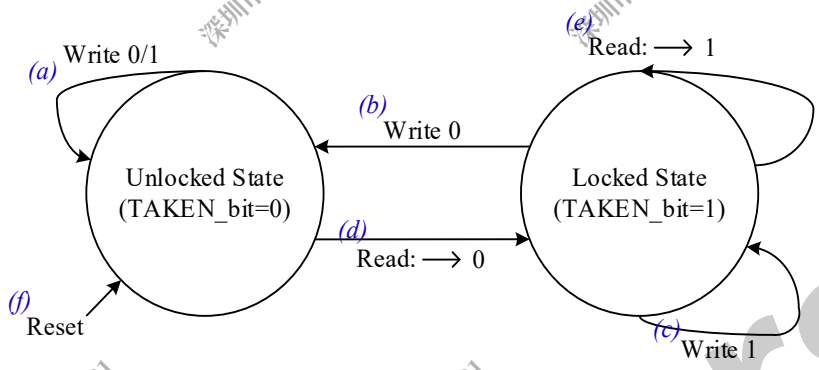
The following figure shows the spinlock state machine.

Figure 2-38 Spinlock State Machine



- When the spinlock is in the unlocked state, writing 0/1 has no effect;
- When the spinlock is in the locked state, writing 0 can convert the corresponding spinlock to the unlocked state;
- When the spinlock is in the locked state, writing 1 has no effect;
- When the spinlock is in the unlocked state, reading the bit can return 0 (it indicates spinlock enters into the locked state);
- When the spinlock is in the locked state, reading the bit can return 1 (it indicates spinlock is in the locked state);
- After reset, the spinlock is in the unlock state by default.

2.15.4 Programming Guidelines

2.15.4.1 Switching the Status

Follow the steps below to switch the lock status of a spinlock.

Step 1 When the read value from SPINLOCKN_LOCK_REG (N=0–31) is 0, the spinlock comes into the locked status.

Step 2 Execute the application codes, and the status of SPINLOCK_STATUS_REG is 1.

Step 3 Write 0 to SPINLOCKN_LOCK_REG (N=0–31), the spinlock converts into the unlocked status, and the corresponding spinlock is released.

2.15.4.2 Processing the Interrupt

The spinlock generates an interrupt when a lock is freed (the lock status converts from the locked status to the unlocked status).

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Follow the steps below to process the interrupt:

Step 1 Configure the interrupt enable bit of the corresponding spinlock in SPINLOCK_IRQ_EN_REG to enable the interrupt.

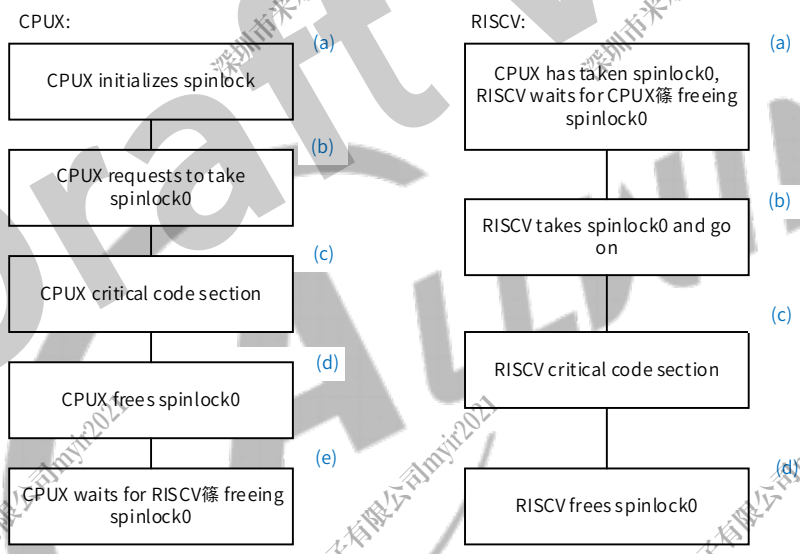
Step 2 The spinlock generates an interrupt when its status converts from the locked status to the unlocked status, and the corresponding bit of the SPINLOCK_IRQ_STA_REG turns to 1.

Step 3 Execute the interrupt handle function and clear the pending bit.

2.15.4.3 Taking/Freeing Spinlock

Take the synchronization between CPUX and RISCV with Spinlock0 as an example, the CPUX and RISCV perform the following steps.

Figure 2-39 CPUX and RISCV Taking/Freeing Spinlock0 Process



CPUX:

a) The CPUX initializes Spinlock.

b) Check lock register0 (SPINLOCK_STATUS_REG0) status. If it is taken, check until CPUX frees spinlock0 and then request to take spinlock0. Otherwise, retry until the lock register0 is taken.

c) Execute CPUX critical code.

d) After executing CPUX critical code, the CPUX frees spinlock0.

The CPUX waits for RISCV to free spinlock0.

RISCV:

a) If the CPUX has taken spinlock0, the RISCV waits for CPUX to free spinlock0.

b) The RISCV requests to take spinlock0. If it fails, retry until the lock register0 is taken.

c) Execute RISCV critical code.

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d) After executing RISCV critical code, the RISCV frees spinlock0.

The following codes are for reference.

----------CPUX----------

Step 1 CPUX initializes Spinlock

```
put_wvalue(SPINLOCK_BGR_REG,0x00010000);
put_wvalue(SPINLOCK_BGR_REG,0x00010001);
```

Step 2 CPUX requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG0);                  //Check lock register0 status
if (rdata != 0) writel (0, SPINLOCK_LOCK_REG0); //If it is taken, check till CPUX frees spinlock0
rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
if (rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0);    //If it fails, retry till lock register0 is taken
```

---------- **CPUX critical code section** ----------

Step 3 CPUX frees spinlock0

```
writel (0, SPINLOCK_LOCK_REG0);                     //CPUX frees spinlock0
```

Step 4 CPUX waits for RISCV' freeing spinlock0

```
writel(readl(SPINLOCK_STATUS_REG0) == 1);           //CPUX waits for RISCV' freeing spinlock0
```

----------RISCV----------

Step 1 CPUX has taken spinlock0, RISCV waits for CPUX' freeing spinlock0

```
while(readl(SPINLOCK_STATUS_REG0) == 1);            //RISCV waits for CPUX' freeing spinlock0
```

Step 2 RISCV takes spinlock0 and go on

```
rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
if (rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0);    //If it fails, retry till lock register0 is taken
```

---------- **RISCV critical code section** ----------

Step 3 RISCV frees spinlock0

```
writel (0, SPINLOCK_LOCK_REG0);                     //RISCV frees spinlock0
```

2.15.5 Register List

Module Name	Base Address
SPINLOCK	0x03005000
S_SPINLOCK	0x07093000

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Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	Spinlock Interrupt Enable Register
SPINLOCK_IRQ_STA_REG	0x0040	Spinlock Interrupt Status Register
SPINLOCK_LOCKID0_REG	0x0080	Spinlock Lockid0 Register
SPINLOCK_LOCKID1_REG	0x0084	Spinlock Lockid1 Register
SPINLOCK_LOCKID2_REG	0x0088	Spinlock Lockid2 Register
SPINLOCK_LOCKID3_REG	0x008C	Spinlock Lockid3 Register
SPINLOCK_LOCKID4_REG	0x0090	Spinlock Lockid4 Register
SPINLOCK_LOCK_REGN	0x0100 + N*0x0004	Spinlock Register N (N = 0 to 31)

2.15.6 Register Description

2.15.6.1 0x0000 Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 256 lock registers 01: This instance has 32 lock registers 10: This instance has 64 lock registers 11: This instance has 128 lock registers
27:9	/	/	/
8	R	0x0	IU0 In-Use flag0, covering lock register0-31 0: All lock registers 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

2.15.6.2 0x0010 Spinlock Register Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LOCK_REG_STATUS SpinLock[i] status 0: The Spinlock is free 1: The Spinlock is taken

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2.15.6.3 0x0020 Spinlock Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LOCK_IRQ_EN SpinLock[i] interrupt enable 0: Disable 1: Enable

2.15.6.4 0x0040 Spinlock Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	LOCK_IRQ_STATUS SpinLock[i] interrupt status 0: No effect 1: Pending Writing 1 clears this bit.

2.15.6.5 0x0080 Spinlock Lockid0 Register (Default Value: 0x7777_7777)

Offset: 0x0080			Register Name: SPINLOCK_LOCKIN0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID0

2.15.6.6 0x0084 Spinlock Lockid1 Register (Default Value: 0x7777_7777)

Offset: 0x0084			Register Name: SPINLOCK_LOCKIN1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID1

2.15.6.7 0x0088 Spinlock Lockid2 Register (Default Value: 0x7777_7777)

Offset: 0x0088			Register Name: SPINLOCK_LOCKIN2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID2

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2.15.6.8 0x008C Spinlock Lockid3 Register (Default Value: 0x7777_7777)

Offset: 0x008C			Register Name: SPINLOCK_LOCKIN3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID3

2.15.6.9 0x0090 Spinlock Lockid4 Register (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: SPINLOCK_LOCKIN4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID4

2.15.6.10 0x0100 + N*0x04 Spinlock Register N (N = 0 to 31) (Default Value: 0x0000_0000)

Offset: 0x0100 + N*0x0004 (N = 0 to 31)			Register Name: SPINLOCKN_LOCK_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TAKEN Lock State Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

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2.16 Thermal Sensor Controller (THS)

2.16.1 Overview

The thermal sensors are common elements in wide range of modern system on chips (SoCs) platform. The thermal sensors are used to constantly monitor the temperature on the chip.

The thermal sensor controller (THS) embeds four thermal sensors. TSENSOR0 is located in the 'big' cores of CPUX; TSENSOR1 is located in the 'LITTLE' cores of CPUX; TSENSOR2 is located in the GPU; TSENSOR3 is located in the NPU;TSENSOR4 is located in the DDR. When the temperature reaches a certain thermal threshold, the thermal sensor can generate interrupts to the software to lower the temperature via the dynamic voltage and frequency scaling (DVFS) technology.

The THS has the following features:

- Two THS controllers
  - THS0, including TSENSOR4
  - THS1, including TSENSOR0, TSENSOR1, TSENSOR2, and TSENSOR3
- Temperature accuracy: ±5°C from -40°C to +60°C, ±3°C from +60°C to +125°C
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

2.16.2 Block Diagram

The following figures show the block diagrams of the THS0 and THS1.

Figure 2-40 THS0 Block Diagram

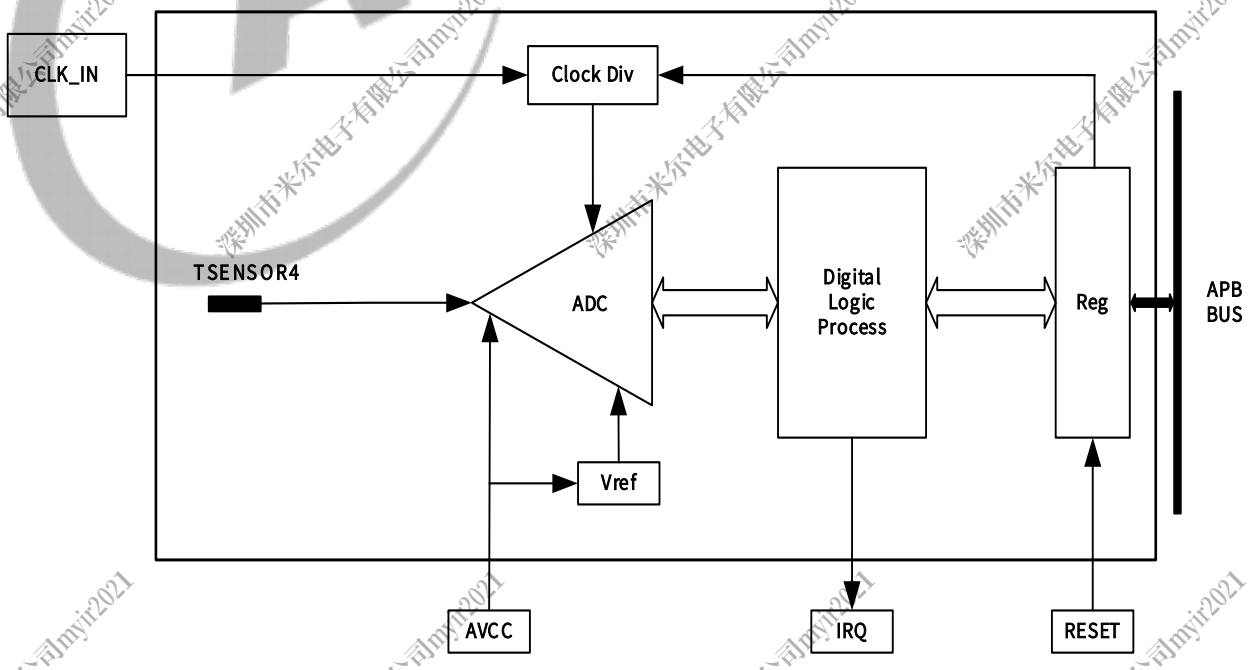

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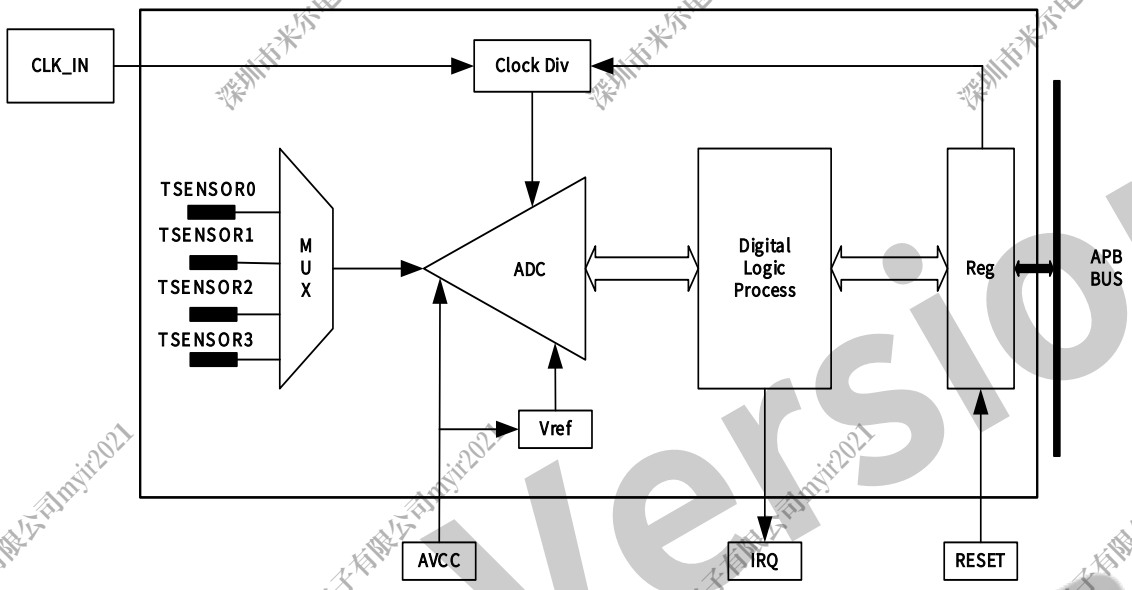
Figure 2-41 THS1 Block Diagram



2.16.3 Functional Description

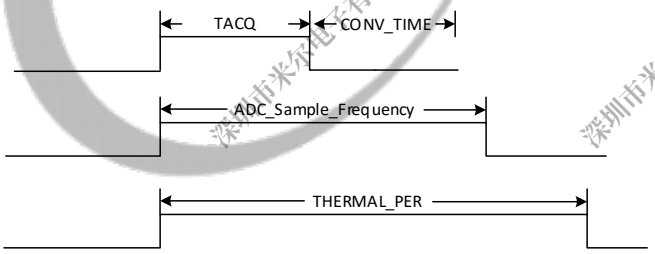
2.16.3.1 Clock Source

Both of THS0 and THS1 get two clock sources: DCXO24M and PCLK. For details about clock configurations, refer to section 2.7 Clock Controller Unit (CCU).

2.16.3.2 Timing Requirements

The following figure shows the timing requirements for the THS module.

Figure 2-42 Thermal Sensor Timing Requirement



CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/24 MHz x 14 Cycles = 0.583 us

TACQ > 1/24 MHz x 24 Cycles

THERMAL_PER > ADC_Sample_Frequency > TACQ + CONV_TIME

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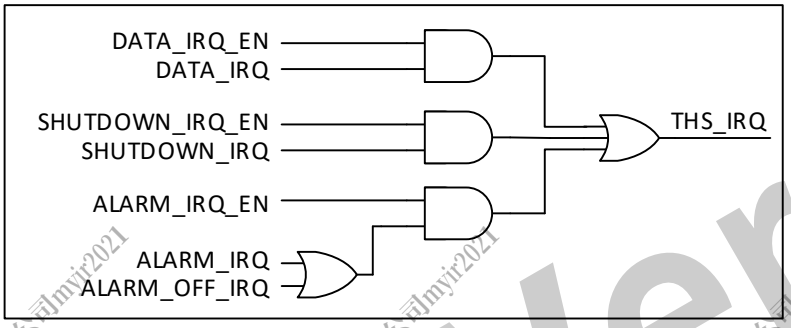
2.16.3.3 Interrupts

The THS module has four interrupt sources: DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ, and ALARM_OFF_IRQ. The following figure shows thermal sensor interrupt sources.

Figure 2-43 Thermal Sensor Controller Interrupt Source



DATA_IRQ

The interrupt is generated when the measured sensor_data is updated.

SHUTDOWN_IRQ

The interrupt is generated when the temperature is higher than the shutdown threshold.

ALARM_IRQ

The interrupt is generated when the temperature is higher than the Alarm_Threshold.

ALARM_OFF_IRQ

The interrupt is generated when the temperature drops to lower than the Alarm_Off_Thershold. It is triggered at the fall edge.

2.16.3.4 THS Temperature Conversion Formula

-40°C to +55°C: T=(sensor_data-2736)/(-13.54)

+55°C to 125°C: T= (sensor_data-2825)/(-15.33)

Unit of T: Celsius degree (°C).

The sensor_data is read from the sensor data register.

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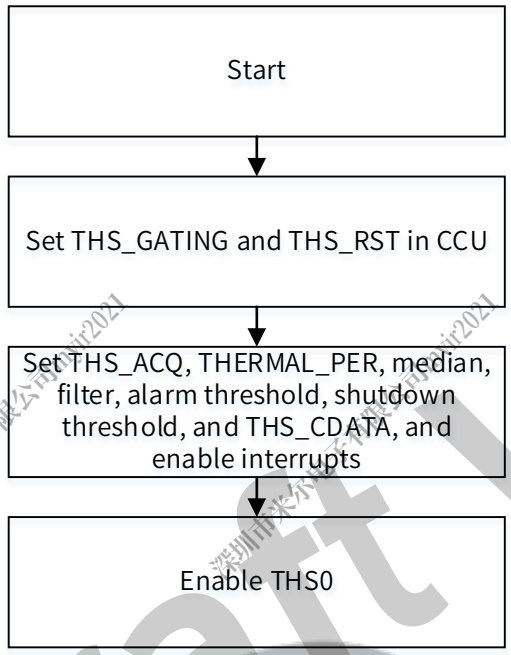
2.16.4 Programming Guidelines

The initial process of the THS is as follows.

Figure 2-44 THS Initial Process



In the final test (FT) stage, the THS is calibrated through the ambient temperature, and the calibration value is written in the SID module. The following table shows the THS0 and THS1 information in the SID.

Table 2-21 THS Information in the SID

eFuse Name	Base Address	Bit	Description
T-sensor Calibration	0x3B-0x3F (72 bits)	35-24	The calibration value of TSENSOR0
		23-12	The calibration value of TSENSOR1
		11-0	ROOM
	0x44-0x48 (72 bits)	35-24	The calibration value of TSENSOR4
		23-12	The calibration value of TSENSOR3
		11-0	The calibration value of TSENSOR2

Before enabling THS, read eFuse value and write the value to TSENSORn_CDATA (n=0, 1, 2, 3, or 4).

Query Mode

the following takes THs0 as an example, THS0 and THS1 are the same.

Step 1 Write 0x1 to the bit [16] of THS_BGR_REG to dessert the reset.

Step 2 Write 0x1 to the bit [0] of THS_BGR_REG to open the THS clock.

Step 3 Write 0x2F to the bit [15:0] of THS0_CTRL to set the ADC acquire time.

Step 4 Write 0x1DF to the bit [31:16] of THS0_CTRL to set the ADC sample frequency divider.

Step 5 Write 0x3A to the bit [31:12] of THS0_PER to set the THS work period.

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Step 6 Write 0x1 to the bit [2] of THS0_FILTER to enable the temperature convert filter.

Step 7 Write 0x1 to the bit [1:0] of THS0_FILTER to select the filter type.

Step 8 Read THS eFuse value from SID, then write the eFuse value to TSENSOR4_CDATA to calibrate THS.

Step 9 Write 0x1 to the bit [0] 0f THS0_EN to enable THS.

Step 10 Read the bit [0] of THS0_DATA_INTS. If it is 1, the temperature conversion is complete.

Step 11 Read the bit [11:0] of TSENSOR4_DATA, and calculate the THS temperature based on section 2.16.3.4 THS Temperature Conversion FormulaTHS Temperature Conversion Formula.

Interrupt Mode

the following takes THs0 as an example, THS0 and THS1 are the same.

Step 1 Write 0x1 to the bit16 of THS_BGR_REG to dessert the reset.

Step 2 Write 0x1 to the bit0 of THS_BGR_REG to open the THS clock.

Step 3 Write 0x2F to the bit [15:0] of THS0_CTRL to set the ADC acquire time.

Step 4 Write 0x1DF to the bit [31:16] of THS0_CTRL to set the ADC sample frequency divider.

Step 5 Write 0x3A to the bit [31:12] of THS0_PER to set the THS work period.

Step 6 Write 0x1 to the bit2 of THS0_FILTER to enable the temperature convert filter.

Step 7 Write 0x1 to the bit [1:0] of THS0_FILTER to select the filter type.

Step 8 Read THS eFuse value from SID, and then write the eFuse value to TSENSOR4_CDATA to calibrate THS.

Step 9 Write 0x1 to the bit [0] of THS0_DATA_INTC to enable the interrupt of THS.

Step 10 Set GIC interface based on IRQ 71.

Step 11 Put the interrupt handler address into the interrupt vector table.

Step 12 Write 0x1 to the bit [0] 0f THS0_EN to enable THS.

Step 13 Read the bit [0] of THS0_DATA_INTS. If it is 1, the temperature conversion is complete.

Step 14 Read the bit [11:0] of TSENSOR4_DATA, and calculate the THS temperature based on section 2.16.3.4 THS Temperature Conversion FormulaTHS Temperature Conversion Formula.

2.16.5 Register List

THS module includes two groups of registers:

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Module Name	Base Address
THS0	0x0200_A000
THS1	0x0200_9400

2.16.5.1 THS0 Register list

Module Name	Base Address
THS0	0x0200_A000

Register Name	Offset	Description
THS0_CTRL	0x0000	THS0 Control Register
THS0_EN	0x0004	THS0 Enable Register
THS0_PER	0x0008	THS0 Period Control Register
THS0_DATA_INTC	0x0010	THS0 Data Interrupt Control Register
THS0_SHUT_INTC	0x0014	THS0 Shut Interrupt Control Register
THS0_ALARM_INTC	0x0018	THS0 Alarm Interrupt Control Register
THS0_DATA_INTS	0x0020	THS0 Data Interrupt Status Register
THS0_SHUT_INTS	0x0024	THS0 Shut Interrupt Status Register
THS0_ALARMO_INTS	0x0028	THS0 Alarm off Interrupt Status Register
THS0_ALARM_INTS	0x002C	THS0 Alarm Interrupt Status Register
THS0_FILTER	0x0030	THS0 Median Filter Control Register
TSENSOR4_ALARM_CTRL	0x0040	TSENSOR4 Alarm threshold Control Register
TSENSRO4_SHUTDOWN_CTRL	0x0080	TSENSRO4 Shutdown threshold Control Register
TSENSOR4_CDATA	0x00A0	TSENSOR4 Calibration Data
TSENSOR4_DATA	0x00C0	TSENSOR4 Data Register

2.16.5.2 THS1 Regsiter List

Module Name	Base Address
THS1	0x0200_9400

Register Name	Offset	Description
THS1_CTRL	0x0000	THS1 Control Register
THS1_EN	0x0004	THS1 Enable Register
THS1_PER	0x0008	THS1 Period Control Register
THS1_DATA_INTC	0x0010	THS1 Data Interrupt Control Register
THS1_SHUT_INTC	0x0014	THS1 Shut Interrupt Control Register
THS1_ALARM_INTC	0x0018	THS1 Alarm Interrupt Control Register
THS1_DATA_INTS	0x0020	THS1 Data Interrupt Status Register

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Register Name	Offset	Description
THS1_SHUT_INTS	0x0024	THS1 Shut Interrupt Status Register
THS1_ALARMO_INTS	0x0028	THS1 Alarm off Interrupt Status Register
THS1_ALARM_INTS	0x002C	THS1 Alarm Interrupt Status Register
THS1_FILTER	0x0030	THS1 Median Filter Control Register
TSENSOR0_ALARM_CTRL	0x0040	TSENSOR0 Alarm threshold Control Register
TSENSOR1_ALARM_CTRL	0x0044	TSENSOR1 Alarm threshold Control Register
TSENSOR2_ALARM_CTRL	0x0048	TSENSOR2 Alarm threshold Control Register
TSENSOR3_ALARM_CTRL	0x004C	TSENSOR3 Alarm threshold Control Register
TSENSOR0&TSENSOR1_SHUTDOWN_CTRL	0x0080	TSENSOR0 & TSENSOR1 Shutdown threshold Control Register
TSENSOR2&TSENSOR3_SHUTDOWN_CTRL	0x0084	TSENSOR2&TSENSOR3 Shutdown threshold Control Register
TSENSOR0&TSENSOR1_CDATA	0x00A0	TSENSOR0 & TSENSOR1 Calibration Data
TSENSOR2&TSENSOR3_CDATA	0x00A4	TSENSOR2&TSENSOR3 Calibration Data
TSENSOR0_DATA	0x00C0	TSENSOR0 Data Register
TSENSOR1_DATA	0x00C4	TSENSOR1 Data Register
TSENSOR2_DATA	0x00C8	TSENSOR2 Data Register
TSENSOR3_DATA	0x00CC	TSENSOR3 Data Register

2.16.6 THS0 Register Description

2.16.6.1 0x0000 THS0 Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS0_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC Acquire Time CLK_IN/ (n + 1) The default value is 2 us.
15:0	R	0x2F	Reserved

2.16.6.2 0x0004 THS0 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS0_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0004			Register Name: THS0_EN
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TSENSOR40_EN Enable temperature measurement sensor 0: Disable 1:Enable

2.16.6.3 0x0008 THS0 Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS0_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature measurement period 4096*(n + 1)/CLK_IN The default value is 10 ms.
11:0	/	/	/

2.16.6.4 0x0010 THS0 Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS0_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TSENSOR4_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR4 0: Disable 1:Enable

2.16.6.5 0x0014 THS0 Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS0_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SHUT_INT_EN Selects shutdown interrupt for TSENSOR4 0: Disable 1:Enable

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2.16.6.6 0x0018 THS0 Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS0_ALARM_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM_INT_EN Selects alarm interrupt for TSENSOR4 0: Disable 1:Enable

2.16.6.7 0x0020 THS0 Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS0_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	TSENSOR4_DATA_IRQ_STS Data interrupt status for TSENSOR4 Write '1' to clear this interrupt.

2.16.6.8 0x0024 THS0 Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS0_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	SHUT_INT_STS Shutdown Interrupt Status for TSENSOR4 Write '1' to clear this interrupt.

2.16.6.9 0x0028 THS0 Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS0_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM_OFF_STS Alarm Interrupt Off Pending for TSENSOR4 Write '1' to clear this interrupt.

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2.16.6.10 0x002C THS0 Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS0_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM_INT_STS Alarm Interrupt Pending for TSENSOR4 Write '1' to clear this interrupt.

2.16.6.11 0x0030 THS0 Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS0_FILTER
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

2.16.6.12 0x0040 THS0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM_T_HOT TSENSOR4 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM_T_HYST TSENSOR4 Alarm Threshold for Hysteresis temperature

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2.16.6.13 0x0080 TSENSOR4 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: TSENSOR4 _SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x4E9	SHUT_T_HOT TSENSOR4 Shutdown Threshold for Hot Temperature

2.16.6.14 0x00A0 TSENSOR4 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: TSENSOR4 _CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x800	TSENSOR4_CDATA TSENSOR4 Calibration Data

2.16.6.15 0x00C0 TSENSOR4 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: TSENSOR4_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR4_DATA Temperature measurement data of TSENSOR4

2.16.7 THS1 Register Description

2.16.7.1 0x0000 THS1 Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS1_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC Acquire Time CLK_IN/ (n + 1) The default value is 2 us.
15:0	R	0x2F	Reserved

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2.16.7.2 0x0004 THS1 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS1_EN
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TSENSOR3_EN Enable Temperature Measurement Sensor3 0: Disable 1:Enable
2	R/W	0x0	TSENSOR2_EN Enable Temperature Measurement Sensor2 0: Disable 1:Enable
1	R/W	0x0	TSENSOR1_EN Enable Temperature Measurement Sensor1 0: Disable 1:Enable
0	R/W	0x0	TSENSOR0_EN Enable Temperature Measurement Sensor0 0: Disable 1:Enable

2.16.7.3 0x0008 THS1 Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS1_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature Measurement Period 4096*(n + 1)/CLK_IN The default value is 10 ms.
11:0	/	/	/

2.16.7.4 0x0010 THS1 Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS1_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TSENSOR3_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR3 0: Disable 1:Enable

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Offset: 0x0010			Register Name: THS1_DATA_INTC
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	TSENSOR2_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR2 0: Disable 1:Enable
1	R/W	0x0	TSENSOR1_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR1 0: Disable 1:Enable
0	R/W	0x0	TSENSOR0_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR0 0: Disable 1:Enable

2.16.7.5 0x0014 THS1 Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS1_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	SHUT_INT3_EN Selects Shutdown Interrupt for TSENSOR3 0: Disable 1:Enable
2	R/W	0x0	SHUT_INT2_EN Selects Shutdown Interrupt for TSENSOR2 0: Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects Shutdown Interrupt for TSENSOR1 0: Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects Shutdown Interrupt for TSENSOR0 0: Disable 1:Enable

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2.16.7.6 0x0018 THS1 Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS1_ALARM_INTC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ALARM_INT3_EN Selects Alarm Interrupt for TSENSOR3 0: Disable 1: Enable
2	R/W	0x0	ALARM_INT2_EN Selects Alarm Interrupt for TSENSOR2 0: Disable 1: Enable
1	R/W	0x0	ALARM_INT1_EN Selects Alarm Interrupt for TSENSOR1 0: Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects Alarm Interrupt for TSENSOR0 0: Disable 1:Enable

2.16.7.7 0x0020 THS1 Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS1_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	TSENSOR3_DATA_IRQ_STS Data Interrupt Status for TSENSOR3 Write '1' to clear this interrupt.
2	R/W1C	0x0	TSENSOR2_DATA_IRQ_STS Data Interrupt Status for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	TSENSOR1_DATA_IRQ_STS Data Interrupt Status for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	TSENSOR0_DATA_IRQ_STS Data Interrupt Status for TSENSOR0 Write '1' to clear this interrupt.

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2.16.7.8 0x0024 THS1 Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS1_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	SHUT_INT3_STS Shutdown Interrupt Status for TSENSOR3 Write '1' to clear this interrupt.
2	R/W1C	0x0	SHUT_INT2_STS Shutdown Interrupt Status for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown Interrupt Status for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown Interrupt Status for TSENSOR0 Write '1' to clear this interrupt.

2.16.7.9 0x0028 THS1 Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS1_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	ALARM_OFF3_STS Alarm Interrupt Off Pending for TSENSOR3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_OFF2_STS Alarm Interrupt Off Pending for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm Interrupt Off Pending for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm Interrupt Off Pending for TSENSOR0 Write '1' to clear this interrupt.

2.16.7.10 0x002C THS1 Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS1_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x002C			Register Name: THS1_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	ALARM_INT3_STS Alarm Interrupt Pending for TSENSOR3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_INT2_STS Alarm Interrupt Pending for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm Interrupt Pending for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS Alarm Interrupt Pending for TSENSOR0 Write '1' to clear this interrupt.

2.16.7.11 0x0030 THS1 Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS1_FILTER
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

2.16.7.12 0x0040 TSENSOR0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: TSENSOR0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT TSENSOR0 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST TSENSOR0 Alarm Threshold for Hysteresis Temperature

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2.16.7.13 0x0044 TSENSOR1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: TSENSOR1_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT TSENSOR1 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST TSENSOR1 Alarm Threshold for Hysteresis Temperature

2.16.7.14 0x0048 TSENSOR2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: TSENSOR2_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT TSENSOR2 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST TSENSOR2 Alarm Threshold for Hysteresis Temperature

2.16.7.15 0x004C TSENSOR3 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x004C			Register Name: TSENSOR3_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM3_T_HOT TSENSOR3 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM3_T_HYST TSENSOR3 Alarm threshold for hysteresis temperature

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2.16.7.16 0x0080 TSENSOR0 & TSENSOR1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: TSENSOR0&TSENSOR1_SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT TSENSOR1 Shutdown Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT TSENSOR0 Shutdown Threshold for Hot Temperature

2.16.7.17 0x0084 TSENSOR2&TSENSOR3 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0084			Register Name: TSENSOR2&TSENSOR3 _SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x4E9	SHUT3_T_HOT TSENSOR3 Shutdown Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT TSENSOR2 Shutdown Threshold for Hot Temperature

2.16.7.18 0x00A0 TSENSOR0 & TSENSOR1 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: TSENSOR0&TSENSOR1_CDATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x800	TSENSOR1_CDATA TSENSOR1 Calibration Data
15:12	/	/	/
11:0	R/W	0x800	TSENSOR0_CDATA TSENSOR0 Calibration Data

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2.16.7.19 0x00A4 TSENSOR2&TSENSOR3 Calibration Data (Default Value: 0x0000_0800)

Offset: 0x00A4			Register Name: TSENSOR2&TSENSOR3 _CDATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x800	TSENSOR3_CDATA TSENSOR3 Calibration Data
15:12	/	/	/
11:0	R/W	0x800	TSENSOR2_CDATA TSENSOR2 Calibration Data

2.16.7.20 0x00C0 TSENSOR0 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: TSENSOR0_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR0_DATA Temperature Measurement Data of TSENSOR0

2.16.7.21 0x00C4 TSENSOR1 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: TSENSOR1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR1_DATA Temperature Measurement Data of TSENSOR1

2.16.7.22 0x00C8 TSENSOR2 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: TSENSOR2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR2_DATA Temperature Measurement Data of TSENSOR2

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2.16.7.23 0x00CC TSENSOR3 Data Register(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: TSENSOR3_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR3_DATA Temperature measurement data of TSENSOR3

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2.17 Timer

2.17.1 Overview

The Timer module implements the timing and counting functions, which includes CPUX_TIMER, CPUS_TIMER, and DSP_TIMER. There are 6 timers in TIMER, 3 timers in CPUS_TIMER, and 6 timers in DSP_TIMER.

The Timer module has the following features:

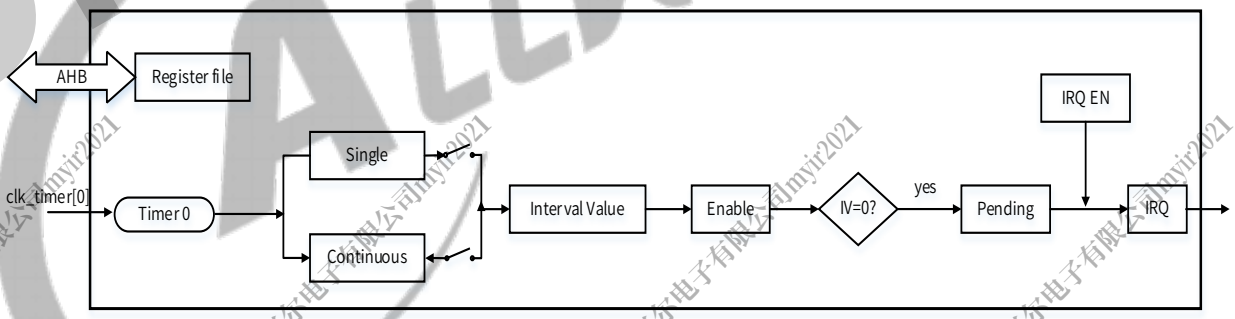
- The AHB port is used to configure the timer register
- Configurable count clock: PRCM/CCU can be switched to 32 kHz, 24 MHz, 16 MHz, and 200 MHz
- Programmable 56-bit down timer
- Supports two timing modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.17.2 Block Diagram

The timer is a 56-bit down counter. The counter value is decremented by 1 on each rising edge of the timer clock.

The following figure shows t NIhe block diagram for the timer.

Figure 2-45 Block Diagram for the Timer



NOTE

timer0 is used for illustration here. Block diagrams for other timers are the same.

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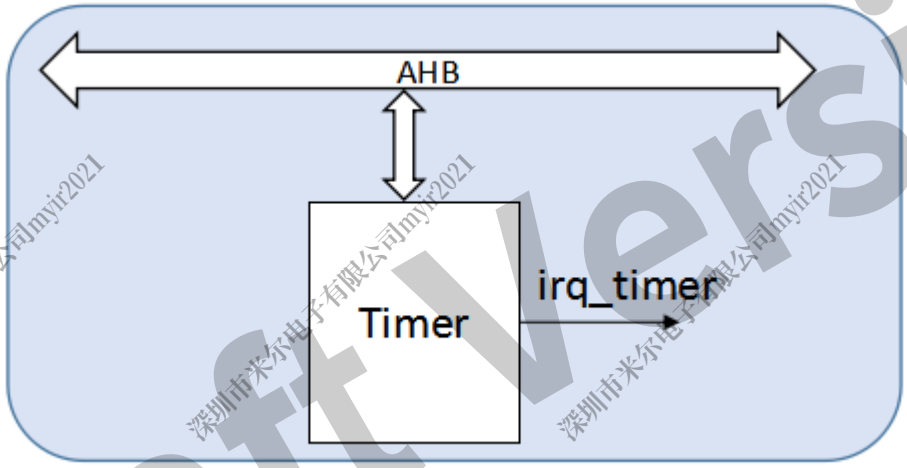
2.17.3 Functional Descriptions

2.17.3.1 Typical Application

The following figure shows the typical application of the Timer module.

Figure 2-46 Timer Typical Application



The Timer is mounted at the AHB bus. The system configures and controls the Timer via the AHB bus.

2.17.3.2 Formula for Calculating the Timer Time

The following formula describes the relationship among timer parameters.

$$T = \frac{\{TIMER_IVH, TIMER_IVL\} - \{TIMER_CVH, TIMER_CVL\}}{f_{clk_timer}}$$

Where,

TIMER_IVH=the higher 24 bits of the interval value, which could be configured by the lower 24 bits of the TIMER_IVH_REG register;

TIMER_IVL=the lower 32 bits of the interval value, which could be configured by the TIMER_IVL_REG register;

TIMER_CVH=the higher 24 bits of the current value, which could be configured by the lower 24 bits of the TIMER_CVH_REG register;

TIMER_CVL=the lower 32 bits of the current value, which could be configured by the TIMER_CVL_REG register;

fclk_timer=the frequency of the timer clock source;

{TIMER_IVH, TIMER_IVL} = 56-bit interval value of the timer;

{TIMER_CVH, TIMER_CVL}= 56-bit current value of the timer.

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2.17.3.3 Timing Modes

The timer has two timing modes: the single counting mode and the periodic mode. You can configure the timing mode via the bit[7] of TIMER_CTRL_REG. The value 0 is for the period mode and value 1 is for the single counting mode.

- Single Counting Mode

In the single counting mode, the timer starts counting from the interval value and generates an interrupt after the counter decreases to 0, and then stops counting. It starts to count again only when the interval value is reloaded.

- Periodic Mode

In the periodic mode, the timer restarts another round of counting after generating the interrupt. It reloads data from the Timer Interval Value and then continues to count.

2.17.4 Programming Guidelines

2.17.4.1 Initializing the Timer

Refer to the following steps to initialize the timer:

Step 1 Configure the timer parameters including the clock source and timing mode by writing TIMER_CTRL_REG. There is no sequence requirement of configuring these parameters.

Step 2 Write the interval value.

a) Write TIMER_IVL bit of TIMER_IVL_REG register and TIMER_IVH bit of TIMER_IVH_REG register to configure the interval value for the timer.

b) Write bit [1] of TIMER_CTRL_REG to load the interval value to the timer. The value of the bit will be cleared automatically after the interval value is loaded.

Step 3 Write bit [0] of TIMER_CTRL_REG to start the timer. Read TIMER_CVL bit of TIMER_CVL_REG register and TIMER_CVH bit of TIMER_CVH_REG register to get the current value of the timer.

NOTE

When performing read or write operations on the current register, operate TIMER_CVL_REG register before TIMER_CVH_REG register.

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2.17.4.2 Processing the Interrupt

Refer to the following steps to process the interrupt:

Step 1 Enable interrupts for the timer: write the enable bit of the corresponding interrupt in TIMER_IRQ_REG for the timer. The timer will generate an interrupt once the count value reaches 0.

Step 2 After the software program enters the interrupt process, write the pending bit of the corresponding interrupt in TIMER_STA_REG to clear the interrupt pending.

Step 3 Resume the interrupt and continue to execute the interrupted process.

2.17.5 Register List

Module Name	Base Address	The value of N
CPUX_TIMER	0x0300 8000	0-5
CPUS_TIMER	0x0709 0400	0-2
DSP_TIMER	0x0712 3000	0-5

Register Name	Offset	Description
TIMER_IRQ_REG	0x0000	Timer IRQ Enable Register
TIMER_STA_REG	0x0004	Timer Status Register
TIMER_SEC_REG	0x0008	Timer Secure Register
TIMER_CTRL_REG	0x0020+0x0020*N	Timer Control Register
TIMER_IVL_REG	0x0024+0x0020*N	Timer Interval Value bit[31:0] Register
TIMER_CVL_REG	0x0028+0x0020*N	Timer Current Value [31:0]bit Register
TIMER_IVH_REG	0x002C+0x0020*N	Timer Interval Value bit[55:32] Register
TIMER_CVH_REG	0x0030+0x0020*N	Timer Current Value [55:32]bit Register

2.17.6 Register Description

2.17.6.1 0x0000 Timer IRQ Enable Register (Default: 0x0000_0000)

Offset: 0x0000			Register Name: TIMER_IRQ_REG
Bit	Read/Write	Default/Hex	Description
31:NUM	/	/	/
NUM-1:0	R/W	0x0	Timer (0-NUM-1) Interrupt Enable 1: Enable 0: Disable

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2.17.6.2 0x0004 Timer Status Register (Default: 0x0000_0000)

Offset: 0x0004			Register Name: TIMER_STA_REG
Bit	Read/Write	Default/Hex	Description
31:NUM	/	/	/
NUM-1:0	R/WC	0x0	Timer (0-NUM-1) Status 1: Pending 0:No effect

2.17.6.3 0x0008 Timer Secure Register (Default: 0x0000_003F)

Offset: 0x0008			Register Name: TIMER_SEC_REG
Bit	Read/Write	Default/Hex	Description
31:NUM	/	/	/
NUM-1:0	R/W	0x3F	Timer (0-NUM-1) Secure Control 1: Secure 0: Non-secure

2.17.6.4 0x0020+0x0020*N(N=0-5) Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x0020+0x0020*N(N=0-5)			Register Name: TIMER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TIMER_MODE Timer Mode 0: Continuous mode. When interval value reached, the timer will restart another round of counting automatically. 1: Single mode. When interval value is reached, the timer will stop counting.
6:2	/	/	/
1	R/W	0x0	TIMER_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it's cleared automatically.

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Offset: 0x0020+0x0020*N(N=0-5)			Register Name: TIMER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TIMER_EN. Timer 0 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

2.17.6.5 0x0024+0x0020*N(N=0-5) Timer Low Interval Value Register (Default: 0x0000_0000)

Offset: 0x0024+0x0020*N(N=0-5)			Register Name:TIMER_IVL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TIMER_IVL Timer Interval Value bit[31:0] Register

2.17.6.6 0x0028+0x0020*N(N=0-5) Timer Low Current Value Register (Default: 0x0000_0000)

NOTE

- The current value register is a 56-bit register. When read or write the current value, the TIMER_CVL should be read or write first.
- Enable the TIMER_EN.bit (bit [0]) of the TIMER_CTRL_REG register and set the bus clock frequency of the Timer to be twice the function clock frequency before reading the current value register.

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Offset: 0x0028+0x0020*N(N=0-5)			Register Name: TIMER_CVL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TIMER_CVL Timer Current Value bit[31:0] Register

2.17.6.7 0x002C+0x0020*N(N=0-5) Timer High Interval Value Register (Default: 0x0000_0000)

Offset: 0x002C+0x0020*N(N=0-5)			Register Name: TIMER_IVH_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	TIMER_IVH Timer Interval Value bit[55:32] Register

2.17.6.8 0x0030+0x0020*N(N=0-5) Timer High Current Value Register (Default: 0x0000_0000)

NOTE

Enable the TIMER_EN.bit (bit [0]) of the TIMER_CTRL_REG register and set the bus clock frequency of the Timer to be twice the function clock frequency before reading the current value register.

Offset: 0x0030+0x0020*N(N=0-5)			Register Name: TIMER_CVH_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	TIMER_CVH Timer Current Value bit[55:32] Register

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2.18 Watchdog Timer (WDT)

2.18.1 Overview

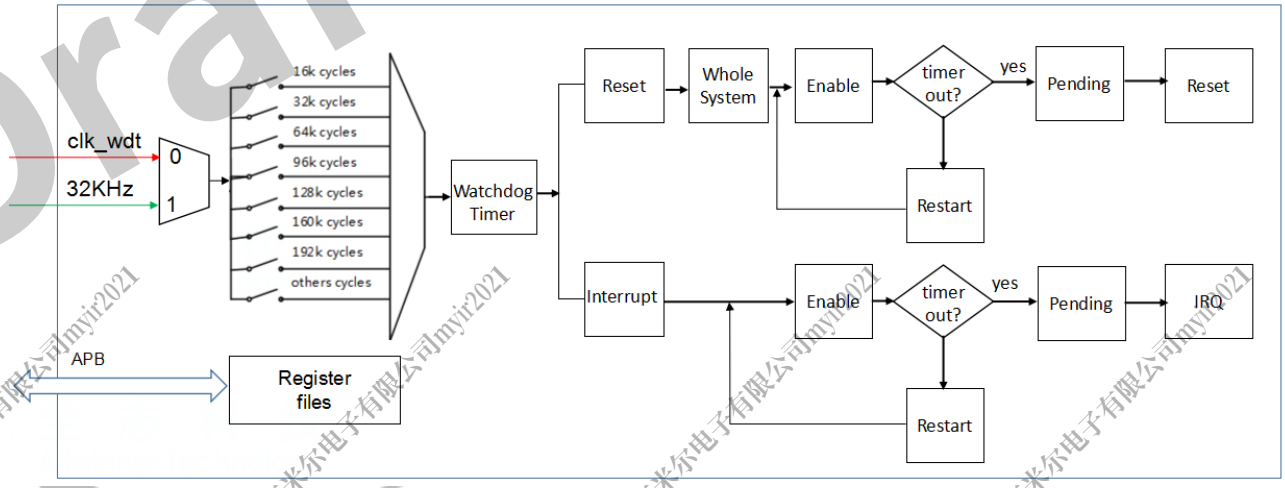
Watchdog is used to transmit a reset signal to reset the entire system after an exception occurs in the system. It has the following features:

- Four watchdog timers: CPUX_WDT in CPUX domain, DSP_WDT, CPUS_WDT and RISCV_WDT in CPUS domain
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

2.18.2 Block Diagram

The following figure shows the functional block diagram of the watchdog module.

Figure 2-47 Watchdog Block Diagram



2.18.3 Functional Descriptions

2.18.3.1 Clock Sources

The clock source of the watchdog is either LOSC (32 kHz) or HOSC/750 (24 MHz/750). Configure the bit [8] of the WDT_CFG_REG to select a clock source.

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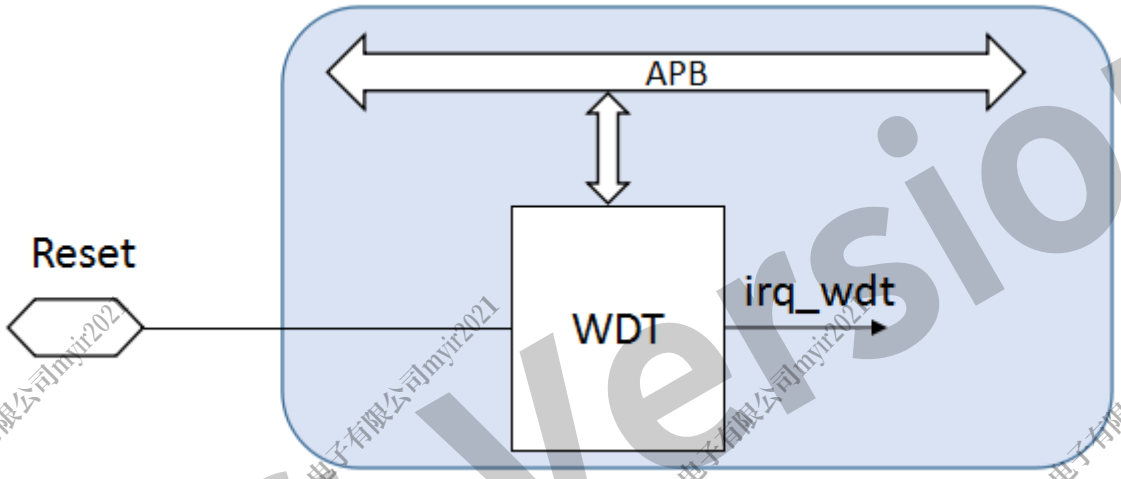
2.18.3.2 Typical Application

Figure 2-48 Watchdog Application Diagram



Watchdog configures register by APB bus.

The system configures the time of watchdog, if the system has no timing for restart watchdog (such as bus hang dead), then watchdog sends out watchdog reset external signal to reset system; meanwhile watchdog outputs signal to RESET pad to reset PMIC.

2.18.3.3 Operating Modes

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. The watchdog has two operating modes.

- Interrupt mode

The bit [1:0] of the WDT_CFG_REG is set to 0x2, when the counter value reaches 0 and the bit [0] of the WDT_IRQ_EN_REG is written to 1, the watchdog generates an interrupt, the watchdog enters into interrupt mode.

- Reset mode

The bit [1:0] of the WDT_CFG_REG is set to 0x1, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

2.18.4 Programming Guidelines

2.18.4.1 Initializing the Watchdog

Follow the steps below to initialize the watchdog:

Step 1 Configure the bit [1:0] of the WDT_CFG_REG to configure the generation of the interrupts or the output of reset signal.

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Step 2 Configure the bit [7:4] of the WDT_MODE_REG to configure the initial count value.

Step 3 Write the bit [0] of the WDT_MODE_REG to 1 to enable the watchdog.

2.18.4.2 Processing the Interrupt

Follow the steps below to process the interrupt:

Step 1 Write the bit [0] of the WDT_IRQ_EN_REG to 1 to enable the interrupt.

Step 2 After enter the interrupt process, write the bit [0] of the WDT_IRQ_STAT to 1 to clear the interrupt pending, and execute the process of waiting for the interrupt.

Step 3 Resume the interrupt and continue to execute the interrupted process.

2.18.4.3 Resetting the Watchdog

In the following instance making configurations for WDT: configure clock source as HOSC/750, configure Interval Value as 1s and configure Watchdog Configuration as to whole system. This instance indicates that reset system after 1s.

```
writel (0x16AA_0001, WDT_CFG_REG);                          //To whole system
writel (0x16AA_0010, WDT_MODE_REG);                         //Interval Value set 1s
writel(readl(WDT_MODE_REG) |(1<<0)|(0x16AA<<16), WDT_MODE_REG);     //Enable WDT
```

2.18.4.4 Restarting the Watchdog

In the following instance making configurations for WDT: configure clock source as HOSC/750, configure Interval Value as 1s and configure Watchdog Configuration as to whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
write (0x16AA_0001, WDT_CFG_REG);                           //To whole system
write (0x16AA_0010, WDT_MODE_REG);                          //Interval Value set 1s
writel(readl(WDT_MODE_REG) |(1<<0)|(0x16AA<<16), WDT_MODE_REG);     //Enable WDT
----other codes---
writel(readl(WDT_CTRL_REG) |(0xA57<<1) | (1<<0), WDT_CTRL_REG); //Write 0xA57 at Key Field and Restart WDT
```

2.18.5 Register List

Module Name	Base Address
CPUX_WDT	0x0205 0000
CPUS_WDT	0x0702 0400
DSP_WDT	0x0710 0400

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Module Name	Base Address
RISCV_WDT	0x0713 2000

Register Name	Offset	Description
WDT_IRQ_EN_REG	0x0000	WDT IRQ Enable Register
WDT_IRQ_STAT	0x0004	WDT Status Register
WDT_SRST_REG	0x0008	WDT Software Reset Register
WDT_CTRL_REG	0x000C	WDT Control Register
WDT_CFG_REG	0x0010	WDT Configuration Register
WDT_MODE_REG	0x0014	WDT Mode Register
WDT_OCFG_REG	0x0018	WDT Output Configuration Register

2.18.6 Register Description

2.18.6.1 0x0000 WDT IRQ Enable Register (Default: 0x0000_0000)

Offset: 0x0000			Register Name: WDT_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WDT Interrupt Enable

2.18.6.2 0x0004 WDT Status Register (Default: 0x0000_0000)

Offset: 0x0004			Register Name: WDT_IRQ_STAT
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	WDT Status WDT IRQ Pending.set 1 to the bit will clear it. 1:pending, WDT interval value is reched 0:No effect

2.18.6.3 0x0008 WDT Software Reset Register Register (Default: 0x0000_0000)

Offset: 0x0008			Register Name: WDT_SRST_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	KEY Field This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15:1	/	/	/

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Offset: 0x0008			Register Name: WDT_SRST_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Soft Reset Enable 0: De-assert 1: Reset System If this bit is used for system reset, the watchdog should be disabled.

2.18.6.4 0x000C WDT Control Register Register (Default: 0x0000_0000)

Offset: 0x000C			Register Name: WDT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:1	W	0x0	Watchdog Key Field Should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	Watchdog Restart 0: No effect 1: Restart the Watchdog 0

2.18.6.5 0x0010 WDT Configuration Register Register (Default: 0x0000_0001)

Offset: 0x0010			Register Name: WDT_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 15:0 can be written with the new value.
15:9	/	/	/
8	R/W	0x0	WDT Clock select 1: LOSC (32 kHz) 0: HOSC / 750 (24MHz/750)
7:2	/	/	/
1:0	R/W	0x1	WDT Configuration 00: / 01: to whole system 10: only interrupt 11: /

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2.18.6.6 0x0014 WDT Mode Register Register (Default: 0x0000_0000)

Offset: 0x0014			Register Name: WDT_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field. This field should be filled with 0x16AA, and then the bit 15:0 can be written with the new value.
15:8	/	//	/
7:4	R/W	0x0	WDT Interval Value. Watchdog clock source is HOSC / 750. If the clock source is turned off, WDT will not work. 0000: 16k cycles (0.5s) 0001: 32k cycles (1s) 0010: 64k cycles (2s) 0011: 96k cycles (3s) 0100: 128k cycles (4s) 0101: 160K cycles (5s) 0110: 192k cycles (6s) 0111: 256k cycles (8s) 1000: 320k cycles (10s) 1001: 384k cycles (12s) 1010: 448k cycles (14s) 1011: 512k cycles (16s) 1100: / 1101: / 1110: / 1111: /
3:1	/	/	
0	R/W	0x0	Watchdog Enable. 0: disable ; 1: enable

2.18.6.7 0x0018 WDT Output Configuration Register Register (Default: 0x0000_001F)

Offset: 0x0018			Register Name: WDT_OCFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 11:0 can be written with the new value.
15:12	/	/	/

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Offset: 0x0018			Register Name: WDT_OCFG_REG
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x1F	WDT OUTPUT CONFIG WDT Reset Valid Time Configuraion T=1/32ms*(N+1) Default 1ms

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3 Memory

3.1 RAW NAND Flash Controller (NDFC)

The NDFC is the NAND flash controller which supports all NAND flash memory available in the market. New types of flash can be supported by software re-configuration.

The NDFC has a built-in on-the-fly error correction code (ECC) feature with BCH algorithm to enhance the reliability. It can detect and correct up to 80 bits' error per 1024 bytes' data. With the on-chip BCH code ECC circuit, the CPU is freed for other tasks. You can disable the ECC feature by software.

The NDFC supports transferring data via the DMA or CPU memory-mapped IO. It provides automatic timing control for reading or writing external Flash and maintains the proper relativity for CLE, CE#, and ALE control signal lines. There are three modes for serial read access: the mode0 is for conventional serial access, the mode1 is for EDO type, and the mode2 is for extension EDO type. The NDFC can monitor the status of the R/B# signal line.

Block management and wear leveling management are implemented in software.

The NDFC has the following features:

- Supports all SLC/MLC flash and EF-NAND memory available in the market
- Supports configuring randomize seed by software
- Software configuration method for various systems and memory types
- Up to 8-bit data bus width
- Supports 2CE/2RB
- Supports 1024, 2048, 4096, 8192, 16384, and 32768 bytes' size per page
- Conventional and EDO serial access method for serial reading Flash
- 80 bits/1 KB on-the-fly BCH code ECC check and error correction
- Output bits' number information about the corrected errors
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers, and interrupt is supported
- One command FIFO
- Two 256x32-bit RAM for Pipeline Procession
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0, and Toggle DDR2.0 RAW NAND FLASH
- Maximum IO rate of 50 MHz in SDR mode, 100 MHz in DDR1.0 and 150MHz in DDR2.0 mode
- Self-debug for NDFC debug

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3.2 SDRAM controller (DRAMC)

The DRAMC has the following features:

- 32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X interface
- Memory capacity up to 4GB
- Clock frequency up to 1066 MHz for DDR3, DDR3L, and LPDDR3
- Clock frequency up to 1200 MHz for DDR4, LPDDR4, and LPDDR4x
- 17 address lines and three bank address lines per channel
- Generate initialization and refresh sequences automatically
- Runtime-configurable parameters setting for application flexibility
- Programmable priority of transferring through multiple ports
- Supports random reading or writing
- Supports Dynamic Frequency Setting(DFS) via hardware
- Supports SSC

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3.3 SD/MMC Host Controller (SMHC)

3.3.1 Overview

The SMHC controls the read/write operations on the secure digital (SD) cards, multimedia cards (MMC), and various extended devices that is based on the secure digital input/output (SDIO) protocol. The processor provides three SMHC interfaces for controlling the SD cards, MMCs, and SDIO devices.

The SMHC has the following features:

- Three SD/MMC host controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (SD3.0)
  - SMHC1, compliant with the protocol Secure Digital I/O (SDIO3.0)
  - SMHC2, compliant with the protocol Multimedia Card (eMMC5.1)
  - Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 5.1)
- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 supports the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Supports HS400 mode and HS200 mode
  - Maximum performance
    - SDR mode 200MHz@1.8V IO pad
    - DDR mode 200MHz@1.8V IO pad
    - SDR mode 50MHz@3.3V IO pad
    - DDR mode 50MHz@3.3V IO pad
- Support block size of 1 to 65535 bytes
- Support hardware CRC generation and error detection
- Supports eMMC boot operation and alternative boot operation
- Supports command queue for eMMC V5.1 device
- Supports serial CMDQ mode for SMHC0/2
- Supports host pull-up control

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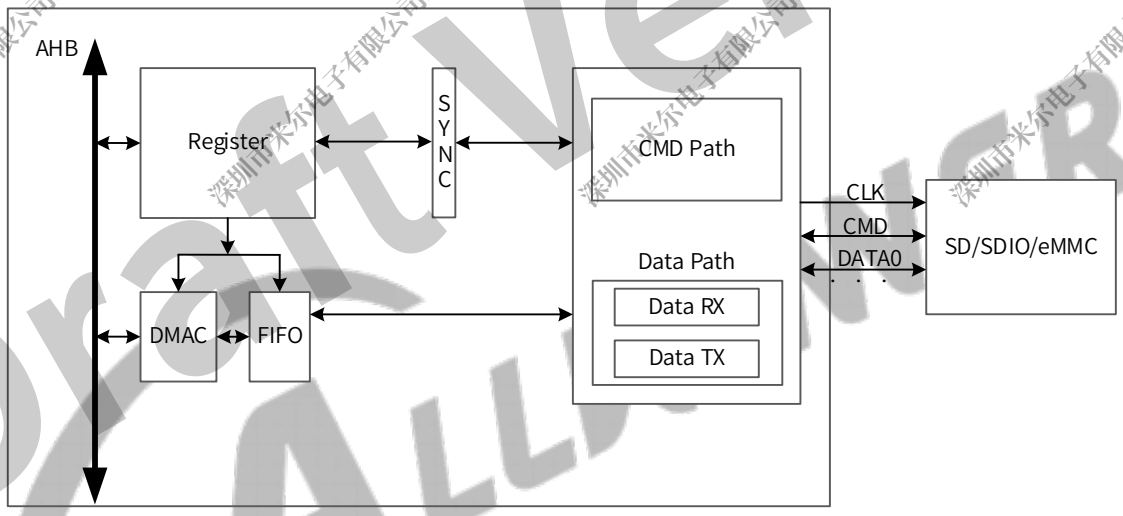
- Supports Command Completion signals and interrupts to host processor, and Command Completion signal disable feature
- Programmable baud rate
- Descriptor-based internal DMA controller
- Internal time-multiplexing 1 KB FIFO for SMHC0/2 transmitting and receiving
- Internal time-multiplexing 4 KB FIFO for SMHC1 transmitting and receiving

3.3.2 Block Diagram

The following figure shows a block diagram of the SMHC.

Figure 3-1 SMHC Block Diagram



SMHC contains the following sub-blocks:

Table 3-1 SMHC Sub-blocks

Sub-block	Description
Register	Used to configure the control signal for reading or writing the SD/SDIO/eMMC.
DMAC	The DMA controller that controls the data transfer between the memory and SMHC.
FIFO	A buffer for the data stream between the memory and the SMHC asynchronous clock domain.
SYNC	Synchronizes the signals from the AHB clock domain to the SMHC clock domain.
CMD Path	Sends commands to or receives commands from the SD/SDIO/eMMC.
Data Path	Consists of Data TX and Data RX sub-modules. The Data TX sends data blocks and the CRC codes to the SD/SDIO/eMMC. The Data RX receives data blocks and the CRC codes from the SD/SDIO/eMMC.

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3.3.3 Functional Description

3.3.3.1 External Signals

The following table describes the external signals of SMHC.

Table 3-2 SMHC External Signals

Signal Name	Description	Type
SMHC0		
SDC0-CMD	Command Signal for SD Card	I/O, OD
SDC0-CLK	Clock for SD Card	O
SDC0-D[3:0]	DATA INPUT AND OUTPUT FOR SD CARD	I/O
SMHC1		
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	I/O
SMHC2		
SDC2-CMD	Command Signal for eMMC	I/O, OD
SDC2-CLK	Clock for eMMC	O
SDC2-D[8:0]	Data Input and Output for eMMC	I/O
SDC2-RST	Reset for eMMC	O
SDC2-DS	Clock input for eMMC	I

3.3.3.2 Clock Sources

The SMHC0/1/2 has 5 different clock sources. You can select one of them as the SMHC clock source. The following table describes the clock sources of the SMHC.

For clock setting, configurations, and gating information, refer to section 2.7 Clock Controller Unit (CCU).

Table 3-3 SMHC0/1 Clock Sources

Clock Sources	Description	Module
HOSC	24 MHz Crystal	CCU
PLL_PERI0(400M)	Peripheral Clock, the default value is 400 MHz	
PLL_PERI0(300M)	Peripheral Clock, the default value is 300 MHz	
PLL_PERI1(400M)	Peripheral Clock, the default value is 400 MHz	
PLL_PERI1(300M)	Peripheral Clock, the default value is 300 MHz	

Table 3-4 SMHC2 Clock Sources

Clock Sources	Description	Module
HOSC	24 MHz Crystal	CCU
PLL_PERI0(800M)	Peripheral Clock, the default value is 800 MHz	
PLL_PERI0(600M)	Peripheral Clock, the default value is 600 MHz	

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Clock Sources	Description	Module
PLL_PERI1(800M)	Peripheral Clock, the default value is 800 MHz	
PLL_PERI1(600M)	Peripheral Clock, the default value is 600 MHz	

3.3.3.3 Timing Diagram

Refer to the following relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard (4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard (5.0)

3.3.3.4 Data Path

The SMHC and SD/SDIO/eMMC contains the following interface buses: CLK, CMD, and DATA 1/4. During one clock cycle, the SMHC can transmit one-bit command with one or two bits' data in 1-ch DATA mode, or four or eight bits' data in 4-ch DATA mode. The CMD is a bidirection channel for initializing the SD/SDIO/eMMC and transmitting commands. It can work in both the open-drain mode and push-pull mode. The DATA is also a bidirection channel. It works in the push-pull mode.

- Reading Data from the SD/SDIO/eMMC

The register configures the signals for the read operation, and synchronize the signals to the SMHC clock domain. Then the Data RX reads data from the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses and writes the data in the FIFO. After that, the DMAC transfers the data from the FIFO to the memory.

- Writing Data to the SD/SDIO/eMMC

The register configures the signals for the write operation, and synchronize the signals to the SMHC clock domain. Then the DMAC reads data from the memory and writes the data to the FIFO. After that, the Data TX reads the data from the FIFO and writes the data to the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses.

3.3.3.5 Package Format

Data transfer over the SD/eMMC bus is based on command and data bitstreams that are initiated by a start bit and terminated by a stop bit. There are three types of SD/eMMC packets: command token, response token, and data packet.

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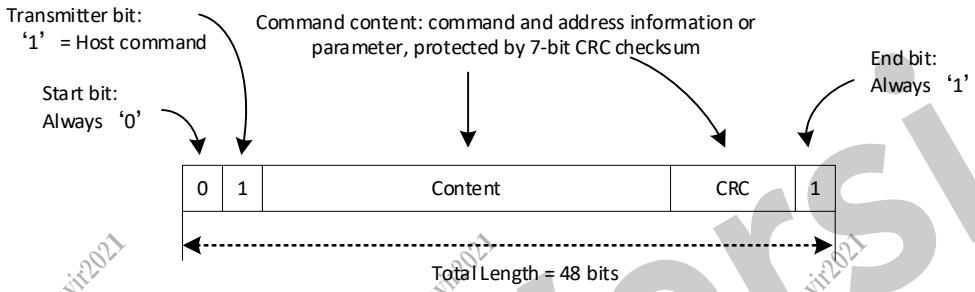
Command Tokens

The command token starts an operation. A command is sent from the host to a device. It is transferred serially on the CMD line. Command tokens have the following coding scheme:

Figure 3-2 Command Token Format



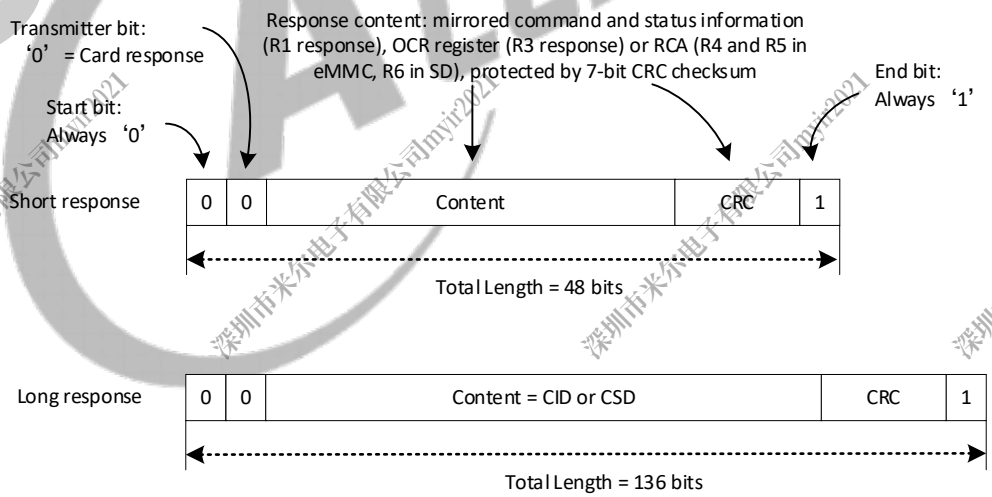
Each command token has 48 bits, preceded by a start bit ('0') and succeeded by an end bit ('1'). To detect transmission errors, each token is protected by CRC bits.

Response Tokens

After receiving a command, the card returns a 48-bit or 136-bit response based on the command type.

A response token is sent from the device to the host as an answer to a previously received command. It is transferred serially on the CMD line.

Figure 3-3 Response Token Format



Data Packet

Data can be transferred from the device to the host or vice versa. Data are transferred via the data lines.

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Figure 3-4 Data Packet Format for SDR

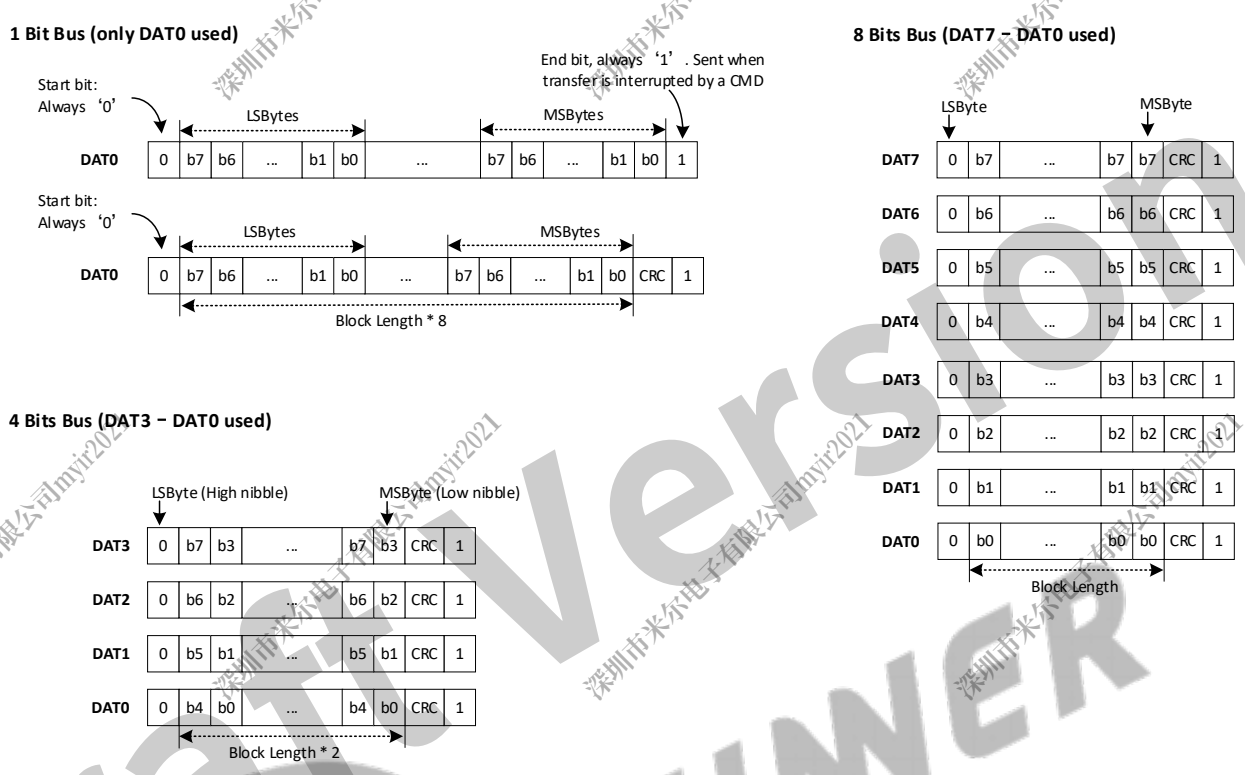

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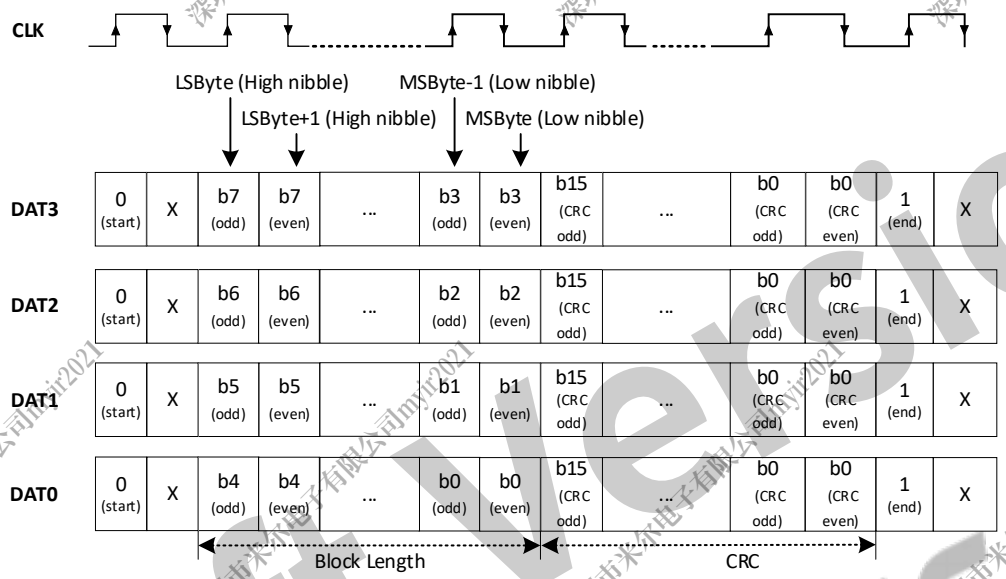
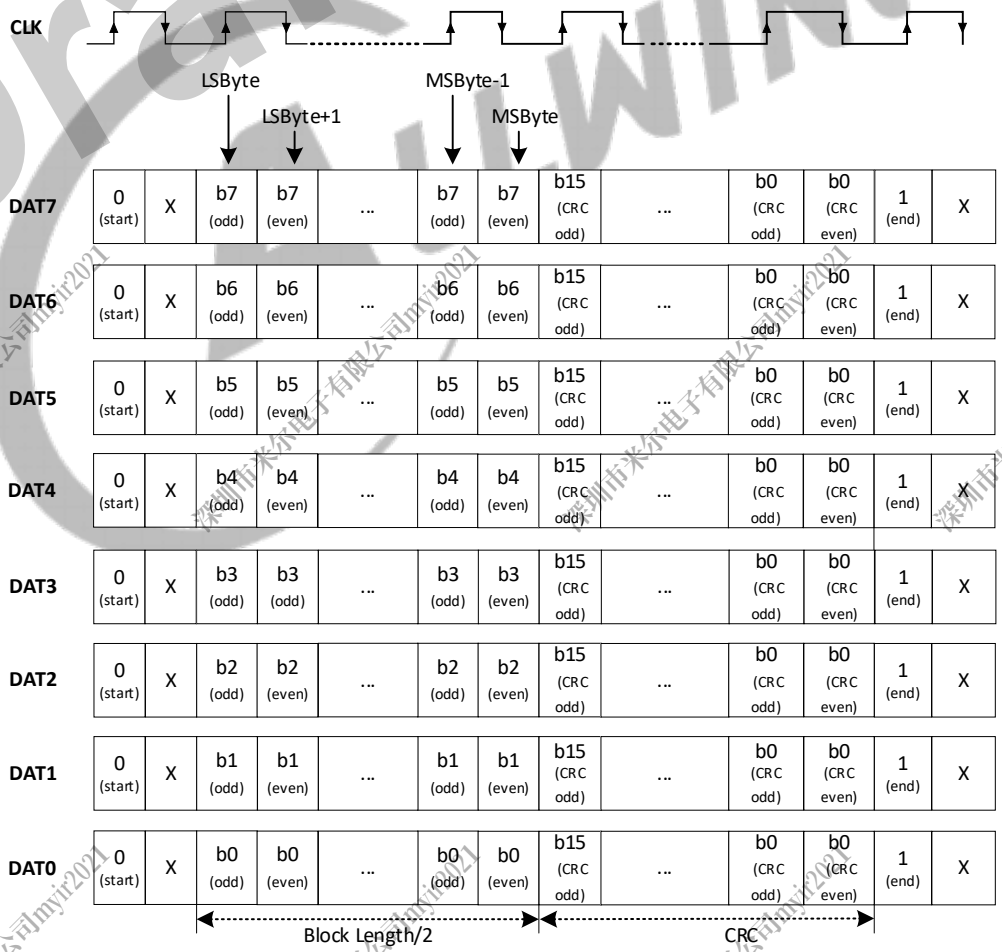
Figure 3-5 Data Packet Format for DDR

4 Bits Bus DDR (DAT3 – DAT0 used)



8 Bits Bus DDR (DAT7 – DAT0 used)



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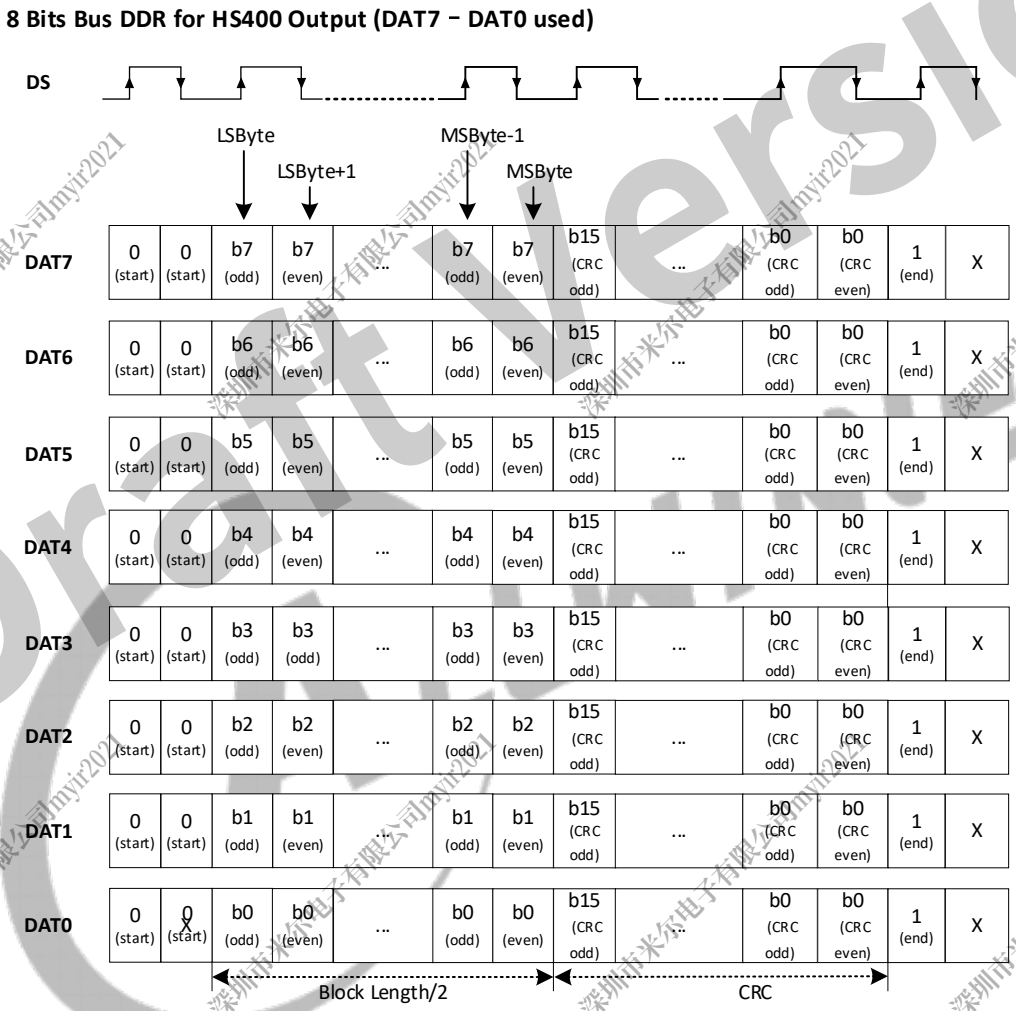
NOTE

- Bytes data are not interleaved but CRCs are interleaved.
- Start and end bits are only valid on the rising edge ("X" indicates "undefined").

Figure 3-6 Data Packet Format for DDR in HS400 Mode



NOTE

- Bytes data are not interleaved but CRCs are interleaved.
- Start bits are valid when Data Strobe is High and Low.
- End bits are only valid when Data Strobe is High ("X" indicates "undefined").

Data Transfer

Data transfers to or from the SD/eMMC card are done in blocks. Single and multiple block operations are widely used during data transfer.

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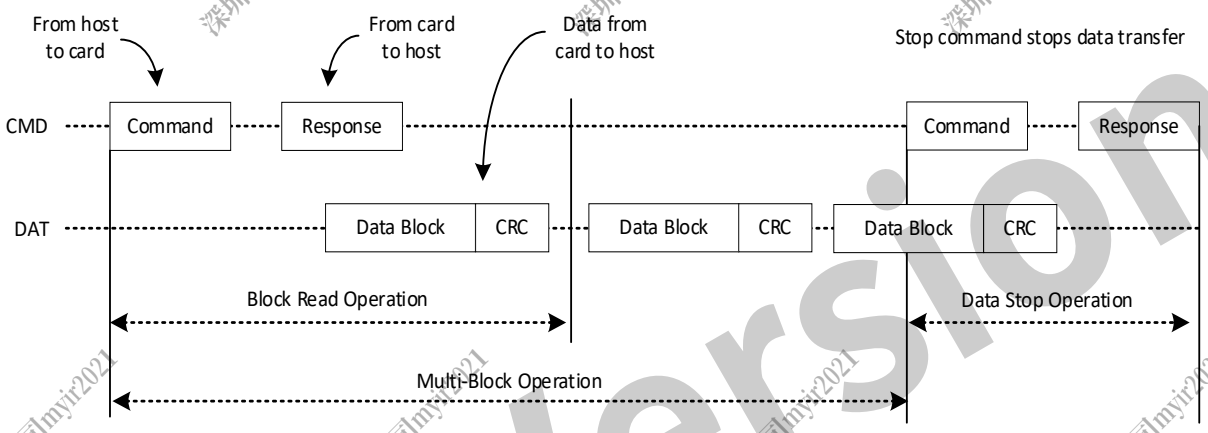
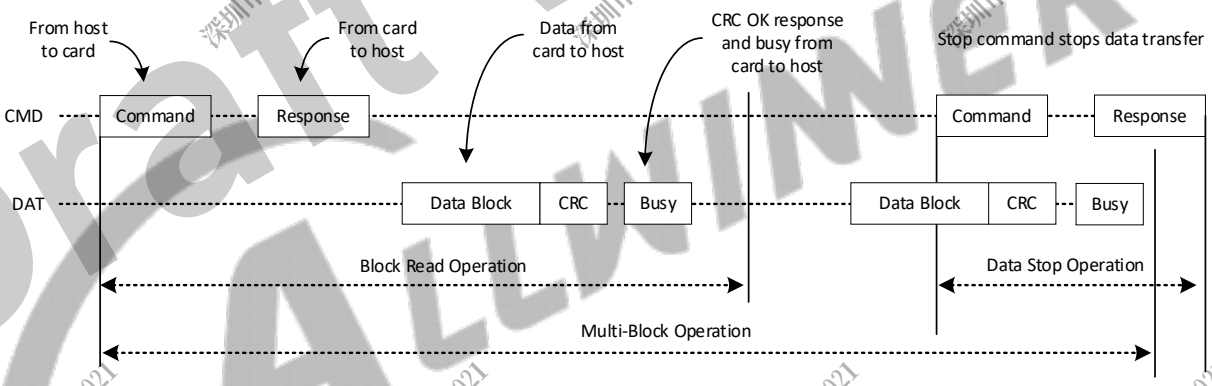
The following figure shows the single-block and multi-block read operation.

Figure 3-7 Single-Block and Multi-Block Read Operation



The following figure shows the single-block and multi-block write operation.

Figure 3-8 Single-Block and Multi-Block Read Operation



3.3.3.6 Phase Offset of the Command and Data

To obtain the command phase or data phase in output timing, follow the steps blow:

Step 1 Configure the MODE_SEL (bit [31]) andor HS400_NEW_SAM_EN (bit [0]) of SMHC_NTSR (offset: 0x005C) to choose the timing mode.

Step 2 Configure the DAT_DRV_PH_SEL (bit [17]) to select data drive phase offset and configureor CMD_DRV_PH_SEL (bit [16]) to select command drive phase offset inof SMHC_DRV_DL (offset: 0x0140) to select data or command drive phase offset.

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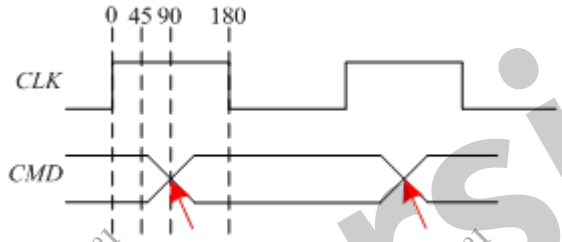
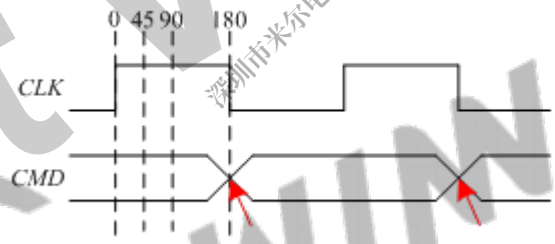
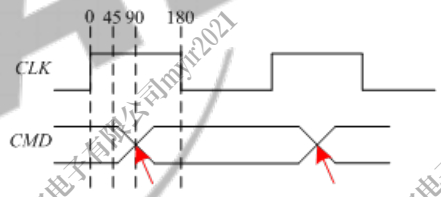
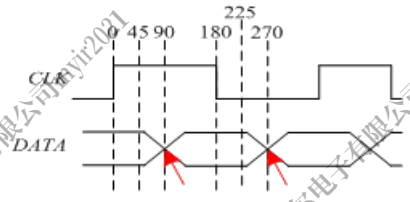
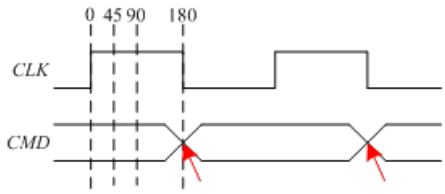
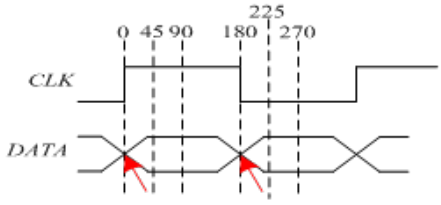
The following table shows the specific configuration of command and data location.

Table 3-5 Command and Data Location

Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
SDR	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data updates at 180 degrees.
DDR4 (1x mode: 0x5c[31]=0)	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 0 or 180 degrees.

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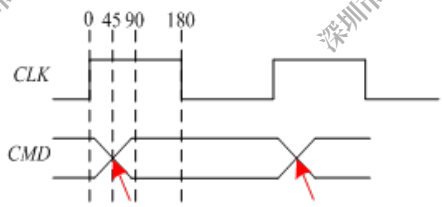
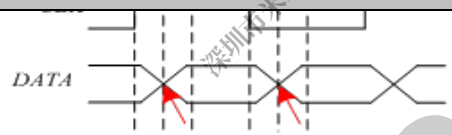
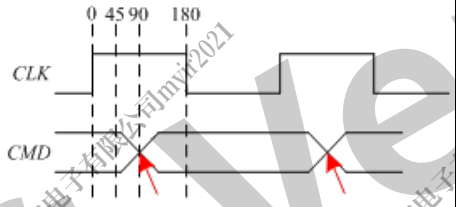
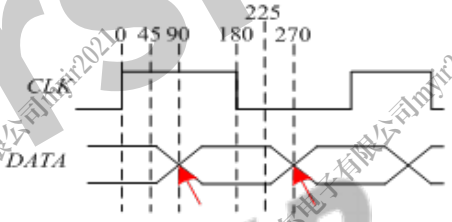
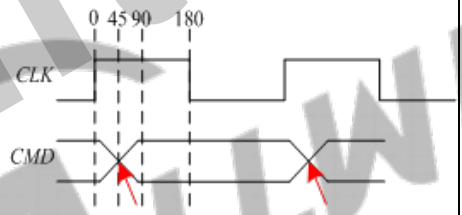
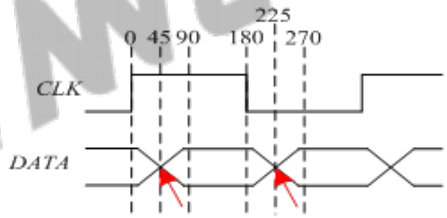
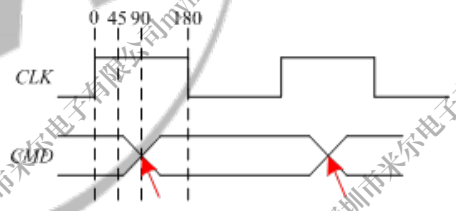
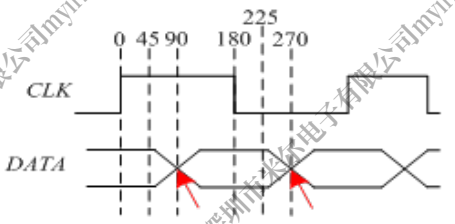
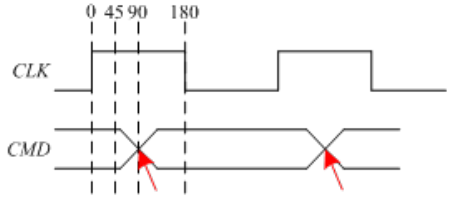
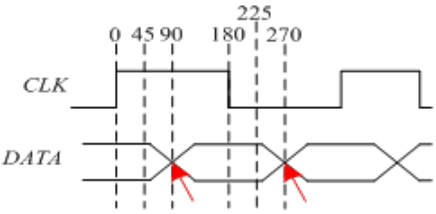
Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
DDR4 (2x mode: 0x5c[31]=1)	0		
		The Command updates at 45 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 45 degrees.	The data update at 90 degrees.
DDR8	0		
		The Command updates at 45 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 90 degrees.	The data update at 90 degrees.
HS400 (1x mode: 0x5c[0]=0)	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.

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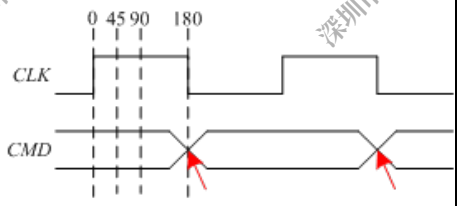
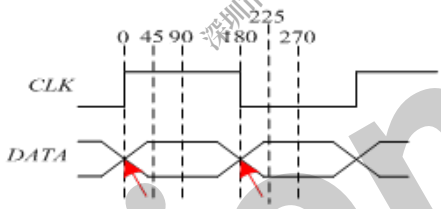
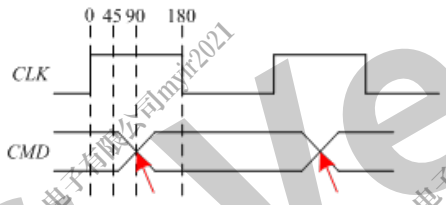
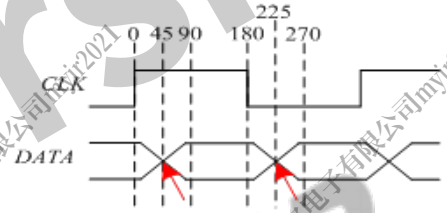
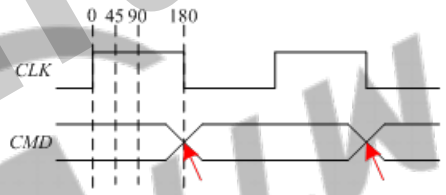
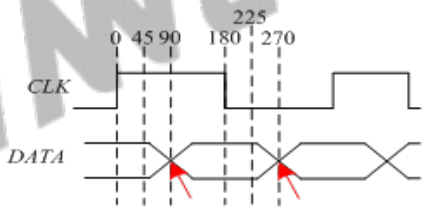
Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
	1		
		The Command updates at 180 degrees.	The data update at 0 or 180 degrees.
HS400 (2x mode: 0x5c[0] =1)	0		
		The Command updates at 90 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 90 degrees.

3.3.3.7 Internal DMA Controller Description

The SMHC has an internal DMA controller (IDMAC) to transfer data between the host memory and SMHC port. With a descriptor, the IDMAC can efficiently move data from the source to destination by automatically loading the next DMA transfer arguments, which needs less CPU intervention. Before transferring data in the IDMAC, the Host CPU should construct a descriptor list, configure arguments of every DMA transfer, and then launch the descriptor and start the DMA.

The IDMAC has an interrupt controller. When enabled, it generates an interrupt to the Host CPU in situations such as data transmission is completed or some error is happened.

IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

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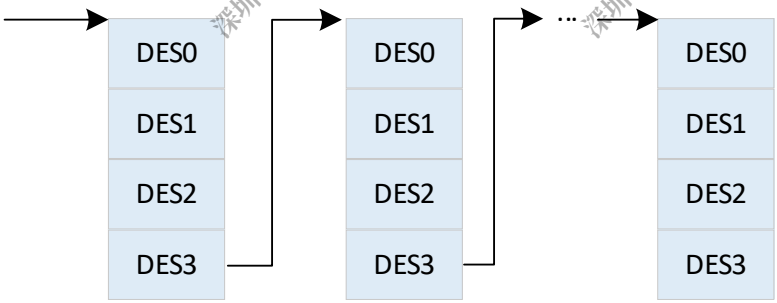
The following figure shows the internal formats of a descriptor.

Figure 3-9 IDMAC Descriptor Structure Diagram



This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 corresponds to the [31:0] bits, DES1 corresponds to the [63:32] bits, DES2 corresponds to the [95:64] bits, and DES3 corresponds the [127:96] bits in a descriptor.

The following table shows the bit definition of DES0.

Table 3-6 DES0 Definition

Bits	Name	Description
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when the transfer is over. **Note: After this bit is cleared to 0, the Host CPU is able to read the transferred data or initiate next transfer by launching a new descriptor.**
30	ERROR	ERR_FLAG When some errors happen in transfer, this bit will be set to 1.
29:5	/	/
4	Chain Flag	CHAIN_MOD When set to 1, this bit indicates that the second address in the descriptor is the next descriptor address. It must be set to 1.
3	First DES Flag	FIRST_FLAG When set to 1, this bit indicates that this descriptor contains the first buffer of data. It must be set to 1 in the first DES.
2	Last DES Flag	LAST_FLAG When set to 1, this bit indicates that the buffers this descriptor points to are the last data buffer.

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Bits	Name	Description
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set to 1, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer the descriptor points to.
0	/	/

The following table shows the bit definition of DES1.

Table 3-7 DES1 Definition

Bits	Name	Description
31:13	/	/
12:0	Buffer size	BUFF_SIZE The bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor.

The following table shows the bit definition of DES2.

Table 3-8 DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR The bits indicate the physical address of the data buffer. It is a word address.

The following table shows the bit definition of DES3.

Table 3-9 DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR The bits indicate the pointer to the physical memory where the next descriptor is present. It is a word address.

3.3.3.8 Calibrating the Delay Chain

There are two delay chains in SMHC: data strobe delay chain and sample delay chain.

- Data strobe delay chain: used to generate delay to make proper timing between Data Strobe and data signals.
- Sample delay chain: used to generate delay to make proper timing between the internal card clock signal and data signals.

Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

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Follow the steps below to calibrate the delay chain:

Step 1 Enable SMHC. In order to calibrate the delay chain by the operation registers in SMHC, the SMHC must be enabled through SMHC Bus Gating Reset Register and SMHCx Clock Register(x=0, 1, or 2).

Step 2 Configure a proper clock for SMHC. The delay chain calibration is based on the clock for SMHC from Clock Control Unit (CCU). The delay chain calibration is an internal function in SMHC and needs no devices. So it is unnecessary to open the clock signal for devices. The recommended clock frequency is 200 MHz.

Step 3 Set proper initial delay value. Writing 0xA0 to delay control register enables Delay Software Enable (bit [7]) and sets initial delay value 0x20 to Delay chain (bit [5:0]). Then write 0x0 to delay control register to clear the value.

Step 4 Write 0x8000 to delay control register to start calibrating the delay chain.

Step 5 Wait until the flag (bit14 in delay control register) of calibration done is set. The number of delay cells is shown at bit [13:8] in delay control register. The delay time generated by these delay cells is equal to the cycle of the SMHC clock nearly. This value is the result of calibration.

Step 6 Calculate the delay time of one delay cell according to the cycle of the SMHC clock and the result of calibration.

3.3.4 Programming Guidelines

3.3.4.1 Initializing SMHC

Before data and commands are exchanged between a card and the SMHC, the SMHC needs to be initialized. Follow the steps below to initialize the SMHC:

Step 1 Configure the corresponding GPIO register as an SMHC in section 8.6 GPIO; reset clock by writing 1 to SMHC_BGR_REG[SMHCx_RST](x=0, 1, or 2), and open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING] (x=0, 1, or 2); select clock sources and set the division factor by configuring the SMHCx_CLK_REG (x = 0, 1, or 2) register.

Step 2 Configure SMHC_CTRL to reset the FIFO and controller, and enable the global interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupts and error abnormal interrupts, and then register the interrupt function.

Step 3 Configure SMHC_CLKDIV to open clock for devices; configure SMHC_CMD as the change clock command (for example 0x80202000); send the update clock command to deliver clocks to devices.

Step 4 Configure SMHC_CMD as a normal command. Configure SMHC_CMDARG to set command parameters. Configure SMHC_CMD to set parameters like whether to send the response,

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the response type, and the response length and then send the commands. According to the initialization process in the protocol, you can finish SMHC initialization by sending the corresponding command one by one.

3.3.4.2 Writing a Single Data Block

To write a single data block, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write one block data to sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD24 (Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, and send CMD24 command to write data to the device.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD24 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

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3.3.4.3 Reading a Single Data Block

To read a single data block, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read one block data from sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD17 command (Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD, and send CMD17 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer and CMD17 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

3.3.4.4 Writing Open-Ended Multiple Data Blocks (CMD25 + Auto CMD12)

To write open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data to sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data

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size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, and send CMD25 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, the data transfer, CMD12 transfer, and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

3.3.4.5 Reading Open-Ended Multiple Data Blocks (CMD18 + Auto CMD12)

To read open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data from sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 command (Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD, and send CMD18 command to read data to the device. When the data transfer is completed, CMD12 will be sent automatically.

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Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, data transfer, CMD12 transfer, and CMD18 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

3.3.4.6 Writing Pre-Defined Multiple Data Blocks (CMD23 + CMD25)

To write pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, and send CMD25 command to write data to the device.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

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Step 8 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step5 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout

3.3.4.7 Reading Pre-Defined Multiple Data Blocks (CMD23 + CMD18)

To read pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 (Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, and send CMD18 command to read data from device to DRAM/SRAM.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD18 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

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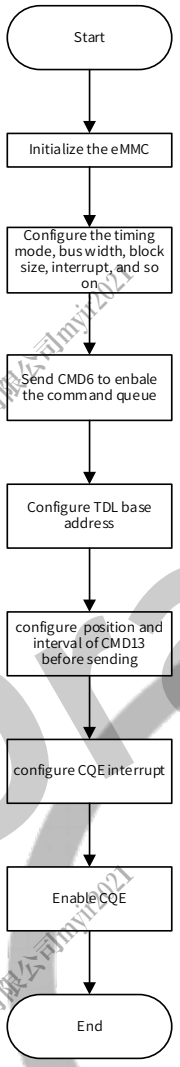
3.3.4.8 Initializing Command Queue for eMMC V5.1 Device

The following figure describes the initialization process of command queue.

Figure 3-10 Initialization Process of Command Queue



Follow the steps below to initialize the command queue:

Step 1 Initialize the eMMC. For detailed initialization steps, refer to section 3.3.4.1 Initializing SMHC.

Step 2 Send CMD6 to configure the timing mode and bus width. Send CMD16 to configure the block size as 512 B.

NOTE

The block size must be set to 512 B. After the command queue is enabled, the block size will not be able to be modified.

Step 3 Send CMD6 to enable the command queue of the eMMC device.

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Step 4 Configure CQTDLBA register to set the base address of the task descriptor list.

NOTE

When the base address of the task descriptor list crosses 4 GB, you need to write the bit [32] of the higher 32-bit address to the bit [0] of the CQTDLBA register and write the lower 32-bit address to the CQTDLBA register.

For example, assume that the base address is 0x106000000. In this case, you need to write the bit [32] of the higher 32-bit address to the bit [0] of the CQTDLBA register and write 0x06000001 to the CQTDLBA register.

Step 5 Configure CQSSC1 register to set how to query the status of the device's task queue.

Step 6 Configure CQIC register to enable/disable interrupt, set interrupt count and timer protection.

Step 7 Configure CQRMEM register to set which errors may trigger a RED interrupt.

Step 8 Configure CQCFG register to enable CQE activity.

eMMC CMDQ supports multiple operation modes, which could be selected by configuring the CMDQ_MODE bit (bit [5:4]) of CQCFG register.

3.3.5 Register List

Module Name	Base Address	Description
SMHC0	0x04020000	
SMHC1	0x04021000	SMHC1 register is the same with SMHC0
SMHC2	0x04022000	SMHC2 register is the same with SMHC0

Register Name	Offset	Description
SMHC_CTRL	0x0000	SMHC Global Control Register
SMHC_CLKDIV	0x0004	SMHC Clock Control Register
SMHC_TMOUT	0x0008	SMHC Timeout Register
SMHC_CTYPE	0x000C	SMHC Bus Width Register
SMHC_BLKSIZ	0x0010	SMHC Block Size Register
SMHC_BYTCNT	0x0014	SMHC Byte Count Register
SMHC_CMD	0x0018	SMHC Command Register
SMHC_CMDARG	0x001C	SMHC Command Argument Register
SMHC_RESP0	0x0020	SMHC Response 0 Register
SMHC_RESP1	0x0024	SMHC Response 1 Register
SMHC_RESP2	0x0028	SMHC Response 2 Register
SMHC_RESP3	0x002C	SMHC Response 3 Register
SMHC_INTMASK	0x0030	SMHC Interrupt Mask Register

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Register Name	Offset	Description
SMHC_MINTSTS	0x0034	SMHC Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	SMHC Raw Interrupt Status Register
SMHC_STATUS	0x003C	SMHC Status Register
SMHC_FIFOTH	0x0040	SMHC FIFO Water Level Register
SMHC_FUNS	0x0044	SMHC FIFO Function Select Register
SMHC_TBC0	0x0048	SMHC Transferred Byte Count Register 0
SMHC_TBC1	0x004C	SMHC Transferred Byte Count Register 1
SMHC_CSDC	0x0054	SMHC CRC Status Detect Control Register
SMHC_A12A	0x0058	SMHC Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SMHC New Timing Set Register
SMHC_HWRST	0x0078	SMHC Hardware Reset Register
SMHC_IDMAC	0x0080	SMHC IDMAC Control Register
SMHC_DLBA	0x0084	SMHC Descriptor List Base Address Register
SMHC_IDST	0x0088	SMHC IDMAC Status Register
SMHC_IDIE	0x008C	SMHC IDMAC Interrupt Enable Register
SMHC_THLD	0x0100	SMHC Card Threshold Control Register
SMHC_SFC	0x0104	SMHC Sample FIFO Control Register
SMHC_A23A	0x0108	SMHC Auto Command 23 Argument Register
EMMC_DDR_SBIT_DET	0x010C	SMHC eMMC4.5 DDR Start Bit Detection Control Register
SMHC_EXT_CMD	0x0138	SMHC Extended Command Register
SMHC_EXT_RESP	0x013C	SMHC Extended Response Register
SMHC_DRV_DL	0x0140	SMHC Drive Delay Control Register
SMHC_SAMP_DL	0x0144	SMHC Sample Delay Control Register
SMHC_DS_DL	0x0148	SMHC Data Strobe Delay Control Register
SMHC_HS400_DL	0x014C	SMHC HS400 New Timing Delay Control Register
SMHC_CIU_CNT	0x0154	SMHC Card interface counter
SMHC_FIFO	0x0200	SMHC FIFO Register
CQCFG	0x0408	Command Queuing Configuration
CQCTL	0x040C	Command Queuing Control
CQIS	0x0410	Command Queuing Interrupt Status
CQISTE	0x0414	Command Queuing Interrupt Status Enable
CQISGE	0x0418	Command Queuing Interrupt Signal Enable
CQIC	0x041C	Command Queuing Interrupt Coalescing
CQTDLBA	0x0420	Command Queuing Task Descriptor List Base Address
CQTDBR	0x0428	Command Queuing Task Doorbell
CQTCN	0x042C	Command Queuing Task Completion Notification
CQDQS	0x0430	Command Queuing Device Queue Status
CQDPT	0x0434	Command Queuing Device Pending Tasks
CQTCLR	0x0438	Command Queuing Task Clear
CQSSC1	0x0440	Command Queuing Send Status Configuration 1

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Register Name	Offset	Description
CQSSC2	0x0444	Command Queuing Send Status Configuration 2
CQCRDCT	0x0448	Command Queuing Command Response for Direct-Command Task
CQRMEM	0x0450	Command Queuing Response Mode Error Mask
CQTERRI	0x0454	Command Queuing Task Error Information
CQCRI	0x0458	Command Queuing Command Response Index
CQCRA	0x045C	Command Queuing Command Response Argument

3.3.6 Register Description

3.3.6.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:18	/	/	/
17:16	R/W	0x0	SRAM_BIST_SEL SRAM BIST Select 2'b00: for SMHC 4K SRAM(1024x32) BIST 2'b01: for CQE SRAM(32x56) BIST 2'b10: for EMCE SRAM BIST 2'b11: Reserved
15:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period

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Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although the HS400 speed mode of eMMC is 8-bit DDR, this field should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data [3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

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3.3.6.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MASK_DAT0 Mask Data0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1 : Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0-255) when HS400_MD_EN is set, this field must be cleared.

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3.3.6.3 0x0008 SMHC Timeout Register (Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device, this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect. Note: Under the following 3 conditions, the timeout limit is half of the set time. 1> DDR8 mode 2> DDR4 and SMHC_NTSR[MODE_SELEC] (0x5C [31]) high 3> HS400 and SMHC_NTSR[HS400_NEW_SAMPLE_EN](0x5C[0]) high
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

3.3.6.4 0x000C SMHC Bus Width Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

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3.3.6.5 0x0010 SMHC Block Size Register (Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

3.3.6.6 0x0014 SMHC Byte Count Register (Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

3.3.6.7 0x0018 SMHC Command Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit will be set in SMHC_RINTSTS register. You should not write any other command before this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.

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Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:18	/	/	/
17	R/W	0x0	R1B_BUSY_HW_DETECT R1b busy hardware detect enable 0: Disable hardware detect r1b busy 1: Enable hardware detect r1b busy
16	R/W	0x0	R1B_RESP R1b response 0: The response type isn't r1b for current command 1: The response type is r1b for current command Note: if STOP_CMD_FLAG set, R1B_RESP will be set by controller when send CMD12, and will be clear by controller when send next command.
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: normal command sending 1: Send initialization sequence before sending this command.

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Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: normal command sending 1: send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bits) 1:Long Response (136 bits)

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Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

3.3.6.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CMD_ARG Command argument

3.3.6.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

3.3.6.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:32] of response

3.3.6.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

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3.3.6.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

3.3.6.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:18	/	/	/
17	R/W	0x0	R1B_BUSY_CLR_INT_EN
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable

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Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

3.3.6.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	M_CARD_REMOVAL_INT Card Removed
30	R	0x0	M_CARD_INSERT Card Inserted
29:18	/	/	/
17	R	0x0	R1B_BUSY_CLR_INT
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.

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Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative.
6	R	0x0	M_RCE_INT Response CRC Error
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

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3.3.6.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:18	/	/	/
17	R/W1C	0x0	R1B_BUSY_CLR R1b busy clear When set, it means that the r1b busy has finished or not set.
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. It is valid at 4-bit or 8-bit bus mode, when it set, host found start bit at data0, but not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared after the last block. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.

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Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0(1-bit bus) or data0-data3(4-bit bus) or data0-data7(8-bit bus). This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bits.

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Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

3.3.6.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:28	/	/	/
27:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA [0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data [3] status level of DATA [3]; checks whether card is present 0: card not present 1: card present

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Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	FSM_STA Command FSM states: 0000: Idle 0001: Send INIT sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn't reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn't reach receive trigger level 1: FIFO reached receive trigger level

3.3.6.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
31	/	/	/

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Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD(4Byte). A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: BSIZE_OF_TRANS = 3, MSize = 16, TX_TL = 240, RX_TL = 15 FIFO_DEPTH = 256 FIFO_SIZE = 256 * 32 = 1K
27	/	/	/
26:16	R/W	0xF	RX_TL RX Trigger Level When BLOCK2K_EXIST is 1'b1: 0x0-0x3FE: RX Trigger Level is 0-1022(Unit is equal to the FIFO_WIDTH) 0x3FF reserved When BLOCK2K_EXIST is 1'b0: 0x0-0xFE: RX Trigger Level is 0-254 (Unit is equal to the FIFO_WIDTH) 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. When CARD_WR_THLD_ENB is set, RX_TL*4 should be less than CARD_WR_THLD. 15 (means greater than 15)
15:11	/	/	/

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Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0	TX_TL TX Trigger Level **When BLOCK2K_EXIST is 1'b1**: 0x1-0x3FF: TX Trigger Level is 1-1023 (Unit is equal to the FIFO_WIDTH) 0x0: no trigger **When BLOCK2K_EXIST is 1'b0**: 0x1-0xFF: TX Trigger Level is 1-255 (Unit is equal to the FIFO_WIDTH) 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)

3.3.6.18 0x0044 SMHC FIFO Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait

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Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

3.3.6.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

3.3.6.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

3.3.6.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x3	CRC_DET_PARA CRC Detect Para 110: HS400 speed mode 011: Other speed mode Others: Reserved

3.3.6.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFF	A12A Auto CMD12 Argument The argument of command 12 automatically send by controller with this field.

3.3.6.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MODE_SEL Mode Select 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:26	/	/	/
25	R/W	0x0	BOOT_DAT_RX_PHASE_CLR After boot ACK, before receive boot data, clear data lines' input phase. 0: Disable 1: Enable
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear the input phase of command lines and data lines during the update clock operation. 0: Disable 1: Enable
23	/	/	/

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Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines' input phase. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines' input phase. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines' input phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command RX phase before sending the command. 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAM_TIM_PHS Data Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0（only for SD2 hs400 mode） Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAM_TIM_PHS Command Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
3:1	/	/	/

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Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HS400_NEW_SAM_EN HS400 New Sample Enable 1：enable hs400 new sample method 0：disable hs400 new sample method

3.3.6.24 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	HW_RST Hardware Reset 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

3.3.6.25 0x0080 SMHC IDMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	Read/Write	Default/Hex	Description
31	W	0x0	DES_LOAD_CTRL When IDMAC fetches a descriptor, if the valid bit of a descriptor is not set, IDMAC FSM will go to the suspend state. Setting this bit will make IDMAC re-fetch descriptor again and do the transfer normally.
30:8	/	/	/
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	/	/	/
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.

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Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

3.3.6.26 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor, is a word(4byte) address

3.3.6.27 0x0088 SMHC IDMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:10	R	0x0	IDMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (SMHC_ IDST [2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved This bit is read-only.
9	R/W1C	0x0	AIS Abnormal Interrupt Summary. Logical OR of the following: SMHC_IDST [2]: Fatal Bus Interrupt SMHC_IDST [4]: Descriptor unavailable bit Interrupt SMHC_IDST [5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.

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Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	NIS Normal Interrupt Summary. Logical OR of the following: SMHC_IDST [0]: Transmit Interrupt SMHC_IDST [1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (SMHC_IDST [12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.

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Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.

3.3.6.28 0x008C SMHC IDMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set, Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set, Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

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3.3.6.29 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	CARD_WR_THLD Card Read/write Threshold Size (Unit: byte)
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disable 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO. **Note: Not support DDR 8-wire mode.**
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

3.3.6.30 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

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Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be change between 0x0 and 0xF, but actually the available value and the position of stopping clock must be decided by the actual situation. The value increase one in this field is linked to one cycle(two cycle in DDR mode) that the position of stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

3.3.6.31 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

3.3.6.32 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/

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Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside host controller based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

3.3.6.33 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When set this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST set, this field will be cleared.

3.3.6.34 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

3.3.6.35 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

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Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C [31] is low, 45^0 at DDR4 mode when 0x5C [31] is high, 90^0 at HS400 mode when 0x5C [0] is low, 45^0 at HS400 mode when 0x5C [0] is high. 1: Data drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C [31] is low, 90^0 at DDR4 mode when 0x5C [31] is high, 180^0 at HS400 mode when 0x5C [0] is low, 90^0 at HS400 mode when 0x5C[0] is high.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C [31] is low, 45^0 at DDR4 mode when 0x5C [31] is high, 90^0 at HS400 mode 1: Command drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C [31] is low, 90^0 at DDR4 mode when 0x5C [31] is high, 180^0 at HS400 mode.
15:0	/	/	/

3.3.6.36 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.

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Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

3.3.6.37 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/ Hex	Description
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.

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Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/ Hex	Description
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

3.3.6.38 0x014C SMHC HS400 New Timing Delay Control Register (Default Value: 0x0000_0800)

Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	HS400_DL_CAL_START HS400 Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	HS400_DL_CAL_DONE HS400 Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in HS400_DL.
13:12	/	/	/

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Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	Read/Write	Default/Hex	Description
11:8	R	0x8	HS400_DL HS400 Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when HS400_DL_CAL_DONE is set.
7	R/W	0x0	HS400_DL_SW_EN Sample Delay Software Enable
6:4	/	/	/
3:0	R/W	0x0	HS400_DL_SW HS400 Delay Software

3.3.6.39 0x0154 SMHC Card interface counter Register (Default Value:0x0)

Offset: 0x0154			Register Name: SMHC_CIU_CNT
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	DATA_PATH_CNT Data Path Counter This field indicates the count value of counters for each stage when host read or write data. When Host read data, this field is one of the following values: 1. The time of wait data start bit 2. The byte count of receive data 3. The count of receive crc16 When Host write data, this field is one of the following values: 1. The byte count of transmit data 2. The count of transmit crc16 3. The time of wait receive CRC status
7:0	/	/	/

3.3.6.40 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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3.3.6.41 0x0408 CQCFG Command Queuing Configuration Register (Default Value: 0x0200_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/He	Description
31:16	R/W	0x200	CQE_BLOCK_SIZE CQE Block Size Configuration It must be 0x200 when CMDQ_MODE is CMDQ or CMDQ_HALF or CMDQ_ALMOST.
15:13	/	/	/
12	R/W	0x0	CQE_DCMD_EN Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1 = Task descriptor in slot #31 is a DCMD Task Descriptor 0 = Task descriptor in slot #31 is a Data Transfer Task Descriptor
11:9	/	/	/
8	R/W	0x0	CQE_TASK_DESC_SIZE Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queuing Enable bit is '0' (command queuing is disabled) Bit Value Description 1 = Task descriptor size is 128 bits 0 = Task descriptor size is 64 bits
7:6	/	/	/

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Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/He	Description
5:4	R/W	0x0	CMDQ_MODE Command Queue Mode select This field is used to select CMDQ mode, there are four kinds of CMDQ mode: ● CMDQ_HALF mode CMD and data can't be transmitted at the same time, but the current task can be sent to the device before the previous task is completed. ● CMDQ_ALMOST mode CMD can be sent at the start of block, and the current task can be sent to the device before the previous task is completed. The Field Value Description 2'b00: Reserved 2'b01: CMDQ_HALF mode 2'b10: CMDQ_ALMOST mode (Not support DDR 8-wire mode) 2'b11: Reserved **Note: The CARD_WR_THLD_ENB must be set and the value of CARD_WR_THLD must be greater than or equal CQE_BLOCK_SIZE when CQE_MODE is CMDQ_ALMOST.**
3:1	/	/	/
0	R/W	0x0	CQE_EN Command Queuing Enable Software shall write '1' this bit when in order to enable command queuing mode (i.e., enable CQE). When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes '1' to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queuing mode, it shall clear all previous tasks if such exist before setting this bit to 0.

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3.3.6.42 0x040C CQCTL Command Queuing Control Register (Default Value: 0x0000_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/He	Description
31:9	/	/	/
8	R/WAC	0x0	CQE_TCL_ALL CQE Task Cleared All Software shall write '1' this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (i.e., Halt bit is 1). When software writes 1, the value of the register is updated to '1', and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is software's responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing '0' to this register shall have no effect.
7:1	/	/	/
0	R/W	0x0	CQE_HALT Host software shall write '1' to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT) When software writes '1', CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state (i.e., resume CQE activity), software shall clear this bit (write '0'). Writing '0' when the value is already '0' shall have no effect.

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3.3.6.43 0x0410 CQIS Command Queuing Interrupt Status Register (Default Value: 0x0000_0000)

This register indicates pending interrupts that require service. Each bit in this registers is asserted in response a specific event, only if the respective bit is set in CQISTE register.

Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/He	Description
31:4	/	/	/
3	R/W1C	0x0	CQIS_TCL Task Cleared This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL).
2	R/W1C	0x0	CQIS_RED Response Error Detected Interrupt This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked.
1	R/W1C	0x0	CQIS_TCC Task Complete Interrupt This status bit is asserted (if CQISTE.TCC=1) when at least one of the following two conditions are met: A task is completed and the INT bit is set in its Task Descriptor Interrupt caused by Interrupt Coalescing logic (see 0)
0	R/W1C	0x0	CQIS_HAC Halt Complete Interrupt This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state.

3.3.6.44 0x0414 CQISTE Command Queuing Interrupt Status Enable Register (Default Value: 0x0000_0000)

This register enables and disables the reporting of the corresponding interrupt to host software in CQIS register. When a bit is set ('1') and the corresponding interrupt condition is active, then the

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bit is CQIS is asserted. Interrupt sources that are disabled ('0') are not indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/He	Description
31:4	/	/	/
3	R/W	0x0	CQISTE_TCL Task Cleared Status Enable 1: CQIS.TCL will be set when its interrupt condition is active 0: CQIS.TCL is disabled
2	R/W	0x0	CQISTE_RED Response Error Detected Status Enable 1: CQIS.RED will be set when its interrupt condition is active 0: CQIS.RED is disabled
1	R/W	0x0	CQISTE_TCC Task Complete Status Enable 1: CQIS.TCC will be set when its interrupt condition is active 0: CQIS.TCC is disabled
0	R/W	0x0	CQISTE_HAC Halt Complete Status Enable 1: CQIS.HAC will be set when its interrupt condition is active 0: CQIS.HAC is disabled

3.3.6.45 0x0418 CQISGE Command Queuing Interrupt Signal Enable Register (Default Value: 0x0000_0000)

This register enables and disables the generation of interrupts to host software. When a bit is set ('1') and the corresponding bit in CQIS is set, then an interrupt is generated. Interrupt sources that are disabled ('0') are still indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/He	Description
31:4	/	/	/
3	R/W	0x0	CQISGE_TCL Task Cleared Signal Enable When set and CQIS.TCL is asserted, the CQE shall generate an interrupt

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Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/He	Description
2	R/W	0x0	CQISGE_RED Response Error Detected Signal Enable When set and CQIS.RED is asserted, the CQE shall generate an interrupt
1	R/W	0x0	CQISGE_TCC Task Complete Signal Enable When set and CQIS.TCC is asserted, the CQE shall generate an interrupt
0	R/W	0x0	CQISGE_HAC Halt Complete Signal Enable When set and CQIS.HAC is asserted, the CQE shall generate an interrupt

3.3.6.46 0x041C CQIC Interrupt Coalescing Register (Default Value: 0x0000_0000)

This register controls the interrupt coalescing feature.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/He	Description
31	R/W	0x0	CQIC_EN Interrupt Coalescing Enable/Disable When set to '0' by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to '1', the interrupt coalescing mechanism is enabled and coalesced interrupts are generated
30:21	/	/	/
20	R	0x0	CQIC_SB Interrupt Coalescing Status Bit This bit indicates to software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (i.e., ICSB is set if and only if IC counter > 0). Bit Value Description 1: At least one task completion has been counted (IC counter >0) 0: No task completions have occurred since last counter reset (IC counter =0)
19:17	/	/	/

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Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/He	Description
16	W	0x0	CQIC_CTR Counter and Timer Reset When host driver writes '1', the interrupt coalescing timer and counter are reset
15	W	0x0	CQIC_CTH_WEN Interrupt Coalescing Counter Threshold Write Enable When software writes '1', the value ICCTH is updated with the contents written at the same cycle. When software writes '0', the value in ICCTH is not updated. Note: Write operations to ICCTH are only allowed when the task queue is empty.
14:13	/	/	/
12:8	R/W	0x0	CQIC_CTH Interrupt Coalescing Counter Threshold Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 Note: ● When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated. ● In order to write to this field, the ICCTHWEN bit must be set at the same write operation.
7	W	0x0	CQIC_TOVAL_WEN Interrupt Coalescing Timeout Value Write Enable When software writes '1', the value ICTOVAL is updated with the contents written at the same cycle. When software writes '0', the value in ICTOVAL is not updated. Note: Write operations to ICTOVAL are only allowed when the task queue is empty.

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Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/He	Description
6:0	R/W	0x0	CQIC_TOVAL Interrupt Coalescing Timeout Value Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 01h (1024 clock periods) and the maximum value is 7Fh (127*1024 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us Note: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation.

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3.3.6.47 0x0420 CQTDLBA Command Queuing Task Descriptor List Base Address Register (Default Value: 0x0000_0000)

This register is used for configuring the lower 32 bits of the byte address of the head of the Task Descriptor List in the host memory.

Offset: 0x0420			Register Name: CQTDLBA
Bit	Read/Write	Default/He	Description
31:0	R/W	0x0	CQE_TDLBA Task Descriptor List Base Address This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KByte boundary.

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3.3.6.48 0x0428 CQTDBR Command Queuing Task Doorbell Register (Default Value: 0x0000_0000)

Using this register, software triggers CQE to process a new task.

Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/He	Description
31:0	R/W1S	0x0	CQE_TDBR Command Queuing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to '0' by CQE in one of the following events: When a task execution is completed (with success or error) The task is cleared using CQTCLR register All tasks are cleared using CQCTL register CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0 by software shall have no impact on the hardware, and will not change the value of the register bit.

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3.3.6.49 0x042C CQTCN Task Completion Notification Register (Default Value: 0x0000_0000)

This register is used by CQE to notify software about completed tasks.

Offset: 0x042C			Register Name: CQTCN
Bit	Read/Write	Default/He	Description
31:0	R/W1C	0x0	CQE_TCN Task Complete Notification CQE shall set bit *n* of this register (at the same time it clears bit *n* of CQTDBR) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

3.3.6.50 0x0430 CQDQS Device Queue Status Register (Default Value: 0x0000_0000)

This register stores the most recent value of the device's queue status.

Offset: 0x0430			Register Name: CQDQS
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DQS Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command, i.e., the device's queue status.

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3.3.6.51 0x0434 CQDPT Device Pending Tasks Register (Default Value: 0x0000_0000)

This register indicates to software which tasks are queued in the device, awaiting execution.

Offset: 0x0434			Register Name: CQDPT
Bit	Read/Writ	Default/He	Description
31:0	R	0x0	CQE_DPT Device Pending Tasks Bit *n* of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasn't been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register.

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3.3.6.52 0x0438 CQTCLR Task Clear Register (Default Value: 0x0000_0000)

This register is used for removing an outstanding task in the CQE. The register should be used only when CQE is in Halt state.

Offset: 0x0438			Register Name: CQTCLR
Bit	Read/Writ	Default/He	Description
31:0	R/W	0x0	CQE_TASK_CLR Command Queuing Task Clear Writing 1 to bit *n* of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCTL register Halt bit. When software writes '1' to a bit in this register, CQE updates the value to '1', and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once clear operation is complete. Software should poll on the CQTCLR until it is cleared to verify clear operation was complete. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register. Writing 0 to a register bit shall have no impact.

3.3.6.53 0x0440 CQSSC1 Send Status Configuration 1 Register (Default Value: 0x0001_1000)

The register controls the when SEND_QUEUE_STATUS commands are sent.

Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Writ	Default/He	Description
31:20	/	/	/

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Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Writ	Default/He	Description
19:16	R/W	0x1	CQE_SSC_CBC Send Status Command Block Counter This field indicates to CQE when to send SEND_QUEUE_STATUS (CMD13) command to inquire the status of the device's task queue. A value of *n* means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-*n*, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. A value of 0 means that SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. A value of 1 means that STATUS command is to be sent during the last block of the transaction.
15:0	R/W	0x1000	CQE_SSC_CIT Send Status Command Idle Timer This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 us

3.3.6.54 0x0444 CQSSC2 Send Status Configuration 2 Register (Default Value: 0x0000_0000)

This register is used for configuring RCA field in SEND_QUEUE_STATUS command argument.

Offset: 0x0444			Register Name: CQSSC2
Bit	Read/Writ	Default/He	Description
31:16	/	/	/

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Offset: 0x0444			Register Name: CQSSC2
Bit	Read/Writ	Default/He	Description
15:0	R/W	0x0	CQE_SSC_RCA Send Queue Status RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS (CMD13) command argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

3.3.6.55 0x0448 CQCRDCT Command Response for Direct-Command Task Register (Default Value: 0x0000_0000)

This register is used for passing the response of a DCMD task to software.

Offset: 0x0448			Register Name: CQCRDCT
Bit	Read/Writ	Default/He	Description
31:0	R	0x0	CQE_DCMD_LAST_RESP Direct Command Last Response This register contains the response of the command generated by the last direct- command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQTDBR register is cleared by CQE.

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3.3.6.56 0x0450 CQRMEM Response Mode Error Mask Register (Default Value: 0xFDF9_A080)

This register controls the generation of Response Error Detection (RED) interrupt.

Offset: 0x0450			Register Name: CQRMEM
Bit	Read/Writ	Default/He	Description
31:0	R/W	0xFDF9A080	CQE_RMEM Response Mode Error Mask This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses. Bit Value Description (for any bit 'i'): 1: When a R1/R1b response is received, with bit 'I' in the device status set, a RED interrupt is generated 0: When a R1/R1b response is received, bit *i* in the device status is ignored The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. Note: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

3.3.6.57 0x0454 CQTERRI Task Error Information Register (Default Value: 0x0000_0000)

This register is updated by CQE when an error occurs on data or command related to a task activity.

When such error is detected by CQE or indicated by the eMMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure.

Offset: 0x0454			Register Name: CQERRI
Bit	Read/Writ	Default/He	Description
31	R	0x0	CQE_DTE_VLD Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0.
30:29	/	/	/

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Offset: 0x0454			Register Name: CQERRI
Bit	Read/Writ	Default/He	Description
28:24	R	0x0	CQE_DTE_TASK_ID Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23:22	/	/	/
21:16	R	0x0	CQE_DTE_CMD_IDX Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	R	0x0	CQE_RME_VLD Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0.
14:13	/	/	/
12:8	R	0x0	CQE_RME_TASK_ID Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7:6	/	/	/

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Offset: 0x0454			Register Name: CQERRI
Bit	Read/Writ	Default/He	Description
5:0	R	0x0	CQE_RME_CMD_IDX Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

3.3.6.58 0x0458 CQCRI Command Response Index Register (Default Value: 0x0000_0000)

This register stores the index of the last received command response.

Offset: 0x0458			Register Name: CQCRI
Bit	Read/Writ	Default/He	Description
31:6	/	/	/
5:0	R	0x0	CQE_LAST_RESP_IDX Last Command Response index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

3.3.6.59 0x045C CQCRA Command Response Argument Register (Default Value: 0x0000_0000)

This register stores the argument of the last received command response.

Offset: 0x045C			Register Name: CQCRA
Bit	Read/Writ	Default/He	Description
31:0	R	0x0	CQE_LAST_RESP_ARG Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

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4 Audio

4.1 Audio Codec

4.1.1 Overview

The Audio Codec is high-performance audio encoder and decoder module which supports DAC/ADC, dynamic range controller (DRC) and dynamic voltage controller (DVC) functions.

The Audio Codec has the following features:

- Two audio digital-to-analog converter (DAC) channels
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 100 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- Three audio outputs
  - One stereo headphone output: HPOUTL/R
  - Two differential lineout outputs: LINEOUTLP/N and LINEOUTRP/N
- Three audio analog-to-digital converter (ADC) channels
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95 ± 3dB SNR@A-weight, -80 ± 3dB THD+N
- Three differential microphone inputs: MICIN1P/1N, MICIN2P/2N, and MICIN3P/3N (for echo reduction)
- Two low-noise analog microphone bias outputs: MBIAS and HBIAS
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA
- Internal ALDO output for AVCC

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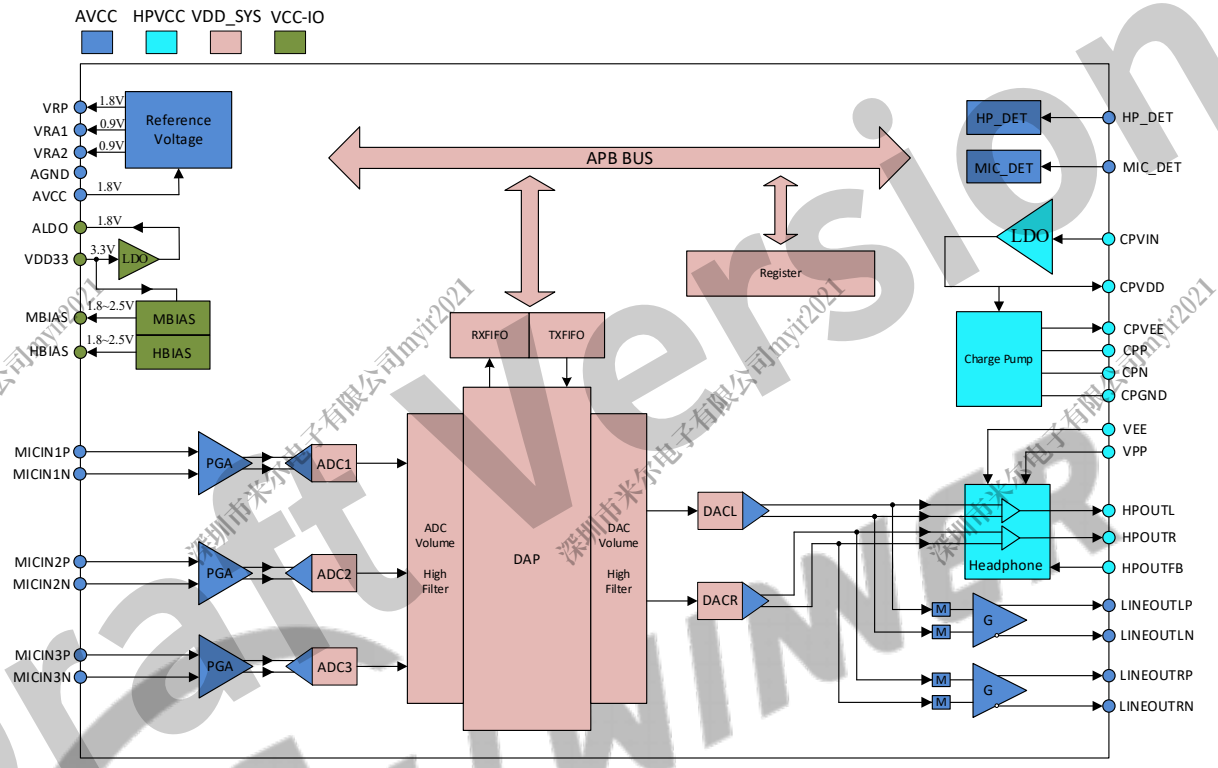
4.1.2 Block Diagram

The following figure shows the block diagram of Audio Codec.

Figure 4-1 Audio Codec Block Diagram



4.1.3 Functional Description

4.1.3.1 External Signals

Table 4-1 Audio Codec External Signals

Signal Name	Description	Type
MICIN1P	Microphone Differential Positive Input 1	AI
MICIN1N	Microphone Differential Negative Input 1	AI
MICIN2P	Microphone Differential Positive Input 2	AI
MICIN2N	Microphone Differential Negative Input 2	AI
MICIN3P	Microphone Differential Positive Input 3	AI
MICIN3N	Microphone Differential Negative Input 3	AI
LINEOUTLP	Lineout Left Channel Positive Differential Output	AO
LINEOUTLN	Lineout Left Channel Negative Differential Output	AO
LINEOUTRP	Lineout Right Channel Positive Differential Output	AO
LINEOUTRN	Lineout Right Channel Negative Differential Output	AO
HPOUTL	Headphone Left Output	AO
HPOUTR	Headphone Right Output	AO
HPOUTFB	Pseudo Differential Headphone Ground Reference	AI

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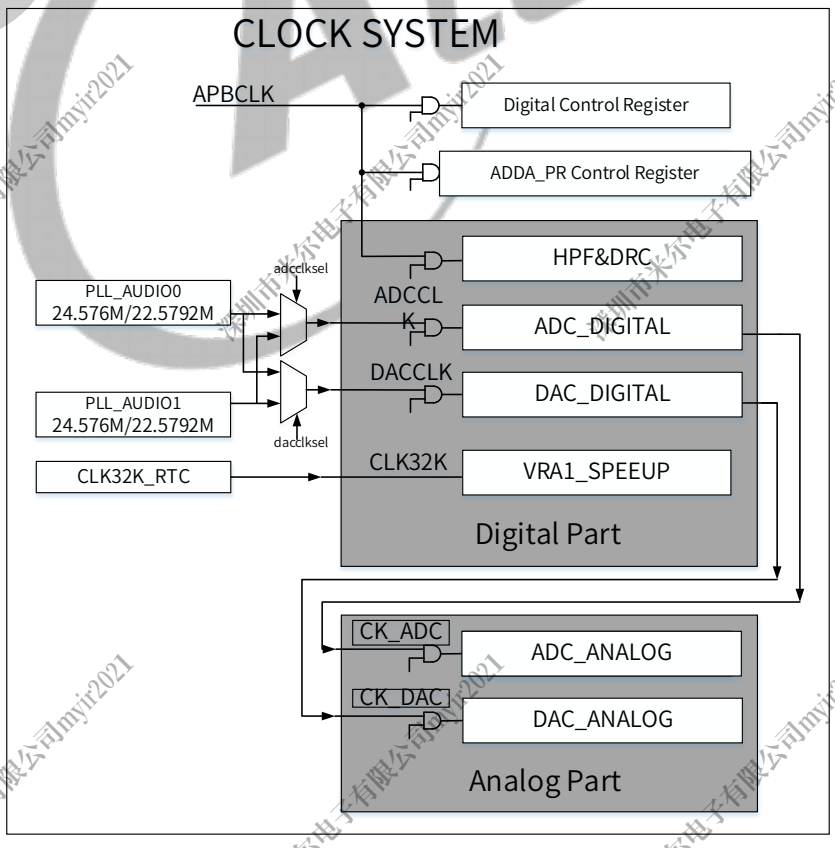
Signal Name	Description	Type
MIC-DET	Headphone MIC detect	AI
HP-DET	Headphone Jack detect	AI
MBIAS	First bias voltage output for main microphone	AO
HBIAS	Second bias voltage output for headset microphone	AO
CPVDD	Analog power for headphone charge pump	P
CPVEE	Charge pump negative voltage output	P
CPVIN	Analog power for LDO	P
AVCC	Power Supply for Analog Part	P
ALDO-OUT	Power Supply for AVCC	P
VDD33	Power Supply for 3.3V Analog Part	P
VEE	Negative Voltage to Headphone	P
VRA1	Internal Reference Voltage	AO
VRA2	Internal Reference Voltage	AO
VRP	Internal Reference Voltage	AO
AGND	Analog Ground	G

4.1.3.2 Clock Sources

The following figure describes the clock source of Audio Codec. For clock setting, configuration, and gating information, refer to section 2.13 Power Reset Clock Management (PRCM).

Figure 4-2 Audio Codec Clock Diagram



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- Digital Part

The clock sources for the digital ADC and DAC are the PLL_AUDIO0 and PLL_AUDIO1. Configure the CLK_SRC_SEL bit (bit [26:24]) of AUDIO_CODEC_ADC_CLK_REG register to select clock sources for ADC. Configure CLK_SRC_SEL bit (bit [26:24]) of AUDIO_CODEC_DAC_CLK_REG register to select clock sources for DAC. The PK-PK jitter of PLL_AUDIO0 and PLL_AUDIO1 should be less than 200 ps.

The clock source for VRA1_SPEEDUP is CLK32K from RTC.

- Analog Part

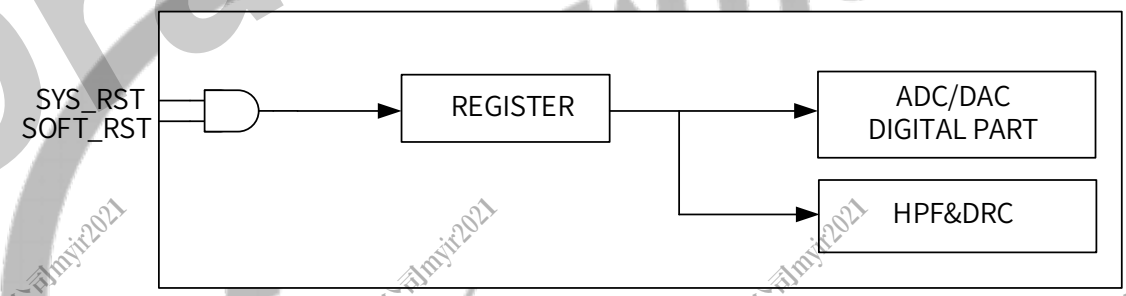
The clock source for the analog part is the CK_ADC and CK_DAC, both of which are divided from the digital part.

4.1.3.3 Reset System

Digital Part Reset System

The following figure shows the reset system of the audio codec digital part.

Figure 4-3 Audio Codec Digital Part Reset System



The DSP_SYS_RST comes from the VDD-SYS domain and is produced by the RTC domain which is controlled by DSP_PRCM. Each domain has the de-bounce to confirm the reset system is strong. For the codec register part, MIX can be reset by the DSP_SYS_RST when being powered on or the system soft is writing the reset control logic. The other parts can be reset by the soft configuration through writing the register.

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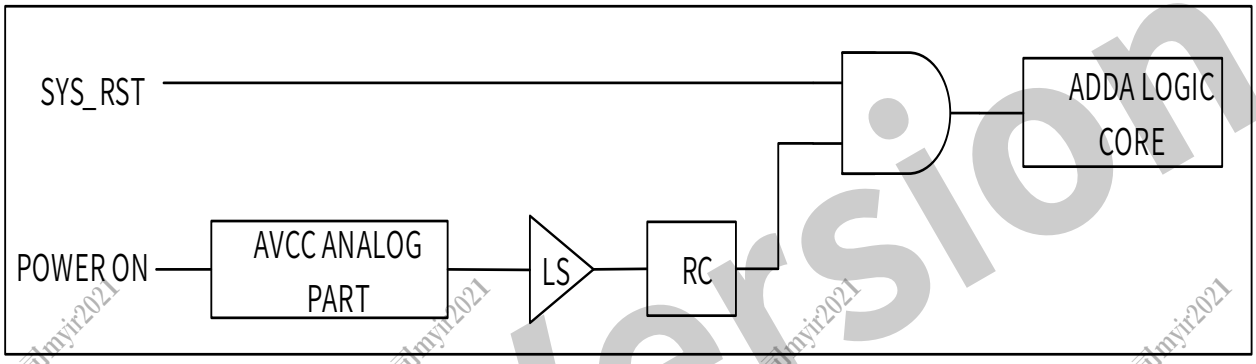
Analog Part Reset System

The following figure shows the reset system of the audio codec analog part.

Figure 4-4 Audio Codec Analog Part Reset System



When AVCC is powered on, it sends the AVCC_POR signal. The AVCC_POR signal passes the level shift and RC filter part to the Audio Codec logic core.

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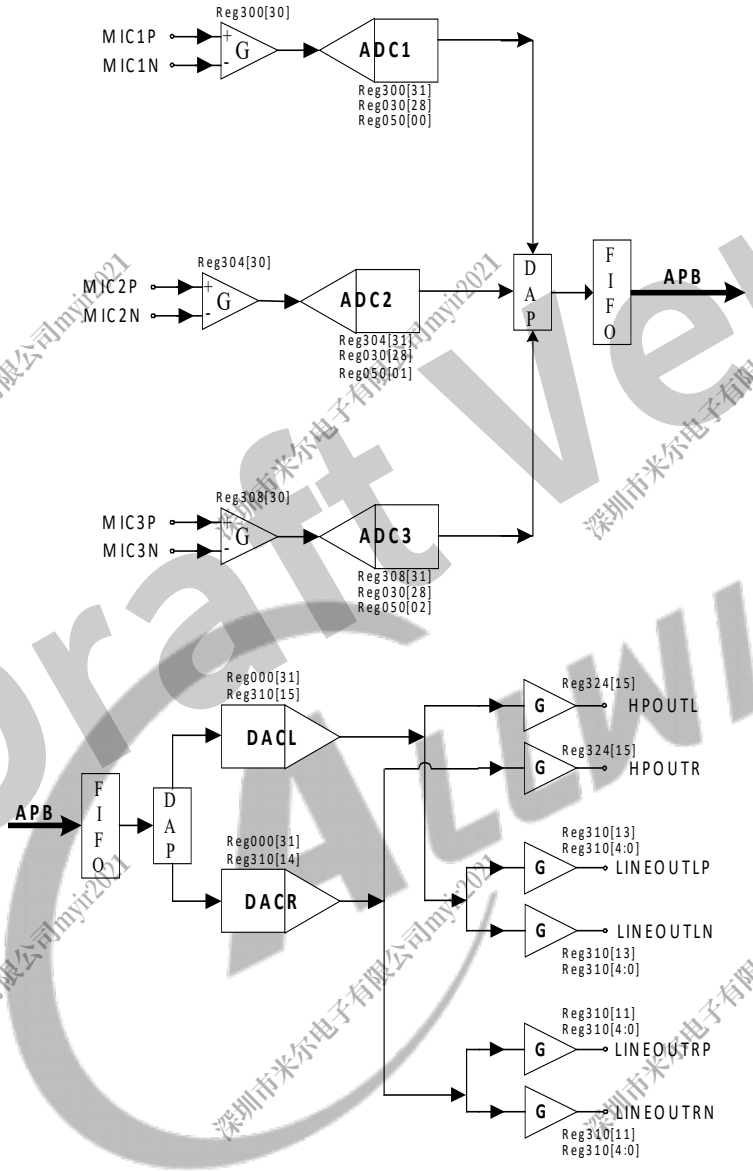
4.1.3.4 Data Path Diagram

The following figure shows a data path of the Audio Codec.

Figure 4-5 Audio Codec Data Path Diagram



4.1.3.5 Three ADCs

The three ADCs are used for recording stereo sound and a reference signal. The sample rates of the three ADCs are independent of the DAC sample rate. The digital ADC part can be enabled or disabled by the bit[28] of the AC_ADC_FIFOC register.

4.1.3.6 Stereo DACs

The stereo DAC sample rate can be configured by setting the register. To save power, the analog DACL can be enabled or disabled by setting the bit [15] of the DAC_REG register, and the analog

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DACR can be enabled or disabled by setting the bit [14] of the DAC_REGregister. The digital DAC part can be enabled or disabled by the bit [31] of the AC_DAC_DPC register.

4.1.3.7 Analog Audio Input Path

The Audio Codec supports 3 analog audio input paths:

- MICIN1P/N
- MICIN2P/N
- MICIN3P/N

The MICIN is a high impedance, low capacitance input suitable for connecting to various differential microphones of different dynamics and sensitivity. The gain for each pre-amplifier can be set independently. MBIAS provide reference voltage for electret condenser type(ECM) microphones.

4.1.3.8 Analog Audio Output Path

The Audio Codec has two types of analog output ports:

- LINEOUTLP
- LINEOUTLN
- LINEOUTRP
- LINEOUTRN
- HPOUTL
- HPOUTR

LINEOUTL/R

LINEOUTL/R provides one differential output to drive line signals to external audio equipment. The LINEOUTLP/N output source from DACL. The LINEOUTRP/N output source from DACR. The volume control is logarithmic with a 43.5 dB rang in 1.5 dB step from -43.5 dB to 0 dB. The LINEOUTL/R output buffer power up or down by bit [13] or bit [11] of DAC_REG (Offset: 0x0310).

Headphone Output

The headphone PA power up or down by bit [15] of HP_REG (Offset: 0x0324). HPOUTL/R can drive a 16R or 32R headphone load without DC capacitors by using Charge Pump to generate the negative rails. HP-FB is the ground loop noise rejection feedback. HBIAS provides reference voltage for electret condenser type (ECM) microphones.

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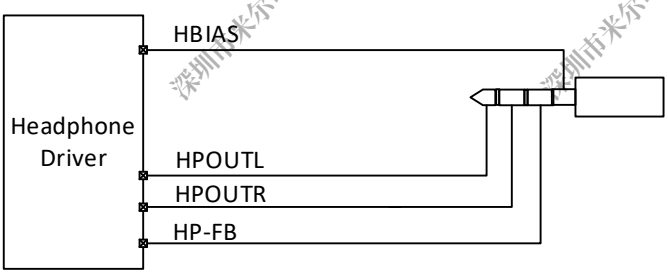
Figure 4-6 Headphone Output Application



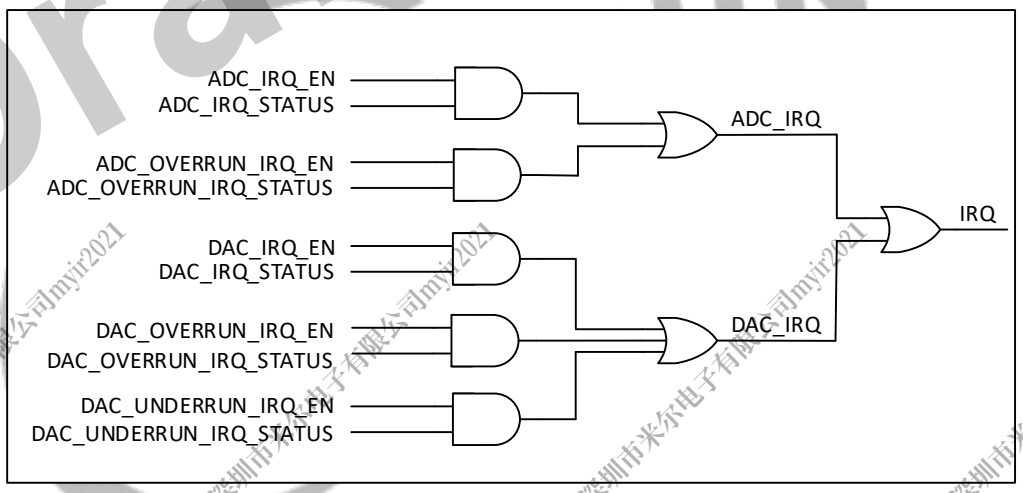
4.1.3.9 Microphone BIAS

The MBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network.

4.1.3.10 Interrupt

The Audio Codec has two groups of interrupt. The following figure describes the Audio Codec interrupt system.

Figure 4-7 Audio Codec Interrupt System



4.1.3.11 Digital Audio Processor (DAP)

The DAP module is used to remove the DC offset and automatically adjusts the volume to a flatten volume level. It mainly consists of two HPF and one DRC.

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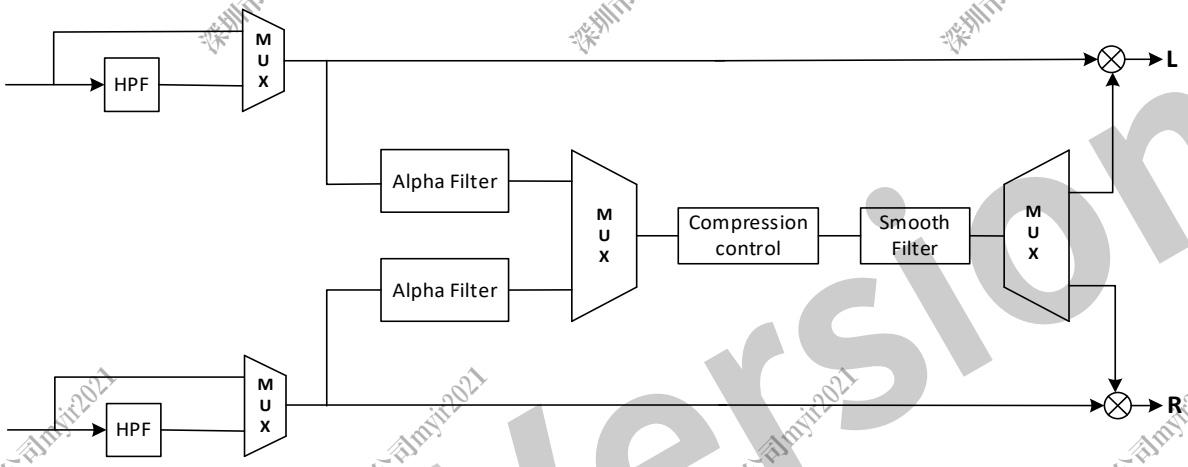
The following figure shows the DAP data flow.

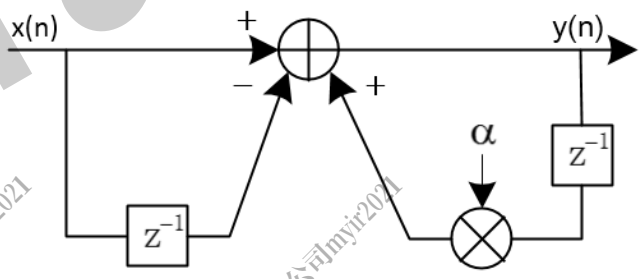
Figure 4-8 DAP Data Flow



HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enabled and disabled. The filter cutoff frhequency is less than 1 Hz that can be removed DC offset from ADC recording. The HPF can also be bypassed.

Figure 4-9 HPF Logic Structure



HPF transfer function is $H(z) = \frac{1 - z^{-1}}{1 - \alpha z^{-1}}$,that is y(n)=αy(n-1)+x(n)-x(n-1).

For cut-off frequency Fpass: w = Fpass/Fs * 2 * pi. Generally, w is small. So, $\alpha < 0, |\alpha| < 1$.

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DRC Function

The DRC scheme has three thresholds, three offsets, and four slopes (all programmable). There is one ganged DRC for the left and right channels. The following figure shows the diagram of DRC input/output.

Figure 4-10 DRC static Curve Parameters

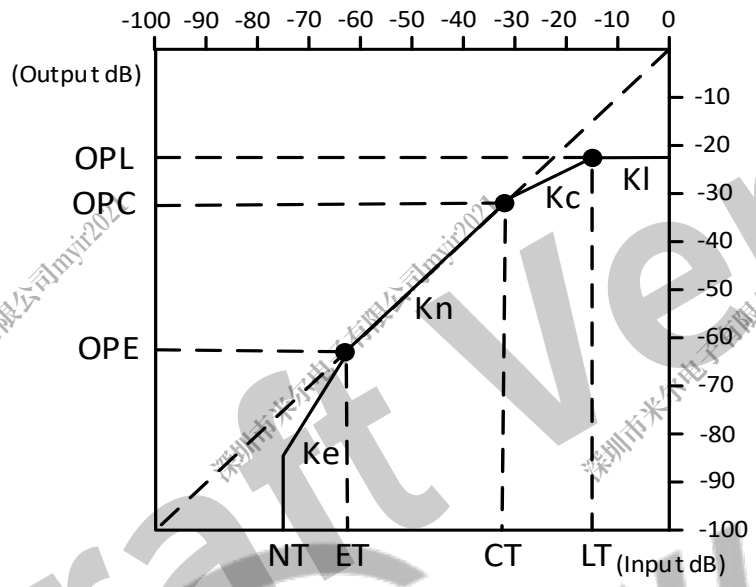
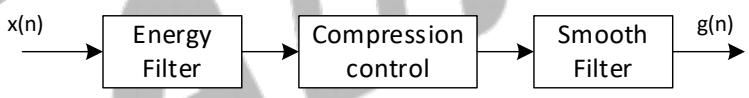


Figure 4-11 DRC Block Diagram



Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

One DRC for left/right and one DRC for subwoofer.

Each DRC has the adjustable threshold, offset, compression levels, programmable energy, attack, and decay time constants.

Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Configure the DRC parameters according to the following guidelines:

- Number format

The Number format is N.M which means there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 9.23 means that there are 9 bits at the left of the decimal point and 23 bits at the right decimal point.

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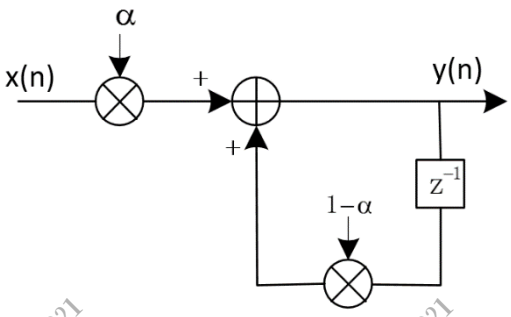
- Energy Filter

The following figure shows the structure of the energy filter.

Figure 4-12 Energy Filter Structure



The Energy Filter is to estimate of the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by $\alpha = 1 - e^{-2.2T_s/ta}$.

- Compression Control

This element has six parameters (ET, CT, LT, Ke, Kn, Kc, Kl, OPL, OPC, OPE), which are all programmable, and the computation will be explained as follows.

Threshold Parameter Computation (T parameter)

The threshold is the value that determines the signal to be compressed or not. When the signal's RMS is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by

$$Tin = -\frac{T_{dB}}{6.0206}$$

Where, T_{dB} must less than zero, the positive value is illegal.

For example, it is desired to set CT=-40dB, then the Tin require to set CT to -40dB is CTin = - (-40dB)/6.0206 = 6.644, CTin is entered as a 32-bit number in 8.24 format.

Therefore, CTin = 6.644 = 0000 0110.1010 0100 1101 0011 1100 0000 = 0x06A4 D3C0 in 8.24 format.

Slope Parameter Computation (K parameter)

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB is for n dB RMS input. The k input to the coefficient ram is computed by

$$K = \frac{1}{n}$$

Where, n is from 1 to 50, and must be integer.

For example, it is desired to set 2:1, then the Kc require to set to 2:1 is Kc = 1/2 = 0.5, Kc is entered as a 32-bit number in 8.24 format.

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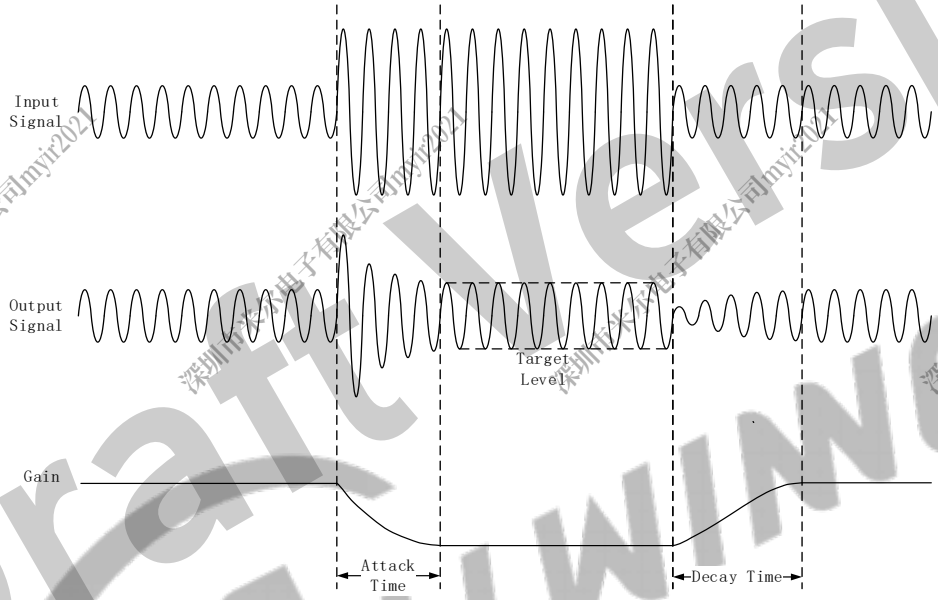
Therefore, Kc = 0.5 = 0000 0000.1000 0000 0000 0000 0000 0000 = 0x0080 0000 in 8.24 format.

- Gain Smooth Filter

The Gain Smooth Filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 1-17. The structure of the Gain Smooth filter is also the Alpha filter, so the rise time computation is the same as the Energy filter which is $\alpha = 1 - e^{-2.2Ts/ta}$.

Figure 4-13 Gain Smooth Filter



4.1.4 Programming Guidelines

4.1.4.1 Playing

Step 1 Codec initialization: configure AUDIO_CODEC_BGR_REG and AUDIO_CODEC_DAC_CLK_REG to open the audio codec bus clock gating, release the bus reset, and open the PLL_AUDIO DAC clock gating; set up PLL_AUDIO0_CTRL_REG to configure PLL_AUDIO0 frequency and enable PLL_AUDIO0. For details of PLL_AUDIO0, refer to section 2.7 Clock Controller Unit (CCU).

Step 2 Set up the sample rate and data transfer format, then open the DAC.

Step 3 Configure the DMA and DMA request.

Step 4 Enable the DAC DRQ and DMA.

4.1.4.2 Recording

Step 1 Codec initialization: configure AUDIO_CODEC_BGR_REG and AUDIO_CODEC_ADC_CLK_REG to open the audio codec bus clock gating, release the bus

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reset, and open the PLL_AUDIO1 ADC clock gating; set up PLL_AUDIO1_CTRL_REG to configure PLL_AUDIO1 frequency and enable PLL_AUDIO1. For details, refer to section 2.13 Power Reset Clock Management (PRCM).

Step 2 Configure the sample rate and data transfer format, then open the ADC.

Step 3 Configure the DMA and DMA request.

Step 4 Enable the ADC DRQ and DMA.

4.1.5 Register List

Module Name	Base Address
AUDIO CODEC	0x07110000

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
DAC_VOL_CTRL	0x0004	DAC Volume Control Register
AC_DAC_FIFOC	0x0010	DAC FIFO Control Register
AC_DAC_FIFOS	0x0014	DAC FIFO Status Register
AC_DAC_TXDATA	0x0020	DAC TX DATA Register
AC_DAC_CNT	0x0024	DAC TX FIFO Counter Register
AC_DAC_DG	0x0028	DAC Debug Register
AC_ADC_FIFOC	0x0030	ADC FIFO Control Register
ADC_VOL_CTRL1	0x0034	ADC Volume Control1 Register
AC_ADC_FIFOS	0x0038	ADC FIFO Status Register
AC_ADC_RXDATA	0x0040	ADC RX Data Register
AC_ADC_CNT	0x0044	ADC RX Counter Register
AC_ADC_DG	0x004C	ADC Debug Register
ADC_DIG_CTRL	0x0050	ADC Digtial Control Register
VRA1SPEEDUP_DOWN_CTRL	0x0054	VRA1Speedup Down Control Register
AC_DAC_DAP_CTRL	0x00F0	DAC DAP Control Register
AC_ADC_DAP_CTR	0x00F8	ADC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register

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Register Name	Offset	Description
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_RPFHRT	0x0124	DAC DRC Right Peak filter High Release Time Coef Register
AC_DAC_DRC_RPFLRT	0x0128	DAC DRC Right Peak filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_RRMSHAT	0x0134	DAC DRC Right RMS Filter High Coef Register
AC_DAC_DRC_RRMSLAT	0x0138	DAC DRC Right RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Threshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Threshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Threshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold
AC_DAC_DRC_HET	0x016C	DAC DRC Expander Threshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Threshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register

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Register Name	Offset	Description
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_RPFHAT	0x0214	ADC DRC Right Peak Filter High Attack Time Coef Register
AC_ADC_DRC_RPFLAT	0x0218	ADC DRC Right Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_RPFHRT	0x0224	ADC DRC Right Peak filter High Release Time Coef Register
AC_ADC_DRC_RPFLRT	0x0228	ADC DRC Right Peak filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_RRMSHAT	0x0234	ADC DRC Right RMS Filter High Coef Register
AC_ADC_DRC_RRMSLAT	0x0238	ADC DRC Right RMS Filter Low Coef Register

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Register Name	Offset	Description
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Threshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Threshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Threshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Threshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Threshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGHS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MNGLS	0x02A8	ADC DRC MIN Gain Low Setting Register

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Register Name	Offset	Description
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
ADC1_REG	0x0300	ADC1 Analog Control Register
ADC2_REG	0x0304	ADC2 Analog Control Register
ADC3_REG	0x0308	ADC3 Analog Control Register
DAC_REG	0x0310	DAC Analog Control Register
DAC2_REG	0x0314	DAC2 Analog Control Register
MICBIAS_REG	0x0318	MICBIAS Analog Control Register
BIAS_REG	0x0320	BIAS Analog Control Register
HP_REG	0x0324	HEADPHONE Analog Control Register
HMIC_CTRL	0x0328	HMIC Control Register
HMIC_STS	0x032C	HMIC Status Register
POWER_REG	0x0348	POWER Analog Control Register

4.1.6 Register Description

4.1.6.1 0x0000 DAC Digital Part Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EN_DA DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels= [7*(21+MODQU [3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/

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Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT=DVC [5:0] *(-1.16dB) 64 steps, -1.16dB/step
11	/	/	/
10:8	R/W	0x1	DITHER_SGM Dither Sigma 000: Reserved 001: 1/2 010: $1/2^2$ 011: $1/2^3$ 100: $1/2^4$ 101: $1/2^5$ 110: $1/2^6$ 111: Reserved
7:4	R/W	0x0	DITHER_SFT Dither Shift Can increase the output amplitude of dither. 0000: $x2^0$ 0001: $x2^1$ 0010: $x2^2$ 0011: $x2^3$ … 1011: $x2^{11}$ 1100: $x2^{12}$ 1101—1111:Reserved
3:2	/	/	/
1	R/W	0x0	DITHER_EN DSM Dither Enable 0: Disable 1: Enable

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Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HUB_EN Audio Hub Enable The bit takes effect only when the EN_DA is set to 1. CPUS Domain: Audio Codec/ I2S0/ I2S1/ I2S2/I2S3/ OWA TXFIFO Hub Enable. 0: Disable 1: Enable

4.1.6.2 0x0004 DAC Volume Control Register (Default Value: 0x0000_A0A0)

Offset: 0x0004			Register Name: DAC_VOL_CTRL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DAC_VOL_SEL DAC Volume Control Selection Enable 0: Disable 1: Enable
15:8	R/W	0xA0	DAC_VOL_L DAC left channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB
7:0	R/W	0xA0	DAC_VOL_R DAC right channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB

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4.1.6.3 0x0010 DAC FIFO Control Register (Default Value: 0x0000_4000)

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	DAC_FS Sample Rate of DAC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: 192 kHz 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: 96 kHz 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 20-bits transmitted audio sample: 00/10: FIFO_I [19:0] = {TXDATA [31:12]} 01/11: FIFO_I [19:0] = {TXDATA [19:0]} For 16-bits transmitted audio sample: 00/10: FIFO_I [19:0] = {TXDATA [31:16], 4'b0} 01/11: FIFO_I[19:0] = {TXDATA[15:0], 4'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, the DRQ request will be de-asserted. N is defined here: 00: IRQ/DRQ De-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/

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Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default/Hex	Description
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL [12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ≤ TXTL Notes: WLEVEL represents the number of valid samples in the TX FIFO Only TXTL[6:0] valid when TXMODE = 0
7	/	/	/
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data
5	R/W	0x0	TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 20 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Under Run IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	FIFO_FLUSH DAC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

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4.1.6.4 0x0014 DAC FIFO Status Register (Default Value: 0x0080_8008)

Offset: 0x0014			Register Name: AC_DAC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/WC	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	R/WC	0x0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/WC	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

4.1.6.5 0x0020 DAC TX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

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4.1.6.6 0x0024 DAC TX FIFO Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: AC_DAC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

4.1.6.7 0x0028 DAC Debug Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select: cksel 0: CODEC Clock from PLL 1: CODEC Clock from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC output channel swap enable, DA_SWP 0: Disable 1:Enable
5:3	/	/	/

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Offset: 0x0028			Register Name: AC_DAC_DG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	ADDA_LOOP_MODE Audio Codec Loop MODE SELECT 000: Disable 001: ADDA LOOP MODE DACL/DACR connect to ADC1/ADC2 010: ADDA LOOP MODE DACL connect to ADC3 1xx: Reserved

4.1.6.8 0x0030 ADC FIFO Control Register (Default Value: 0x0000_0400)

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable
27:26	R/W	0x0	ADCFDT ADC FIFO Delay Time for writing Data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms
25	R/W	0x0	ADCDFEN ADC FIFO Delay Function for writing Data after EN_AD 0: Disable 1: Enable

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Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 20-bits received audio sample: Mode 0: RXDATA [31:0] = {FIFO_O [19:0], 12'h0} Mode 1: RXDATA [31:0] = {12{FIFO_O [19]}, FIFO_O [19:0]} For 16-bits received audio sample: Mode 0: RXDATA [31:0] = {FIFO_O [19:4], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[19]}, FIFO_O[19:4]}
23:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START Only if RX_SYNC_EN set 1, RX_SYNC_EN_START can take effect. CPUS Domain： Audio Codec/ I2S0/ I2S1/ I2S2/ DMIC/ OWA RX Synchronize Enable Start. 0: Disable 1: Enable
20	R/W	0x0	RX_SYNC_EN Audiocodec RX Synchronize Enable 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 20 bits
15:12	/	/	/
11:4	R/W	0x40	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL [5:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ Generated when WLEVEL ＞ RXTL[5:0] Notes: WLEVEL represents the number of valid samples in the RX FIFO

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Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self-clear to '0'.

4.1.6.9 0x0034 ADC Volume Control1 Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: ADC_VOL_CTRL1
Bit	Read/Write	Default/Hex	Description
31:24	R	0xA0	PLACE_HOLDER No meaning
23:16	R/W	0xA0	ADC3_VOL ADC3 channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB

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Offset: 0x0034			Register Name: ADC_VOL_CTRL1
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0xA0	ADC2_VOL ADC2 channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB
7:0	R/W	0xA0	ADC1_VOL ADC1 channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB

4.1.6.10 0x0038 ADC FIFO Status Register (Default Value: 0x0000_0001)

Offset: 0x0038			Register Name: AC_ADC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:17	/	/	/
16:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/

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Offset: 0x0038			Register Name: AC_ADC_FIFOS
Bit	Read/Write	Default/Hex	Description
3	R/WC	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/WC	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	R	0x1	PLACE_HOLDER No meaning

4.1.6.11 0x0040 ADC RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_ADC_RXDATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

4.1.6.12 0x0044 ADC RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

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4.1.6.13 0x004C ADC Debug Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	AD_SWP2 ADC output channel swap enable (for digital filter) 0: Disable 1: Enable Note:ADC3 and ADC4(2`b0) swap data.
24	R/W	0x0	AD_SWP1 ADC output channel swap enable (for digital filter) 0: Disable 1: Enable Note:ADC1 and ADC2 swap data.
23:0	/	/	/

4.1.6.14 0x0050 ADC Digtial Control Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ADC_DIG_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	ADC3_VOL_EN ADC3 Volume Control Enable 0: Disable 1: Enable
16	R/W	0x0	ADC1_2_VOL_EN ADC1/2 Volume Control Enable 0: Disable 1: Enable
15:3	/	/	/
2:0	R/W	0x0	ADC_CHANNEL_EN Bit 2: ADC3 enable Bit 1: ADC2 enable Bit 0: ADC1 enable

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4.1.6.15 0x0054 VRA1Speedup Down Control Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: VRA1SPEEDUP_DOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:05	/	/	/
4	R	0x0	VRA1SPEEDUP_DOWN_STATE Only if VAR1SPEEDUP_DOWN_Further_CTRL (0x310[22]) set 0, VAR1Speedup Down State is valid. 0: VAR1Speedup_Down not work 1: VAR1Speedup_Down work
3:2	/	/	/
1	R/W	0x0	VRA1SPEEDUP_DOWN_CTRL VAR1Speedup Down Manual Control Enable 0: Disable, VAR1Speedup Down convert 1 after bus RST release 32ms. 1: Enable,VAR1Speedup Down convert 1 immediately.
0	R/W	0x0	VRA1SPEEDUP_DOWN_RST_CTRL VAR1Speedup Down RST Manual Control Enable 0: Disable, VAR1Speedup Down convert 1 after bus RST release 32ms. 1: Enable,VAR1Speedup Down reset 0 immediately.

4.1.6.16 0x00F0 DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0X0	DDAP_EN DAP for DRC Enable 0: Bypass 1: Enable
30	/	/	/
29	R/W	0X0	DDAP_DRC_EN DRC Enable Control 0: Disable 1: Enable
28	R/W	0X0	DDAP_HPF_EN HPF Enable Control 0: Disable 1: Enable

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Offset: 0x00F0			Register Name: AC_DAC_DAP_CTRL
Bit	Read/Write	Default/Hex	Description
27:0	/	/	/

4.1.6.17 0x00F8 ADC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ADC_DAP0_EN DAP for ADC1/2 Enable (Adjust the position, and two DRCs use the same parameter) 0: bypass 1:enable
30	/	/	/
29	R/W	0x0	ADC_DRC0_EN ADC DRC0 Enable Control 0: disable 1:enable
28	R/W	0x0	ADC_HPF0_EN ADC HPF0 Enable Control 0: disable 1:enable
27	R/W	0x0	ADC_DAP1_EN ADC DAP1 Enable Control This bit is to control the DAP for ADC3.
26	/	/	/
25	R/W	0x0	ADC_DRC1_EN ADC DRC1 enable control 0: disable 1:enable
24	R/W	0x0	ADC_HPF1_EN ADC HPF1 enable control 0: disable 1:enable
23:0	/	/	/

4.1.6.18 0x0100 DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

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Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0xFF	DAC_DRC_HHPF_COE HPF coefficient setting and the data is 3.24 format.

4.1.6.19 0x0104 DAC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	DAC_DRC_LHPF_COE HPF coefficient setting and the data is 3.24 format.

4.1.6.20 0x0108 DAC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0	DAC_DRC_DELAY_BUF_STATE DRC delay buffer data output state when DRC delay function is enable and the DRC function disable. After disable DRC function and this bit go to 0, the user should write the DRC delay function bit to 0; 0: not complete 1 : is complete
14:10	/	/	/
13:8	R/W	0	DAC_DRC_SIGNAL_DELAY_TIME_SET Signal delay time setting 6'h00: (8x1) fs 6'h01: (8x2) fs 6'h02: (8x3) fs ---------- 6'h2e: (8*47) fs 6'h2f: (8*48) fs 6'h30 -- 6'h3f: (8*48) fs Delay time = 8*(n+1) fs, n<6'h30; When the delay function is disable, the signal delay time is unused.

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Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	DAC_DRC_DELAY_BUF_EN The delay buffer use or not when the DRC disable and the DRC buffer data output completely 0: don't use the buffer 1 : use the buffer
6	R/W	0x0	DAC_DRC_GAIN_MAX_LIMIT_EN DRC gain max limit enable 0: disable 1 : enable
5	R/W	0x0	DAC_DRC_GAIN_MIN_LIMIT_EN DRC gain min limit enable. when this function enables, it will overwrite the noise detect function. 0: disable 1 : enable
4	R/W	0x0	DAC_DRC_DETECT_NOISE_EN Control the DRC to detect noise when ET enable 0: disable 1 : enable
3	R/W	0x0	DAC_DRC_SIGNAL_FUNC_SEL Signal function Select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	DAC_DRC_DELAY_FUNC_EN Delay function enable 0: disable 1: enable When the Delay function enable is disable, the Signal delay time is unused.

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Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	DAC_DRC_LT_EN DRC LT enable 0: disable 1: enable When the DRC LT is disable the LT, Kl and OPL parameter is unused.
0	R/W	0x0	DAC_DRC_ET_EN DRC ET enable 0: disable 1: enable When the DRC ET is disable the ET, Ke and OPE parameter is unused.

4.1.6.21 0x010C DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x000B	DAC_DRC_LPFHAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.22 0x0110 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	DAC_DRC_LPFLAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

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4.1.6.23 0x0114 DAC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0114 0x0000_000B)

Offset: 0x0114			Register Name: AC_DAC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x000B	DAC_DRC_RPFHAT The right peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.24 0x0118 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	DAC_DRC_RPFLAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.25 0x011CDAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	DAC_DRC_LPFHRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

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4.1.6.26 0x0120 DAC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	DAC_DRC_LPFLRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.27 0x0124 DAC DRC Right Peak filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0124			Register Name: AC_DAC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	DAC_DRC_RPFHRT The right peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.28 0x0128 DAC DRC Right Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0128			Register Name: AC_DAC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	DAC_DRC_RPFLRT The right peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.29 0x012CDAC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

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Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0001	DAC_DRC_LRMSHAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24.(The default value is 10ms)

4.1.6.30 0x0130 DAC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_LRMSLAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.31 0x0134 DAC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0134			Register Name: AC_DAC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0001	DAC_DRC_RRMSHAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24.(The default value is 10ms)

4.1.6.32 0x0138 DAC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0138			Register Name: AC_DAC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_RRMSLAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24.(10ms)

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4.1.6.33 0x013CDAC DRC Compressor Threshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	DAC_DRC_HCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.34 0x0140 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	DAC_DRC_LCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.35 0x0144 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	DAC_DRC_HKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (The default value is <2 : 1>)

4.1.6.36 0x0148 DAC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0000	DAC_DRC_LKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is <2 : 1>)

4.1.6.37 0x014C DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	DAC_DRC_HOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.38 0x0150 DAC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	DAC_DRC_LOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.39 0x0154 DAC DRC Limiter Threshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	DAC_DRC_HLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

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4.1.6.40 0x0158 DAC DRC Limiter Threshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	DAC_DRC_LLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

4.1.6.41 0x015C DAC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0005	DAC_DRC_HKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50:1>)

4.1.6.42 0x0160 DAC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	DAC_DRC_LKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50 :1>)

4.1.6.43 0x0164 DAC DRC Limiter High Output at Limiter Threshold (Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	DAC_DRC_HOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

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4.1.6.44 0x0168 DAC DRC Limiter Low Output at Limiter Threshold (Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	DAC_DRC_LOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

4.1.6.45 0x016C DAC DRC Expander Threshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	DAC_DRC_HET The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

4.1.6.46 0x0170 DAC DRC Expander Threshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	DAC_DRC_LET The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

4.1.6.47 0x0174 DAC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0500	DAC_DRC_HKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

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4.1.6.48 0x0178 DAC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.49 0x017C DAC DRC Expander High Output at Expander Threshold (Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	DAC_DRC_HOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.50 0x0180 DAC DRC Expander Low Output at Expander Threshold (Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	DAC_DRC_LOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.51 0x0184 DAC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0100	DAC_DRC_HKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.52 0x0188 DAC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.53 0x018C DAC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	DAC_DRC_SFHAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.54 0x0190 DAC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x5600	DAC_DRC_SFLAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.55 0x0194 DAC DRC Smooth Filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	DAC_DRC_SFHRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.56 0x0198 DAC DRC Smooth Filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	DAC_DRC_SFLRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.57 0x019C DAC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xFE56	DAC_DRC_MXGHS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB. (The default value is -10dB)

4.1.6.58 0x01A0 DAC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	DAC_DRC_MXGLS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB. (The default value is -10dB)

4.1.6.59 0x01A4 DAC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	DAC_DRC_MNGHS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.60 0x01A8 DAC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	DAC_DRC_MNGLS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

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4.1.6.61 0x01AC DAC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	DAC_DRC_EPSHC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.62 0x01B0 DAC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	DAC_DRC_EPSLC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.63 0x01B8 DAC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	DAC_DRC_HPFHGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.64 0x01BC DAC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_HPFLGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

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4.1.6.65 0x0200 ADC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0xFF	ADC_DRC_HHPFC HPF coefficient setting and the data is 3.24 format.

4.1.6.66 0x0204 ADC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	ADC_DRC_LHPFC HPF coefficient setting and the data is 3.24 format.

4.1.6.67 0x0208 ADC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ADC_DRC_DELAY_BUF_OUTPUT_STATE DRC delay buffer data output state when DRC delay function is enable and the DRC function disable. After disable DRC function and this bit go to 0, the user should write the DRC delay function bit to 0; 0: not complete 1 : is complete
14:10	/	/	/

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Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
13:8	R/W	0x0	ADC_DRC_SIGNAL_DELAY_TIME_SET Signal delay time setting 6'h00: (8x1) fs 6'h01: (8x2) fs 6'h02: (8x3) fs ---------- 6'h2e: (8*47) fs 6'h2f: (8*48) fs 6'h30 -- 6'h3f: (8*48) fs Delay time = 8*(n+1) fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	ADC_DRC_DELAY_BUF_EN The delay buffer use or not when the dry disable and the DRC buffer data output completely 0: don't use the buffer 1 : use the buffer
6	R/W	0x0	ADC_DRC_GAIN_MAX_LIMIT_EN DRC gain max limit enable 0: disable 1 : enable
5	R/W	0x0	ADC_DRC_GAIN_MIN_LIMIT_EN DRC gain min limit enable. when this function enables, it will overwrite the noise detect function. 0: disable 1 : enable
4	R/W	0x0	ADC_DRC_DETECT_NOISE_EN Control the DRC to detect noise when ET enable 0: disable 1 : enable

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Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	ADC_DRC_SIGNAL_FUNC_SEL Signal function Select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	ADC_DRC_DELAY_FUNC_EN Delay function enable 0: disable 1: enable When the Delay function enable is disable, the Signal delay time is unused.
1	R/W	0x0	ADC_DRC_LT_EN DRC LT enable 0: disable 1: enable DRC LT enable 0: disable 1: enable When the DRC LT is disable the LT, Kl and OPL parameter is unused.
0	R/W	0x0	ADC_DRC_ET_EN DRC ET enable 0: disable 1: enable When the DRC ET is disable the ET, Ke and OPE parameter is unused.

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4.1.6.68 0x020C ADC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x000B	ADC_DRC_LPFHAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.69 0x0210 ADC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	ADC_DRC_LPFLAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.70 0x0214 ADC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0214			Register Name: AC_ADC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x000B	ADC_DRC_RPFHAT The right peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

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4.1.6.71 0x0218 ADC DRC Right Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0218			Register Name: AC_ADC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	ADC_DRC_RPFLAT The right peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(The default value is 1ms)

4.1.6.72 0x021C ADC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	ADC_DRC_LPFHRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.73 0x0220 ADC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	ADC_DRC_LPFLRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

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4.1.6.74 0x0224 ADC DRC Right Peak filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0224			Register Name: AC_ADC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	ADC_DRC_RPFHRT The right peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.75 0x0228 ADC DRC Right Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	ADC_DRC_RPFLRT The right peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.76 0x022C ADC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	ADC_DRC_LRMSHAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.77 0x0230 ADC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x2BAF	ADC_DRC_LRMSLAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.78 0x0234 ADC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0234			Register Name: AC_ADC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0001	ADC_DRC_RRMSHAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.79 0x0238 ADC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0238			Register Name: AC_ADC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	ADC_DRC_RRMSLAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.80 0x023C ADC DRC Compressor Threshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	ADC_DRC_HCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

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4.1.6.81 0x0240 ADC DRC Compressor Slope High Setting RegisterB (Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	ADC_DRC_LCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.82 0x0244 ADC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	ADC_DRC_HKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (The default value is <2 : 1>)

4.1.6.83 0x0248 ADC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (The default value is <2 : 1>)

4.1.6.84 0x024C ADC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xF95B	ADC_DRC_HOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.85 ADC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0250 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	ADC_DRC_LOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.86 0x0254 ADC DRC Limiter Threshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	ADC_DRC_HLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

4.1.6.87 0x0258 ADC DRC Limiter Threshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	ADC_DRC_LLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

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4.1.6.88 0x025C ADC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0005	ADC_DRC_HKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50:1>)

4.1.6.89 0x0260 ADC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	ADC_DRC_LKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50:1>)

4.1.6.90 0x0264 ADC DRC Limiter High Output at Limiter Threshold (Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	ADC_DRC_HOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

4.1.6.91 0x0268 ADC DRC Limiter Low Output at Limiter Threshold (Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	ADC_DRC_LOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

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4.1.6.92 0x026C ADC DRC Expander Threshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	ADC_DRC_HET The expander threshold setting, which set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.93 0x0270 ADC DRC Expander Threshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	ADC_DRC_LET The expander threshold setting, which set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.94 0x0274 ADC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0500	ADC_DRC_HKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.95 0x0278 ADC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0000	ADC_DRC_LKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.96 0x027C ADC DRC Expander High Output at Expander Threshold (Default Value: 0x0000F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	ADC_DRC_HOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.97 0x0280 ADC DRC Expander Low Output at Expander Threshold (Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	ADC_DRC_LOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.98 0x0284 ADC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	ADC_DRC_HKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

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4.1.6.99 0x0288 ADC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.100 0x028C ADC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	ADC_DRC_SFHAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.101 0x0290 ADC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	ADC_DRC_SFLAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.102 0x0294 ADC DRC Smooth Filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

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Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0000	ADC_DRC_SFHRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.103 0x0298 ADC DRC Smooth Filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	ADC_DRC_SFLRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.104 0x029C ADC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFE56	ADC_DRC_MXGHS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (The default value is -10dB)

4.1.6.105 0x02A0 ADC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	ADC_DRC_MXGLS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (The default value is -10dB)

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4.1.6.106 0x02A4 ADC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	ADC_DRC_MNGHS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.107 0x02A8 ADC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	ADC_DRC_MNGLS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.108 0x02AC ADC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	ADC_DRC_EPSHC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.109 0x02B0 ADC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x640C	ADC_DRC_EPSLC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.110 0x02B8 ADC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	ADC_DRC_HPFHGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.111 0x02BC ADC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_HPFLGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.112 0x0300 ADC1 Analog Control Register (Default Value:0x001C_C055)

Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
31	R/W	0x0	ADC1_EN ADC1 Channel Enable 0: Disable 1: Enable
30	R/W	0x0	MIC1_PGA_EN MIC1 PGA Enable 0: Disable 1: Enable

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Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
29	R/W	0x0	ADC1 Dither Control 0: New Dither Off 1: New Dither On
28:26	R/W	0x0	/
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 0: No Level 1: Min Level 2: Middle Level 3:Max Level
23:22	R/W	0x0	/
21:20	R/W	0x1	ADC1_OUTPUT_CURRENT ADC1 high gain OP Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7uA
19:18	R/W	0x3	ADC1_PGA_CTRL_RCM ADC1 PGA Common Mode Input Impedance Control for MIC 0: 100 kΩ 1: 75 kΩ 2: 50 kΩ 3: 25 kΩ
17:16	R/W	0x0	ADC1_PGA_IN_VCM_CTRL ADC1 PGA Common-Mode Voltage Control 0: 900mV 1: 800mV 2: 750mV 3: 700mV
15:14	R/W	0x3	IOPADC ADC1-ADC3 Bias Current Select 00: 1uA 01: 2uA 10: 3uA 11: 4uA
13	R/W	0x0	/

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Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
12:8	R/W	0x0	ADC1_PGA_GAIN_CTRL ADC1 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
7:6	R/W	0x1	ADC1_IOPAAF ADC1 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA For example: ADC1_REG<15:14> =11，IOPADC=4uA 00: 1.50*4uA=6uA 01: 1.75*4uA=7uA 10: 2.00*4uA=8uA 11: 2.25*4uA=9uA
5:4	R/W	0x1	ADC1_IOPSDM1 ADC1 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

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Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
3:2	R/W	0x1	ADC1_IOPSDM2 ADC1 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
1:0	R/W	0x1	ADC1_IOPMIC ADC1 OP MIC Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

4.1.6.113 0x0304 ADC2 Analog Control Register (Default Value:0x001C_0055)

Offset: 0x0304			Register Name: ADC2_REG
Bit	R/W	Default	Description
31	R/W	0x0	ADC2_EN ADC2 Channel Enable 0: Disable 1: Enable
30	R/W	0x0	MIC2_PGA_EN MIC2 PGA Enable 0: Disable 1: Enable
29	R/W	0x0	ADC2 Dither Control 0: New Dither Off 1: New Dither On
28:26	R/W	0x0	/
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 0: No Level 1: Min Level 2: Middle Level 3:Max Level
23:22	R/W	0x0	/

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Offset: 0x0304			Register Name: ADC2_REG
Bit	R/W	Default	Description
21:20	R/W	0x1	ADC2_OUTPUT_CURRENT ADC2 high gain OP Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7uA
19:18	R/W	0x3	ADC2_PGA_CTRL_RCM ADC2 PGA Common Mode Input Impedance Control for MICIN 0: 100 kΩ 1: 75 kΩ 2: 50 kΩ 3: 25 kΩ
17:16	R/W	0x0	ADC2_PGA_IN_VCM_CTRL ADC2 PGA Common-Mode Voltage Control 0: 900mV 1: 800mV 2: 750mV 3: 700mV
15:13	/	/	/
12:8	R/W	0x0	ADC2_PGA_GAIN_CTRL ADC2 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB

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Offset: 0x0304			Register Name: ADC2_REG
Bit	R/W	Default	Description
7:6	R/W	0x1	ADC2_IOPAAF ADC2 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
5:4	R/W	0x1	ADC2_IOPSDM1 ADC2 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
3:2	R/W	0x1	ADC2_IOPSDM2 ADC2 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
1:0	R/W	0x1	ADC2_IOPMIC1 ADC2 OP MIC1 Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

4.1.6.114 0x0308 ADC3 Analog Control Register (Default Value:0x001C_0055)

Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
31	R/W	0x0	ADC3_EN ADC3 Channel Enable 0: Disable 1: Enable
30	R/W	0x0	MIC3_PGA_EN MIC3 PGA Enable 0: Disable 1: Enable

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Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
29	R/W	0x0	ADC3 Dither Control 0: New Dither Off 1: New Dither On
28:26	R/W	0x0	/
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 0: No Level 1: Min Level 2: Middle Level 3:Max Level
23:22	R/W	0x0	/
21:20	R/W	0x1	ADC3_OUTPUT_CURRENT ADC3 high gain OP Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7uA
19:18	R/W	0x3	ADC3_PGA_CTRL_RCM ADC3 PGA Common Mode Input Impedance Control for MICIN 0: 100 kΩ 1: 75 kΩ 2: 50 kΩ 3: 25 kΩ
17:16	R/W	0x0	ADC3_PGA_IN_VCM_CTRL ADC3 PGA Common-Mode Voltage Control 0: 900mV 1: 800mV 2: 750mV 3: 700mV
15:13	/	/	/

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Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
12:8	R/W	0x0	ADC3_PGA_GAIN_CTRL ADC3 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
7:6	R/W	0x1	ADC3_IOPAAF ADC3 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
5:4	R/W	0x1	ADC3_IOPSDM1 ADC3 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
3:2	R/W	0x1	ADC3_IOPSDM2 ADC3 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

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Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
1:0	R/W	0x1	ADC3_IOPMIC ADC3 OP MIC Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

4.1.6.115 0x0310 DAC Analog Control Register (Default Value:0x0455_0100)

Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
31	R/W	0x0	CURRENT_TEST_SELECT Internal Current Sink Test Enable (from MICIN3P pin) 0: Normal 1: For Debug
30:28	R/W	0x0	HEADPHONE_GAIN 000: -0dB 001: -6dB 010: -12dB 011: -18dB 100: -24dB 101: -30dB 110: -36dB 111:-42dB
27:26	R/W	0x1	IOPHPDRV HPDRVL/R OP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
25:24	R/W	0x0	CPLDO_VOLTAGE 00:0.9V 01:1.0V 10:1.1V 11:1.2V

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Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
23:22	R/W	0x1	OPDRV_CUR. OPDRV output stage current setting 00:6uA 01:7uA 10:8uA 11:9uA
21:20	R/W	0x1	IOPVRS VRA2 Buffer OP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
19:18	R/W	0x1	ILINEOUTAMPS LINEOUTL/R AMP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
17:16	R/W	0x1	IOPDACS OPDAC Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
15	R/W	0x0	DACL_EN DACL Enable 0: Disable 1: Enable
14	R/W	0x0	DACR_EN DACR Enable 0: Disable 1: Enable
13	R/W	0x0	LINEOUTLEN Left Channel LINEOUT Enable 0: Disable 1: Enable
12	R/W	0x0	LMUTE DACL to Left Channel LINEOUT Mute Control 0: Mute 1: Not mute

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Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
11	R/W	0x0	LINEOUTREN Right Channel LINEOUT Enable 0: Disable 1: Enable
10	R/W	0x0	RMUTE DACR to Right Channel LINEOUT Mute Control 0: Mute 1: Not mute
9:8	R/W	0x1	ICPLDO CPLDO Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
7	R/W	0x0	CPLDO_ENABLE 0: Disable 1:Enable
6:5	R/W	0x0	/
4:0	R/W	0x0	LINEOUT Volume Control, Total 30 level from 0x1F to 0x02 with the volume 0dB to -43.5dB, -1.5dB/step, mute when 00000 & 00001.

4.1.6.116 0x0314 DAC2 Analog Control Register (Default Value:0x0000_0000)

Offset: 0x0314			Register Name: DAC2_REG
Bit	R/W	Default	Description
31:18	R/W	0x0	/
17:16	R/W	0x0	CKDAC_DELAY_SET clock delay time after CKDAC 0: min 3: max
15	R/W	0x0	DACL/R_CHOPPER_ENABLE DACL/R chopper enable 0: chopper disable 1: chopper enable
14	R/W	0x0	DACL/R_CHOPPER_NOL_ENABLE DACL/R chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled

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Offset: 0x0314			Register Name: DAC2_REG
Bit	R/W	Default	Description
13:12	R/W	0x0	DACL/R_CHOPPER_CKSET DACL/R chopper clock frequency Fs:6.144MHz 0: 96 kHz 1: 192 kHz 2: 384 kHz 3: 768 kHz
11:10	R/W	0x0	DACL/R_CHOPPER_DELAY_SET Control DACL/R chopper clock delay time after CKDAC 0: Min 3: Max
9:8	R/W	0x0	DACL/R_CHOPPER_NOL_DELAY_SET Control DACL/R chopper clock non-overlapping time 0: Min when DAC_CHOPPER_NOL_ENABLE=1 3: Max when DAC_CHOPPER_NOL_ENABLE=1
7	R/W	0x0	LINEOUTL/R_CHOPPER_ENABLE LINEOUTL/R chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	LINEOUTL/R_CHOPPER_NOL_ENABLE LINEOUTL/R chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
5:4	R/W	0x0	LINEOUTL/R_CHOPPER_CKSET LINEOUTL/R chopper clock frequency Fs:6.144MHz 0: 96kHz 1: 192kHz 2: 384kHz 3: 768kHz
3:2	R/W	0x0	LINEOUTL/R_CHOPPER_DELAY_SET Control LINEOUTL/R chopper clock delay time after CKDAC 0: Min 3: Max
1:0	R/W	0x0	LINEOUTL/R_CHOPPER_NOL_DELAY_SET Control LINEOUTL/R chopper clock non-overlapping time 0: Min when LINEOUT_CHOPPER_NOL_ENABLE=1 3: Max when LINEOUT_CHOPPER_NOL_ENABLE=1

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4.1.6.117 0x0318 MICBIAS Analog Control Register (Default Value:0x4000_3030)

Offset: 0x0318			Register Name: MICBIAS_REG
Bit	R/W	Default	Description
31	R/W	0x0	/
30:28	R/W	0x4	SELDETADCFS Select sample interval of the ADC sample 000: 2ms … 100: 32ms … 111: 256ms
27:26	R/W	0x0	SELDETADCDB Select debounce time when jack removal 00: 128ms 01: 256ms 10: 512ms 11: 1024ms
25:24	R/W	0x0	SELDETADCBF Select the time to enable HBIAS before MICADC work 00: 2ms 01: 4ms 10: 8ms 11: 16ms
23	R/W	0x0	JACKDETEN Jack detect enable 0: Disable 1: Enable
22:21	R/W	0x0	SELDETADCDY Select the delay time to pull low the MICDET when jack removal 00: 0.5ms 01: 1ms 10: 1.5ms 11: 2ms
20	R/W	0x0	MICADCEN Microphone detect ADC enable 0: Disable 1: Enable
19	R/W	0x0	POPFREE When this bit is 0, HBIAS MICADC is controlled by register

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Offset: 0x0318			Register Name: MICBIAS_REG
Bit	R/W	Default	Description
18	R/W	0x0	Det Mode 0: Jack in pull low 1: Jack in pull high
17	R/W	0x0	AUTOPLEN Enable the function to auto pull low MICDET when jack removal 0: Disable 1: Enable
16	R/W	0x0	MICDETPL When this bit is 1and AUTOPLEN is 0, the MICDET is pull to GND
15	R/W	0x0	HMICBIASEN Headphone Microphone Bias Enable 0: Disable 1: Enable
14:13	R/W	0x1	HBIASSEL HMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.55V
12	R/W	0x1	HMIC BIAS chopper enable 0: Disable 1: Enable
11:10	R/W	0x0	HMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1MHz 11: 2MHz
9:8	R/W	0x0	/
7	R/W	0x0	MMICBIASEN Master Microphone Bias Enable 0: Disable 1: Enable
6:5	R/W	0x1	MBIASSEL MMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V

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Offset: 0x0318			Register Name: MICBIAS_REG
Bit	R/W	Default	Description
4	R/W	0x1	MMIC BIAS chopper enable 0: Disable 1: Enable
3:2	R/W	0x0	MMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1MHz 11: 2MHz
1:0	R/W	0x0	/

4.1.6.118 0x031C Ramp Control Register (Default Value:0x0018_0000)

Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
31	R/W	0x0	RAMP RISE INT En 0: Enable 1:Disable
30	R/W1C	0x0	RAMP RISE INT RK Increase Upward Finish and Rampen Pull Down Instruction 0: No Pending IRQ 1: Ramp Rise Finish Pending Interrupt Write '1' to clear this interrupt
29	R/W	0x0	RAMP FALL INT EN 0: Enable 1:Disable
28	R/W1C	0x0	RAMP FALL INT RK Downward Decrease Finish and Rampen Pull Down Instruction 0: No Pending IRQ 1: Ramp Fall Finish Pending Interrupt Write '1' to clear this interrupt
27:25	/	/	/
24	R/W	0x0	RAMP SOFT RESET 0: Disable 1:Enable
23:21	/	/	/

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Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
20:16	R/W	0x18	RAMP_CLK_DIV_M Analog Ramp Clk Div Freq Value: M (from 0 to 31, Default:24). Ana_Ramp_Clk= 24MHz/(M+1) Default Ramp Clk Freq: 24MHz/(24+1)=960 kHz
15	R/W	0x0	HP PULL OUT EN 0: Disable 1:Enable
14:12	R/W	0x0	RAMP HOLD STEP 000: 9600 001: 19200 010: 38400 011: 76800 100: 96000 101: 115200 110: 153600 111: 192000 Ramp Hold Time = Ramp Hold Step/Ramp Clk Freq When Ramp Clk Freq equal to 960 kHz, Corresponding Ramp Hold time of each gear: 000: 9600/960 kHz=10ms 001: 19200/960 kHz=20ms 010: 38400/960 kHz=40ms 011: 76800/960 kHz=80ms 100: 96000/960 kHz=100ms 101: 115200/960 kHz=120ms 110: 153600/960 kHz=160ms 111: 192000/960 kHz=200ms
11:10	/	/	/
9:8	R/W	0x0	GAP STEP 00: ramp step 01: ramp step*2 10: ramp step*3 11: ramp step*4
7	/	/	/

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Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
6:4	R/W	0x0	RAMP STEP RK Frequency Gear, Control Ramp Rise/Fall Total Time 000: 20 001: 30 010: 40 011: 60 100: 80 101: 120 110: 160 111: 240 Ramp Rise/Fall Total Time = (Ramp Step/Ramp Clk Freq) *4096 When Default Ramp Clk Freq equal to 960 kHz, Corresponding time of each gear: 000: (20/960 kHz) *4096=85.3ms 001: (30/960 kHz) *4096=128ms 010: (40/960 kHz) *4096=170.6ms 011: (60/960 kHz) *4096=256ms 100: (80/960 kHz) *4096=341.3ms 101: (120/960 kHz) *4096=512ms 110: (160/960 kHz) *4096=682.6ms 111: (240/960 kHz)*4096=1024ms
3	R/W	0x0	RMD_EN Ramp Manual Down Enable 0: Disable 1: Enable
2	R/W	0x0	RMU_EN Ramp Manual Up Enable 0: Disable 1: Enable
1	R/W	0x0	RMC_EN Ramp Manual Control Enable 0: Disable, and there is no signal output for DAC. 1: Enable
0	R/W	0x0	RD_EN Ramp Digital Enable 0: Disable 1: Enable

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4.1.6.119 0x0320 BIAS Analog Control Register (Default Value:0x0000_0080)

Offset: 0x0320			Register Name: BIAS_REG
Bit	R/W	Default	Description
31:8	R/W	0x0	/
7:0	R/W	0x80	BIASDATA Bias Current Register Setting Data This 8-bit register is not controlled by the AUDIO CODEC reset, only controlled by the system bus reset.

4.1.6.120 0x0324 HEADPHONE Analog Control Register (Default Value:0x8080_0C44)

Offset: 0x0324			Register Name: HP_REG
Bit	R/W	Default	Description
31:24	R/W	0x80	HPRCALIVERIFY Right Headphone calibration Setting Data
23:16	R/W	0x80	HPLCALIVERIFY Left Headphone calibration Setting Data
15	R/W	0x0	HPPA_EN Right & Left Headphone PA Enable 0: Disable; 1: Enable
14:12	R/W	0x0	/
11	R/W	0x1	HPINPUTENABLE When this bit is write to 0, the input stage of headphone disabled
10	R/W	0x1	HPOUTPUTENABLE When this bit is write to 0, the output stage of headphone disabled
9:8	R/W	0x0	HPPA_DEL Headphone delay time when start up 00: 4ms 01: 8ms 10: 16ms 11: 32ms
7:6	R/W	0x1	CP_CLKS Charge Pump Clock select 00: 250k 01: 330k 10: 660k 11: 1000k

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Offset: 0x0324			Register Name: HP_REG
Bit	R/W	Default	Description
5	R/W	0x0	HPCALIMODE HEADPHONE calibration equilibration MODE select 0: equilibration mode 1: no equilibration
4	R/W	0x0	HPCALIVERIFY HEADPHONE calibration in verify mode enable 0: Disable; 1: Enable
3	R/W	0x0	HPCALIFIRST When this bit is write to 1 , HEADPHONE Calibration once before enable
2:0	R/W	0x4	HPCALICKS HEADPHONE Calibration clock frequency select 000: 4 … 100: 64 … 111: 512

4.1.6.121 0x0328 HMIC Control Register (Default Value: 0x0000_0008)

Offset: 0x0328			Register Name: HMIC_CTRL
Bit	R/W	Default	Description
31:23	/	/	/
22:21	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11 : Down by 8, 16Hz
20:16	R/W	0x0	MDATA_Threshold The threshold of MIC_DET pending When HMIC_M is not set, and the deviation between the current obtained value and the threshold exceeds MDATA_Threshold_Debounce at twice time, the interrupt is pending.

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Offset: 0x0328			Register Name: HMIC_CTRL
Bit	R/W	Default	Description
15:14	R/W	0x0	HMIC_SF HMIC Smooth Filter setting The compare value of MIC interrupt is the value after Smooth Filter. 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8
13:10	R/W	0x0	HMIC_M Debounce when the MIC Key down or up. 0000:1 samlpe data 0001:2 samlpe data ... 1111:16 samlpe data
9:6	R/W	0X0	HMIC_N Debounce when earphone plug in or pull out 125ms-2s 0000:125ms 0001:250ms ... 1111:2s
5:3	R/W	0x1	MDATA_Threshold_Debounce 000:0 001:1 010:2 011:3 100:4 101:5 110:6 111:7 11: Reserve (default 1) When a MDATA value is added, if the variation is beyond this threshold, the MIC interrupt will be pending
2	R/W	0x0	JACK_OUT_IRQ_EN MIC Detect Interrupt Set 0: disable 1 : enable
1	R/W	0x0	JACK_IN_IRQ_EN MIC Detect Interrupt Set 0: disable 1 : enable

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Offset: 0x0328			Register Name: HMIC_CTRL
Bit	R/W	Default	Description
0	R/W	0x0	MIC_DET_IRQ_EN MIC Detect Interrupt Set 0: Disable 1:Enable

4.1.6.122 0x032C HMIC Status Register (Default Value: 0x0000_6000)

Offset: 0x032C			Register Name: HMIC_STS
Bit	R/W	Default	Description
31:15	/	/	/
14:13	R/W	0x3	MDATA_DISCARD After MIC DATA data receiving, the first N-data will be discarded. N defined as follows: 00: 0; None discarded 01: 1; 1-data discarded 10: 2; 2-data discarded 11: 4; 4-data discarded
12:8	R	0x0	HMIC_DATA HMIC Average Data
7:5	/	/	/
4	R/W1C	0x0	JACK_DET_OIRQ Jack output detect Pending interrupt 0: No Pending IRQ 1: Pending IRQ Writing 1 clear pending
3	R/W1C	0x0	JACK_DET_IIRQ Jack input detect pending interrupt 0: No Pending IRQ 1: Pending IRQ Writing 1 clear pending
2:1	/	/	/
0	R/W1C	0x0	MIC_DET_ST. MIC Detect Pending interrupt 0: No pending IRQ 1: Pending IRQ Writing 1 clear pending

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4.1.6.123 0x0348 POWER Analog Control Register (Default Value:0x8800_3711)

Offset: 0x0348			Register Name: POWER_REG
Bit	R/W	Default	Description
31	R/W	0x1	ALDO_EN 0: Disable 1: Enable
30	R/W	0x0	/
29	R/W	0x0	VAR1SPEEDUP_DOWN_Further_CTRL VRA1Speedup Down Further Control in AUDIO CODEC Analog 0: Digital Signal Interface Pin l_vra1speedup (vra1_speedup_down) Normally Control VRA1 Speedup down 1:Manual Control Finish VRA1 Speedup down, Ignore Digital Signal Interface Pin l_vra1speedup (vra1_speedup_down) Control
28	R/W	0x0	/
27	R/W	0x1	LDO for VRP Chopper Enable 0: Disable 1: Enable
26:25	R/W	0x0	LDO for VRP chopper clock select 00: 250 kHz 01: 500 kHz 10: 1MHz 11: 2MHz
24	R/W	0x0	VRP_LDO_EN LDO for VRP Enable Control 0: Disable 1:Enable
23:17	R/W	0x0	/
16	R	0x0	AVCCPOR AVCCPOR Monitor
15	R/W	0x0	BG_BUFFER_DISABLE 0: Enable 1: Disable

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Offset: 0x0348			Register Name: POWER_REG
Bit	R/W	Default	Description
14:12	R/W	0x3	ALDO_OUTPUT_VOLTAGE ALDO Output Voltage Control 0: 2.03 V 4: 1.73 V 1: 1.95 V 5: 1.67 V 2: 1.87 V 6: 1.61 V 3: 1.80 V 7: 1.56V When the BG output voltage is 0.9V, the voltages above are the values of this bit. When the BG output voltage is not 0.9V, it is needed to convert the above voltages according to the corresponding ratio to get the actual ALDO ouput voltages.
11:8	R/W	0x7	BG_ROUGH_TRIM BG Output ROUGH Voltage Rough Trimming Every step is 25 mV. The BG output voltage range is from 710 mV to 1085 mV. The default output voltage is 885 mV.
7:0	R/W	0x11	BG_FINE_TRIM BG Output Voltage Fine Trimming Only lower 6-bit is used and every step is 0.5 mV. The BG output voltage range is from 0 to 32.5 mV. The default output voltage is 15 mV. **Note: This register is only controlled by system bus clock and reset.**

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4.2 I2S/PCM

4.2.1 Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format, and TDM mode format.

The I2S/PCM controller includes the following features:

- Four I2S/PCM external interfaces (I2S0, I2S1, I2S2, and I2S3) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- FIFOs for transmitting and receiving data
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width ≤ 24.576 MHz)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

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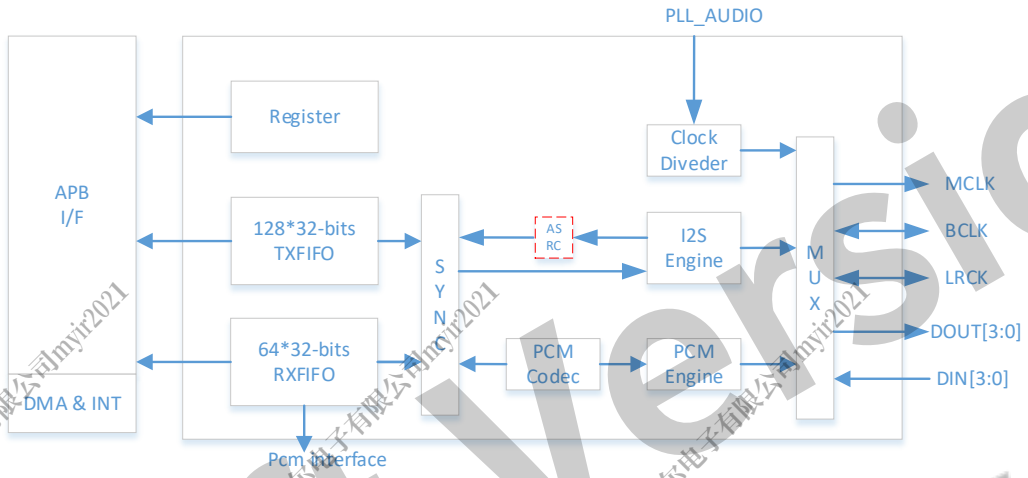
4.2.2 Block Diagram

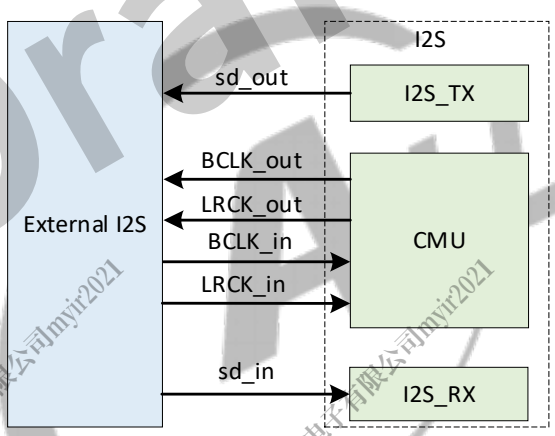
The following figure shows the functional block diagram of the I2S/PCM interface.

Figure 4-14 I2S/PCM Interface System Block Diagram



The following figure shows the typical application of the I2S/PCM interface.

Figure 4-15 Typical Application of I2S/PCM Interface



The I2S/PCM interface system integrates one I2S_TX and one I2S_RX.

- The I2S_TX is for playing music in I2S or PCM format.
- The I2S_RX is for receiving data in I2S or PCM format.
- When the I2S works in the master mode, the external I2S module provides BCLK_in and LRCK_in for the clock management unit (CMU), and the I2S_TX and I2S_RX work with the two external clocks.
- When the I2S works in the slave mode, the CMU provides clocks BCLK_out and LRCK_out for the external I2S module, and the I2S_TX and I2S_RX work with the internal clocks.

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4.2.3 Functional Description

4.2.3.1 External Signals

The following table describes the external signals of the I2S/PCM interface.

LRCK and BCLK are bidirectional I/O. When the I2S/PCM interface works in the Master mode, LRCK and BCLK are output pins. When the I2S/PCM interface works in the Slave mode, LRCK and BCLK are input pins.

MCLK is an output pin for external devices. DOUT are the serial data output pins and DIN are the serial data input pins. For details about General Purpose I/O port, refer to section 8.6 GPIO.

Table 4-2 I2S/PCM External Signals

Signal Name	Description	Type
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[3:0]	I2S0/PCM0 Serial Data Input Channel [3:0]	I
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM01Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S2-DOUT[3:0]	I2S2/PCM2 Serial Data Output Channel [3:0]	O
I2S2-DIN[3:0]	I2S2/PCM2 Serial Data Input Channel [3:0]	I
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S3-DOUT[3:0]	I2S3/PCM3 Serial Data Output Channel [3:0]	O
I2S3-DIN[3:0]	I2S3/PCM3 Serial Data Input Channel [3:0]	I
I2S3-MCLK	I2S3 Master Clock	O
I2S3-LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3-BCLK	I2S3/PCM3 Bit Rate Clock	I/O

4.2.3.2 Clock Sources

The following table describes the clock sources for I2S/PCM. For clock setting, configurations, and gating information, refer to section 2.13 Power Reset Clock Management (PRCM).

Table 4-3 I2S/PCM Clock Sources

Clock Source	Description	Module
PLL_AUODIO(4x)	By default, PLL_AUDIO(4X) is 98.2856 MHz.	CCU

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Clock Source	Description	Module
PLL_AUDIO1 (DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1 (DIV2) is 1536 MHz, and PLL_AUDIO1 (DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1 (DIV5)		

4.2.3.3 Timing Diagram

The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode, and TDM mode. The software can select the modes by setting I2S/PCM_CTL. The following figures describe the waveforms for SYNC, BCLK, DOUT, and DIN in different modes.

Each sampling period contains an LRCK. The low level of LRCK is the left channel corresponding to the even slots, and the high level is the right channel corresponding to the odd slots. Each slot is the sampling point of a mono channel. The sampling period can support the transmission of 2/4/8/16 slots. The BCLK corresponds to the serial data bit.

Figure 4-16 I2S Standard Mode Timing

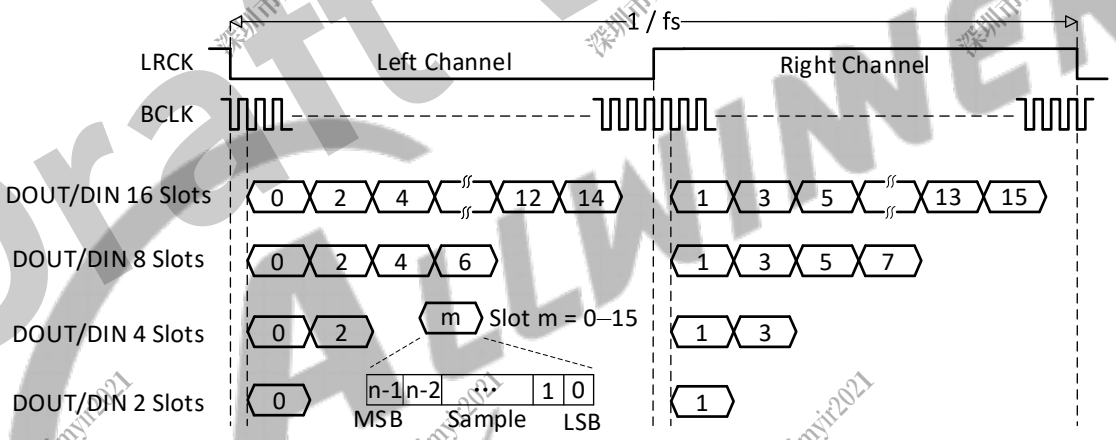

Figure 4-17 Left-Justified Mode Timing

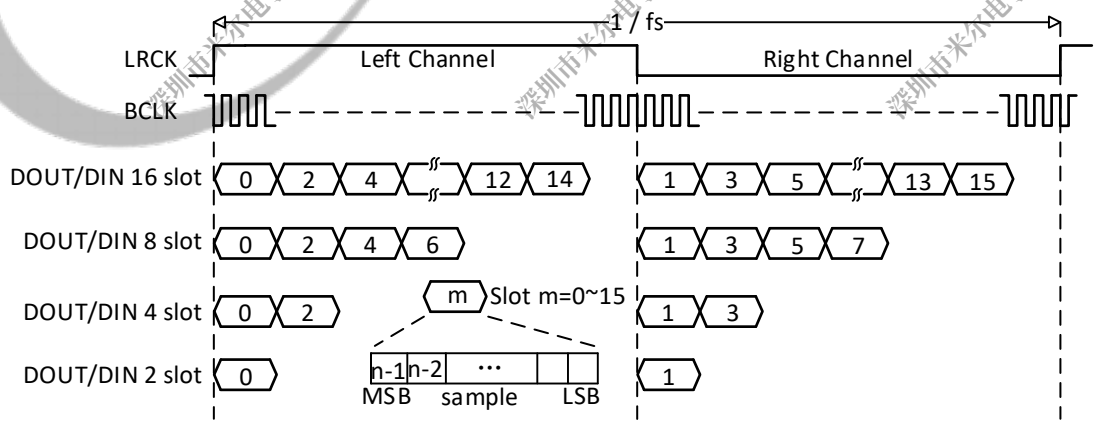

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Figure 4-18 Right-Justified Mode Timing

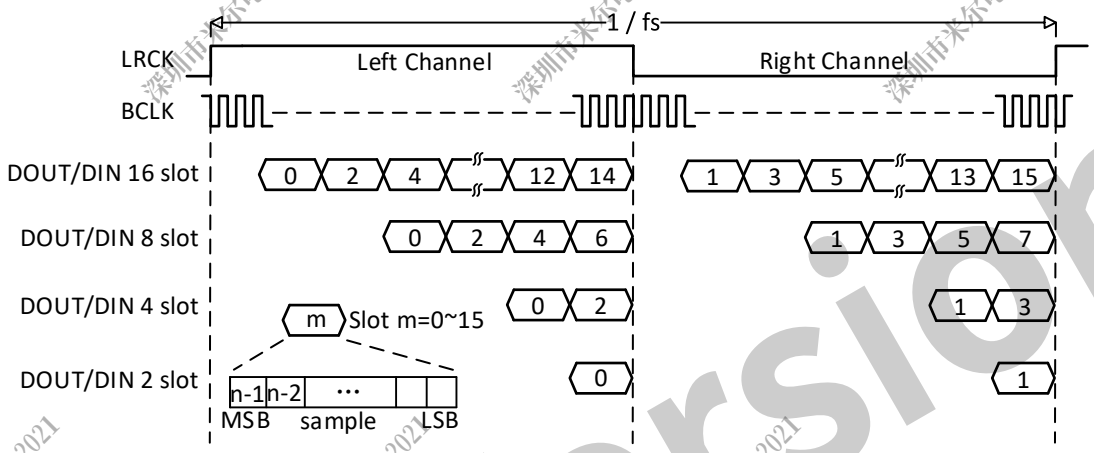


Figure 4-19 PCM Long Frame Mode Timing

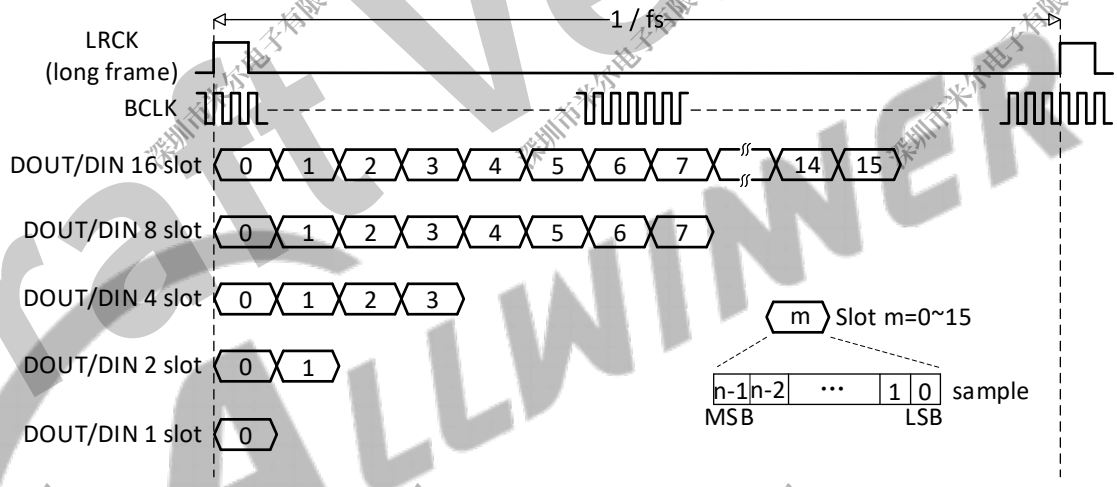
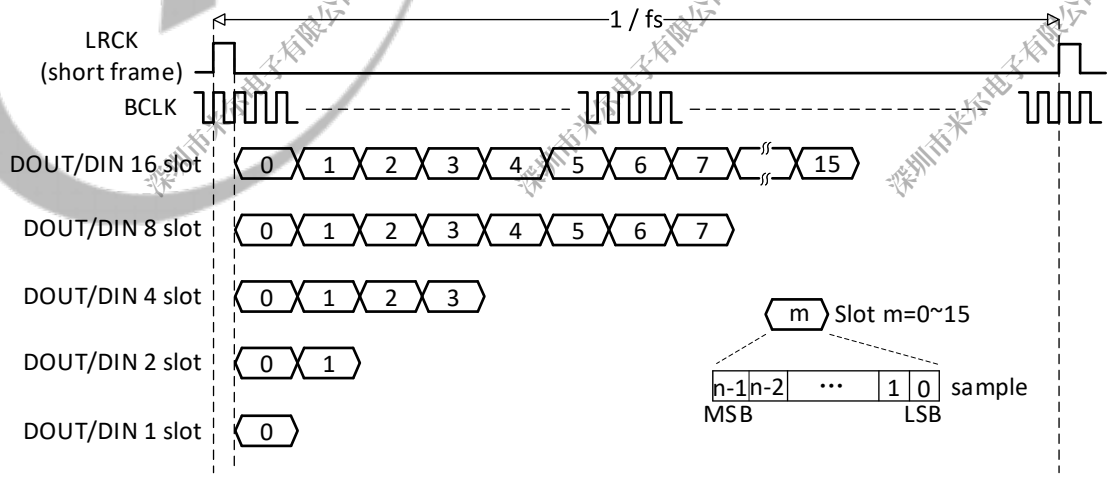


Figure 4-20 PCM Short Frame Mode Timing (one BCLK cycle)



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4.2.3.4 ASRC

The ASRC module supports sampling rate conversion between the up-sampling and down-sampling. The ASRC also supports sampling rate conversion between dual-channel audio data, and the size of the sampling data is up to 24 bits.

The ASRC module has the following features:

- Typical THD + N: -130 dB (Range: -125 dB to -139 dB)
- Supports sampling rate conversion between the up-sampling and down-sampling to implement the sampling rate conversion for stereo data
  - The up-sampling ratio ranges from 1 to 7.5x
  - The down-sampling ratio ranges from 8 to 1x
- Supports sampling rate conversion between two identical frequencies
- Sampling rate for both the input and output range is from 8 kHz to 192 kHz and can be decimal
- Sampling rate can be configured manually or via adaptive generation
- The ASRC input is connected to I2S RX_FIFO_WDATA [31:8], and the input data is 24-bit MSB big-endian. For the input data that is less than 24 bits, use zeros to pad out the values at the low bits instead of high bits
- The ASRC needs some time to calculate the result. The output outsamplea/b will keep 0 during the calculation, and then change to the valid value when the result comes out

Calculating the ASRC Latency

Calculate the ASRC up-sampling and down-sampling latency according to the following formulas.

$$\text{Upsampling Latency} = \text{Phase Delay} + \text{FIFO Delay} = 32 + 16 = 48 \text{ Input Sample Periods}$$

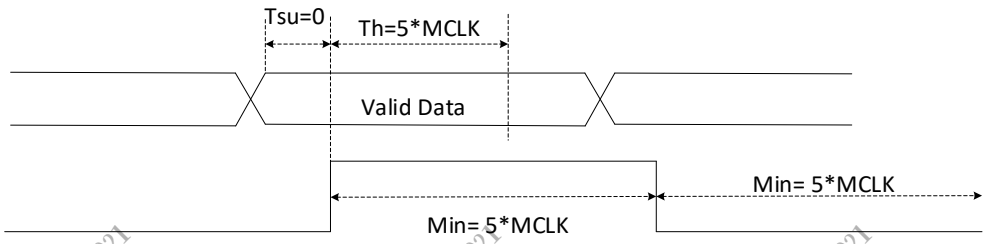
$$\text{Downsampling Latency} = \text{Phase Delay} + \text{FIFO Delay} = (32 * f_{sout}/f_{sin}) + 16 \text{ Input Sample Periods}$$

ASRC Timing

The MCLK samples the input clock CLKIN to generate pulse signals.

The following figure shows the timing requirements for the inputs.

Figure 4-21 Timing Requirements for Inputs



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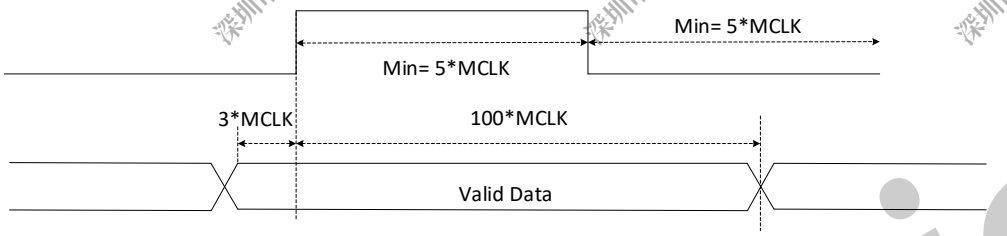
The following figure shows the timing requirements for the outputs.

Figure 4-22 Timing Requirements for Outputs



For the up-sampling, $F_{MCLK} = F_{sout} * 1350$

For the down-sampling, $F_{MCLK} = F_{sin} * 0.30 + F_{sout} * 295$

The following table provides the proper values of MCLK in MHz with different Fsin and Fsout in kHz.

Table 4-4 Proper MCLK Values with Different Fsin and Fsout

Fsin \ Fsout	32	44.1	48	88.2	96	144	192
32	45	60	65	120	130	195	260
44.1	55	60	65	120	130	195	260
48	60	65	65	120	130	195	260
88.2	105	105	110	120	130	195	260
96	110	115	115	125	130	195	260
144	160	165	165	175	180	195	260
192	210	215	215	225	230	245	260

NOTE

The units for Fsin and Fsout are kHz and MCLK is MHz.

4.2.3.5 Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup, and Enable/Disable module.

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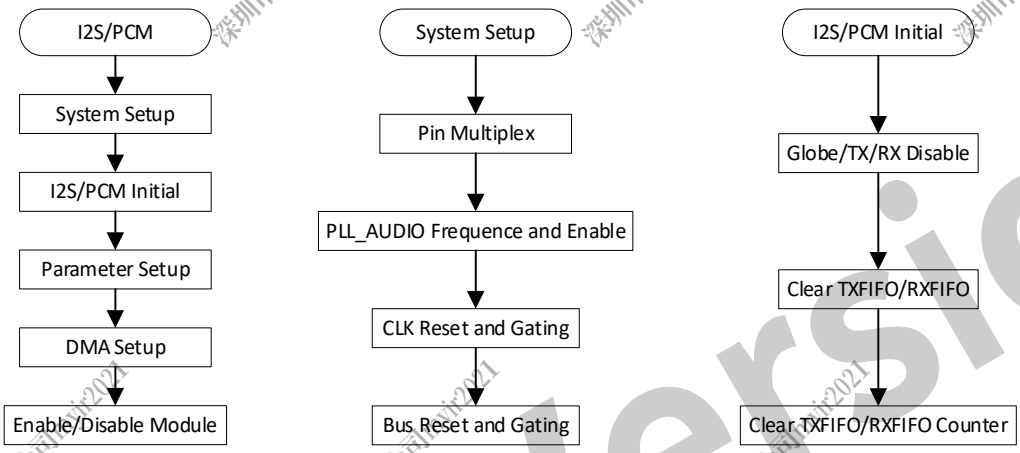
The following figure shows the whole operation flow of I2S/PCM.

Figure 4-23 I2S/PCM Operation Flow



Step 1 System Setup and I2S/PCM Initialization

The clock source for the I2S/PCM should be followed. Firstly, disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE] in the CCU or PRCM. Secondly, set up the frequency of the PLL_AUDIO in the PLL_AUDIOx Control Register. After that, enable the I2S/PCM gating through the I2S/PCMx_CLK_REG when you checkout that the PLL_AUDIOx Control Register[LOCK] becomes to 1. At last, reset and enable the I2S/PCM bus gating by setting I2S_BGR_REG.

After the system setup, the register of I2S/PCM can be setup. Firstly, initialize the I2S/PCM. You should close the Globe Enable bit (I2S/PCM_CTL[0]), Transmitter Block Enable bit (I2S/PCM_CTL[2]), and Receiver Block Enable bit (I2S/PCM_CTL[1]) by writing 0. After that, clear the TX/RX FIFO by writing 0 to the bit[25:24] of I2S/PCM_FCTL. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to I2S/PCM_TXCNT and I2S/PCM_RXCNT.

Step 2 Parameter Setup and DMA Setup

First, you can set up the I2S/PCM of master and slave. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of the slot, the channel slot number, and the trigger level, and so on. The setup of the register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the section 2.8 DMA Controller (DMAC). In this module, you just enable the DRQ.

Step 3 Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing I2S/PCM_CTL[TXEN]/I2S/PCM_CTL[RXEN]. After that, enable I2S/PCM by writing 1 to I2S/PCM_CTL[Globe Enable]. Write 0 to the Globe Enable bit to disable I2S/PCM.

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4.2.4 Programming Guidelines

4.2.4.1 Application Example of Processing ASRC Input and Output Data

The following example shows a typical application of ASRC: the input data is 24-bit valid, and the output data is a 32-bit data whose highest 24 bits are valid output and the lowest eight bits are padded out with zeros.

To implement the application, configure the sample resolution and slot width as 32 bits. Follow the steps below:

Step 1 For the input register: 0x04 [6:4] sample_res = 3`h7, 0x04 [2:0] slot_width = 3`h7.

The format of the input data: 32'hXXXXXXXX, where, bit [31] is the MSB and X is the valid data bit.

Step 2 For the output register: 0x04 [6:4] sample_res = 3`h7, 0x04 [2:0] slot_width = 3`h7

The format of the output data: 32'hXXXXXX00, where, bit [31] is the MSB, X is the valid data bit, and bit [7:0] are the padded zeros.

4.2.4.2 Converting the Sampling Rate with ASRC

Converting a 48 kHz sampling rate to 16 kHz is the most common scenario in actual applications. Follow the steps below to convert the sampling rate from 48 kHz to 16 kHz for the 32-bit data.

Step 1 Configure the PLL_AUDIO Register

a) Configure PLL_AUDIO_CTRL_REG[31:0] as 0x8814AB01. That is, PLL_AUDIO = 24*(171+1)/ (1+1)/ (1+0)/ (1+20) = 98.286 MHz. According to the relationship among the Fsin, Fsout, and MCLK, the MCLK should be greater than 60 MHz. In the simulation phase, the HOSC frequency is 25 MHz, so the output frequency of PLL_AUDIO should be 25*(171+1)/ (1+1)/ (1+0)/ (1+20) = 102.381 MHz. In the IC test phase, configure the frequency of PLL_AUDIO according to its actual output frequency.

b) It is suggested that you configure the ASRC MCLK as an equal-duty-cycle signal. You can specify an odd number for bit[21:16] (PLL_POST_DIV_P) of PLL_AUDIO_CTRL_REG to get an equal-duty-cycle output clock of PLL_AUDIO.

c) Configure bit[25:24] of I2S3_ASRC_CLK_REG as 0x00 to select the PLL_AUDIO(4X).

Step 2 Configure the I2S Registers

a) Configure bit[7:4] (BCLKDIV) of I2S/PCM_CLKD as 4`h9, that is, the frequency of BCLK will be 98.286 MHz/32 = 3.072 MHz.

b) Configure bit[17:8] (LRCK_PERIOD) of I2S/PCM_FMT0 as 10`h1F. That is, the LRCK_PERIOD width is configured as 32 BLCKs and can generate the ASRC CLKIN with a 48 kHz sampling rate. ($\frac{3.072\,\text{MHz}}{32*2}=48\,\text{kHz}$)

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c) Configure bit[6:4] (Sample Resolution bits) of I2S/PCM_FMT0 as 3`h7 to specify the sample resolution as 32-bit.

d) Configure bit[2:0] (Slot Width bits) of I2S/PCM_FMT0 as 3`h7 to specify the slot width as 32-bit.

Step 3 Configure the ASRC Registers

a) Configure bit[16] (clock gate) of MCLKCFG as 1`h1 to open the clock gating.

b) Configure bit[3:0] (division factor) of MCLKCFG as 1`h1 to specify the division factor as 1.

c) Configure bit[20] (clock gate) of FsoutCFG as 1`h1 to open the clock gating.

d) Configure bit[19:16] (clock select) of FsoutCFG as 4`h0 to select I2S0_ASRC_CLK as the clock source.

e) Configure bit[7:4] (the first division factor) of FsoutCFG as 16`h13 to configure the first division factor as 128.

f) Configure bit[3:0] (the second division factor) of FsoutCFG as 16`h10 to configure the second division factor as 48.

g) Configure the ASRC ratio.

To configure the ASRC ratio manually, configure bit[31] (Manual Configuration of ASRC Ratio Enable) of ASRCMANCFG as 1`h1 to enable the manual configuration of ASRC ratio. Configure bit[25:0] of ASRCMANCFG as 26`h155555 to specify the ratio value as 0x155555. The calculation formula for the ratio value: Dec2Hex (Fsout/Fsin) *222). In this example, Fsout/Fsin = 16 kHz/48 kHz =1/3, then the ratio is 0x155555.

To configure the ASRC ratio automatically, configure bit[31] (Manual Configuration of ASRC Ratio Enable) of ASRCMANCFG as 1`h0 to enable the automatic configuration of ASRC ratio. Then the system will automatically calculate the ratio value based on the MCLK, Fsout, and Fsin.

4.2.5 Register List

Module Name	Base Address	Comments
I2S|PCM0	0x07112000	Use for Speech Input.
I2S|PCM1	0x07113000	I2S|PCM1 register is the same with I2S|PCM0 .
I2S|PCM2	0x07114000	I2S|PCM2 register is the same with I2S|PCM0.
I2S|PCM3	0x07115000	I2S|PCM3 register is the same with I2S|PCM0.

Register Name	Offset	Description
I2S|PCM_CTL	0x0000	I2S|PCM Control Register
I2S|PCM_FMT0	0x0004	I2S|PCM Format Register 0
I2S|PCM_FMT1	0x0008	I2S|PCM Format Register 1

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Register Name	Offset	Description
I2S|PCM_ISTA	0x000C	I2S|PCM Interrupt Status Register
I2S|PCM_RXFIFO	0x0010	I2S|PCM RXFIFO Register
I2S|PCM_FCTL	0x0014	I2S|PCM FIFO Control Register
I2S|PCM_FSTA	0x0018	I2S|PCM FIFO Status Register
I2S|PCM_INT	0x001C	I2S|PCM DMA And Interrupt Control Register
I2S|PCM_TXFIFO	0x0020	I2S|PCM TXFIFO Register
I2S|PCM_CLKD	0x0024	I2S|PCM Clock Divide Register
I2S|PCM_TXCNT	0x0028	I2S|PCM TX Sample Counter Register
I2S|PCM_RXCNT	0x002C	I2S|PCM RX Sample Counter Register
I2S|PCM_CHCFG	0x0030	I2S|PCM Channel Configuration Register
I2S|PCM_TX0CHSEL	0x0034	I2S|PCM TX0 Channel Select Register
I2S|PCM_TX1CHSEL	0x0038	I2S|PCM TX1 Channel Select Register
I2S|PCM_TX2CHSEL	0x003C	I2S|PCM TX2 Channel Select Register
I2S|PCM_TX3CHSEL	0x0040	I2S|PCM TX3 Channel Select Register
I2S|PCM_TX0CHMAP0	0x0044	I2S|PCM TX0 Channel Mapping Register0
I2S|PCM_TX0CHMAP1	0x0048	I2S|PCM TX0 Channel Mapping Register1
I2S|PCM_TX1CHMAP0	0x004C	I2S|PCM TX1 Channel Mapping Register0
I2S|PCM_TX1CHMAP1	0x0050	I2S|PCM TX1 Channel Mapping Register1
I2S|PCM_TX2CHMAP0	0x0054	I2S|PCM TX2 Channel Mapping Register0
I2S|PCM_TX2CHMAP1	0x0058	I2S|PCM TX2 Channel Mapping Register1
I2S|PCM_TX3CHMAP0	0x005C	I2S|PCM TX3 Channel Mapping Register0
I2S|PCM_TX3CHMAP1	0x0060	I2S|PCM TX3 Channel Mapping Register1
I2S|PCM_RXCHSEL	0x0064	I2S|PCM RX Channel Select Register
I2S|PCM_RXCHMAP0	0x0068	I2S|PCM RX Channel Mapping Register0
I2S|PCM_RXCHMAP1	0x006C	I2S|PCM RX Channel Mapping Register1
I2S|PCM_RXCHMAP2	0x0070	I2S|PCM RX Channel Mapping Register2
I2S|PCM_RXCHMAP3	0x0074	I2S|PCM RX Channel Mapping Register3
MCLKCFG	0x0080	I2S|PCM ASRC MCLK Configure Register
FsoutCFG	0x0084	I2S|PCM ASRC Out Sample Configure Register
FsinEXTCFG	0x0088	I2S|PCM In Sample Pluse Extend Configure Register
ASRCEN	0x008C	I2S|PCM ASRC Enable Configure Register
ASRCMANCFG	0x0090	I2S|PCM ASRC Manual Configure Register
ASRCRATIOSTAT	0x0094	I2S|PCM ASRC Ratio State Configure Register
ASRCFIFOSTAT	0x0098	I2S|PCM ASRC FIFO State Configure Register
ASRCMBISTCFG	0x009C	I2S|PCM ASRC MBIST Test Configure Register
ASRCMBISTSTA	0x00A0	I2S|PCM ASRC MBIST Test State Configure Register

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4.2.6 Register Description

4.2.6.1 0x0000 I2S|PCM Control Register (Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S|PCM_CTL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START Only if RX_SYNC_EN set 1, RX_SYNC_EN_START can take effect. Audio Codec / I2S0 / I2S1 / I2S2/I2S3/ DMIC /OWA RX Synchronize Enable Start. 0: Disable 1: Enable
20	R/W	0x0	RX_SYNC_EN I2S RX Synchronize Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x1	BCLK_OUT Bit Clock Direction Select 0: Input 1: Output
17	R/W	0x1	LRCK_OUT LR Clock Direction Select 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	DOUT3_EN Data3 Output Enable 0: Disable, Hi-Z State 1: Enable
10	R/W	0x0	DOUT2_EN Data2 Output Enable 0: Disable, Hi-Z State 1: Enable
9	R/W	0x0	DOUT1_EN Data1 Output Enable 0: Disable, Hi-Z State 1: Enable

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Offset: 0x0000			Register Name: I2S|PCM_CTL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	DOUT0_EN Data0 Output Enable 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	DOUT_MUTE_EN Data Output Mute Enable 0: Normal Transfer 1: Force DOUT to Output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 0: PCM Mode offset 0: Long Frame offset 1: Short Frame 1: Left Mode offset 0: LJ Mode offset 1: I2S Mode 2: Right-Justified Mode 3: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When Set '1' , Connecting the DOUT with the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

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4.2.6.2 0x0004 I2S|PCM Format Register 0 (Default Value: 0x0000_0033)

Offset: 0x0004			Register Name: I2S|PCM_FMT0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	LRCK_WIDTH (Only Apply in PCM Mode) LRCK Width 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When Apply in I2S / Left-Justified / Right-Justified Mode: 0: Left Channel When LRCK is Low 1: Left Channel When LRCK is High When Apply in PCM Mode: 0: PCM LRCK Asserted at the Negative Edge 1: PCM LRCK Asserted at the Positive Edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM Mode: Number of BCLKs within (Left + Right) channel width. I2S / Left-Justified / Right-Justified Mode: Number of BCLKs within each individual channel width (Left or Right). N+1 For example: N = 7: 8 BCLKs width ... N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY BCLK Polarity Select 0: Normal Mode, DOUT Drive Data at Negative Edge 1: Invert Mode, DOUT Drive Data at Positive Edge

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Offset: 0x0004			Register Name: I2S|PCM_FMT0
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER Edge Transfer 0: DOUT Drive Data and DIN Sample Data at the Different BCLK Edge 1: DOUT Drive Data and DIN Sample Data at the Same BCLK Edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN Sample Data at Positive Edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN Sample Data at Positive Edge.
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

4.2.6.3 0x0008 I2S|PCM Format Register 1 (Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S|PCM_FMT1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

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Offset: 0x0008			Register Name: I2S|PCM_FMT1
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	RX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or Audio Gain Padding at LSB Position 01: Sign Extension at MSB Position 10: Reserved 11: Transfer 0 after each Sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits U-law 11: 8-bits A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits U-law 11: 8-bits A-law

4.2.6.4 0x000C I2S|PCM Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S|PCM_ISTA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Underrun Pending Interrupt Write '1' to clear this interrupt.

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Offset: 0x000C			Register Name: I2S|PCM_ISTA
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Overrun Pending Interrupt Write '1' to clear this interrupt.
4	R	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No Pending IRQ 1: TXFIFO Empty Pending Interrupt When Data in TXFIFO are Less than TX Trigger Level
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: RXFIFO Underrun Pending Interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No Pending IRQ 1: RXFIFO Overrun Pending IRQ Write '1' to clear this interrupt.
0	R	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ When Data in RXFIFO are More than RX Trigger Level

4.2.6.5 0x0010 I2S|PCM RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S|PCM_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

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4.2.6.6 0x0014 I2S|PCM FIFO Control Register (Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S|PCM_FCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable Only if TXEN set 1, HUB_EN can take effect. Audio Codec / I2S0/ I2S1/ I2S2/ OWA TXFIFO Hub Enable. 0: Disable 1: Enable
30:26	/	/	/
25	R/WAC	0x0	FTX Flush TX FIFO Write '1' to flush TXFIFO, self-clear to '0'.
24	R/WAC	0x0	FRX Flush RX FIFO Write '1' to flush RXFIFO, self-clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid Data at the MSB of TXFIFO Register 1: Valid Data at the LSB of TXFIFO Register Example for 20-bits Transmitted Audio Sample: Mode 0: TXFIFO [31:0] = {APB_WDATA [31:12], 12'h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}

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Offset: 0x0014			Register Name: I2S|PCM_FCTL
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO Register 01: Expanding Received Sample Sign Bit at MSB of RXFIFO Register 10: Truncating Received Samples at High Half-word of RXFIFO Register and Low Half-word of RXFIFO Register is Filled by '0' 11: Truncating Received Samples at Low Half-word of RXFIFO Register and High Half-word of RXFIFO Register is Expanded by Its Sign Bit Example for 20-bits Received Audio Sample: Mode 0: APB_RDATA [31:0] = {RXFIFO [31:12], 12'h0} Mode 1: APB_RDATA [31:0] = {12{RXFIFO [31]}, RXFIFO [31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO [31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}}

4.2.6.7 0x0018 I2S|PCM FIFO Status Register (Default Value: 0x1080_0080)

Offset: 0x0018			Register Name: I2S|PCM_FSTA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No Room for New Sample in TXFIFO 1: More than One Room for New Sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No Available Data in RXFIFO 1: More than One Sample in RXFIFO (>= 1 Word)
7	R	0x1	PLACE_HOLDER NO Meaning
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

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4.2.6.8 0x001C I2S|PCM DMA and Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S|PCM_INT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

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4.2.6.9 0x0020 I2S|PCM TXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S|PCM_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

4.2.6.10 0x0024 I2S|PCM Clock Divide Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S|PCM_CLKD
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCLKO_EN MCLK Out Enable 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to '1', MCLK should be output.
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

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Offset: 0x0024			Register Name: I2S|PCM_CLKD
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

4.2.6.11 0x0028 I2S|PCM TX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S|PCM_TXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

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4.2.6.12 0x002C I2S|PCM RX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S|PCM_RXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

4.2.6.13 0x0030 I2S|PCM Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S|PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ TX Slot Value in Half Cycle of BCLK 0: Normal Mode for the Last Half Cycle of BCLK in the Slot 1: Turn to Hi-Z State for the Last Half Cycle of BCLK in the Slot
8	R/W	0x0	TX_STATE The state of transmission line When there is No Transmission 0: Transfer Level 0 When Not Transferring Slot 1: Turn to Hi-Z State (TDM) When Not Transferring Slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot Number Which between CPU/DMA and RXFIFO 0: 1 Channel or Slot ... 7: 8 Channels or Slots 8: 9 Channels or Slots ... 15:16 Channels or Slots

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Offset: 0x0030			Register Name: I2S|PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot Number Which between CPU/DMA and TXFIFO 0: 1 Channel or Slot ... 7: 8 Channels or Slots 8: 9 Channels or Slots ... 15:16 Channels or Slots

4.2.6.14 0x0034 I2S|PCM TX0 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S|PCM_TX0CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX0_OFFSET TX0 offset Tune, TX0 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX0_CHSEL TX0 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX0_CHEN TX0 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.15 0x0038 I2S|PCM TX1 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: I2S|PCM_TX1CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

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Offset: 0x0038			Register Name: I2S|PCM_TX1CHSEL
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	TX1_OFFSET TX1 offset Tune, TX1 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX1_CHSEL TX1 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX1_CHEN TX1 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.16 0x003C I2S|PCM TX2 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: I2S|PCM_TX2CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX2_OFFSET TX2 offset Tune, TX2 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX2_CHSEL TX2 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots

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Offset: 0x003C			Register Name: I2S|PCM_TX2CHSEL
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	TX2_CHEN TX2 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.17 0x0040 I2S|PCM TX3 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: I2S|PCM_TX3CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX3_OFFSET TX3 offset Tune, TX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX3_CHSEL TX3 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX3_CHEN TX3 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

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4.2.6.18 0x0044 I2S|PCM TX0 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S|PCM_TX0CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH15_MAP TX0 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX0_CH14_MAP TX0 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX0_CH13_MAP TX0 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX0_CH12_MAP TX0 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x0044			Register Name: I2S|PCM_TX0CHMAP0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX0_CH11_MAP TX0 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX0_CH10_MAP TX0 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX0_CH9_MAP TX0 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX0_CH8_MAP TX0 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.19 0x0048 I2S|PCM TX0 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S|PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH7_MAP TX0 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX0_CH6_MAP TX0 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX0_CH5_MAP TX0 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX0_CH4_MAP TX0 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x0048			Register Name: I2S|PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX0_CH3_MAP TX0 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX0_CH2_MAP TX0 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX0_CH1_MAP TX0 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX0_CH0_MAP TX0 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.20 0x004C I2S|PCM TX1 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: I2S|PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX1_CH15_MAP TX1 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX1_CH14_MAP TX1 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX1_CH13_MAP TX1 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX1_CH12_MAP TX1 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x004C			Register Name: I2S|PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX1_CH11_MAP TX1 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX1_CH10_MAP TX1 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX1_CH9_MAP TX1 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX1_CH8_MAP TX1 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.21 0x0050 I2S|PCM TX1 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: I2S|PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX1_CH7_MAP TX1 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX1_CH6_MAP TX1 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX1_CH5_MAP TX1 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX1_CH4_MAP TX1 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x0050			Register Name: I2S|PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX1_CH3_MAP TX1 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX1_CH2_MAP TX1 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX1_CH1_MAP TX1 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX1_CH0_MAP TX1 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.22 0x0054 I2S|PCM TX2 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S|PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX2_CH15_MAP TX2 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX2_CH14_MAP TX2 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX2_CH13_MAP TX2 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX2_CH12_MAP TX2 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x0054			Register Name: I2S|PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX2_CH11_MAP TX2 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX2_CH10_MAP TX2 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX2_CH9_MAP TX2 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX2_CH8_MAP TX2 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.23 0x0058 I2S|PCM TX2 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: I2S|PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX2_CH7_MAP TX2 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX2_CH6_MAP TX2 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX2_CH5_MAP TX2 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX2_CH4_MAP TX2 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x0058			Register Name: I2S|PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX2_CH3_MAP TX2 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX2_CH2_MAP TX2 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX2_CH1_MAP TX2 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX2_CH0_MAP TX2 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.24 0x005C I2S|PCM TX3 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: I2S|PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX3_CH15_MAP TX3 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX3_CH14_MAP TX3 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX3_CH13_MAP TX3 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX3_CH12_MAP TX3 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x005C			Register Name: I2S|PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX3_CH11_MAP TX3 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX3_CH10_MAP TX3 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX3_CH9_MAP TX3 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX3_CH8_MAP TX3 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.25 0x0060 I2S|PCM TX3 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: I2S|PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX3_CH7_MAP TX3 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX3_CH6_MAP TX3 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX3_CH5_MAP TX3 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX3_CH4_MAP TX3 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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Offset: 0x0060			Register Name: I2S|PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	TX3_CH3_MAP TX3 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX3_CH2_MAP TX3 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX3_CH1_MAP TX3 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX3_CH0_MAP TX3 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.26 0x0064 I2S|PCM RX Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S|PCM_RXCHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

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Offset: 0x0064			Register Name: I2S|PCM_RXCHSEL
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	RX_OFFSET RX offset Tune, RX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	/	/	/

4.2.6.27 0x0068 I2S|PCM RX Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S|PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH15_SELECT Rx channel 15 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH14_SELECT Rx channel 14 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

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Offset: 0x0068			Register Name: I2S|PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH13_SELECT Rx channel 13 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH12_SELECT Rx channel 12 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.28 0x006C I2S|PCM RX Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S|PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH11_SELECT Rx channel 11 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 0: 1st Sample … 7: 8th Sample 8: 9th Sample … 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH10_SELECT Rx channel 10 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 0: 1st Sample … 7: 8th Sample 8: 9th Sample … 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH9_SELECT Rx channel 9 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

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Offset: 0x006C			Register Name: I2S|PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH8_SELECT Rx channel 8 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.29 0x0070 I2S|PCM RX Channel Mapping Register2(Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: I2S|PCM_RXCHMAP2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH7_SELECT Rx channel 7 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

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Offset: 0x0070			Register Name: I2S|PCM_RXCHMAP2
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH6_SELECT Rx channel 6 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH5_SELECT Rx channel 5 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11: 8	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/

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Offset: 0x0070			Register Name: I2S|PCM_RXCHMAP2
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x0	RX_CH4_SELECT Rx channel 4 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.30 0x0074 I2S|PCM RX Channel Mapping Register3(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: I2S|PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH3_SELECT Rx channel 4 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH2_SELECT Rx channel 2 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

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Offset: 0x0074			Register Name: I2S|PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH1_SELECT Rx channel 1 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH0_SELECT Rx channel 0 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

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4.2.6.31 0x0080 I2S|PCM ASRC MCLK Configure Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: MCLKCFG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	ASRC_MCLK_GATE ASRC Clock Gate Enable 0: Gated 1: Not gated
15:4	/	/	/
3:0	R/W	0x0	ASRC_MCLK_FREQ_DIV_COE Frequency Division Coefficient 4'd0 = Res (no output), 4'd1 = 1x, 4'd2 = 1/2x, 4'd3 = 1/4x, 4'd4 = 1/6x, 4'd5 = 1/8x, 4'd6 = 1/12x, 4'd7 = 1/16x, 4'd8 = 1/24x, 4'd9 = 1/32x, 4'd10 = 1/48, 4'd11 = 1/64x, 4'd12 = 1/96x, 4'd13 = 1/128x, 4'd14 = 1/176x, 4'd15 = 1/192x, others = Res

4.2.6.32 0x0084 I2S|PCM ASRC Out Sample Configure Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: F_{SOUT}CFG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	FSOUT_GATE Fsout Clock Gate Enable Control 0: Gated 1: Not gated

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Offset: 0x0084			Register Name: F_{SOUT}CFG
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	FSOUT_CLK_SRC_SEL Fsout Clock Source Select 00: I2S0_ASRC_CLK 01: ACLK 10: ACLKM 11: BCLK Others: Reserved
15:8	/	/	/
7:4	R/W	0x0	FSOUT_CLK_FREQ_DIV_COE1 Fsout Frequency Division Coefficient 1 The First Division Factor It has two levels of frequency division, the first level is bit [7:4], the second level is bit [3:0], and the frequency division factors are multiplied by the two division factors, the division relationship of the two divisions are the same. 4'd0 = Res (no output), 4'd1 = 1x, 4'd2 = 1/2x, 4'd3 = 1/4x, 4'd4 = 1/6x, 4'd5 = 1/8x, 4'd6 = 1/12x, 4'd7 = 1/16x, 4'd8 = 1/24x, 4'd9 = 1/32x, 4'd10 = 1/48, 4'd11 = 1/64x, 4'd12 = 1/96x, 4'd13 = 1/128x, 4'd14 = 1/176x, 4'd15 = 1/192x

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Offset: 0x0084			Register Name: F_{SOUT}CFG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	FSOUT_CLK_FREQ_DIV_COE2 Fsout Frequency Division Coefficient 2 The Second Division Factor 4'd0 = Res (no output), 4'd1 = 1x, 4'd2 = 1/2x, 4'd3 = 1/4x, 4'd4 = 1/6x, 4'd5 = 1/8x, 4'd6 = 1/12x, 4'd7 = 1/16x, 4'd8 = 1/24x, 4'd9 = 1/32x, 4'd10 = 1/48, 4'd11 = 1/64x, 4'd12 = 1/96x, 4'd13 = 1/128x, 4'd14 = 1/176x, 4'd15 = 1/192x

4.2.6.33 0x0088 I2S|PCM IN Sample Pulse Extend Configure Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: FsinEXTCFG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EXTEND_EN Extend Enable 0: Disabled 1: Enabled Enable the bit when using ASRC.
15:0	R/W	0x0	EXTEND_VALUE Extend value The Cycle Number of Pulse Extend The cycle is BCLK clock and is 1 at least.

4.2.6.34 0x008C I2S|PCM ASRC Enable Configure Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: ASRCEN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x008C			Register Name: ASRCEN
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	ASRC_EN ASRC Function Enable 0: Disabled 1: Enabled

4.2.6.35 0x0090 I2S|PCM ASRC Manual Configure Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: ASRCMANCFG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ASRC_RATIO_MANUAL_EN Manual Configuration of ASRC Ratio Enable 0: Disabled 1: Enabled
30:26	/	/	/
25:0	R/W	0x0	ASRC_RATIO_VALUE_MANUAL_CFG ASRC Ratio Value Manual Configuration The ratio value is an unsigned 26-bit number and uses 4.22 data format, which means there are 4 bits to the left of the decimal point and 22 bits to the right of the decimal point.

4.2.6.36 0x0094 I2S|PCM ASRC Ratio State Configure Register (Default Value: 0x0040_0000)

Offset: 0x0094			Register Name: ASRCRATIOSTAT
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R	0x0	ASRC_BUF_OVERFLOW_STA ASRC Receive Data Buffer Overflow State It can control the mute with lock. 0: No overflow 1: Overflow
28	R	0x0	ADAPT_COMPUT_LOCK Adaptive Ratio Computational Lock 0: Unlocked 1: Locked
27:26	/	/	/
25:0	R	0x400000	ADAPT_COMPUT_VALUE Adaptive Ratio Computational Value

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4.2.6.37 0x0098 I2S|PCM ASRC FIFO State Configure Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: ASRCFIFOSTAT
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0x0	ASRC_RX_FIFO_FULL_LEVAL ASRC RXFIFO Full Level The manually-configured FIFO fill level for the ratio value of the received data.

4.2.6.38 0x009C I2S|PCM ASRC MBIST Test Configure Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: ASRCMBISTCFG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	ASRC_RAM_BIST_EN ASRC RAM BIST Enable Enable the RAM BIST.
7:1	/	/	/
0	R/W	0x0	ASRC_ROM_BIST_EN ASRC ROM BIST Enable Enable the ROM BIST.

4.2.6.39 0x00A0 I2S|PCM ASRC MBIST Test State Configure Register (Default Value: 0x0000_0002)

Offset: 0x00A0			Register Name: ASRCMBISTSTA
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R	0x0	ROM_BIST_ERROR_XOR ROM Bist Error Xor
17	R	0x0	ROM_BIST_ERROR_SUM ROM Bist Error Sum
16	R	0x0	ROM_BUSY_STATUS ROM Busy Status 1: ROM busy 0: ROM IDLE
15:8	/	/	/
7	R	0x0	RAM_BIST_ERR_STATUS RAM Bist Error Status 1: Error 0: No Effect

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Offset: 0x00A0			Register Name: ASRCMBISTSTA
Bit	Read/Write	Default/Hex	Description
6:4	R	0x0	RAM_BIST_ERROR_PATTERN. RAM Bist Error Pattern.
3:2	R	0x0	RAM_BIST_ERROR_CYCLE RAM Bist Error Cycle.
1	R	0x1	RAM_STOP_STATUS RAM Stop Status 1: Stop 0: Running
0	R	0x0	RAM_BUSY_STATUS RAM Busy Status 1: RAM busy 0: RAM IDLE.

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4.3 DMIC

4.3.1 Overview

The DMIC controller supports one 8-channel digital microphone interface and can output 128 fs or 64 fs (fs = ADC sample rate).

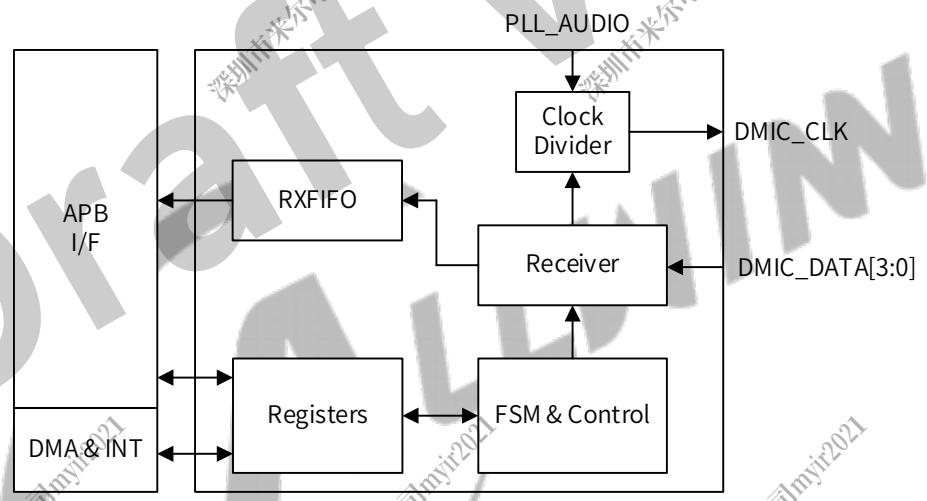
The DMIC controller includes the following features:

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

4.3.2 Block Diagram

The following figure shows a block diagram of the DMIC.

Figure 4-24 DMIC Block Diagram



4.3.3 Functional Description

4.3.3.1 External Signals

The following table describes the external signals of DMIC.

Table 4-5 DMIC External Signals

Signal Name	Description	Type
DMIC-DATA[3:0]	Digital Microphone Data Input	I
DMIC-CLK	Digital Microphone Clock Output	O

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4.3.3.2 Clock Sources

The following table describes the clock source for DMIC. For clock setting, configurations, and gating information, refer to section 2.13 Power Reset Clock Management (PRCM).

Table 4-6 DMIC Clock Sources

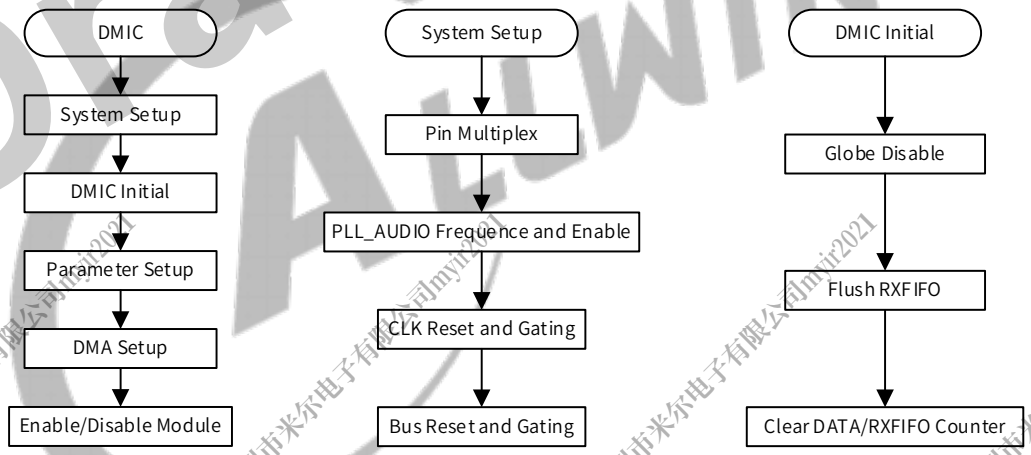
Clock Source	Description	Module
PLL_AUODIO(4x)	By default, PLL_AUDIO(4X) is 98.2856 MHz.	CCU
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz, and PLL_AUDIO1(DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1(DIV5)		

4.3.3.3 Operation Mode

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, channel setup, DMA setup, and Enable/Disable module.

The following figure shows the flow chart of the whole operation, the system setup, and the DMIC initialization.

Figure 4-25 DMIC Operation Mode



Step 1 System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO because the DMIC port is a multiplex pin. For functions of the multiplex pins, refer to section 8.6 GPIO.

Perform the following steps for the clock source. Firstly, disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE]. Secondly, set up the frequency of the PLL_AUDIO in PLL_AUDIOx Control Register. Then enable PLL_AUDIO. After that, enable the DMIC gating through DMIC_CLK_REG when you checkout that the LOCK bit of PLL_AUDIOx Control Register becomes 1. At last, reset and enable the DMIC bus gating by DMIC_BGR_REG.

After the system setup, the register of DMIC can be setup. Firstly, initialize the DMIC. You should close the globe enable bit (DMIC_EN[8]), data channel enable bit (DMIC_EN[7:0]) by writing 0 to it. After that, flush the RXFIFO by writing 1 to DMIC_RXFIFO_CTR[31]. At last, you can clear the Data/RXFIFO counter by writing 1 to DMIC_RXFIFO_STA, DMIC_CNT.

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Step 2 Parameter Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over-sample rate, the channel number, the RXFIFO output mode, the RXFIFO trigger level, and so on. The setup of the register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in section 2.8 DMA Controller (DMAC). In this module, you just enable the DRQ.

Step 3 Enable and Disable DMIC

To enable the function, you can enable the data channel enable bit (DMIC_EN[7:0]) by writing 1 to it. After that, enable DMIC by writing 1 to the Globe Enable bit (DMIC_EN[8]). Write 0 to DMIC_EN[8] to disable DMIC

4.3.4 Register List

Module Name	Base Address
DMIC	0x0711 1000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_DATA	0x0010	DMIC DATA Register
DMIC_INTC	0x0014	DMIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	DATA0 And DATA1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	DATA2 And DATA3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register
DMIC_REV	0x0050	DMIC Revision Register

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4.3.5 Register Description

4.3.5.1 0x0000 DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	RX_SYNC_EN_START Audio Subsys RX Synchronize Enable Start Includes Audio Codec/I2S0/I2S1/I2S2/I2S3/DMIC/OWA. The bit takes effect only when RX_SYNC_EN is set to 1. 0: Disabled 1: Enabled
28	R/W	0x0	RX_SYNC_EN DMIC RX Synchronize Enable 0: Disabled 1: Enabled
27:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disabled 1: Enabled
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel Enable 0: Disabled 1: Enabled
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disabled 1: Enabled
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel Enable 0: Disabled 1: Enabled
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disabled 1: Enabled

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Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel Enable 0: Disabled 1: Enabled
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disabled 1: Enabled
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel Enable 0: Disabled 1: Enabled
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disabled 1: Enabled

4.3.5.2 0x0004 DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

4.3.5.3 0x0008 DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

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Offset: 0x0008			Register Name: DMIC_CTR
Bit	Read/Write	Default/Hex	Description
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5 ms 01: 10 ms 10: 20 ms 11: 30 ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disabled 1: Enabled
7	R/W	0x0	DATA3 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
6	R/W	0x0	DATA2 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
5	R/W	0x0	DATA1 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
4	R/W	0x0	DATA0 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Supports 8 kHz to 24 kHz) 1: 64 (Supports 16 kHz to 48 kHz)

4.3.5.4 0x0010 DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMIC_DATA

4.3.5.5 0x0014 DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

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Offset: 0x0014			Register Name: DMIC_INTC
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disabled 1: Enabled
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disabled 1: Enabled
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disabled 1: Enabled

4.3.5.6 0x0018 DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DMIC_INTS
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing '1' to clear this interrupt or automatically clear if the interrupt condition fails.
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing '1' to clear this interrupt or automatically clear if the interrupt condition fails.

4.3.5.7 0x001C DMIC RXFIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing '1' to flush RXFIFO, self-clear to '0'
30:10	/	/	/

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Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register For 24-bit received audio sample: Mode 0: RXDATA [31:0] = {RXFIFO_O [20:0], 11'h0} Mode 1: RXDATA [31:0] = {8{RXFIFO_O [20]}, RXFIFO_O [20:0], 3'h0} For 16-bit received audio sample: Mode 0: RXDATA [31:0] = {RXFIFO_O [20:5], 16'h0} Mode 1: RXDATA[31:0] = {16{RXFIFO_O[20]}, RXFIFO_O[20:5]}
8	R/W	0x0	Sample Resolution 0: 16-bit 1: 24- bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV [7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV [7:0]) WLEVEL represents the number of valid samples in the DMIC RXFIFO

4.3.5.8 0x0020 DMIC RXFIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R	0x1	Reserved
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

4.3.5.9 0x0024 DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC enable channel numbers are (N + 1).

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4.3.5.10 0x0028 DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

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Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

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Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

4.3.5.11 0x002C DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: DMIC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMIC_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is read by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After being updated by the initial value, the counter register should count on the base of this initial value. Note: It is used for Audio/Video Synchronization.

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4.3.5.12 0x0030 DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xA0	DATA1L_VOL Data1 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL Data1 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA0L_VOL Data0 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

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Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0xA0	DATA0R_VOL Data0 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

4.3.5.13 0x0034 DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xA0	DATA3L_VOL Data3 Light Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA3R_VOL Data3 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

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Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0xA0	DATA2L_VOL Data2 Light Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL Data2 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

4.3.5.14 0x0038 High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	HPF_DATA3_CHR_EN High Pass Filter DATA3 Right Channel Enable 0: Disabled 1: Enabled
6	R/W	0x0	HPF_DATA3_CHL_EN High Pass Filter DATA3 Left Channel Enable 0: Disabled 1: Enabled
5	R/W	0x0	HPF_DATA2_CHR_EN High Pass Filter DATA2 Right Channel Enable 0: Disabled 1: Enabled

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Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	HPF_DATA2_CHL_EN High Pass Filter DATA2 Left Channel Enable 0: Disabled 1: Enabled
3	R/W	0x0	HPF_DATA1_CHR_EN High Pass Filter DATA1 Right Channel Enable 0: Disabled 1: Enabled
2	R/W	0x0	HPF_DATA1_CHL_EN High Pass Filter DATA1 Left Channel Enable 0: Disabled 1: Enabled
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disabled 1: Enabled
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disabled 1: Enabled

4.3.5.15 0x003C High Pass Filter Coefficient Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00FFAA45	HPF_COE High Pass Filter Coefficient

4.3.5.16 0x0040 High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00FFD522	HPF_GAIN High Pass Filter Gain

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4.4 One Wire Audio (OWA)

4.4.1 Overview

The One Wire Audio (OWA) provides a serial bus interface for audio data. This interface is widely used for consumer audio.

The OWA includes the following features:

- One OWA TX and One OWA RX
- Compliance with S/PDIF interface
- IEC-60958 and IEC-61937 transmitter and receiver functionality
- IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- TXFIFO and RXFIFO
  - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
  - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Multiple function clock
  - Separate clock for OWA TX and OWA RX
  - The clock of TX function includes 24.576 MHz and 22.5792 MHz
  - The clock of RX function includes 24.576*8 MHz
- Supports hardware parity on TX/RX
  - Hardware parity generation on the transmitter
  - Hardware parity checking on the receiver
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter

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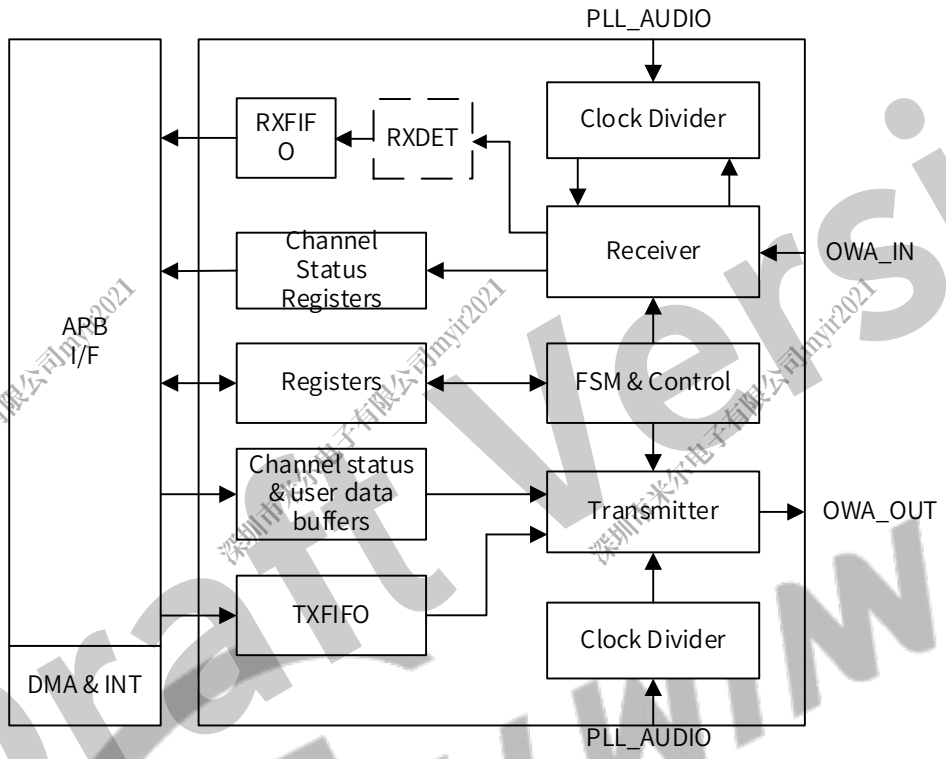
4.4.2 Block Diagram

The following figure shows the OWA block diagram.

Figure 4-26 OWA Block Diagram



OWA contains the following sub-blocks:

Table 4-7 OWA Sub-blocks

Sub-block	Description
Registers	Analyze the configuration parameter, DMA requests, and IRQ feedbacks.
Receiver	Parses the frame header and receives the data.
Transmitter	Sends the data
FSM	Finite state machine
Clock Divider	Clock divider circuit

4.4.3 Functional Description

4.4.3.1 External Signals

The OWA is a Biphasic-Mark Encoding Digital Audio Transfer protocol. In this protocol, the CLK signal and data signal are transferred in the same line. The following table describes the external signals of OWA. OWA-OUT is the output pin for the output CLK and DATA, and OWA-IN is the input pin for the input CLK and DATA.

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Table 4-8 OWA External Signals

Signal Name	Description	Type
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O

4.4.3.2 Clock Sources

The OWA has separate clock for OWA_TX and OWA_RX. The following tables describe the clock sources for OWA_TX and OWA_RX. For clock setting, configurations and gating information, refer to section 2.13 Power Reset Clock Management (PRCM).

Table 4-9 OWA_TX Clock Sources

Clock Sources	Description	Module
PLL_AUODIO(4x)	By default, PLL_AUDIO(4X) is 98.2856 MHz.	CCU
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz, and PLL_AUDIO1(DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1(DIV5)		

Table 4-10 OWA_RX Clock Sources

Clock Sources	Description	Module
PERI0_300M	By default, PERI0_300M is 300 MHz.	CCU
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz, and PLL_AUDIO1(DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1(DIV5)		

4.4.3.3 Biphase-Mark Code (BMC)

In the OWA format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal—the data pin. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. The following figure and table show how data is encoded to the BMC format.

The frequency of the clock is twice the data bit rate, as shown in the following figure. Also, the clock is always programmed to 128 x fs, where fs is the sample rate. The device receiving in the OWA format can recover the clock and frame information from the BMC signal.

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Figure 4-27 OWA Biphase-Mark Code

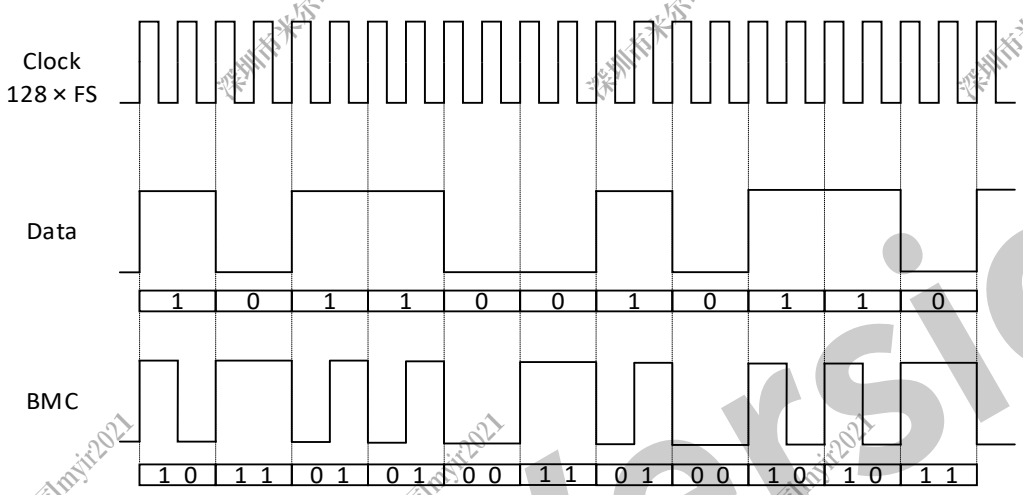


Table 4-11 Biphase-Mark Encoder

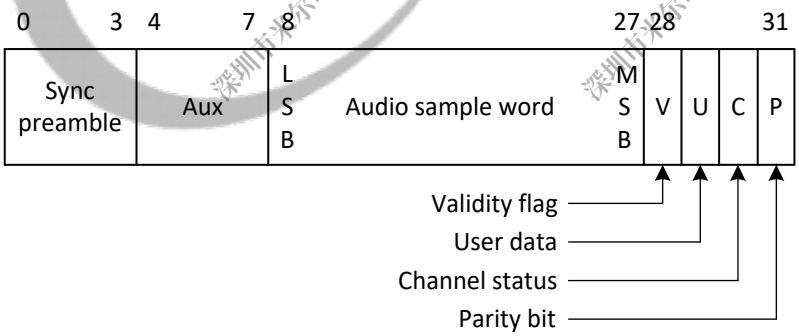
Data	Previous State	BMC
0	0	11
0	1	00
1	0	10
1	1	01

4.4.3.4 IEC60958 Transmit Format

The OWA supports digital audio data transfer and receive. It also supports full-duplex synchronous work mode. The software can set the work mode by the OWA Control Register.

Every audio sample transmitted in a sub-frame consists of 32-bit, numbered from 0 to 31. The following figure shows a sub-frame.

Figure 4-28 OWA Sub-Frame Format



Bits 0-3 carry one of the four permitted preambles to signify the type of audio sample in the current sub-frame. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row.

Bits 4-27 carry the audio sample word in linear 2s-complement representation. The most-significant bit (MSB) is carried by bit 27. When a 24-bit coding range is used, the least-significant

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bit (LSB) is in bit 4. When a 20-bit coding range is used, bit [8:27] carry the audio sample word with the LSB in bit 8. Bit [4:7] may be used for other applications and are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field may carry any other information.

Bit 28 carries the validity bit (V) associated with the main data field in the sub-frame.

Bit 29 carries the user data channel (U) associated with the main data field in the sub-frame.

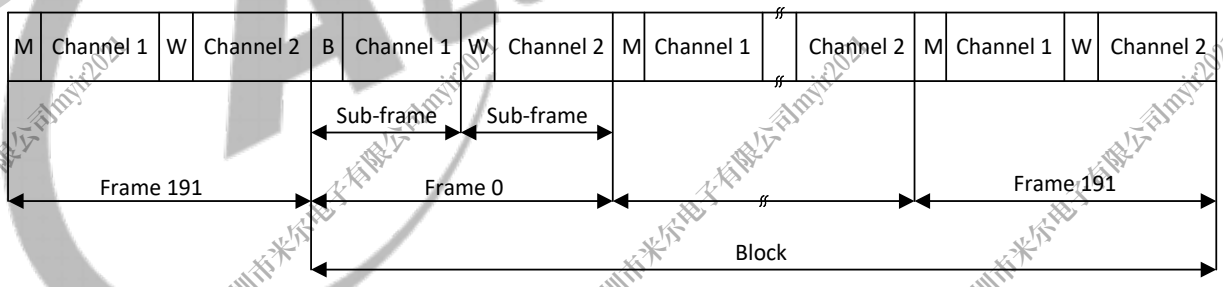
Bit 30 carries the channel status information (C) associated with the main data field in the sub-frame. The channel status indicates if the data in the sub-frame is a digital audio or some other type of data.

Bit 31 carries a parity bit (P) such that bit 4-31 carry an even number of 1s and an even number of 0s (even parity). As shown in the following table, the preambles (bit 0-3) are also defined with even parity.

Table 4-12 Preamble Codes

Preamble Code	Previous Logical State	Logical State	Description
B (or Z)	0	1110 1000	Start of a block and sub-frame 1
M (or X)	0	1110 0010	Sub-frame 1
W (or Y)	0	1110 0100	Sub-frame 2

Figure 4-29 OWA Frame/Block Format



4.4.3.5 IEC61937 Transmit Format

IEC 61937 applies to the digital audio interface by using the IEC 60958 series for the conveying of non-linear PCM encoded audio bitstreams. The non-linear PCM encoded audio bitstream is transferred by using the basic 16-bit data area of the IEC 60958 subframes, i.e. in time-slots 12 to 27. Because the non-linear PCM encoded audio bitstream to be transported is at a lower data rate than that supported by the IEC 60958 interface, the audio bitstream is broken into a sequence of discrete data-bursts, and stuffing between the data-bursts is necessary.

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IEC 60958 Data Burst

The method of placing the data into the IEC 60958 bitstream is to format the data to be transmitted into data-bursts and to send each data-burst in a continuous sequence of IEC 60958 frames.

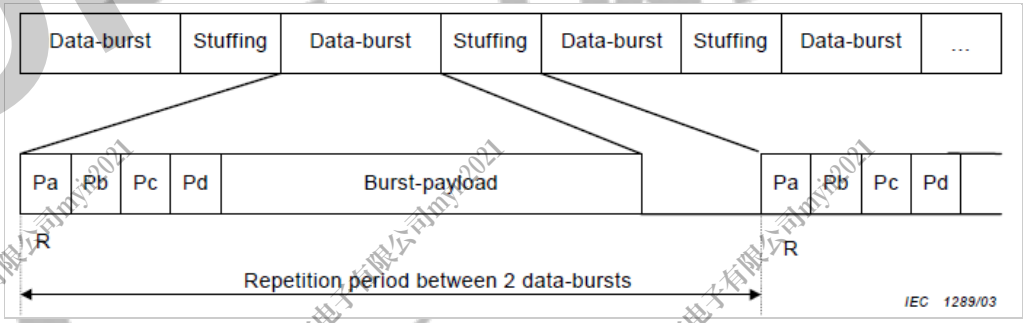
Table 4-13 Bit Allocation of Data-Burst in IEC 60958 Subframes

Subframe	Bit of subframes				
	MSB b27	b26	b25 ..... b14	b13	LSB b12
Frame 0; subframe B or M	0	1		14	15
Frame 0; subframe W	16	17		30	31
Frame 1; subframe B or M	32	33		46	47
Frame 1; subframe W	48	49		62	63
Frame 2; subframe B or M	64	65		78	79
----------			----------		
Last subframe B or M of data-burst	n-32	n-31		n-18	n-17
Last subframe W of data-burst	n-16	n-15		n-2	n-1

Data Burst Format

Each data-burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc and Pd) followed by the burst-payload which contains data of an encoded audio frame.

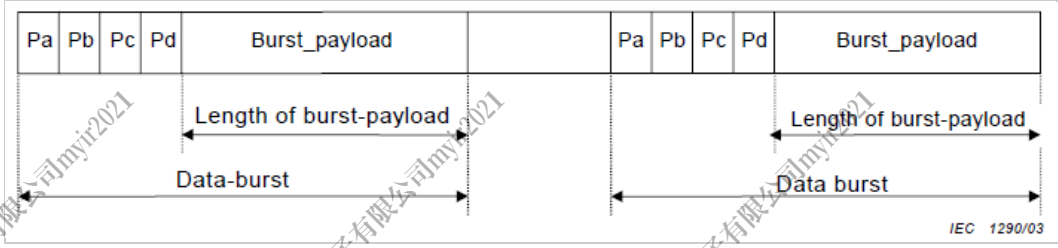
Figure 4-30 Data-Burst Format



- Burst-preamble

The burst-preamble consists of four mandatory fields. Pa and Pb represent a synchronization word. Pc gives information about the type of data, and some information/control for the receiver. Pd gives the length of the burst-payload, and is limited to 65535 bits in the case of Pd represent bits' length, or is limited to 65535 bytes in the case of Pd represent bytes' length.

Figure 4-31 Data-burst Preamble



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The four preamble words are contained in two sequential IEC 60958 frames. The frame beginning the data-burst contains preamble word Pa in subframe 1, and Pb in subframe 2. The next frame contains Pc in subframe 1 and Pd in subframe 2. When placed into an IEC 60958 subframe, the MSB of a 16-bit burst-preamble word is placed into time-slot 27 and the LSB is placed into time-slot 12.

Figure 4-32 Data-burst Preamble words

Preamble word	Length of field	Contents	Value MSB..LSB
Pa	16-bit	Sync word 1	F872h
Pb	16-bit	Sync word 2	4E1Fh
Pc	16-bit	Burst-info	Table 5
Pd	16-bit	Length-code	Number of bits or number of bytes according to data-type

- Burst-information

The 16-bit burst-information contains information about the data which will be found in the data-burst.

Figure 4-33 Fields of Burst-information

Bits of Pc	Value	Contents	Remark
0 – 6		Data-type	See IEC 61937-2
7	0	Error-flag indicating a valid burst-payload	
	1	Error-flag indicating that the burst-payload may contain errors	
8 – 12		Data-type-dependent info	
13 – 15	0	Bitstream-number	
NOTE The repetition period of pause data-bursts depends on the application in which IEC 60958 is used to convey encoded audio bitstreams.			

The 7-bit data-type is defined in bits 0-6 of the burst-preamble Pc, the bit 6 is the MSB. This data-type field indicates the format of the burst-payload, which will be conveyed in the data-burst. Typical properties of a data-type are the reference point and repetition period of the burst, which is the number of sampling periods of the audio between the reference point of the current data-burst and the reference point of the next data-burst. The reference point is inherently defined for each data-type.

The error-flag bit is available to indicate if the contents of the data-burst contain data errors. If a data-burst is thought to be error-free, or if the data source does not know if the data contains errors, then the value of this bit is set to a '0'. If the data source does know that a particular data-burst contains some errors this bit may be set to a '1'. The usage of this bit by receiver is optional.

The meaning of the 5-bit data-type-dependent info depends on the value of the data-type.

The 3-bit bitstream-number indicates to which bitstream the data-burst belongs. Eight codes (0-7) are available so that up to eight independent bitstreams may be multiplexed in one bitstream in a time multiplex. Each independent bitstream shall use a unique bit-streamnumber.

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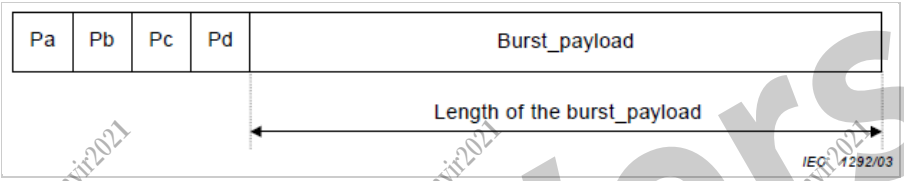
- Length-code

The length-code indicates the number of bits or bytes according to data-type within the databurst, from 0 to 65535. The size of the Pa, Pb, Pc and Pd is not counted in the value of the length-code. In other words, the length-code indicates the number of bits of the burst-payload in bits, plus the conditional length of Pe and Pf, or the number of bytes of the burst-payload in bytes, plus the conditional length of Pe and Pf if exists.

Figure 4-34 Length of the Burst-Payload Specified by Pd



4.4.3.6 Audio Sample Ratio Detection

The sampling rate is calculated according to the data pulse back-stepping method. In the first phase lock of the CDR, find 1 Frame period, count by using the high-speed sampling clock, and read the counting value of the pulse, then the sampling rate can be calculated.

Table 4-14 The Corresponding Relation between Different System Clock and Sample Ratio

	Sample Clock Cycles		
TX Sample Rate(kHz)	196.608 MHz-SysClk	200 MHz-SysClk	300 MHz-SysClk
22.05	8916(±5)	9070(±5)	13605(±5)
24	8192(±5)	8333(±5)	12500(±5)
32	6144(±5)	6250(±5)	9375(±5)
44.1	4458(±5)	4535(±5)	6802(±5)
48	4096(±5)	4166(±5)	6250(±5)
96	2048(±5)	2083(±5)	3125(±5)
176.4	1114(±5)	1133(±5)	1700(±5)
192	1024(±5)	1041(±5)	1562(±5)

4.4.3.7 Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, channel setup, DMA setup and enable/disable module. The following sections describe these five steps.

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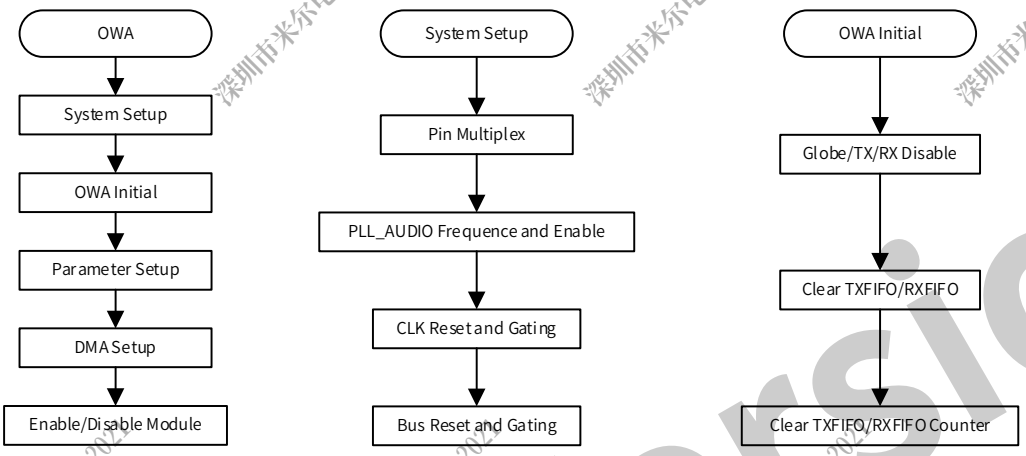
Figure 4-35 OWA Operation Flow



Step 1 System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO because the OWA port is a multiplex pin. You can find the function in section 8.6 GPIO.

The clock source for the OWA should be followed. Firstly, reset the audio PLL in PLL_AUDIOx Control Register. Secondly, set up the frequency of the Audio PLL in the PLL_AUDIOx Control Register. After that, enable the OWA gating. Lastly, enable the OWA bus gating.

After the system setup, the register of OWA can be set up. Firstly, reset the OWA by writing 1 to OWA_CTL[0] and clear the TX/RX FIFO by writing 1 to OWA_FCTL[17:16]. After that, enable the globe enable bit by writing 1 to OWA_CTL[1] and clear the interrupt and TX/RX counter by setting OWA_ISTA and OWA_TX_CNT/OWA_RX_CNT.

Step 2 Parameter Setup and DMA Setup

You can set up the audio type, clock divider ratio, the sample format, and the trigger level, and so on. The setup of the register can be found in the specification.

The OWA supports two methods to transfer the data. The most common way is DMA; the configuration of DMA can be found in section 3.9 “DMAC”. In this module, you just enable the DRQ in OWA_INT[7].

Step 3 Enable and Disable OWA

To enable the function, you can enable TX/RX by writing OWA_TX_CFIG[31]/OWA_RX_CFIG[0]. After that, enable OWA by writing 1 to OWA_CTL[1]. Writing 0 to OWA_CTL[1] to disable process.

4.4.4 Programming Guidelines

4.4.4.1 Configuring RX CDR

The RX_CDR_MANUAL bit (bit [5]) of OWA_RX_CFIG register decides whether manual mode or automatic mode is used for clock recovery.

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- Automatic Mode (default mode)

Configure RX_CDR_MANUAL bit as 1'b0 to choose automatic mode.

- Manual Mode

The manual mode could be chosen by configuring RX_CDR_MANUA bit as 1'b1. In this mode, you can select RX CDR from preamble X (11100010) or preamble X (00011101) by configuring the RX_CDR_PREAMBLE bit (bit [2]) of OWA_RX_CFIG register. The operation steps are as follows:

Step 1 Configure the INSERT_INT_EN bit (bit [16]) of OWA_EXP_ISTA register to enable insert interrupt.

Step 2 Insert TX device and wait for a while.

Step 3 Keep reading the INSERT_INT bit (bit [0]) of OWA_EXP_ISTA register until INSERT_INT = 1.

Step 4 Keep reading the RX_LOCK_FLAG bit (bit [4]) of OWA_RX_CFIG register for a software-setting period.

- If the value of RX_LOCK_FLAG bit turns to 1, it is unnecessary to configure the RX_CDR_PREAMBLE bit (bit [2]) of OWA_RX_CFIG register.
- If the value of RX_LOCK_FLAG bit doesn't turn to 1, configure the RX_CDR_PREAMBLE bit (bit [2]) of OWA_RX_CFIG register to the opposite value.

4.4.5 Register List

Module Name	Base Address
OWA	0x0711 6000

-

Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control Register
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_RX_CFIG	0x0008	OWA RX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_RXFIFO	0x0010	OWA RXFIFO Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_RX_CNT	0x0028	OWA RX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1
OWA_RXCHSTA0	0x0034	OWA RX Channel Status Register0
OWA_RXCHSTA1	0x0038	OWA RX Channel Status Register1
OWA_INSERT_REDET_CTL	0x003C	OWA Insert Redetect Control Register

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Register Name	Offset	Description
OWA_EXP_CTL	0x0040	OWA Expand Control Register
OWA_EXP_ISTA	0x0044	OWA Expand Interrupt Status Register
OWA_EXP_INFO_0	0x0048	OWA Expand Information Register0
OWA_EXP_INFO_1	0x004C	OWA Expand Information Register1
OWA_EXP_DBG_0	0x0050	OWA Expand Debug Register0
OWA_EXP_DBG_1	0x0054	OWA Expand Debug Register1

4.4.6 Register Description

4.4.6.1 0x0000 OWA General Control Register (Default Value: 0x0000_0080)

Offset: 0x0000			Register Name: OWA_CTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/WAC	0x0	RST_RX Reset RX 0: Normal 1: Reset Self-clear to '0'.
11:10	/	/	/
9:5	R/W	0x4	MCLKDIV MCLK Clock Divide Ratio MCLK Divide Ratio from PLL_AUDIO 00000: Divide by 128 00001: Divide by 2 00010: Divide by 4 00011: Divide by 6 00100: Divide by 8 00101: Divide by 10 00110: Divide by 12 00111: Divide by 14 01000: Divide by 16 01001: Divide by 18 01010: Divide by 20 01011: Divide by 22 01100: Divide by 24 ..... 11111: Divide by 62
4	/	/	/

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Offset: 0x0000			Register Name: OWA_CTL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	MCLKEN MCLK Enable 0: Disable 1: Enable
2	R/W	0x0	LOOP Loopback Test 0: Normal Mode 1: Loopback Test When the bit is set to '1', the DOUT and DIN need be connected.
1	R/W	0x0	GEN Global Enable Disabling this bit overrides the operations of enabling and flushing all FIFOs by any other blocks or channels. 0: Disabled 1: Enabled
0	R/W	0x0	RST_TX Reset TX 0: Normal 1: Reset Self-clear to 0.

4.4.6.2 0x0004 OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_SINGLE_MODE TX Single Channel Mode 0: Disabled 1: Enabled
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select when TX FIFO Underrun 0: Sending 0 1: Sending the last audio Note: This bit is only valid in PCM mode.
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio (Valid bit of both sub-frame set to 1)

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Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	Read/Write	Default/Hex	Description
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX Clock Divide Ratio Clock divide ratio = TX_TATIO + 1 Fs = PLL_AUDIO/[(TX_TATIO + 1)*64*2]
3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A and B set to 0 1: Channel status A and B generated from TX_CHSTA
0	R/W	0x0	TXEN TX Enable 0: Disabled 1: Enabled

4.4.6.3 0x0008 OWA RX Configure Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	RX_CDR_MANUAL RX CDR mode 0: Automatic (in this mode, RX_CDR_PREAMBLE does not need to be configured) 1: Manual (in this mode, if the header code is not able to be received accurately, RX_CDR_PREAMBLE needs to be configured)
4	R	0x0	RX_LOCK_FLAG RX Lock Flag 0: Unlocked 1: Locked
3	R/W	0x0	RX_CHST_SRC RX Channel State Source Select 0: RX_CH_STA register holds status from Channel A 1: RX_CH_STA register holds status from Channel B

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Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	RX_CDR_PREAMBLE RX channel CDR Preamble Type 0: support CDR from preamble X (11100010) 1: support CDR from preamble X (00011101)
1	R/W	0x0	CHST_CP Channel Status Capture 0: Idle or Capture End 1: Capture Channel Status Start The field must be set to 1 at each operation (such as recording). When set to '1', the system starts to capture the channel status. When finished, the bit will automatically turn to '0'.
0	R/W	0x0	RXEN 0: Disabled 1: Enabled

4.4.6.4 0x000C OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	RX_LOCK_INT RX Lock Interrupt 0: No Pending IRQ 1: RX Lock Pending Interrupt (RX_LOCK_FLAG turns from 0 to 1) Write '1' to clear this interrupt.
17	R/W1C	0x0	RX_UNLOCK_INT RX Unlock Pending Interrupt 0: No Pending IRQ 1: RX Unlock Pending Interrupt (RX_LOCK_FLAG turns from 0 to 1) Write 1 to clear this interrupt.
16	R/W1C	0x0	RX_PARERRI_INT RX Parity Error Pending Interrupt 0: No Pending IRQ 1: RX Parity Error Pending Interrupt Write "1" to clear this interrupt.
15:7	/	/	/

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Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: FIFO Underrun Pending Interrupt Writing "1" to clear this interrupt.
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Writing "1" to clear this interrupt.
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Writing "1" to clear this interrupt or automatically clear if the interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: RXFIFO Overrun Pending Write '1' to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if the interrupt condition fails.

4.4.6.5 0x0010 OWA RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: OWA_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA The host can get one sample by reading this register, A channel data is first, and then the B channel data.

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4.4.6.6 0x0014 OWA FIFO Control Register (Default Value: 0x0004_0200)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable The bit takes effect only when the TXEN is set to 1. Audio codec/I2S0/I2S1/I2S2/I2S3/OWA TXFIFO Hub Enable. 0: Disabled 1: Enabled
30	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self-clear to '0'.
29	R/W1C	0x0	FRX Write '1' to flush RXFIFO, self-clear to '0'.
28:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START The bit takes effect only when the RX_SYNC_EN is set to 1. Audio Codec/I2S0/I2S1/I2S2/I2S3/DMIC/OWA RX Synchronize Enable Start. 0: Disabled 1: Enabled
20	R/W	0x0	RX_SYNC_EN OWA RX Synchronize Enable 0: Disabled 1: Enabled
19:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition. Trigger Level = TXTL
11	/	/	/
10:4	R/W	0x20	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/

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Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode0, 1) 0: Valid data at the MSB of TXFIFO Register 1: Valid data at the LSB of TXFIFO Register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO [23:0] = {APB_WDATA [31:12], 4'h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode(Mode 0,1,2,3) 00: Expanding '0' at LSB of RXFIFO Register 01: Expanding received sample sign bit at MSB of RXFIFO Register 10: Truncating received samples at high half-word of RXFIFO Register and low half-word of RXFIFO Register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO Register and high half-word of RXFIFO Register is expanded by its sigh bit Mode 0: APB_RDATA [31:0] = {RXFIFO [23:0], 8'h0} Mode 1: APB_RDATA [31:0] = {8'RXFIFO [23], RXFIFO [23:0]} Mode 2: APB_RDATA [31:0] = {RXFIFO [23:8], 16'h0} Mode 3: APB_RDATA[31:0] = {16'RXFIFO[23], RXFIFO[23:8]}

4.4.6.7 0x0018 OWA FIFO Status Register (Default Value: 0x8080_0000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	Read/Write	Default/Hex	Description
31	R	0x1	TXE TXFIFO Empty (indicate the TXFIFO is not full) 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
30:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)

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Offset: 0x0018			Register Name: OWA_FSTA
Bit	Read/Write	Default/Hex	Description
14:7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

4.4.6.8 0x001C OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	RX_LOCKI_EN RX LOCK Interrupt Enable 0: Disabled 1: Enabled
17	R/W	0x0	RX_UNLOCKI_EN RX UNLOCK Interrupt Enable 0: Disabled 1: Enabled
16	R/W	0x0	RX_PARERRI_EN RX PARITY ERORR Interrupt Enable 0: Disabled 1: Enabled
15:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disabled 1: Enabled
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disabled 1: Enabled
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disabled 1: Enabled
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disabled 1: Enabled
3	/	/	/

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Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable When set to '1', RXFIFO DMA Request is asserted if data is available in RXFIFO. 0: Disabled 1: Enabled
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disabled 1: Enabled
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disabled 1: Enabled

4.4.6.9 0x0020 OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. A channel data is first, and then the B channel data.

4.4.6.10 0x0024 OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After updated by the initial value, the counter register should count on the base of this initial value.

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4.4.6.11 0x0028 OWA RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: OWA_RX_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX counter register can be set to any initial value at any time. After being updated by the initial value, the counter register should count on the base of this value.

4.4.6.12 0x002C OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1 kHz 0001: Not indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved

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Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01 to 11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 µs/15 µs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100 to 111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001 to 111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application This bit must be fixed to “0”.

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4.4.6.13 0x0030 OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz 0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz

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Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	Read/Write	Default/Hex	Description
3:1	R/W	0x0	WL Sample Word Length For bit 0 = “0”: 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

4.4.6.14 0x0034 OWA RX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not Matched

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Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1 kHz 0001: Not Indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the Kind of Equipment that Generates the digital audio interface Signal.
7:6	R/W	0x0	MODE Mode 00: Default mode 01 to 11: Reserved

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Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
5:3	R/W	0x0	EMP Emphasis Additional Format Information For bit 1 = '0', Linear PCM Audio mode: 000: 2 Audio channels without pre-emphasis 001: 2 Audio channels with 50 μs/15 μs pre-emphasis 010: Reserved (For 2 Audio channels with pre-emphasis) 011: Reserved (For 2 Audio channels with pre-emphasis) 100 to 111: Reserved For bit 1 = '1', Other than Linear PCM applications: 000: Default state 001 to 111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No Copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application

4.4.6.15 0x0038 OWA RX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition is not be used 11: No copying is permitted

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Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz 0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = '0': 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = '1': 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum Audio sample word length is 20 bits 1: Maximum Audio sample word length is 24 bits

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4.4.6.16 0x003C OWA Insert Redetect Control Register (Default Value:0x0000_0180)

Offset: 0x003C			Register Name: S|PDIF_INSERT_REDET_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x1	INSERT_REDET_MONITOR_ENABLE Insert Re-detect Monitor Enable 0: disable 1: enable
7:0	R/W	0x80	INSERT_REDET_MONITOR_ENABLE Insert Re-detect Monitor Length The unit is one 32KHz cycle.

4.4.6.17 0x0040 OWA Expand Control Register (Default Value: 0x0000_000F)

Offset: 0x0040			Register Name: OWA_EXP_CTL
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	BURST_DATAOUT_SELECT Burst data output select 0: Burst preamble and payload 1: Burst payload
29:16	R/W	0x0	REPEAT_PERIOD_OF_FR_NUM The number for the repetition period of the burst frame Configure this field according to RX data. A mismatch between the configuration data and the received data will result in an error interrupt.
15	R/W	0x0	UNIT_SELECT Unit Select Configure this field according to RX data type 0: In units of 16-bit 1: In units of 2-byte
14	R/W	0x0	OWA_RX_MODE_MAN OWA RX Protocol Select 0: IEC60958 1: IEC61937
13	R/W	0x0	OWA_RX_MODE OWA RX Mode Select 0: Manual Ctrl. Configure by OWA RX_MODE_MAN 1: Auto Ctrl. Configure by the channel status values resolved by hardware

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Offset: 0x0040			Register Name: OWA_EXP_CTL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	AUDIO_DATA_BITORDER_EN Audio Data Bitorder Enable 0: The audio data received by RX is stored directly into FIFO 1: The audio data received by RX is reversed high and low bits, then stored into FIFO
11	R/W	0x0	DATA_LENGTH_BITORDER_EN Data Length Bitorder Enable 0: The received PD data is as the length of the valid audio data 1: The received PD data is reversed high and low bits, then as the length of the valid audio data
10	R/W	0x0	DATA_TYPE_BITORDER_EN Data Type Bitorder Enable 0: The received PC data is as the data length of the valid audio 1: The received PC data is reversed high and low bits, then as the length of the valid audio data
9	R/W	0x0	SYNCW_BITORDER_EN 0: Pa/Pb is the sync code of audio data 1: Pa/Pb reversed high and low bits is the sync code of audio data
8	R/W	0x0	INSERT_DETECTION_ENABLE Insert Detection Enable 0: Disable 1: Enable
7:0	R/W	0x0F	INSERT_DETECTION_NUM Insert Detection Number Configure how many jumping edges are detected to generate an insertion interrupt

4.4.6.18 0x0044 OWA Expand Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	PD_CHANGE_INT_EN PD_LENGTH_CHANGE Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	PC_PAUSE_STOP_INT PC_PAUSE_BURSTS_STOP Interrupt Enable 0: Disable 1: Enable
22	R/W	0x0	PC_BITSTRM_CHANGE_INT_EN PC_BITSTREAM_CHANGE Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	PC_ERR_FLAG_INT PC_ERROR_FLAG Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	PC_DTYPE_CHANGE_INT_EN PC_DATATYPE_CHANGE Interrupt Enable 0: Disable 1: Enable
19	R/W	0x0	RPDB_ERR_INT_EN RPDB_ERROR Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PCPD_CAP_INT_EN PCPD_CAP Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PAPB_CAP_INT_EN PAPB_CAP Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	INSERT_INT_EN INSERT Interrupt Enable 0: Disable 1: Enable
15:9	/	/	/
8	R/W1C	0x0	PD_CHANGE_INT PD CHANGE INT 0: No Pending IRQ 1: PD Data length information is change. (except Pause/Null data burst type) Write '1' to clear this interrupt.

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Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	PC_PAUSE_STOP_INT Audio bitstream is interrupted. When stopped, the interface becomes idle. 0: No Pending IRQ 1: PC Pause burst Stop, frame sequence discontinued. Transmitters may optionally use the STOP value to indicate that the transmission of the current encoded Write '1' to clear this interrupt.
6	R/W1C	0x0	PC_BITSTRM_CHANGE_INT PC BITSTRM CHANGE INT 0: No Pending IRQ 1: PC Bitstream Number is change. Bitstream Number indicates which bitstream the data burst belongs. (except Pause/Null data bursts type) Write '1' to clear this interrupt.
5	R/W1C	0x0	PC_ERR_FLAG_INT PC ERR FLAG INT 0: No Pending IRQ 1: PC Error-flag is available to indicate if the contents of the data-burst contain data errors (except Pause/Null data bursts type). The using of this bit by receivers is optional. Write '1' to clear this interrupt.
4	R/W1C	0x0	PC_DTYPE_CHANGE_INT PC DTYPE CHANGE INT 0: No Pending IRQ 1: PC Datatype (except Pause/Null data type) information is change Write '1' to clear this interrupt.
3	R/W1C	0x0	RPDB_ERR_INT RPDB ERR INT 0: No Pending IRQ 1: Hardware counts the repetition period of the burst frame is different from register configuration number Write '1' to clear this interrupt.

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Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	PCPD_CAP_INT PCPD CAP INT 0: No Pending IRQ 1: IEC61937 mode captures PC and PD Write '1' to clear this interrupt.
1	R/W1C	0x0	PAPB_CAP_INT PAPB CAP INT 0: No Pending IRQ 1: IEC61937 mode captures PA and PB Write '1' to clear this interrupt.
0	R/W1C	0x0	INSERT_INT INSERT INT 0: No Pending IRQ 1: OWA RX detects device insertion Write '1' to clear this interrupt.

4.4.6.19 0x0048 OWA Expand Information Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: OWA_EXP_INFO_0
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PC_DATA PC Data information
15:0	R	0x0	PD_DATA PD Data information

4.4.6.20 0x004C OWA Expand Information Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: OWA_EXP_INFO_1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	REPET_PERIOD_OF_FR_VALUE Repetition period of the burst frame value Check whether the repetition period of the burst frame calculated by hardware is consistent with the configuration value.
15:0	R	0x0	SR_VALUE Sample Rate Value Read this value after RX_LOCK.

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4.4.6.21 0x0050 OWA Expand Debug Register 0 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: OWA_EXP_DBG_0
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	IEC61937_DATA_CAP_FSM IEC61937 Data Captures State Machine 000: IDLE 001: SYNC_PA 010: SYNC_PB 011: DTYPE_PC 100: DLEN_PD 101: RX_ACTIVE
15:0	R	0x0	DATA_CAP_NUM Remains Data Counter Value See the value of the sampled valid data in real time.

4.4.6.22 0x0054 OWA Expand Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: OWA_EXP_DBG_1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	REPET_PERIOD_OF_FR_CNT Repetition period of the burst frame counter See the value of repetition period counter in real time.
15:0	R	0x0	SR_CNT Sample Rate Counter See the value of audio sample ratio in real time.

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Figures

Figure 5-1 DE Block Diagram 756

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5 Video and Graphics

5.1 Display Engine (DE)

The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 5-1.

The DE has the following features:

- Output size up to 4096 x 2048
- Supports seven alpha blending channels for main display and two display outputs
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports AFBC buffer decoder
- Supports vertical keystone correction
- Input format
  - Semi-planar of YUV422/YUV420/YUV411/P010/P210
  - Planar of YUV422/YUV420/ YUV411
  - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Output format: 8-bit or 10-bit YUV444/YUV422/YUV420/RGB444
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- 10-bit processing path for HDR video
- SmartColor5.0 for excellent display experience
  - Adaptive de-noising for compression noise or mosquito noise with yuv420/422 input
  - Adaptive super resolution scaler
  - Adaptive local dynamic contrast enhancement
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement (blue-stretch, green-stretch, and fresh tone correction) and
  - Skin tone protection
  - Hue gain, saturation gain, and value gain controller
  - Fully programmable color matrix
  - Dynamic gamma
- Supports write back for high efficient dual display and miracast

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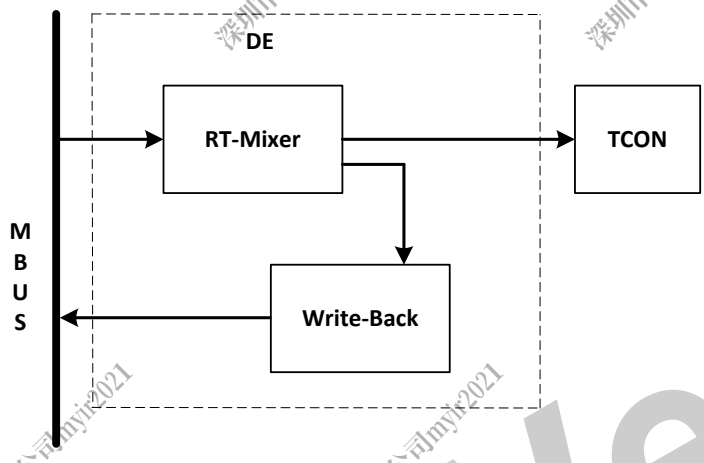
- Supports register configuration queue for register update function

Figure 5-1 DE Block Diagram



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5.2 De-interlacer (DI)

The De-interlacer (DI) converts the interlaced input video frame to progressive video frame.

The DI has the following features:

- Only off-line processing mode
- Video resolution from 32x32 to 2048x1280 pixel
- Input data format: 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined
- Output data format
  - 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined for DIT
  - YV12/planar YUV422 for TNR
- Weave/pixel-motion-adaptive de-interlace method
- Temporal noise reduction
- Film mode detection with video-on-film detection
- Performance
  - Module clock 120MHz for 1080P@60Hz YUV420 with all functions enable
  - Module clock 150MHz for 1080P@60Hz YUV422 with all functions enable

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5.3 Graphic 2D (G2D)

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- layer size up to 2048x2048 pixels
- Input format and output format contain the following:
  - YUV422 (semi-planar and planar format)
  - YUV420 (semi-planar and planar format)
  - P010, P210, P410, and Y8
  - ARGB8888, XRGB8888, RGB888, ARGB4444, ARGB1555, ARGB2101010, and RGB565
- Multiple rotation types
  - Horizontal flip and vertical flip
  - 0, 90, 180, or 270 degrees' rotation in clockwise direction

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5.4 Video Engine

5.4.1 Video Decoding

The Video Decoding consists of Video Control Firmware(VCF) running on ARM processor and embedded hardware Video Engine(VE). VCF gets the bitstream from topper software, parses bitstream, invokes the Video Engine, and generates the decoding image sequence. The decoder image sequence is transmitted by the video output controller to the display device under the control of the topper software.

The Video Decoding has the following features:

- Supports ITU-T H.265 Main/Main10, level 6.1
  - Maximum video resolution:8192x4320
  - Maximum decoding rate: 3840x2160@60fps, 10bit
- Supports VP9 Profile0/ Profile2, level 6.1
  - Maximum video resolution: 8192 x 4320
  - Maximum decoding rate: 3840x2160@60fps, 10bit
- Supports ITU-T H.264 Base/Main/High Profile@Level 4.2
  - Maximum video resolution: 3840 x 2160
  - Maximum decoding rate: 3840x2160@30fps, 8bit
- Supports ITU-T H.263 Base Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports VP8
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG4 Simple/ Advanced Simple Profile@Level 5
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG2 Main Profile, High Level
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG1 Main Profile, High Level
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps

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- Supports XVID
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports Sorenson Spark
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports AVS/AVS+ Jizhun Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports JPEG JFIF file format, Not Support Non-interleaved Scan
  - Maximum video resolution: 16384 x 16384
  - Maximum decoding rate: 1920x1080@60fps

5.4.2 Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPEG). The VE supports H.264 encoding, and JPEG supports JPEG/MJPEG encoding.

5.4.2.1 VE

The VE is a CODEC that supports H.264 protocol based on ASIC. It is custom-made for the IPC usage and features high compressing rate, low CPU usage, short delay and low power consumption.

The VE has the following features:

- Supports ITU-T H.264 High profile/Main profile/Baseline profile @Level 4.2 encoding
- Supports 16x16, 8x8 and 4x4 block sizes
- Search Range [H:+/-128, V: +/-24]
- Suports frame level and MB level rate control and supports three bit rate control modes: Constant Bit Rate (CBR), Variable Bit Rate (VBR), and FIXEDQP
- Motion compensation with 1/2 or 1/4 pixel precision
- Transform 4x4 and transform 8x8
- CABAC and CAVLC entropy encoding
- In-loop deblocking filter
- Multi-slice encoding
- Supports normal functions: intra-refresh, inter-only-in-P-frame
- Supports special functions: dynamic search window range

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- Supports region of interest(ROI) encoding with custom QP map
- Supports OSD front-end overlaying

5.4.2.2 JPEG

The JPEG is a high-performance JPEG encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPEG has the following features:

- ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - YCbCr4:2:2
  - YCbCr4:4:4
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlaying
- Supports the color-to-gray function

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6 Video Output Interfaces

6.1 eDP1.3

6.1.1 Overview

The Embedded Display Port (eDP) is a standard protocol in the digital display field. It is completely compatible with DP and consists of main link, auxiliary channel, and hot plugging.

The eDP includes the following features:

- Up to 2.5K@60fps and 4K@30fps
- 1-lane, 2-lane, or 4-lane transmission, up to 2.7 Gbps/lane
- Video formats: RGB, YCbCr4:4:4, and YCbCr4:2:2
- Color depth: 8-bit and 10-bit per channel
- Supports I2S interface
  - Supports mono sound, stereo sound, and 7.1 surround sound
  - Maximum sampling rate: 192 kHz
- Full link training
- Hot plug detection
- AUX channel
  - Maximum working frequency: 1MHz
  - Adopts Manchester-II encoding
- Clock spread spectrum
- Programmable voltage swing and pre-emphasis
- Embedded ESD

6.1.2 Functional Descriptions

6.1.2.1 External Signals

The following table describes the external I/O signals of the eDP module.

Table 6-1 eDP External Signals

Signal Name	Description	Type
EDP-AUXN	AUX channel Negative Input/Output	A I/O
EDP-AUXP	AUX channel Positive Input/Output	A I/O
EDP-HPD	Hot Plug Detection Signal	AI

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Signal Name	Description	Type
EDP-REXT	eDP External Reference Resistor	AO
EDP-TX0N	eDP Negative Output of Data Channel0	AO
EDP-TX0P	eDP Positive Output of Data Channel0	AO
EDP-TX1N	eDP Negative Output of Data Channel1	AO
EDP-TX1P	eDP Positive Output of Data Channel1	AO
EDP-TX2N	eDP Negative Output of Data Channel2	AO
EDP-TX2P	eDP Positive Output of Data Channel2	AO
EDP-TX3N	eDP Negative Output of Data Channel3	AO
EDP-TX3P	eDP Positive Output of Data Channel3	AO
VCC18-EDP	1.8V Analog Supply	P
VDD09-EDP	0.9V Digital Supply	P

6.1.2.2 PLL Configuration

Allwinner eDP TX IP contains a core PLL to generate core clock and high speed half-rate bit clock required for normal operation from the reference clock. If the additional pixel PLL is included, it can generate the pixel clock for controller from the reference clock.

- Core PLL VCO Clock

The frequency of core PLL VCO clock is controlled by pre-div divider (corepll_prediv [5:0], 0x0180[13:8]) and feedback divider (corepll_fbdiv [11:0], 0x0180[19:16]and 0x0180[31:24]). The pre-PLL VCO frequency is calculated as:

fcorevco = fref / corepll_prediv [5:0] * corepll_fbdiv [11:0]

For fractional operation, the fractional divider (corepll_frac [23:0], 0x0184 [7:0], 0x0184 [15:8] and 0x0184 [23:16]) should be turned on by setting the fractional divider control register (corepll_frac_pd [1:0], 0x0180[5:4]) to 2'b00. The core PLL VCO frequency is calculated as:

fcorevco = fref / corepll_prediv [5:0] * (corepll_fbdiv [11:0] +corepll_frac [23:0]/2^{24})

- Bit Clock

The frequency of bit clock should be half of the channel data rate and is controlled by post-div divider (corepll_postdiv [1:0], 0x0188[3:2]). The frequency of bit clock is calculated as:

fbitclk = fcorevco / corepll_postdiv [1:0]

- Core Clock

The frequency of core clock is calculated as:

fcoreclk = fbitclk / 10

- Pixel PLL VCO Clock

The frequency of pixel PLL VCO clock is controlled by pre-div divider (pixelpll_prediv [5:0], 0x00A1 [5:0]) and feedback divider (pixelpll_fbdiv [11:0], 0x0190 [19:16] and 0x0190 [31:24]). The pixel PLL VCO frequency is calculated as:

fpixelvco = fref / pixelpll_prediv [5:0] * pixelpll_fbdiv [11:0]

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For fractional operation, the fractional divider (pixelpll_frac [23:0], 0x019C [7:0], 0x019C [15:8] and 0x019C [23:16]) should be turned on by setting the fractional divider control register (pixelpll_frac_pd [1:0], 0x0190[5:4]) to 2'b00. The pixel PLL VCO frequency is calculated as:

fpixelvco = fref / pixelpll_prediv [5:0] * (pixelpll_fbdiv [11:0] +pixelpll_frac [23:0]/2^{24})

- Pixel Clock

The frequency of pixel clock is controlled by pixel clock divider a (pixelpll_pclkdiva [4:0], 0x0194 [4:0]), divider b (pixelpll_pclkdivb [1:0], 0x0194[9:8]) and divider c (pixelpll_pclkdivc [4:0], 0x0194 [20:16]). When pixelpll_pclkdiva [4:0] is set to be 5'h01, the frequency of pixel clock is calculated as:

fpclk = fpixelvco / (2*pixelpll_pclkdivb [1:0] *pixelpll_pclkdivc [4:0])

When pixelpll_pclkdiva [4:0] is not set to be 5'b01, the frequency of pixel clock is calculated as:

fpclk = fpixelvco / (2*pixelpll_pclkdiva [4:0] * pixelpll_pclkdivc [4:0])

NOTE

- The VCO running frequency should be kept in the range from 1 GHz to 3 GHz for core PLL and pixel PLL.
- PLL should be power down before configuration.

Table below gives the recommended core PLL configuration with 24MHz reference clock for typical link rates.

Table 6-2 Recommended Core PLL Configuration with 24MHz Reference Clock

Link Rate	1.62G	2.7G
core PLL VCO	1.62GHz	2.7GHz
bit clock	0.81GHz	1.35GHz
core clock	81MHz	135MHz
24MHz reference clock		
corepll_prediv[5:0]	6'h02	6'h02
corepll_fbdiv[11:0]	12'h087	12'h0e1
corepll_postdiv[1:0]	2'b01	2'b01
corepll_frac_pd[1:0]	2'b11	2'b11
corepll_frac[23:0]	24'b0	24'b0

Table below gives the recommended pixel PLL configuration with 24MHz reference clock for typical video formats.

Table 6-3 Recommended Pixel PLL Configuration with 24MHz Reference Clock

Video Format	720P/60	1080P/60	2160P/30
pixel PLL VCO	2.376GHz	2.376GHz	2.376GHz
pixel clock	74.25MHz	148.5MHz	297MHz
24MHz reference clock			

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Video Format	720P/60	1080P/60	2160P/30
pixelpll_prediv[5:0]	6'h01	6'h01	6'h01
pixelpll_fbdiv[11:0]	12'h063	12'h063	12'h063
pixelpll_pclkdiva[4:0]	5'h01	5'h01	5'h01
pixelpll_pclkdivb[1:0]	2'b01	2'b01	2'b01
pixelpll_pclkdivc[4:0]	5'h08	5'h04	5'h02
pixelpll_frac_pd[1:0]	2'b11	2'b11	2'b11
pixelpll_frac[23:0]	24'b0	24'b0	24'b0

6.1.2.3 Termination Configuration

In order to improve the signal quality, the termination resistance should match the impedance of PCB trace to minimize reflection. The differential characteristic impedance of differential pair trance on PCB is typical 100Ω. Thus the differential termination resistance of the receiver is preferred to be 100Ω around.

The termination resistance could be manually set by writing the differential termination resistance control registers (rtm [5:0], 0x01C4[5:0]/0x01C4[13:8]/0x01C4[21:16]/0x01C4[29:24]) with reference value for 4 data channels and AUX channel, respectively. The reference value for TT corner is calculated as:

RT = 4000 / rtm [5:0]

For example, if rtm [5:0] is set to 6'h28 and the decimal value is 40, the differential termination resistance will be 100Ω for TT corner. If rtm [5:0] is set to 6'h00, the termination resistance will be turned off. However, the termination resistance value varies along with the process variation.

Allwinner eDP TX IP also employs a resistance calibration mechanism to eliminate the process variation. The resistance calibration compares the termination resistor with the off-chip reference resistor, and adjusts its value to the target value set by calibration control register (rcal_sel [1:0], 0x01C0[26:25]) with insignificant error. The calibration result will be stored in calibration result register (rcal_val [5:0], 0x01C0[5:0]). After calibration, the transmitter termination resistance will be configured according to the calibration result.

The configuration method for termination resistance is controlled by the calibration bypass register (rcal_byp, 0x01C0[15]). If the termination resistance is desired to be set with the manual method, the resistance calibration should be bypassed.

The termination resistance calibration is configured as follow:

Step 1 configure the resistance calibration clock divider (0x01C0[14:8] and 0x01C0[23:16]) to set the clock frequency to be 100KHz around. For example, if the system clock is 100MHz, write 15'd1000 to the divider register.

Step 2 configure the resistance calibration target value (0x01C0[26:25]). For example, if 100Ω differential termination resistance is desired, write 2'b00 to register 0x01C0[26:25].

Step 3 configure the calibration bypass register (0x01C0[15]) to start the resistance calibration by writing 1'b1 to 0x01C0[15] firstly and then writing 1'b0 to register 0x01C0[15]. A falling

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edge of 0x01C0[15] will trigger the startup of the automatic resistance calibration. After calibration is done, the termination resistance of data channels and AUX channel will be configured according to the calibration result.

6.1.2.4 Transmitter Configuration

The transmitter in each data channel adopts 3-tap FFE (Feed Forward Equalizer) to compensate the channel loss, including the pre-cursor tap, main cursor tap and post-cursor tap. The pre-cursor tap and the post-cursor tap serve as the pre-emphasis.

The output levels of above 3 taps are all programmable and controlled by the driver current bias (Ibias). Ibias can be adjusted by current bias control register (isel [3:0], 0x01A8[3:0] 0x01A8[7:4] 0x01A4[27:24] and 0x01A4[31:28]) and is calculated as:

Ibias = 160uA + 40uA * isel [3:0]

There are also independent registers to adjust the levels of 3 taps, respectively.

The main cursor tap could be adjusted by registers output voltage level control registers (mainsel [4:0], 0x01AC[12:8]/0x01AC[4:0]/0x01A8[28:24]/0x01A8[20:16]) for 4 TMDS channels, respectively, and the output current level is calculated as:

Imain = Ibias * mainsel [4:0]

The pre-cursor tap could be adjusted by pre-cursor pre-emphasis level control registers (presel [2:0], 0x01B0[6:4]/0x01B0[2:0]/0x01B0[14:12]/0x01B0[10:8]) for 4 TMDS data channels, respectively, and the output current level is calculated as:

Ipre = Ibias * presel [2:0]

The post-cursor tap could be adjusted by post-cursor pre-emphasis level control registers (postsel [3:0], 0x01AC [23:20]/0x01AC [19:16]/0x01AC [31:28]/0x01AC [27:24]) for 4 TMDS channels, respectively, and the output current level is calculated as:

Ipost = Ibias * postsel [3:0]

The pre-cursor pre-emphasis level is calculated as:

Lpre = 20 * log [(Imain + Ipre) / (Imain – Ipre)]

The post-cursor pre-emphasis level is calculated as:

Lpost = 20 * log [(Imain + Ipost) / (Imain – Ipost)]

The combinations of different levels of 3 taps result in different transmitter eye and output voltage levels for different data pattern. The pre-emphasis levels should be carefully adjusted according to the actual condition to minimize the ISI introduced by the TX end. The following table gives the recommended transmitter configuration for different data rates.

Table 6-4 Recommended Transmitter Configuration for Different Data Rates

Register	Level	1.62Gbps	2.7Gbps
isel[3:0]	Voltage Swing Level 0	4’b0000	4’b0000
	Voltage Swing Level 1	4’b0010	4’b0010

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Register	Level	1.62Gbps	2.7Gbps
	Voltage Swing Level 2	4'b0100	4'b0100
	Voltage Swing Level 3	4'b0110	4'b0110
mainsel[4:0]		5'b11111	5'b11111
postsel[3:0]	Pre-emphasis Level 0	4'b0000	4'b0000
	Pre-emphasis Level 1	4'b0001	4'b0001
	Pre-emphasis Level 2	4'b0010	4'b0010
	Pre-emphasis Level 3	4'b0011	4'b0011
presel[2:0]		3'b000	3'b000

6.1.2.5 SSC Configuration

Allwinner eDP TX IP contains SSC function for data channel to deal with possible EMI problem. The features the SSC modulation are listed as follow:

- Support down spread and center spread modulation.
- Support 3-bit programmable modulation depth from 500ppm to 32000ppm.
- Support default triangular wave and programmable wave modulation.
- Support adjustable modulation frequency.

The SSC modulation is configured as follows:

Step 1 Configure the modulation mode control register (0x0180[20]) to select down spread or center spread.

Step 2 Configure the modulation frequency control register (0x0188[27:24]) to select SSC modulation frequency.

Step 3 Configure the modulation amplitude control register (0x0188[30:28]) to select SSC modulation amplitude.

Step 4 Configure the fractional PLL enable register (0x0180[5:4]) to 2'b00.

Step 5 Configure the SSC modulation enable register (0x0180[21]) to 1'b0.

The SSC modulation frequency is calculated as:

$f_{ssc} = f_{ref}$ /corepll_prediv[5:0]/ 128 / decimal value of 0x0188[27:24]

The default setting results in down spread SSC modulation with 31.25KHz frequency and 4000ppm amplitude with 24MHz reference clock.

6.1.3 Register List

Module Name	Base Address
EDP	0x0572_0000

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Register Name	Offset	Description
EDP_HPD_SCALE	0x0018	EDP HPD Scale Register
EDP_RST	0x001C	EDP Reset Register
EDP_HPD_EVENT	0x0080	HPD Event Status Register
EDP_HPD_INT	0x0084	Enable Hpd Plug Interrupt Register
EDP_HPD_PLUG	0x0088	HPD Plug Event Register
EDP_HPD_EN	0x008C	HPD Plug EN Register
EDP_CAPACITY	0x0100	Capacity Register
EDP_ANA_PLL_FBDIV	0x0180	CORE Pll Fbdiv Register
EDP_ANA_PLL_FRAC	0x0184	Core Pll Frac Register
EDP_ANA_PLL_POSDIV	0x0188	Core Pll Postdiv Register
EDP_ANA_PIXELPLL_FBDIV	0x0190	Pixel Pll Feedback Divide Register
EDP_ANA_PIXELPLL_DIV	0x0194	Pixel Pll Divider Register
EDP_ANA_PIXELPLL_FRAC	0x019C	Pixel Pll Frac Register
EDP_TX32_ISEL_DRV	0x01A4	Lane 32 Current Bias Control Register
EDP_TX_MAINSEL	0x01A8	Output Voltage Control Register
EDP_TX_POSTSEL	0x01AC	Post-cursor Pre-Emphasis Register
EDP_TX_PRESEL	0x01B0	Pre-cursor Pre-Emphasis Register
EDP_TX_RCAL_SEL	0x01C0	The Resistance Calibration Register
EDP_VIDEO_STREAM_EN	0x0200	Video_Stream Enable Register
EDP_SYNC_POLARITY	0x020C	Polarity of Hsync and Vsync Register
EDP_HACTIVE_BLANK	0x0210	H acitve and Blank Register
EDP_VACTIVE_BLANK	0x0214	V acitve and Blank Register
EDP_HWIDTH_FRONT_PORCH	0x0218	Hs Width and H Front Porch Register
EDP_VWIDTH_FRONT_PORCH	0x021C	Vs Width and V Front Porch Register
EDP_FRAME_UNIT	0x0220	Transfer Unit Register
EDP_SYNC_START	0x0224	Vstart and Hstart Register
EDP_MSA_MISC0	0x0228	MSA Miscellaneous0 Field Register
EDP_MSA_MISC1	0x022C	MSA Miscellaneous1 Field Register
EDP_HBLAN_LINK_CYC	0x0230	Hblank Link CYC Register
EDP_AUDIO	0x0300	Audio Register
EDP_PHY_AUX	0x0400	Phy Aux Register
EDP_AUX_TIMEOUT	0x0404	Aux Timeout Register
EDP_AUX_DATA1	0x0408	Aux Data1 Register
EDP_AUX_DATA2	0x040C	Aux Data2 Register
EDP_AUX_DATA3	0x0410	Aux Data3 Register
EDP_AUX_DATA4	0x0414	Aux Data4 Register
EDP_AUX_START	0x0418	Aux Write/Read Request Start register
EDP_AUDIO_VBLANK_EN	0x0500	Audio Vblank Transmit Register
EDP_AUDIO_HBLANK_EN	0x0504	Audio Hblank Transmit Register
EDP_BIST_CFG	0x2010	EDP Bist Control Register
EDP_RES1000_CFG	0x2014	EDP Res 1000 Config Register

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6.1.4 Register description

6.1.4.1 0x0018 EDP HPD Scale Register (default value 32篠h0800_0000)

Offset: 0x0018			Register Name: EDP_HPD_SCALE
Bit	Read/Write	Default/Hex	Description
31:4	R/W	0	/
3	R/W	0	REG_HPD_SCALE Scaling HPD Counter for Fast Simulation 0: Normal 1: Scaling
2:0	/	/	/

6.1.4.2 0x001C EDP Reset Register (default value 32篠h0000_0000)

Offset: 0x001C			Register Name: EDP_RST
Bit	Read/Write	Default/Hex	Description
31:4	R/W	0	/
3	R/W	0	REG_RESET_AUDIO 0: Normal 1: Reset
2	/	/	/
1	R/W	0	REG_RESET_PHY Reset PHY Logic 0: Normal 1: Reset
0	/	/	/

6.1.4.3 0x0080 EDP HPD Event Register (default value 32篠h0000_0000)

Offset: 0x0080			Register Name: EDP_HPD_EVENT
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0	STA_AUX_REPLY_EVENT
0	R	0	STA_HPD_EVENT HPD event, can be cleared by STA_HPD_PLUG

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6.1.4.4 0x0084 EDP HPD Interrupt Register (default value 32篠h0000_0000)

Offset: 0x0084			Register Name: EDP_HPD_INT
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0	Enable_aux_reply_event
0	R/W	0	ENABLE_HPD_PLUG_EVENT 1'b1 : Enable HPD plug interrupt

6.1.4.5 0x0088 EDP HPD Plug Register (default value 32篠h0000_0000)

Offset: 0x0088			Register Name: EDP_HPD_PLUG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0	HDP disconnection event, and this bit can be cleared by writing 1'b1.
1	R/W	0	STA_HPD_PLUG HPD Plug event, can be clear by write 1'b1
0	/	/	/

6.1.4.6 0x008C EDP HPD Enable Register (default value 32篠h0000_0000)

Offset: 0x008C			Register Name: EDP_HPD_EN
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0	HPD_PLUG_EN 1'b1:enable HPD plug event to assert the interrupt output
0	/	/	/

6.1.4.7 0x0100 EDP Capacity Register (default value 32篠h8001_0000)

Offset: 0x0100			Register Name: EDP_CAPACITY
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:26	R/W	0	EDP_PHY_RATE Rate Set for PHY. 3'b000: PHY rate setting by reg0x0100[5:4] 3'b001:2.16G 3'b010:2.43G
25:12	/	/	/

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Offset: 0x0100			Register Name: EDP_CAPACITY
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0	Transmit Enable Enable transmitter on the per lane. Bit8: lane 0 Bit9: lane 1 Bit10: lane 2 Bit11: lane 3
7:6	R/W	0	PHY_LANES number of lanes active: 2'b00:1 lane 2'b01:2 lanes 2'b10:4 lanes
5:4	R/W	0	PHY_RATE rate set for the PHY. 2'b00: RBR 1.62 G 2'b01: HBR 2.7G 2'b10/2'b11:reserved
3:0	R/W	0	TPS_SEL selects the training pattern. 0000: No training pattern. Normal stream data is transmitted instead. 0001: TPS1 0010: TPS2 0011: TPS3 0100: TPS4 0110: PRBS7 Others: Reserved

6.1.4.8 0x0180 EDP Analog Core PLL1 Register (default value 32篠h5830_0130)

Offset: 0x0180			Register Name: EDP_ANA_PLL_FBDIV
Bit	Read/Write	Default/Hex	Description
31:24	R/W	8'h58	REG_COREPLL_FBDIV [7:0] CORE PLL feedback divide value
23:22	/	/	/
21	R/W	1	REG_DISABLE_SSCG 1'b0: Enable SSC 1'b1: Disable SSC
20	R/W	1	REG_DOWNSPREAD 1'b0: Center spread 1'b1: Down spread

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Offset: 0x0180			Register Name: EDP_ANA_PLL_FBDIV
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0	EG_COREPLL_FBDIV [11:8] CORE PLl Feedback Divide Value
15:14	/	/	/
13:8	R/W	1	DA_COREPLL_PREDIV [5:0] CORE PLL Reference Divide Value
7:6	/	/	/
5:4	R/W	2'b11	DA_COREPLL_FRAC_PD [1:0] Fractional Divider Control Register
3:1	/	/	/
0	R/W	0	REG_COREPLL_PD 1: power down pixel PLL

6.1.4.9 0x0184 EDP Analog Core PLL2 Register (default value 32篠h2200_0000)

Offset: 0x0184			Register Name: EDP_ANA_PLL_FRAC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	REG_COREPLL_FRAC [7:0] The fractional part of CORE PLL feedback divide value
15:8	R/W	0	REG_COREPLL_FRAC [15:8] The fractional part of CORE PLL feedback divide value
7:0	R/W	0	REG_COREPLL_FRAC [23:16] The fractional part of CORE PLL feedback divide value

6.1.4.10 0x0188 EDP Analog Core Pll3 Register (default value 32篠h4700_0090)

Offset: 0x0188			Register Name: EDP_ANA_PLL_POSDIV
Bit	Read/Write	Default/Hex	Description
31	/	/	/

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Offset: 0x0188			Register Name: EDP_ANA_PLL_POSDIV
Bit	Read/Write	Default/Hex	Description
30:28	R/W	2'b10	REG_SPREAD [2:0] SSC Modulation Amplitude Control 3'b000: 0 ppm 3'b001: 500 ppm 3'b010: 1000 ppm 3'b011: 2000 ppm 3'b100: 4000 ppm 3'b101: 8000 ppm 3'b110: 16000 ppm 3'b111: 32000 ppm
27:24	R/W	4'b0111	REG_DIVVAL [3:0] SSC modulation frequency control
3:2	R/W	0	DA_COREPLL_POSTDIV [1:0] CORE PLL reference divide value 2'b00: divide by 1 2'b01: divide by 2 2'b10: divide by 4 2'b11: divide by 8
1:0	/	/	/

6.1.4.11 0x018C EDP Analog AUX CLOCK Register (default value 0x0100_0000)

Offset: 0x018C			Register Name: EDP_ANA_AUX_CLOCK
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0	da_corepll_clk_div_16m AUX CLK sources from aux_16m which is divided by bitclock. Because it is an integer division, the configured value makes aux_16M close to 16 MHz. aux_16m=bitclock/8/da_corepll_clk_div_16m

6.1.4.12 0x0190 EDP Analog Pixel Pll1 Register (default value 32篠h5000_0430)

Offset: 0x0190			Register Name: EDP_ANA_PIXELPLL_FBDIV
Bit	Read/Write	Default/Hex	Description
31:24	R/W	8'h50	DA_PIXELPLL_FBDIV [7:0] PIXEL PLL feedback divide value
23:20	/	/	/

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Offset: 0x0190			Register Name: EDP_ANA_PIXELPLL_FBDIV
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0	DA_PIXELPLL_FBDIV [11:8] PIXEL PLL feedback divide value
15:14	/	/	/
13:8	R/W	4	DA_PIXELPLL_PREDIV [5:0] PIXEL PLL reference divide value
5:4	R/W	2'b11	DA_PIXELPLL_FRAC_PD [1:0] Fractional divider control register
0	R/W	0	REG_PIXELPLL_PD 1: power down pixel PLL

6.1.4.13 0x0194 EDP Analog Pixel Pll2 Register (default value 32篠h0101_0001)

Offset: 0x0194			Register Name: EDP_ANA_PIXELPLL_DIV
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	1	PIXEL PLL divider c [4:0] divide by 1~31
15:10	/	/	/
9:8	R/W	0	PIXEL PLL divider b [1:0] 2'b00: divide by 1 2'b01: divide by 2 2'b10: divide by 3 2'b11: divide by 5
7:5	/	/	/
4:0	R/W	1	PIXEL PLL divider a [4:0] divide by 1~31

6.1.4.14 0x019C EDP Analog Pixel Pll3 Register (default value 32篠h0000_0000)

Offset: 0x019C			Register Name: EDP_ANA_PIXELPLL_FRAC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	da_pixelpll_frac [7:0] The fractional part of PIXEL PLL feedback divide value
15:8	R/W	0	da_pixelpll_frac [15:8] The fractional part of PIXEL PLL feedback divide value

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Offset: 0x019C			Register Name: EDP_ANA_PIXELPLL_FRAC
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0	da_pixelpll_frac [23:16] The fractional part of PIXEL PLL feedback divide value

6.1.4.15 0x01A4 EDP Current Bias Control Register (default value 32篠h5500_0F0F)

Offset: 0x01A4			Register Name: EDP_TX32_ISEL_DRV
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x5	da_tx_isel_drv_d3[3:0] Current bias control register of lane3. Ibias = 160uA + 40uA * isel[3:0]
27:24	R/W	0x5	da_tx_isel_drv_d2[3:0] Current bias control register of lane2. Ibias = 160uA + 40uA * isel[3:0]

6.1.4.16 0x01A8 EDP TX Voltage Register (default value 32篠h1010_0055)

Offset: 0x01A8			Register Name: EDP_TX_MAINSEL
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	da_tx_mainsel_d2[4:0] Output voltage level control registers of lane2. Imain = Ibias * mainsel[4:0]
20:16	R/W	0x10	da_tx_mainsel_d3[4:0] Output voltage level control registers of lane3. Imain = Ibias * mainsel[4:0]
7:4	R/W	0x5	da_tx_isel_drv_d1[3:0] Current bias control register of lane1. Ibias = 160uA + 40uA * isel[3:0]
3:0	R/W	0x5	da_tx_isel_drv_d0[3:0] Current bias control register of lane0. Ibias = 160uA + 40uA * isel[3:0]

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6.1.4.17 0x01AC EDP TX Pre-emphasis1 Register (default value 32篠h0202_1010)

Offset: 0x01AC			Register Name:EDP_TX_POSTSEL
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x2	da_tx_postsel_d1[3:0] Post-cursor pre-emphasis level control registers of lane1. Ipost = Ibias * postsel[3:0]
27:24	R/W	0x2	da_tx_postsel_d0[3:0] Post-cursor pre-emphasis level control registers of lane0. Ipost = Ibias * postsel[3:0]
23:20	R/W	0x2	da_tx_postsel_d3[3:0] Post-cursor pre-emphasis level control registers of lane3. Ipost = Ibias * postsel[3:0]
19:16	R/W	0x2	da_tx_postsel_d2[3:0] Post-cursor pre-emphasis level control registers of lane2. Ipost = Ibias * postsel[3:0]
12:8	R/W	0x2	da_tx_mainsel_d0[4:0] Output voltage level control registers of lane0. Imain = Ibias * mainsel[4:0]
4:0	R/W	0x2	da_tx_mainsel_d1[4:0] Output voltage level control registers of lane1. Imain = Ibias * mainsel[4:0]

6.1.4.18 0x01B0 EDP TX Pre-emphasis2 Register (Default value 32篠hF000_0000)

Offset: 0x01B0			Register Name:EDP_TX_PRESEL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0	4'b1111: Current regulation, adjust the amplitude by the isel in 0x1A8 and 0x1AC. 4'b0000: Voltage regulation, adjust the amplitude by the mainsel in 0x1A8 and 0x1AC.
23:15	/	/	/
14:12	R/W	0	da_tx_presel_d1[2:0] Pre-cursor pre-emphasis level control registers of lane1. Ipre = Ibias * presel[2:0]

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Offset: 0x01B0			Register Name:EDP_TX_PRESEL
Bit	Read/Write	Default/Hex	Description
10:8	R/W	0	da_tx_presel_d0[2:0] Pre-cursor pre-emphasis level control registers of lane0. Ipre = Ibias * presel[2:0]
6:4	R/W	0	da_tx_presel_d3[2:0] Pre-cursor pre-emphasis level control registers of lane3. Ipre = Ibias * presel[2:0]
2:0	R/W	0	da_tx_presel_d2[2:0] Pre-cursor pre-emphasis level control registers of lan2. Ipre = Ibias * presel[2:0]

6.1.4.19 0x01C0 EDP Resistance Calibration Register (default value 32篠h020e_8100)

Offset: 0x01C0			Register Name: EDP_TX_RCAL_SEL
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:25	R/W	0x1	reg_bg_rcal_sel [1:0] The resistance calibration, adjust the termination resistor to approach the off-chip reference resistor.
23:16	R/W	0x0e	reg_rtcal_freqdiv [7:0] The resistance calibration clock divider.
15	R/W	0x1	reg_rtcal_bypass Control the configuration method for termination resistance.
14:8	R/W	0x1	reg_rtcal_freqdiv [14:8] The resistance calibration clock divider.
5:0	R/W	0x0	reg_bg_rcal_val [5:0] The resistance calibration result.

6.1.4.20 0x0200 EDP Video Stream Set Register (default value 32篠h0100_0000)

Offset: 0x0200			Register Name: EDP_VIDEO_STREAM_EN
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

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Offset: 0x0200			Register Name: EDP_VIDEO_STREAM_EN
Bit	Read/Write	Default/Hex	Description
24	R/W	1	reg_alt_screamble_reset alternate_scrambler_reset_capable, a setting of 0 indicates that this is an eDP device that can use the eDP alternate scrambler reset value of FFFEh
23:21	/	/	/
20:16	R/W	0	video_mapping the bit width of each color 5'd0: RGB 6bits 5'd1: RGB 8bits 5'd2: RGB 10bits 5'd3: RGB 12bits 5'd4: RGB 16bits 5'd5: YCbCR4:4:4 8bits 5'd6: YCbCr4:4:4 10bits 5'd7: YCbCr4:4:4 12bits 5'd8: YCbCr4:4:4 16bits 5'd9: YCbCR4:2:2 8bits 5'd10: YCbCr4:2:2 10bits 5'd11: YCbCr4:2:2 12bits 5'd12: YCbCr4:2:2 16bits
15:6	/	/	/
5	R/W	0	Video_stream_en 0:vide0 stream disable 1: video stream enable
4:0	/	/	/

6.1.4.21 0x020C EDP Sync Polarity Register (default value 32篠h0000_0000)

Offset: 0x020C			Register Name: EDP_SYNC_POLARITY
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0	eg_tx_polarity [1:0] polarity of hsync and vsync. bit1: Hsync polarity bit0: Vsync polarity if the vsync/hsync of simulation video source is active low, then the corresponding bit in reg_tx_polarity should set 0; or active high

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6.1.4.22 0x0210 EDP Horizontal Active Blank Register (default value 32篠h0280_0280)

Offset: 0x0210			Register Name: EDP_HACTIVE_BLANK
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h0280	reg_tx_hactive [15:0] Active horizontal pixels per line
15:2	R/W	14'hA0	reg_tx_hblank [13:0]/htotal – hactive
1:0	/	/	/

6.1.4.23 0x0214 EDP Vertical Active Blank Register (default value 32篠h002D_01E0)

Offset: 0x0214			Register Name: EDP_VACTIVE_BLANK
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h002D	reg_tx_vblank [15:0] vtotal – vactive
15:0	R/W	16'h01E0	reg_tx_vactive [15:0] Active vertical pixels per line

6.1.4.24 0x0218 EDP Horizontal Width Front Porch Register (default value 32篠h0060_0010)

Offset: 0x0218			Register Name: EDP_HWIDTH_FRONT_PORCH
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h0060	reg_tx_hswidth [15:0] Hsync width
15:0	R/W	16'h0010	reg_tx_h_front_porch [15:0] htotal – hactive – hstart

6.1.4.25 0x021C EDP Vertical Width Front Porch Register (default value 32篠h0020_000A)

Offset: 0x021C			Register Name: EDP_VWIDTH_FRONT_PORCH
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h0060	reg_tx_hswidth [15:0] Hsync width
15:0	R/W	16'h0010	reg_tx_h_front_porch [15:0] htotal – hactive – hstart

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6.1.4.26 0x0220 EDP Frame Unit Register (default value 32篠h0280_C796)

Offset: 0x0220			Register Name:EDP_FRAME_UNIT
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0	reg_avg_per_tu_frac fractional portion of average valid symbol per Transfer Unit, calculate formula refer to DP spec. For example, pixel clock is 27M RGB888, @2.7Gbps 4lanes,then average valid symbol per Transfer Unit = 4.8, configure reg_avg_per_tu_frac to 8
15:14	/	/	/
13:7	R/W	7’h0f	reg_line_rd_thres An asynchronous FIFO needed to deal with video data from pixel clock domain to link clock domain, reg_line_rd_thres is related to read enable of FIFO. According to video format and main link rate, this value may changed as following description: reg_line_rd_thres = average valid symbol per TU<6?7'd32: hblank < 80? 7'd12:7'd16;
6:0	R/W	7’h16	reg_avg_per_tu_int integer portion of average valid symbol per Transfer Unit, calculate formula refer to DP spec. For example, pixel clock is 27M RGB888, @2.7Gbps 4lanes, then average valid symbol per Transfer Unit = 4.8, configure reg_avg_per_tu_int to 4

6.1.4.27 0x0224 EDP Sync Start Register (default value 32篠h0023_0090)

Offset: 0x0224			Register Name: EDP_SYNC_START
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16’h0043	reg_tx_vstart [15:0] Vsync width + Vback porch width
15:0	R/W	16’h0090	reg_tx_hstart [15:0] Hsync width + Hback porch width

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6.1.4.28 0x0228 EDP MSA MISC0 Register (default value 32'h0000_0000)

Offset: 0x0228			Register Name:EDP_MSA_MISC0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	reg_tx_msa_misc0[7:0] MSA Miscellaneous0 field bit0: 1'b0, IP Link clock and main video stream clock asynchronous. tips: the bit must set 1'b0. bit1~bit7: color encoding format, please refer to DP spec for example: 6'b0000000, 6'b 0010000, 6'b 0100000, 6'b 0110000, 6'b 1000000 (6,8, 10, 12, 16 bits/color respectively)
23:0	/	/	/

6.1.4.29 0x022C EDP MSA MISC1 Register (default value 32'h0000_0000)

Offset: 0x022C			Register Name:EDP_MSA_MISC1
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	reg_tx_msa_misc1[7:0] MSA Miscellaneous1 field please refer to DP spec
23:0	/	/	/

6.1.4.30 0x0230 EDP Horizontal Blank Link Cycle Register (default value 32'h0000_005A)

Offset: 0x0230			Register Name: EDP_HBLAN_LINK_CYC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	16'h005A	hblank_link_cyc How many link clock cycles of hblank. hblank *link_clk/pixel_clk, For example, pixel clock is 27M hblank 138, @2.7Gbps 4lanes, hblank_link_cyc = 138*67.5/27. link_clk = symbol clock /4

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6.1.4.31 0x0300 EDP Audio Register (default value 32篠h1200_1A02)

Offset: 0x0300			Register Name:EDP_AUDIO
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0	audio_mute 1'b1: Sets the AudioMute_Flag in VB-ID 1'b0: Clears the AudioMute_Flag in VB-ID.
14:12	R/W	1	audio_channel_num Number of audio channels. 3'b000:1 channel 3'b001:2 channel Others:8 channel
11:10	/	/	/
9:5	R/W	5'h10	audio_data_width Indicates the bit width of the data samples at input. 5'b10000: 16 bits 5'b10100: 20 bits 5'b11000: 24 bits
4:1	R/W	1	audio_data_en Indicates whether the input data is valid. Bit 1: indicates whether the channels 1,2 input data is valid. Bit 2: indicates whether the channels 3,4 input data is valid. Bit 3: indicates whether the channels 5,6 input data is valid. Bit 4: indicates whether the channels 7,8 input data is valid. tips: must be consistent with audio_channel_num(0x0300[14:12])
0	R/W	0	Audio_interface_sel 1'b0: select I2S as input(default) 1'b1:select OWA as input

6.1.4.32 0x0400 EDP AUX Command Register (default value 32篠h0000_0000)

Offset: 0x0400			Register Name:EDP_PHY_AUX
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0	cfg_phy_aux_enc_cmd [31:0] CMD(4bits)

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Offset: 0x0400			Register Name:EDP_PHY_AUX
Bit	Read/Write	Default/Hex	Description
27:8	R/W	0	addr(20bits)
7:4	/	/	/
3:0	R/W	0	len(4bits)

6.1.4.33 0x0404 EDP AUX Reply Register (default value)

Offset: 0x0404			Register Name: EDP_AUX_TIMEOUT
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	/	aux_timeout as described in spec, TX must wait for a Reply Time-out period of 400us before initiating the next AUX Request transaction. When timeout, this bit will set to 1
16	R	/	Aux_reply_received 1'b1: waiting for AUX_REPLY 1'b0: received AUX_REPLY
15:8	/	/	/
7:4	R	/	Aux_reply_cmd 4'b0000: ack 4'b0001:nack
3:0	/	/	/

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6.1.4.34 0x0408 EDP AUX Data1 Register (default value 32篠h0000_0000)

Offset: 0x0408			Register Name:EDP_AUX_DATA1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	cfg_phy_aux_data [127:0], composed of 16'h0408, 16'h040C, 16/h0410, 16'h0414, totally 16bytes, including data(8bits*16), payload for write request or read request. tips: for a write request, filled attached data needs to be transmitted for a read reply, stored the replied data write request: cfg_phy_aux_data [31:0]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [7:0]: write to DPCD address+0 as the byte0 cfg_phy_aux_data [31:24]: write to DPCD address+3 as the byte3 read reply: cfg_phy_aux_data [31:0]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [7:0]: read from DPCD address+0 as the byte0 cfg_phy_aux_data [31:24] read from DPCD address+3 as the byte3

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6.1.4.35 0x040C EDP AUX Data2 Register (default value 32篠h0000_0000)

Offset: 0x040C			Register Name:EDP_AUX_DATA2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	write request: cfg_phy_aux_data [63:32]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [39:32]: write to DPCD address+4 as the byte4 cfg_phy_aux_data [63:56]: write to DPCD address+7 as the byte7 read reply: cfg_phy_aux_data [63:32]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [39:32]: read from DPCD address+4 as the byte4 cfg_phy_aux_data [63:56] read from DPCD address+7 as the byte7

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6.1.4.36 0x0410 EDP AUX Data3 Register (default value 32篠h0000_0000)

Offset: 0x0410			Register Name:EDP_AUX_DATA3
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	write request: cfg_phy_aux_data [95:64]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example: cfg_phy_aux_data [71:64]: write to DPCD address+8 as the byte8 cfg_phy_aux_data [95:88]: write to DPCD address+11 as the byte11 read reply: cfg_phy_aux_data [95:64]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [71:64]: read from DPCD address+8 as the byte8 cfg_phy_aux_data [95:88] read from DPCD address+11 as the byte11

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6.1.4.37 0x0414 EDP AUX Data4 Register (default value 32篠h0000_0000)

Offset: 0x0414			Register Name:EDP_AUX_DATA4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	write request: cfg_phy_aux_data [127:96]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [103:96]: write to DPCD address+12 as the byte12 cfg_phy_aux_data [127:120]: write to DPCD address+15 as the byte15 read reply: cfg_phy_aux_data [127:96]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [103:96]: read from DPCD address+12 as the byte12 cfg_phy_aux_data [127:120] read from DPCD address+15 as the byte15

6.1.4.38 0x0418 EDP AUX Start Register (default value 32篠h0000_0000)

Offset: 0x0418			Register Name:EDP_AUX_START
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	W/R	0	cfg_phy_aux_start the trigger signal to start a write/read request by AUX requester (Source to Device), write 0 or 1.

6.1.4.39 0x0500 EDP Audio Vertical Blank Enable Register (default value 32篠h0000_0000)

Offset: 0x0500			Register Name: EDP_AUDIO_VBLANK_EN
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	W/R	0	sdp_audio_stream_vertical_en 1'b1: Enable audio stream is transmitted during vertical blanking period.

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Offset: 0x0500			Register Name: EDP_AUDIO_VBLANK_EN
Bit	Read/Write	Default/Hex	Description
0	W/R	0	sdp_audio_timestamp_vertical_en 1'b1: Enable send audio timestamp SDP once every video frame during vertical blanking period.

6.1.4.40 0x0504 EDP Audio Horizontal Blank Enable Register (default value 32篠h0000_0000)

Offset: 0x0504			Register Name: EDP_AUDIO_HBLANK_EN
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	W/R	0	sdp_audio_stream_horizontal_en 1'b1: Enable audio stream is transmitted during horizontal blanking period.
0	W/R	0	sdp_audio_timestamp_horizontal_en 1'b1: Enable send audio timestamp SDP once every video frame during horizontal blanking period

6.1.4.41 0x2010 EDP Bist Configuration Register (default value 32篠h0000_0000)

Offset: 0x2010			Register Name: EDP_BIST_CFG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0	Bist test pass flag
4	R	0	Bist test done flag
3:2	/	/	/
1	W/R	0	Bist test enable
0	W/R	0	Bist test select

6.1.4.42 0x2014 EDP RES1000 Configuration Register (default value 32篠h0000_0033)

Offset: 0x2014			Register Name:EDP_RES1000_CFG
Bit	Read/Write	Default/Hex	Description
31:9	R/W	0x0	Reserved
8	R/W	0x0	reg_sel,1000ohms resistor manual control enable,0:disable 1,enable
7:6	R/W	0x0	Reserved
5:0	R/W	0x33	di_reg[5:0], 1000ohms resistor manual control bits

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6.2 MIPI DSI

The Display Serial Interface is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.02 and a D-PHY module which is compliance with MIPI DPHY specification V1.1.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI V1.02
- Up to 1.5 Gbit/s for each lane
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports 4+4-lane MIPI DSI, up to 2560 x 1600@60fps, 3840x2160@45fps, and 4096 x 2160@45fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Continuous and non-continuous lane clock modes
- Generic commands support bidirectional communication in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Supports hardware checksum

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6.3 TCON LCD

6.3.1 Overview

The Timing Controller_LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- Three TCON LCD controllers: TONC_LCD0, TCON_LCD1, and TCON_LCD2
- TCON_LCD0 supports the following
  - Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
  - Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
  - Supports LVDS interface with dual link, up to 1920 x 1080@60fps
  - Supports LVDS interface with single link, up to 1366 x 768@60fps
  - Dither function for RGB888, RGB666, and RGB565
  - Supports i8080 interface, up to 800 x 480@60fps
  - Supports BT.656 interface for NTSC and PAL
  - Supports MIPI DSI interface with dual link, up to 2560x1600@60fps, 3840x2160@45fps and 4096x2160@45fps
  - Supports MIPI DSI interface with single link, up to 1920x1200@60fps
- TCON_LCD1 supports MIPI DSI interface with single link, up to 1920x1200@60fps
- TCON_LCD2 supports the following:
  - Supports RGB interface with DE/SYNC mode, up to 1280x720@60fps
  - Supports serial RGB/dummy RGB interface, up to 800x480@60fps
  - Supports LVDS interface with dual link, up to 1920x1080@60fps
  - Supports LVDS interface with single link, up to 1366x768@60fps
  - Supports i8080 interface, up to 800x480@60fps
  - Supports BT656 interface for NTSC and PAL
  - Dither function for RGB888, RGB666, and RGB565

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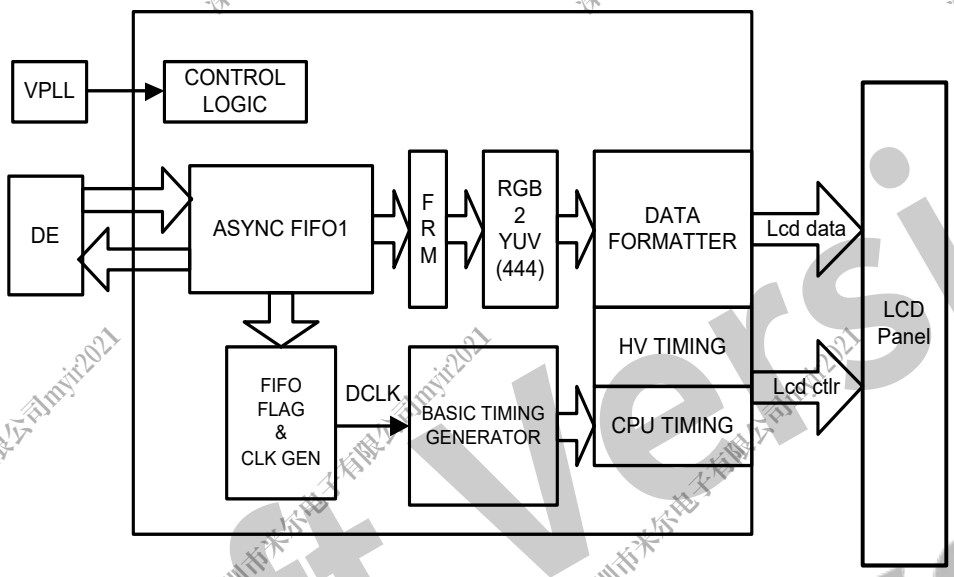
6.3.2 Block Diagram

Figure 6-1 TCON_LCD Block Diagram



6.3.3 Functional Description

6.3.3.1 External Signals

The following table describes the external I/O signals of LCD and LVDS.

Table 6-5 TCON_LCD External Signals

Signal Name	Description	Type
LCD0-D[23:0]	LCD Data Input/Output	I/O
LCD0-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD0-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD0-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD0-DE	LCD Data Output Enable	O
LCD0-TRIG	LCD0 Sync It is input from peripherals for sync	I
LCD1-D[23:0]	LCD Data Input/Output	I/O
LCD1-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD1-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD1-HSYNC	LCD Horizontal Sync It indicates one new scan line	O

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Signal Name	Description	Type
LCD1-DE	LCD Data Output Enable	O
LCD1-TRIG	LCD1 Sync It is input from peripherals for sync	I
LCD2-TRIG	LCD2 Sync It is input from peripherals for sync	I
LVDS0-D[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	AO
LVDS0-D[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	AO
LVDS0-CKN	LVDS0 Negative Port of Clock	AO
LVDS0-CKP	LVDS0 Positive Port of Clock	AO
LVDS1-D[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	AO
LVDS1-D[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	AO
LVDS1-CKN	LVDS1 Negative Port of Clock	AO
LVDS1-CKP	LVDS1 Positive Port of Clock	AO
LVDS2-D[3:0]P	LVDS2 Positive Port of Data Channel [3:0]	AO
LVDS2-D[3:0]N	LVDS2 Negative Port of Data Channel [3:0]	AO
LVDS2-CKP	LVDS2 Positive Port of Clock	AO
LVDS2-CKN	LVDS2 Negative Port of Clock	AO
LVDS3-D[3:0]P	LVDS3 Positive Port of Data Channel [3:0]	AO
LVDS3-D[3:0]N	LVDS3 Negative Port of Data Channel [3:0]	AO
LVDS3-CKP	LVDS3 Positive Port of Clock	AO
LVDS3-CKN	LVDS3 Negative Port of Clock	AO

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

Table 6-6 The Correspondence between LCD and RGB

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0			
LCD0-D23	R4	R5	R7
LCD0-D22	R3	R4	R6
LCD0-D21	R2	R3	R5
LCD0-D20	R1	R2	R4
LCD0-D19	R0	R1	R3
LCD0-D18	-	R0	R2
LCD0-D17	-	-	R1
LCD0-D16	-	-	R0
LCD0-D15	G5	G5	G7
LCD0-D14	G4	G4	G6
LCD0-D13	G3	G3	G5
LCD0-D12	G2	G2	G4
LCD0-D11	G1	G1	G3
LCD0-D10	G0	G0	G2

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LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0-D9	-	-	G1
LCD0-D8	-	-	G0
LCD0-D7	B4	B5	B7
LCD0-D6	B3	B4	B6
LCD0-D5	B2	B3	B5
LCD0-D4	B1	B2	B4
LCD0-D3	B0	B1	B3
LCD0-D2	-	B0	B2
LCD0-D1	-	-	B1
LCD0-D0	-	-	B0
LCD1			
LCD1-D23	R4	R5	R7
LCD1-D22	R3	R4	R6
LCD1-D21	R2	R3	R5
LCD1-D20	R1	R2	R4
LCD1-D19	R0	R1	R3
LCD1-D18	-	R0	R2
LCD1-D17	-	-	R1
LCD1-D16	-	-	R0
LCD1-D15	G5	G5	G7
LCD1-D14	G4	G4	G6
LCD1-D13	G3	G3	G5
LCD1-D12	G2	G2	G4
LCD1-D11	G1	G1	G3
LCD1-D10	G0	G0	G2
LCD1-D9	-	-	G1
LCD1-D8	-	-	G0
LCD1-D7	B4	B5	B7
LCD1-D6	B3	B4	B6
LCD1-D5	B2	B3	B5
LCD1-D4	B1	B2	B4
LCD1-D3	B0	B1	B3
LCD1-D2	-	B0	B2
LCD1-D1	-	-	B1
LCD1-D0	-	-	B0

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The multiplex relationship among LCD, LVDS, and DSI is shown as follows.

Table 6-7 The Correspondence among LCD, LVDS, and DSI.

LCD I/O	LVDS I/O	DSI I/O
LCD0		
LCD0-D0	/	/
LCD0-D1	/	/
LCD0-D2	LVDS0-D0P	DSI0-D0P
LCD0-D3	LVDS0-D0N	DSI0-D0N
LCD0-D4	LVDS0-D1P	DSI0-D1P
LCD0-D5	LVDS0-D1N	DSI0-D1N
LCD0-D6	LVDS0-D2P	DSI0-CKP
LCD0-D7	LVDS0-D2N	DSI0-CKN
LCD0-D8	/	/
LCD0-D9	/	/
LCD0-D10	LVDS0-CKP	DSI0-D2P
LCD0-D11	LVDS0-CKN	DSI0-D2N
LCD0-D12	LVDS0-D3P	DSI0-D3P
LCD0-D13	LVDS0-D3N	DSI0-D3N
LCD0-D14	LVDS1-D0P	DSI1-D0P
LCD0-D15	LVDS1-D0N	DSI1-D0N
LCD0-D16	/	/
LCD0-D17	/	/
LCD0-D18	LVDS1-D1P	DSI1-D1P
LCD0-D19	LVDS1-D1N	DSI1-D1N
LCD0-D20	LVDS1-D2P	DSI1-CKP
LCD0-D21	LVDS1-D2N	DSI1-CKN
LCD0-D22	LVDS1-CKP	DSI1-D2P
LCD0-D23	LVDS1-CKN	DSI1-D2N
LCD0-CLK	LVDS1-D3P	DSI1-D3P
LCD0-DE	LVDS1-D3N	DSI1-D3N
LCD0-HSYNC	/	/
LCD0-VSYNC	/	/
LCD1		
LCD1-D0	LVDS2-D0P	/
LCD1-D1	LVDS2-D0N	/
LCD1-D2	LVDS2-D1P	/
LCD1-D3	LVDS2-D1N	/
LCD1-D4	LVDS2-D2P	/
LCD1-D5	LVDS2-D2N	/
LCD1-D6	LVDS2-CKP	/
LCD1-D7	LVDS2-CKN	/
LCD1-D8	LVDS2-D3P	/

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LCD I/O	LVDS I/O	DSI I/O
LCD1-D9	LVDS2-D3N	/
LCD1-D10	LVDS3-D0P	/
LCD1-D11	LVDS3-D0N	/
LCD1-D12	LVDS3-D1P	/
LCD1-D13	LVDS3-D1N	/
LCD1-D14	LVDS3-D2P	/
LCD1-D15	LVDS3-D2N	/
LCD1-D16	LVDS3-CKP	/
LCD1-D17	LVDS3-CKN	/
LCD1-D18	LVDS3-D3P	/
LCD1-D19	LVDS3-D3N	/
LCD1-D20	/	/
LCD1-D21	/	/
LCD1-D22	/	/
LCD1-D23	/	/
LCD1-CLK	/	/
LCD1-DE	/	/
LCD1-HSYNC	/	/
LCD1-VSYNC	/	/

6.3.3.2 Clock Sources

The following table describes the clock sources of TCON_LCD.

Table 6-8 TCON_LCD Clock Sources

Clock sources	Description	Module
PLL_VIDEO0(3x)	By default, PLL_VIDEO0(4x) is 1188 MHz, PLL_VIDEO0(3x) is 792MHz.	CCU
PLL_VIDEO0(4x)		
PLL_VIDEO1(3x)	By default, PLL_VIDEO1(4x) is 1188 MHz, PLL_VIDEO1(3x) is 792MHz.	
PLL_VIDEO1(4x)		
PLL_VIDEO2(4x)	By default, PLL_VIDEO2(4x) is 1188 MHz.	
PLL_VIDEO3(4x)	By default, PLL_VIDEO3(4x) is 1188 MHz.	
PLL_PERI0(2x)	By default, PLL_PERI0(2x) is 1.2 GHz.	

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6.3.3.3 Control Signal and Data Port Mapping

NOTE

The mapping relationship between LCD1 signals and data port is the same as the multiplexing between LCD0 signals and data port, except LVDS and DSI.

For multiplex relationship among LCD, LVDS, and DSI, please refer to Table 6-7 The Correspondence among LCD, LVDS, and DSI.

		SYNC RGB				YUV		DC	CPU Cmd	CPU 18-bit	CPU 18-bit							CPU 16-bit	CPU 18-bit			CPU 16-bit		CPU 18-bit		LVDS		DSI	
External I/O	Internal pin	Para	Serial RGB			BT656	BT601	YUV422		256K	256K							64K	256K			64K		256K		Single Link		DSI 0	DSI 1
			1st	2nd	3rd						1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd	LVDS0	LVDS1		
LCD0_VSYNC	IO0	VSYNC					VSYNCC	VSYNC			CS																		
LCD0_HSYNC	IO1	HSYNC					HSYNC				RD																		
LCD0_CLK	IO2	DCLK				PCLK	DCLK	DCLK			WR																D3N		D3N
LCD0_DE	IO3	DE					DE	HSYNC			RS																D3P		D3P
LCD0_D23	D23	R7							D23	R5	R5	B5	G5	R5		R5	B5	R4									CKN		D2N
LCD0_D22	D22	R6							D22	R4	R4	B4	G4	R4		R4	B4	R3									CKP		D2P
LCD0_D21	D21	R5							D21	R3	R3	B3	G3	R3		R3	B3	R2									D2N		CKN
LCD0_D20	D20	R4							D20	R2	R2	B2	G2	R2		R2	B2	R1									D2P		CKP
LCD0_D19	D19	R3							D19	R1	R1	B1	G1	R1		R1	B1	R0									D1N		D1N
LCD0_D18	D18	R2							D18	R0	R0	B0	G0	R0		R0	B0	G5									D1P		D1P
LCD0_D17	D17	R1							D17																		D0N		D0N
LCD0_D16	D16	R0							D16																		D0P		D0P
LCD0_D15	D15	G7							D15	G5								G4											
LCD0_D14	D14	G6							D14	G4								G3											
LCD0_D13	D13	G5							D13	G3																D3N		D3	
LCD0_D12	D12	G4	D71	D72	D73	D7	D7	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2	D3P		D3P	
LCD0_D11	D11	G3	D61	D62	D63	D6	D6	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1	CKN		D2	
LCD0_D10	D10	G2	D51	D52	D53	D5	D5	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0	CKP		D2P	
LCD0_D9	D9	G1							D9																				
LCD0_D8	D8	G0							D8																				
LCD0_D7	D7	B7	D41	D42	D43	D4	D4	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5	D2N		CK	
LCD0_D6	D6	B6	D31	D32	D33	D3	D3	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4	D2P		CK	
LCD0_D5	D5	B5	D21	D22	D23	D2	D2	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3	D1N		D1	
LCD0_D4	D4	B4	D11	D12	D13	D1	D1	D1	D4	B2								B1				G4	B1	G5	B2	D1P		D1P	
LCD0_D3	D3	B3	D01	D02	D03	D0	D0	D0	D3	B1								B0				G3	B0	G4	B1	D0N		D0	
LCD0_D2	D2	B2							D2	B0														G3	B0	D0P		D0P	
LCD0_D1	D1	B1							D1																				
LCD0_D0	D0	B0							D0																				

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6.3.3.4 HV interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are defined as:

Table 6-9 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

Figure 6-2 HV Interface Vertical Timing

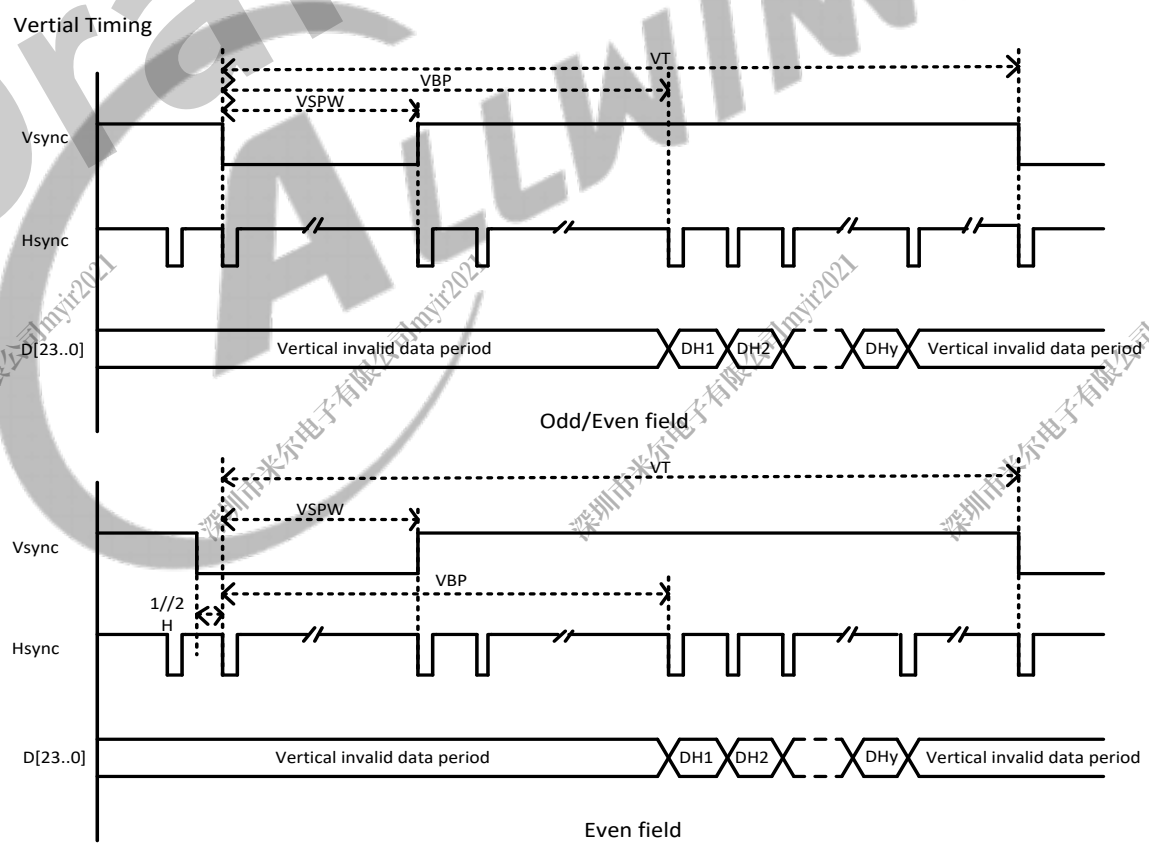

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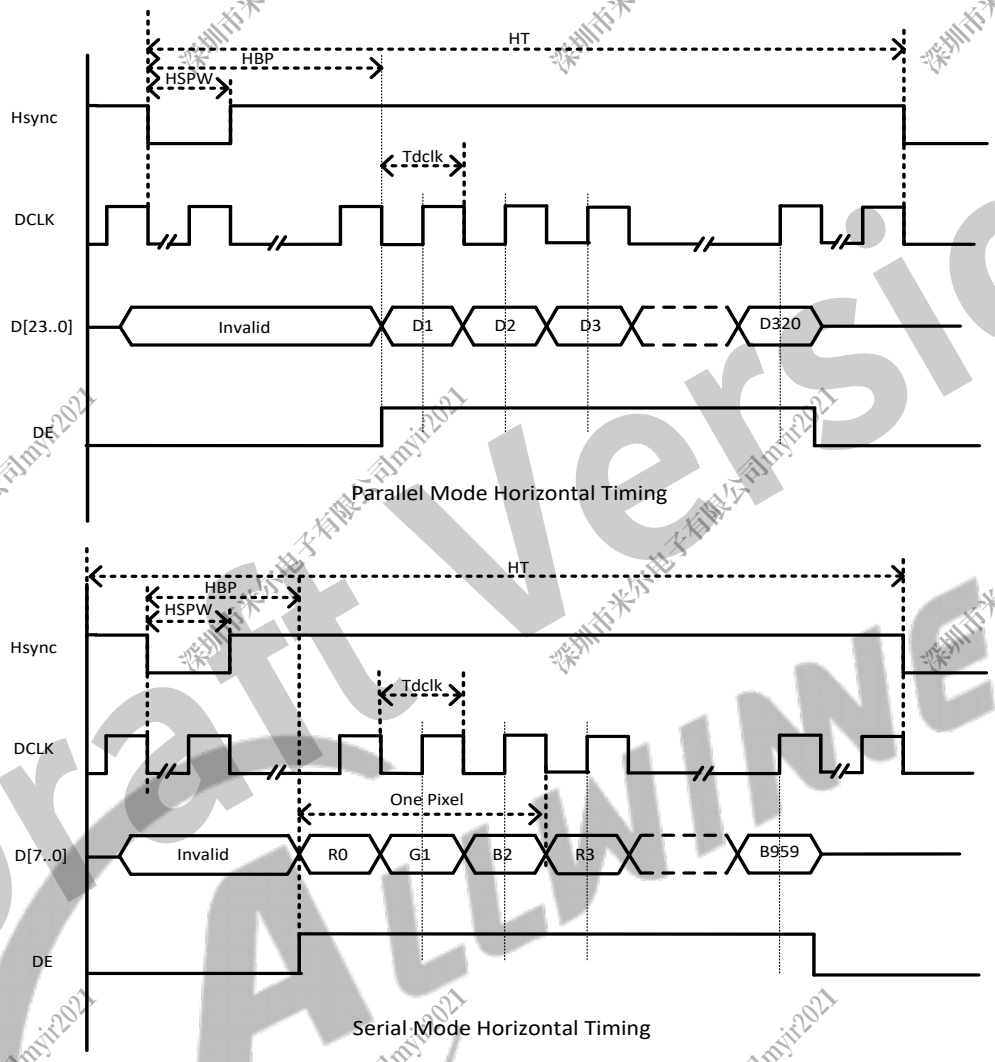
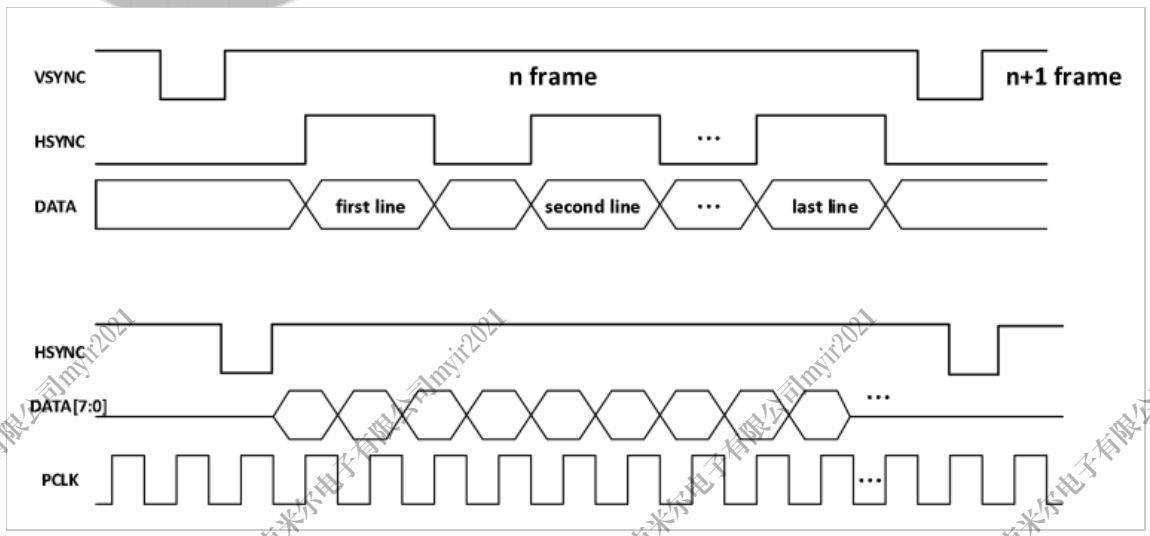
Figure 6-3 HV Interface Horizontal Timing



6.3.3.5 DC (Digital Camera) Interface

Figure 6-4 DC Interface Timing



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6.3.3.6 BT.656 Interface

When the data in YUV format is transmitted in HV mode, TCON_LCD0 needs to use ITU-R BT.656 protocol. Compared with standard CSI interface, there are not synchronous signals, such as FIELD, VSYN, and HSYN, for BT.656 interface. The horizontal and vertical synchronization information of images are built in the BT.656 data stream. BT.656 data format only includes PCLK signal, DVLD signal (unnecessary), and data bus signal. The BT.656 protocol provides 8-bit width and interlaced data of YUV422 format. The encoding format for each line is as follows:

Line=End of Active Video (EAV) + horizontal blanking data (80H/10H) + Start of Active Video (SAV) + valid data (UYVY)

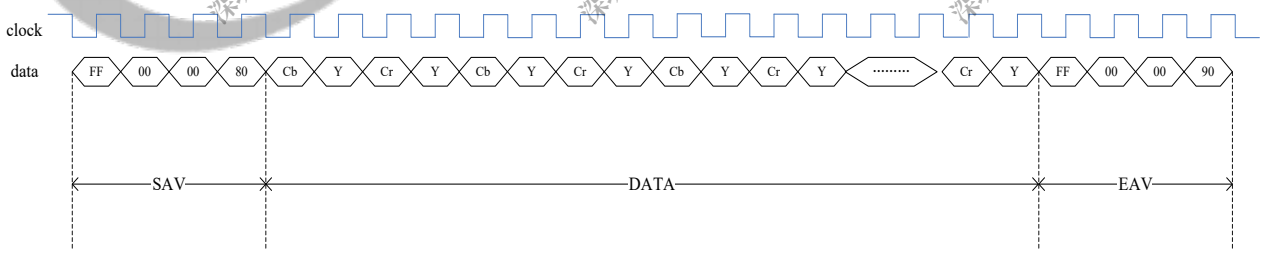
Both of EAV and SAV consist of a 4-bytes sequence in the following format: FF 00 00 XY. The first three bytes are fixed as hexadecimal 8'hFF 8'h00 8'h00. The fourth byte of XY is used to control the format. The assignment of the XY bit is shown in the following table.

Table 6-10 Analysis of XY Signal

BIT	7	6	5	4	3	2	1	0
XY	1'b1	F	V	H	P3	P2	P1	P0
F	0: during field 1 1: during field 2							
V	1: during field blanking 0: field active							
H	0: in SAV 1: in EAV							
P3~P0	protection bits. Single channel: P3=V^H，P2=F^H，P1=F^V，P0=F^V^H Multi-Channel: Channel ID							

During single-channel data transmission, P3~P0 is used for calibration. The transmission timing is shown in the following figure.

Figure 6-5 Singl-channel Transmission Timing



In programming, the final output format is finished in rgb2yuv, which means the 8-bit data format output by rgb2yuv is the format shown above. ctrl_data_out just inplement the pin-mapping of the data.

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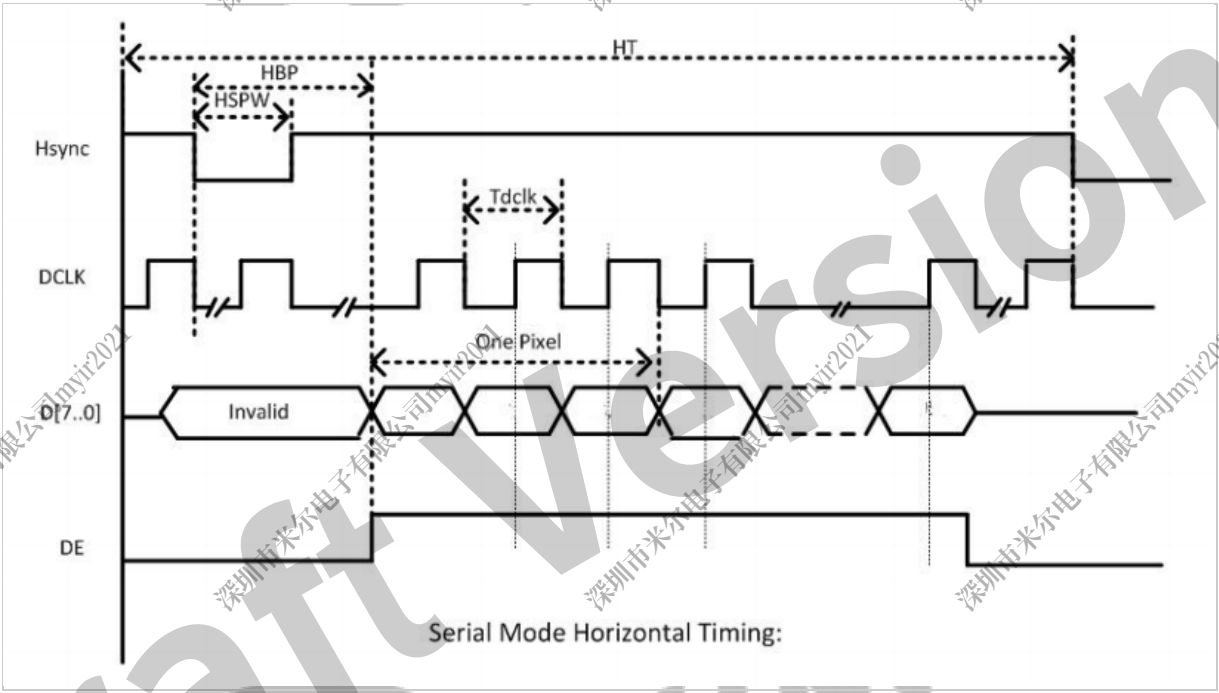
6.3.3.7 BT.601 Interface

Figure 6-6 BT.601 Interface Timing



6.3.3.8 i8080 Interface

The i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. The CPU control signals are active low.

Table 6-11 CPU Panel Signals

Signal Name	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

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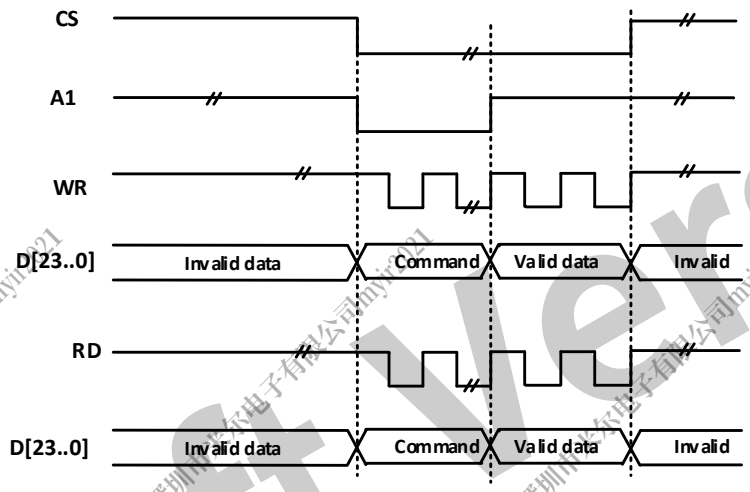
The following figure relationship between basic timing and CPU timing. WR is 180o delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

Figure 6-7 i8080 Interface Timing



When CPU I/F is in IDLE state, it can generate WR/RD timing by setting “Lcd_CPUI/F”. The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

6.3.3.9 LVDS Interface

Table 6-12 LVDS Panel Signals

Signal Name	Description	Type
CKP	The positive port of clock	O
CKN	The negative port of clock	O
D0P	The positive port of data channel 0	O
D0N	The negative port of data channel 0	O
D1P	The positive port of data channel 1	O
D1N	The negative port of data channel 1	O
D2P	The positive port of data channel 2	O
D2N	The negative port of data channel 2	O
D3P	The positive port of data channel 3	O
D3N	The negative port of data channel 3	O

NOTE

T527 adopts 7:1 LVDS interface.

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The following figures show the timing of LVDS interface.

Figure 6-8 LVDS Single Link JEDIA Mode Interface Timing

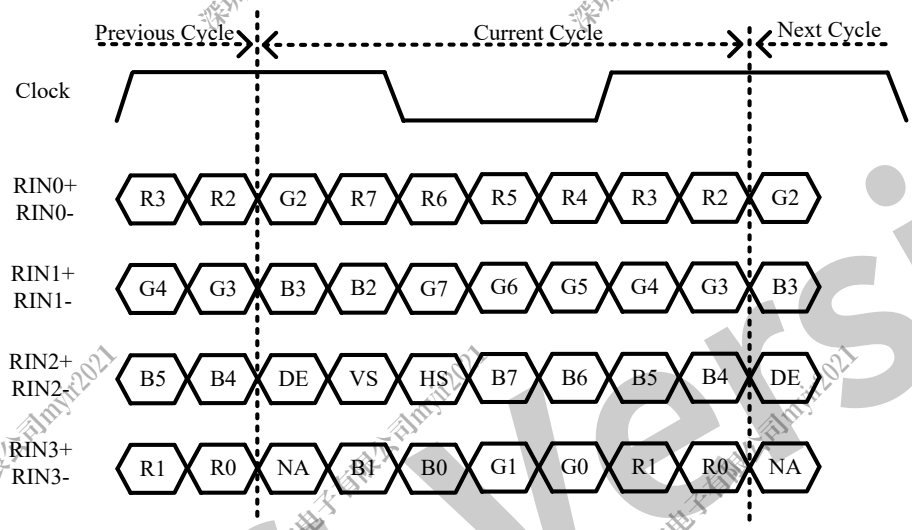
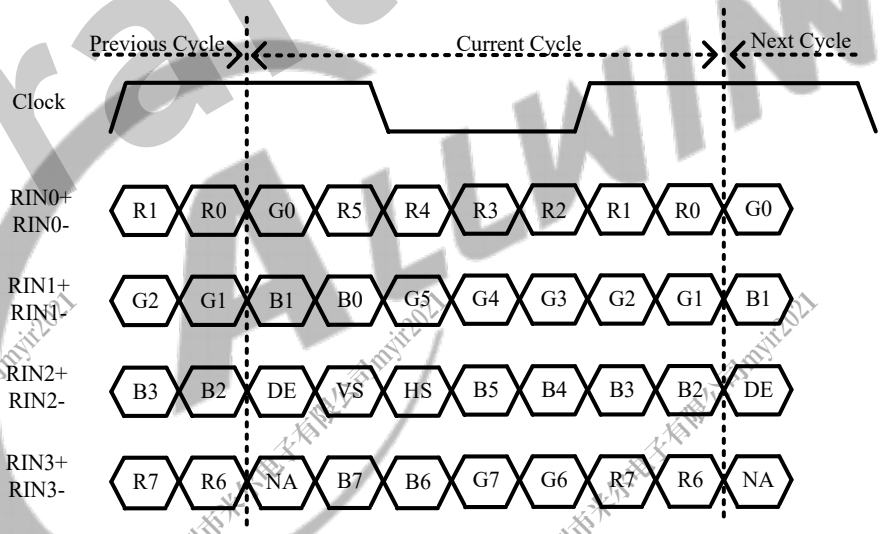


Figure 6-9 LVDS single link NS Mode interface timing



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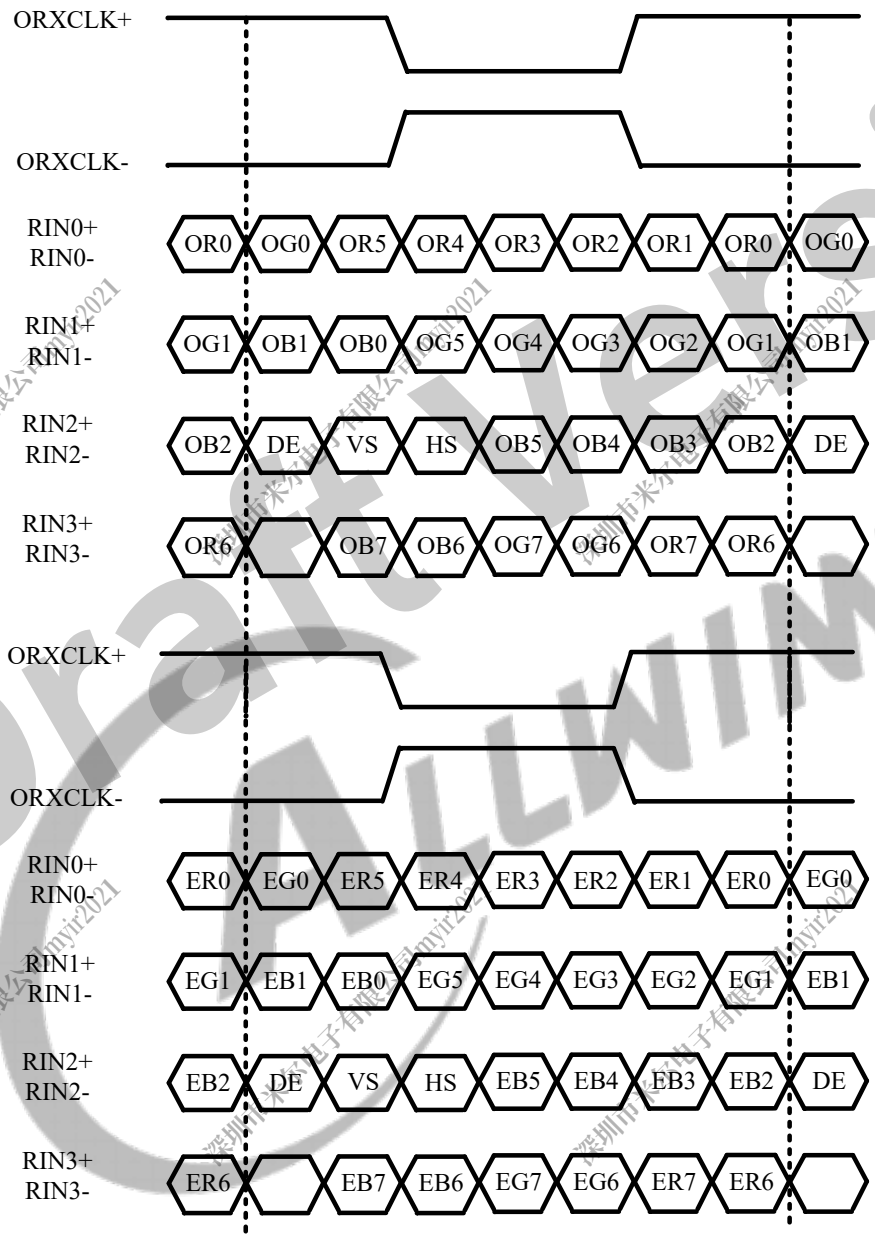
The following figure shows the timing of one mode of the dual-link LVDS, in which odd pixel channel and even pixel channel output to a single-monitor. Dual-link can be configured in the LVDS_DUAL_CHANEL_SRC_SEL bit (bit [30]) of LCD_LVDS_ANA0_REG register.

Figure 6-10 LVDS Dual Link NS Mode Interface Timing



6.3.3.10 CEU Module

This module enhances color data from DE .

R′ = Rr*R + Rg*G + Rb*B + Rc

G′ = Gr*R + Gg*G + Gb*B + Gc

B′ = Br*R + Bg*G + Bb*B + Bc

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb s13 (-16, 16)

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Rc, Gc, Bc	s19 (-16384, 16384)
R, G, B	u8 [0-255]

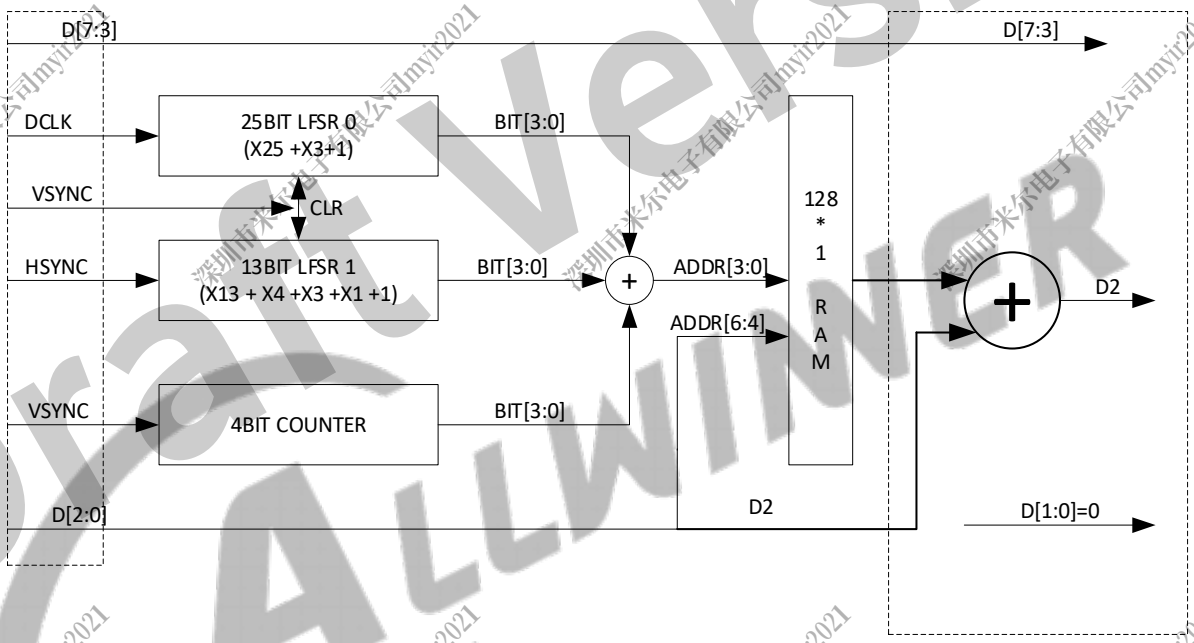
R′ has the range of [Rmin, Rmax]

G′ has the range of [Rmin, Rmax]

B′ has the range of [Rmin, Rmax]

6.3.3.11 FRM Module

Figure 6-11 FRM Module



6.3.3.12 MIPI DSI Notes

The requirements on MIPI DSI mode are as follows.

- When using MIPI DSI as display interface, the data clk of TCON needs be started firstly.
- When it is used with DSI video mode, the setting of block space needs to meet the following relationship.

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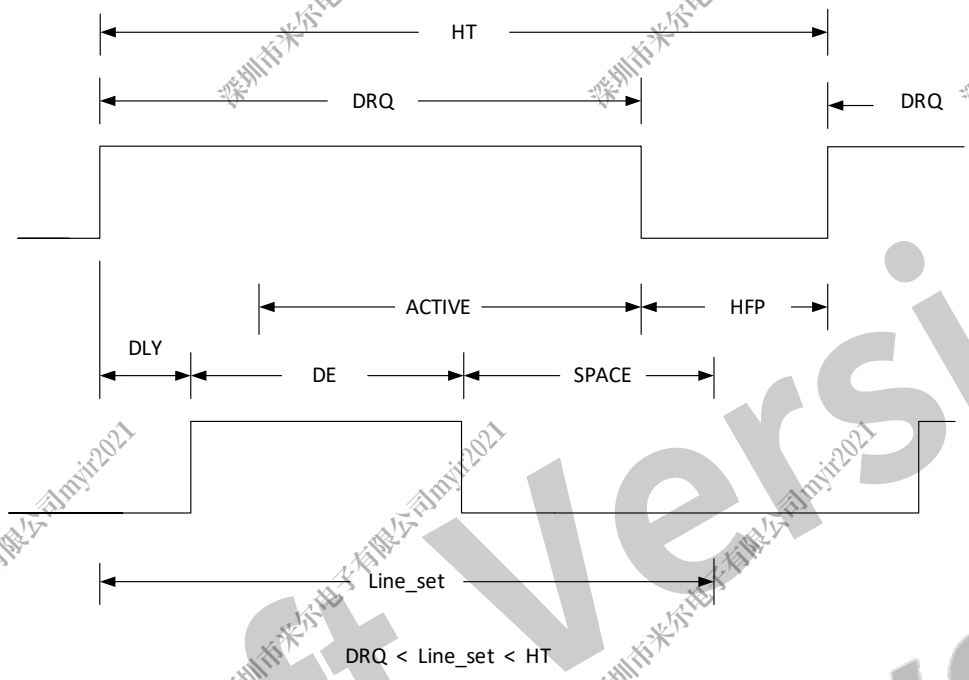
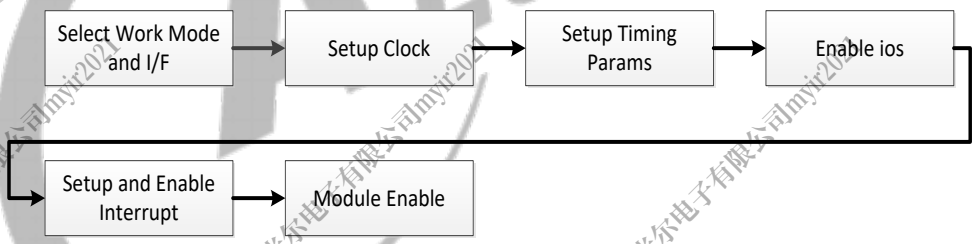
Figure 6-12 The Data Timing of MIPI DSI Video Mode



6.3.4 Programming Guidelines

6.3.4.1 Enabling HV Mode

Figure 6-13 HV Mode Initial Process



Parallel RGB

Step 1 Select HV interface type

Configure LCD_CTL_REG[LCD_IF] (reg0x40) to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE] (reg0x58) to 0 to select 24bit/1cycle parallel mode.

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24bit/1cycle parallel mode;

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Step 2 Clock configuration

NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0–2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

lcd_dev[sel]->lcd_dclk.dclk_en = en;

lcd_dev[sel]->lcd_dclk.dclk_div = div;

Step 3 Set sequence parameters

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASIC2_REG.VT needs be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic0.x = x-1;

lcd_dev[sel]->lcd_basic0.y = y-1;

lcd_dev[sel]->lcd_basic1.ht = ht-1;

lcd_dev[sel]->lcd_basic1.hbp = hbp-1;

lcd_dev[sel]->lcd_basic2.vt = vt*2;

lcd_dev[sel]->lcd_basic2.vbp = vbp-1;

lcd_dev[sel]->lcd_basic3.hspw = hspw-1;

lcd_dev[sel]->lcd_basic3.vspw = vspw-1;

Step 4 Open IO output

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0~3_INV (reg0x88).

Step 5 Set and open interrupt function

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The LCD_GINT0_REG (reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG (reg0x8) sets the interrupt line position of Line interrupt mode.

V interrupt:

lcd_dev[sel]->lcd_gint0.vb_en = 1;

Line interrupt:

lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

lcd_dev[sel]->lcd_gint0.line_en = 1;

Step 6 Open module enable

Enable LCD_CTL_REG.LCD_EN (reg0x40) and LCD_GCTL_REG.LCD_EN (reg0x00).

lcd_dev[sel]->lcd_ctl.lcd_en = 1;

lcd_dev[sel]->lcd_gctl.lcd_en = 1;

The following table is an example of typical parameter configuration.

Table 6-13 HV Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB
	LCD_CTL_REG (0x0040)	32'h0000_0041	Select HV (Sync+DE) mode
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actule value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0010_0000	/

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Step	Register	Typical Value of Simulation	Description
	LCD_GINT0_REG (0x004)	32'h2000_0000	/
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

Step 1 Select HV interface type

Set LCD_CTL_REG.LCD_IF (reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE (reg0x58) to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;

Step 2,3. Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASIC2_REG.VT needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;

6.3.4.2 Enabling DC Mode

The DC mode configuration process is similar to the parallel mode of HV mode.

6.3.4.3 Enabling BT.656 Mode

The BT.656 mode configuration process is similar to the parallel mode of HV mode. The following table is an example of typical parameter configuration.

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Table 6-14 BT.656 Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB
	LCD_CTL_REG (0x0040)	32'h0000_0041	Select HV (Sync+DE) mode
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actule value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0010_0000	/
	LCD_GINT0_REG (0x004)	32'h2000_0000	/
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

6.3.4.4 Enabling BT.601 Mode

The BT.601 mode configuration process is similar to the parallel mode of HV mode.

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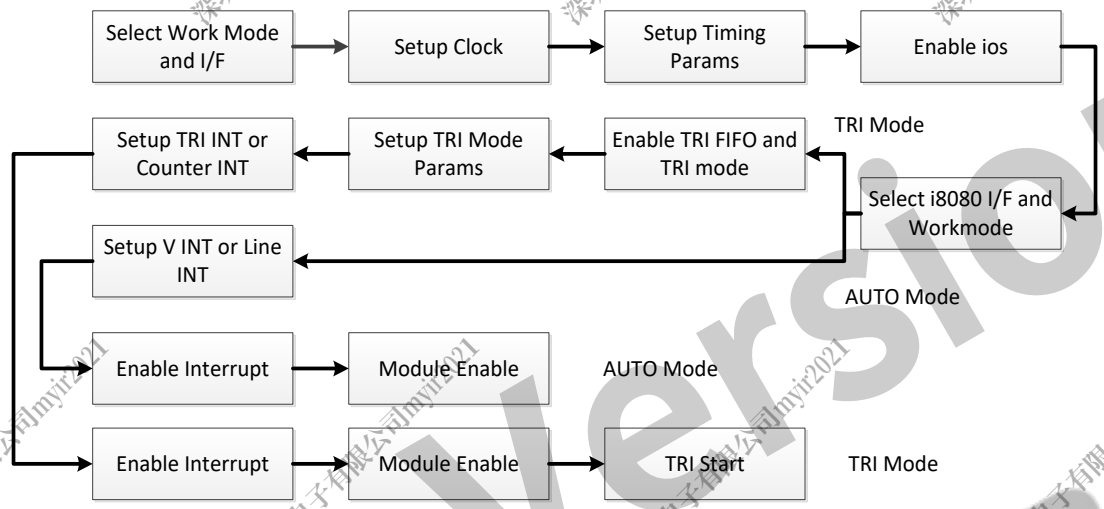
6.3.4.5 Enabling i8080 Mode

Figure 6-14 i8080 Mode Initial Process



Step 1 Select i8080 interface type.

Step 2 The step is the same as HV mode, but pulse adjustment function is invalid.

Step 3 The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.

Step 4 The step is the same as HV mode.

Step 5 Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------**If For TRI mode**----------

Step 6 Open TRI FIFO switch, and TRI mode function.

Step 7 Set parameters of TRI mode, including block size, block space and block number.

NOTE

- When output interface is parallel mode, then the setting value of block space parameter is not less than 20.
- When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.
- When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.
- When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

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Step 8 Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.

Step 9 Open the total switch of interrupt.

Step 10 Open the total enable of interrupt.

Step 11 Operate “tri start” operation (the bit1 of LCD_CPU_IF_REG is set to "1").

----------If For Auto mode----------

Step 6 Set and open V interrupt or Line interrupt, the step is the same as HV mode.

Step 7 Open module total enable.

6.3.5 Register List

Module Name	Base Address
TCON_LCD0	0x0550 1000
TCON_LCD1	0x0550 2000
TCON_LCD2	0x0573 1000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04(N=0~5)	LCD FRM Seed Register
LCD_FRM_TAB_REG	0x002C+N*0x04(N=0~3)	LCD FRM Table Register
LCD_3D_FIFO_REG	0x003C	LCD 3D Fifo Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register

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Register Name	Offset	Description
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1
LCD_LVDS_IF_REG	0x0084	LCD LVDS Interface Register
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG0	0x0110+N*0x4(N=0~2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_MUL_REG1	0x0120+N*0x4(N=0~2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_MUL_REG2	0x0130+N*0x4(N=0~2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10(N=0~2)	LCD CEU Coefficient Register1
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04(N=0~2)	LCD CEU Coefficient Register2
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
LCD_LVDS_ANA0_REG	0x0220	LCD LVDS Analog Register0
LCD_LVDS_ANA1_REG	0x0224	LCD LVDS Analog Register1
FSYNC_GEN_CTRL_REG	0x0228	LCD FSYNC Generate Control Register
FSYNC_GEN_DLY_REG	0x022C	LCD FSYNC Generate Delay Register
LCD_SYNC_CTL_REG	0x0230	LCD Sync Control Register
LCD_SYNC_POS_REG	0x0234	LCD Sync Position Register
LCD_SLAVE_STOP_POS_REG	0x0238	LCD Slave Stop Position Register

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6.3.6 Register Description

6.3.6.1 0x0000 LCD Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN When it's disabled, the module will be reset to idle state. 0: Disable 1: Enable
30:0	/	/	/

6.3.6.2 0x0004 LCD Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_VB_INT_EN Enable the Vb interrupt. 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN Enable the line interrupt. 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN Enable the trigger finish interrupt. 0: Disable 1: Enable
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN Enable the trigger counter interrupt. 0: Disable 1: Enable
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/

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Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 match the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when CPU trigger mode finish. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when SYNC by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W0C	0x0	FSYNC_INT_INV Enable the FSYNC interrupt set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame. Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the FSYNC signal in every frame. Write 0 to clear it.

6.3.6.3 0x0008 LCD Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger (including inactive lines). Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:0	/	/	/

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6.3.6.4 0x0010 LCD FRM Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_FRM_EN Enable the dither function. 0: Disable 1:Enable
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R The R component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
5	R/W	0x0	LCD_FRM_MODE_G The G component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
4	R/W	0x0	LCD_FRM_MODE_B The B component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST Set the test mode of dither function. 00: FRM 01: Half 5/6bit, half FRM 10: Half 8bit, half FRM 11: Half 8bit, half 5/6bit

6.3.6.5 0x0014+N*0x04(N=0~5) LCD FRM Seed Register (Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04(N=0~5)			Register Name: LCD_FRM_SEED_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

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Offset: 0x0014+N*0x04(N=0~5)			Register Name: LCD_FRM_SEED_REG
Bit	Read/Write	Default/Hex	Description
24:0	R/W	0x0	SEED_VALUE Set the seed for LFSR used in dither function. N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Note: avoid set it to 0.

6.3.6.6 0x002C+N*0x04(N=0~3) LCD FRM Table Register (Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0~3)			Register Name: LCD_FRM_TAB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

6.3.6.7 0x003C LCD 3D FIFO Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	3D_FIFO_BIST_EN Enable the 3D FIFO bist test function. 0: Disable 1: Enable
30:24	/	/	/
23:20	R/W	0x0	3D_FIFO_OVERLAP The number of overlap when dual DSI mode = 3D_FIFO_OVERLAP, only valid when 3D_FIFO_SETTING set as 2.
19:15	/	/	/
14:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line = 3D_FIFO_HALF_LINE_SIZE+1, only valid when 3D_FIFO_SETTING set as 2.

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Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	Read/Write	Default/Hex	Description
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING Set the work mode of 3D FIFO. 0: Bypass 1: Used as normal FIFO 2: Used as 3D interlace FIFO 3: Reserved

6.3.6.8 0x0040 LCD Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN It executes at the beginning of the first blank line of LCD timing. 0: Disable 1: Enable
30:26	/	/	/
25:24	R/W	0x0	LCD_IF Set the interface type of LCD controller. 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved
23	R/W	0x0	LCD_RB_SWAP Enable the function to swap red data and blue data in FIFO1. 0: Default 1: Swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20	R/W	0x0	LCD_INTERLACE_EN This flag is valid only when LCD_EN == 1 0: Disable 1: Enable
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DLY The unit of delay is T_{line}. NOTE: valid only when LCD_EN == 1

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Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL LCD Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reversed 111: Gridding Check

6.3.6.9 0x0044 LCD Data Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable. 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others: Reversed
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk /DCLKDIV Note: 1.If dclk1&dclk2 used, DCLKDIV >=6 2.If only dclk is used, DCLKDIV >=1

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6.3.6.10 0x0048 LCD Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	WIDTH_X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_Y Panel height is Y+1

6.3.6.11 0x004C LCD Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel:HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

6.3.6.12 0x0050 LCD Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

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6.3.6.13 0x0054 LCD Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk Note: HT > (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

6.3.6.14 0x0058 LCD HV Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	HV_MODE Set the HV mode of LCD controller. 0000: 24bit/1cycle parallel mode 1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(CCIR656)
27:26	R/W	0x0	RGB888_ODD_ORDER Serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7...). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_EVEN_ORDER Serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8...). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B

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Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
23:22	R/W	0x0	YUV_SM Serial YUV mode Output sequence 2-pixel-pair of every scan line. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0x0	YUV_EAV_SAV_F_LINE_DLY Set the delay line mode. 00: F toggle right after active video line 01: delay 2 line (CCIR PAL) 10: delay 3 line (CCIR NTSC) 11:reserved
19	R/W	0x0	CCIR_CSC_DIS Select '0' LCD convert source from RGB to YUV. 0: Enable 1: Disable Only valid when HV mode is "1100".
18:0	/	/	/

6.3.6.15 0x0060 LCD CPU Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	CPU_MODE Set the CPU interface work mode. 0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/

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Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
23	R	0x0	WR_FLAG The status of write operation. 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG The status of read operation. 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by VSYNC
16	R/W	0x0	FLUSH Direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
15:3	/	/	/
2	R/W	0x0	TRI_FIFO_EN Enable the trigger FIFO. 0: Disable 1: Enable
1	R/W1S	0x0	TRI_START Software must make sure write '1' only when this flag is '0'. Write '1' to start a frame flush, write'0' has no effect. This flag indicated frame flush is running.
0	R/W	0x0	TRI_EN Enable trigger mode. 0: Trigger mode disable 1: Trigger mode enable

6.3.6.16 0x0064 LCD CPU Panel Write Data Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus.

6.3.6.17 0x0068 LCD CPU Panel Read Data Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus.

6.3.6.18 0x006C LCD CPU Panel Read Data Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus.

6.3.6.19 0x0084 LCD LVDS Interface Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_LVDS_EN Enable LVDS interface. 0: Disable 1: Enable
30	R/W	0x0	LCD_LVDS_LINK Select work in single link mode or dual link mode. 0: Single link 1: Dual link
29	R/W	0x0	LCD_LVDS_EVEN_ODD_DIR Set the order of even field and odd field. 0: normal 1: reverse

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Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	LCD_LVDS_DIR Set the LVDS direction. 0: Normal 1: Reverse
27	R/W	0x0	LCD_LVDS_MODE Set the LVDS data mode. 0: NS mode 1: JEIDA mode
26	R/W	0x0	LCD_LVDS_BITWIDTH Set the bit width of data. 0: 24bit 1: 18bit
25	R/W	0x0	LCD_LVDS_DEBUG_EN Enable LVDS debug function. 0: Disable 1: Enable
24	R/W	0x0	LCD_LVDS_DEBUG_MODE Set the output signal in debug mode. 0: Mode0 Random data 1: Mode1 Output CLK period=7/2 LVDS CLK period
23	R/W	0x0	LCD_LVDS_CORRECT_MODE Set the LVDS correct mode. 0: Mode0 1: Mode1
22:21	/	/	/
20	R/W	0x0	LCD_LVDS_CLK_SEL Select the clock source of LVDS. 0: Revered 1: LCD CLK
19:5	/	/	/
4	R/W	0x0	LCD_LVDS_CLK_POL Set the clock polarity of LVDS. 0: Reverse 1: Normal
3:0	R/W	0x0	LCD_LVDS_DATA_POL Set the data polarity of LVDS. 0: Reverse 1: Normal

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6.3.6.20 0x0088 LCD IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IO_OUTPUT_SEL When set as '1', d [23:0], IO0, Io1, IO3 sync to dclk. 0: Normal output 1: Register output
30	/	/	/
29:28	R/W	0x0	DCLK_SEL Set the phase offset of clock and data in hv mode. 00: Used DCLK0(normal phase offset) 01: Used DCLK1(1/3 phase offset) 10: Used DCLK2(2/3 phase offset) Others: Reserved
27	R/W	0x0	IO3_INV Enable invert function of IO3. 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV Enable invert function of IO2. 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV Enable invert function of IO1. 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV Enable invert function of IO0. 0: Not invert 1: Invert
23:0	R/W	0x0	Data_INV LCD output port D [23:0] polarity control, with independent bit control. 0: Normal polarity 1: Invert the specify output

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6.3.6.21 0x008C LCD IO Control Register (Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN Set the endian of data bits. 0: Normal 1: Bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN Enable the output of IO3. 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN Enable the output of IO2. 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUR_TRI_EN Enable the output of IO1. 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN Enable the output of IO0. 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D [23:0] output enable, with independent bit control. 1: Disable 0: Enable

6.3.6.22 0x00FC LCD Debug Register (Default Value: 0x2000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	LCD_FIFO_UNDERFLOW The flag shows whether the FIFOs in underflow status. 0: Not underflow 1: Underflow
30	/	/	/

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Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
29	R	0x1	LCD_FIELD_POL The flag indicates the current field polarity. 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line.
15:0	/	/	/

6.3.6.23 0x0100 LCD CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CEU_EN Enable CEU function. 0: bypass 1: enable
30	R/W	0x0	BT656_F_MASK BT656 F Mask 0: disable 1: enable
29	R/W	0x0	BT656_F_MASK_VALUE BT656 F Mask Value 0/1
28:0	/	/	/

6.3.6.24 0x0110+N*0x04(N=0~2) LCD CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_MUL_REG0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Rr N=1: Rg N=2: Rb

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6.3.6.25 0x0120+N*0x04(N=0~2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x0120+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_MUL_REG1
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Gr N=1: Gg N=2: Gb

6.3.6.26 0x0130+N*0x04(N=0~2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0130+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_MUL_REG2
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Br N=1: Bg N=2: Bb

6.3.6.27 0x011C+N*0x10(N=0~2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0~2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19bit value, range of (-16384, 16384). N=0: Rc N=1: Gc N=2: Bc

6.3.6.28 0x0140+N*0x04(N=0~2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255].
15:8	/	/	/

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Offset: 0x0140+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255].

6.3.6.29 0x0160 LCD CPU Panel Trigger Register0 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set >20*pixel.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

6.3.6.30 0x0164 LCD CPU Panel Trigger Register1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

6.3.6.31 0x0168 LCD CPU Panel Trigger Register2 (Default Value: 0x0020_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x20	START_DLY T_{dly} = (Start_Delay +1) * be_clk*8.
15	R/W	0x0	TRANS_START_MODE Select the FIFOs used in CPU mode. 0: ECC_FIFO+TRI_FIFO 1: TRI_FIFO

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Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
14:13	R/W	0x0	SYNC_MODE Set the sync mode in CPU interface. 0x: Auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

6.3.6.32 0x016C LCD CPU Panel Trigger Register3 (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE When set as 01, Tri_Counter_Int occur in cycle of (Count_N+1) ×(Count_M+1) ×4 dclk. When set as 10 or 11, io0 is map as TE input 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor.
7:0	R/W	0x0	COUNTER_M The value of counter factor.

6.3.6.33 0x0170 LCD CPU Panel Trigger Register4 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN Enable the plug mode used in DSI command mode. 0: disable 1:enable
27:25	/	/	/
24	R/W	0x0	A1_First_Valid Valid in first Block.

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Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
23:0	R/W	0x0	D23_TO_D0_First_Valid Valid in first Block.

6.3.6.34 0x0174 LCD CPU Panel Trigger Register5 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	A1_NON_First_Valid Valid in Block except first.
23:0	R/W	0x0	D23_TO_D0_NON_First_Valid Valid in Block except first.

6.3.6.35 0x01F0 LCD Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, the LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, the LCD controller allow dram controller to change frequency. The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE Select the save mode 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM (If 3D FIFO is bypassed, this mode is not available.) 011: safe at 2 and safe at sync active 100: safe at line

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6.3.6.36 0x0220 LCD LVDS Analog Register0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LVDS_EN_MB Enable the bias circuit of the LVDS_ANA module. 0: Disable 1: Enable
30	R/W	0x0	LVDS_DUAL_CHANEL_SRC_SEL Dual Channel LVDS Source Selection 0: Single-monitor driven by dual-link LVDS. LVDS0 outputs even pixels from TCON source. LVDS1 outputs odd pixels from TCON source. 1: Dual-monitor displays identical screen. LVDS0 and LVDS1 output the same pixels.
29	R/W	0x0	EN_LVDS Enable LVDS.
28	R/W	0x0	EN_24M Enable the 24M Clock.
27:25	/	/	/
24	R/W	0x0	LVDS_HPREN_DRVC Enable Clock Channel Drive 0: Disable 1: Enable
23:20	R/W	0x0	LVDS_HPREN_DRV Enable Data Channel [3:0] Drive 0: Disable 1: Enable
19:17	R/W	0x0	LVDS_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 0: 216 mV 1: 252 mV 2: 276 mV 3: 312 mV 4: 336 mV 5: 372 mV 6: 395 mV 7: 432 mV
16	R/W	0x0	LVDS_REG_DENC Choose data output or PLL test clock output in LVDS_TX.
15:12	R/W	0x0	LVDS_REG_DEN Choose data output or PLL test clock output in LVDS_TX.
11	/	/	/

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Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	Read/Write	Default/Hex	Description
10:8	R/W	0x0	LVDS_REG_R Adjust current flowing through rload of rx to change the common signals amplitude. 0: 0.925 V 1: 0.950 V 2: 0.975 V 3: 1.000 V 4: 1.025 V 5: 1.050 V 6: 1.075 V 7: 1.100 V
7:5	/	/	/
4	R/W	0x0	LVDS_REG_PLRC LVDS Clock Channel Direction 0: Normal 1: Reverse
3:0	R/W	0x0	LVDS_REG_PLR LVDS Data Channel [3:0] Direction 0: Normal 1: Reverse

6.3.6.37 0x0224 LCD LVDS Analog Register1(Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: LCD_LVDS_ANA1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LVDS_EN_MB Enable the bias circuit of the LVDS_ANA module. 0: Disable 1: Enable
30	R/W	0x0	/
29	R/W	0x0	EN_LVDS Enable LVDS.
28	R/W	0x0	EN_24M Enable the 24M Clock
27:25	/	/	/
24	R/W	0x0	LVDS_HPREN_DRVC Enable Clock Channel Drive. 0: Disable 1: Enable
23:20	R/W	0x0	LVDS_HPREN_DRV Enable data channel [3:0] drive 0: Disable 1: Enable

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Offset: 0x0224			Register Name: LCD_LVDS_ANA1_REG
Bit	Read/Write	Default/Hex	Description
19:17	R/W	0x0	LVDS_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 0: 216 mV 1: 252 mV 2: 276 mV 3: 312 mV 4: 336 mV 5: 372 mV 6: 395 mV 7: 432 mV
16	R/W	0x0	LVDS_REG_DENC Choose data output or PLL test clock output in LVDS_TX.
15:12	R/W	0x0	LVDS_REG_DEN Choose data output or PLL test clock output in LVDS_TX.
11	/	/	/
10:8	R/W	0x0	LVDS_REG_R Adjust current flowing through Rload of Rx to change the common signals amplitude. 0: 0.925 V 1: 0.950 V 2: 0.975 V 3: 1.000 V 4: 1.025 V 5: 1.050 V 6: 1.075 V 7: 1.100 V
7:5	/	/	/
4	R/W	0x0	LVDS_REG_PLRC LVDS Clock Channel Direction 0: Normal 1: Reversed
3:0	R/W	0x0	LVDS_REG_PLR LVDS Data Channel [3:0] Direction 0: Normal 1: Reversed

6.3.6.38 0x0228 LCD FSYNC Generate Control Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:8	R/W	0x0	SENSOR_DIS_TIME Delay 0–2047 Hsync Period When HSYNC_POL_SEL is 0, the actual delay is sensor_dis_time-1. When HSYNC_POL_SEL is 1, the actual delay is sensor_dis_time.
7	/	/	/

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Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	SENSOR_ACT1_VALUE Sensor Active1 Value 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	SENSOR_ACT0_VALUE Sensor Active0 Value 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	SENSOR_DIS_VALUE Sensor Disable Value 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	HSYNC_POL_SEL Hsync Polarity Select 0: normal 1: opposite hsync to hysnc counter
1	R/W	0x0	SEL_VSYNC_EN Select Vsync Enable 0: select vsync falling edge to start state machine 1: select vsync rising edge to start state machine
0	R/W	0x0	FSYNC_GEN_EN Fsync Generate Enable 0: disable 1: enable

6.3.6.39 0x022C LCD FSYNC Generate Delay Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	SENSOR_ACT0_TIME Delay 0~4095 Pixel clk Period The actual delay is sensor_act0_time+1.
15:12	/	/	/
11:0	R/W	0x0	SENSOR_ACT1_TIME Delay 0~4095 Pixel clk Period The actual delay is sensor_act1_time+1.

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6.3.6.40 0x0230 LCD Sync Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: LCD_SYNC_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	LCD_CTRL_WORK_MODE LCD Controller Work mode 0: Single DSI mode 1:Dual DSI mode
7:5	/	/	/
4	R/W	0x0	LCD_CYRL_SYNC_MASTER_SLAVE LCD Controller Sync Master Slave 0: Master 1: Slave Note: Only use in Single DSI mode.
3:1	/	/	/
0	R/W	0x0	LCD_CTRL_SYNC_MODE LCD Controller Sync Mode 0: Sync in the first time 1: Sync every frame Note: Only use in Single DSI mode.

6.3.6.41 0x0234 LCD Sync Position Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	LCD_Sync_Pixel_Num Set the pixel number of master LCD controller which is used to trigger the slave LCD controller to start working. This value is the number of pixels between the trigger point and the end of the line. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) Note: Only use in Single DSI mode.
15:12	/	/	/

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Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x0	LCD_Sync_Line_Num Set the line number of master LCD controller which is used to trigger the slave LCD controller to start working. Note: It is only set in master LCD controller. It is not necessarily to set in slave LCD controller. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) Note: Only use in Single DSI mode.

6.3.6.42 0x0238 LCD Slave Stop Position Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name:LCD_SLAVE_STOP_POS_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
7:0	R/W	0x0	STOP_VAL Set the stop position of the slave LCD.This value is the number of pixels between the stop position and the end of the HFP. Stop_pos = HFP - Stop_val. NOTE:0<Stop_pos<HFP-2 Note: Only use in Single DSI mode.

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6.4 TCON TV

6.4.1 Overview

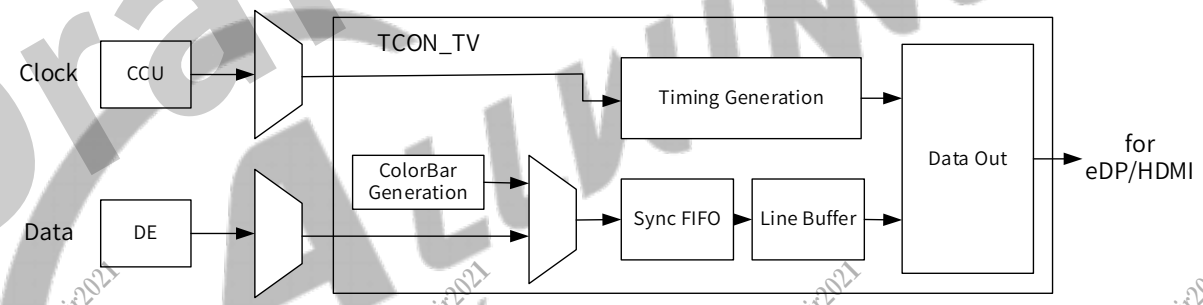
The Timing Controller_TV（TCON_TV）is a module that processes video signals received from systems using a complicated arithmetic and then generates control signals and transmits them to the eDP1.3.

The TCON_TV includes the following features:

- Two TCON TV controllers: TCON_TV0 for HDMI 2.0b and TCON_TV1 for eDP1.3
- Up to 4K@60Hz.
- Output format:
  - 8-bit or 10-bit pixel depth
  - HV

6.4.2 Block Diagram

Figure 6-15 TCON_TV Block Diagram



6.4.3 Functional Description

6.4.3.1 Clock Sources

The following table describes the clock sources of TCON_TV.

Table 6-15 TCON_TV Clock Sources

Clock Sources	Description	Module
PLL_VIDEO0(4x)	By default, PLL_VIDEO0(4x) is 1188 MHz.	CCU
PLL_VIDEO1(4x)	By default, PLL_VIDEO1(4x) is 1188 MHz.	
PLL_VIDEO2(4x)	By default, PLL_VIDEO2(4x) is 1188 MHz.	
PLL_VIDEO3(4x)	By default, PLL_VIDEO3(4x) is 1188 MHz.	
PLL_PERI0(2x)	By default, PLL_PERI0(2x) is 1.2 GHz.	

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6.4.3.2 Panel Interface

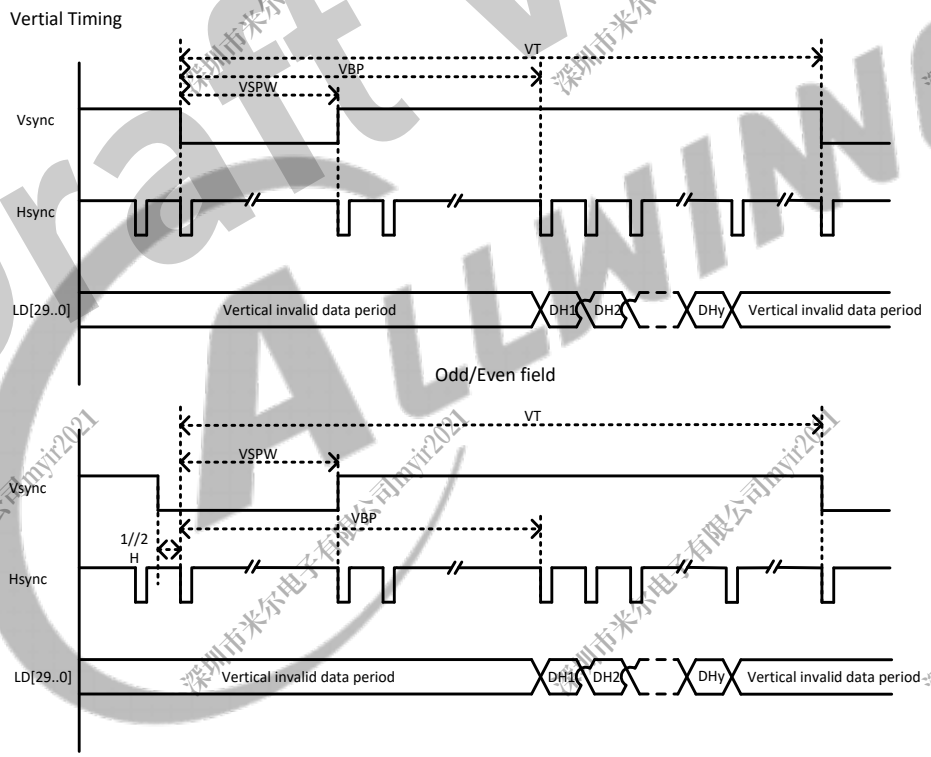
HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications. Its signals are defined as:

Table 6-16 HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[29..0]	30Bit RGB/YUV output from input FIFO for panel	O

HV control signals are active low.

Figure 6-16 HV Interface Vertical Timing



6.4.4 Register List

Module Name	Base Address
TCON_TV0	0x05503000
TCON_TV1	0x05504000

Register Name	Offset	Description
TV_GCTL_REG	0x000	TV Global Control Register

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Register Name	Offset	Description
TV_GINT0_REG	0x004	TV Global Interrupt Register0
TV_GINT1_REG	0x008	TV Global Interrupt Register1
TV_SRC_CTL_REG	0x040	TV Source Control Register
TV_CTL_REG	0x090	TV Control Register
TV_BASIC0_REG	0x094	TV Basic Timing Register0
TV_BASIC1_REG	0x098	TV Basic Timing Register1
TV_BASIC2_REG	0x09C	TV Basic Timing Register2
TV_BASIC3_REG	0x0A0	TV Basic Timing Register3
TV_BASIC4_REG	0x0A4	TV Basic Timing Register4
TV_BASIC5_REG	0x0A8	TV Basic Timing Register5
TV_IO_POL_REG	0x088	TV SYNC Signal Polarity Register
TV_IO_TRI_REG	0x08C	TV ISYNC Signal IO Control Register
TV_DEBUG_REG	0x0FC	TV Debug Register
TV_CEU_CTL_REG	0x100	TV CEU Control Register
TV_CEU_COEF_MUL_REG	0x110+N*0x04	TV CEU Coefficient Register0 (N=0,1,2,4,5,6,8,9,10)
TV_CEU_COEF_RANG_REG	0x140+N*0x04	TV CEU Coefficient Register2 (N=0,1,2)
TV_SAFE_PERIOD_REG	0x1F0	TV Safe Period Register
TV_FILL_CTL_REG	0x300	TV Fill Data Control Register
TV_FILL_BEGIN_REG	0x304+N*0x0C	TV Fill Data Begin Register (N=0,1,2)
TV_FILL_END_REG	0x308+N*0x0C	TV Fill Data End Register (N=0,1,2)
TV_FILL_DATA_REG	0x30C+N*0x0C	TV Fill Data Value Register (N=0,1,2)
TV_FILL_DATA2_REG	0x328	TV Fill Data2 Value Register
TV_FILL_DATA3_REG	0x32C	TV Fill Data3 Value Register
TV_DATA_IO_POL0_REG	0x330	TCON Data IO Polarity Control 0
TV_DATA_IO_POL1_REG	0x334	TCON Data IO Polarity Control 1
TV_DATA_ IO_TRI0_REG	0x338	TCON Data IO Enable Control 0
TV_DATA_ IO_TRI1_REG	0x33C	TCON Data IO Enable Control 1
TV_PIXELDEPTH_MODE_REG	0x340	TV Pixeldepth Mode Control Register

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6.4.5 Register Description

6.4.5.1 0x0000 TV Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TV_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TV_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30:2	/	/	/
1	R/W	0	HDMI_PAD_SEL HDMI-CEC/HDMI-SCLI/HDMI SDA signal PAD selection 0: Input from private PAD 1: Input from GPIO
0	/	/	/

6.4.5.2 0x0004 TV Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TV_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0	TV_VB_INT_EN 0: Disable 1: Enable
29	/	/	/
28	R/W	0	TV_LINE_INT_EN 0: disable 1: enable
27:15	/	/	/
14	R/W0C	0	TV_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W0C	0	TV_LINE_INT_FLAG trigger when SY1 match the current TV scan line Write 0 to clear it.
11:0	/	/	/

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6.4.5.3 0x0008 TV Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TV_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0	TV_LINE_INT_NUM Scan line for TV line trigger (including inactive lines) Setting it for the specified line for trigger 1. SY1 is write- only when LINE_TRG1 is disabled.

6.4.5.4 0x0040 TV Source Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0	TV_SRC_SEL: 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

6.4.5.5 0x0090 TV Control Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TV_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TV_EN 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0	START_DELAY This is for DE.
3:2	/	/	/
1	R/W	0	TV_SRC_SEL 0: Reserved 1: BLUE data The priority of this bit is higher than TV_SRC_SEL(bit[2:0]) in TV_SRC_CTL_REG.
0	/	/	/

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6.4.5.6 0x0094 TV Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: TV_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	XI Source width is X+1
15:12	/	/	/
11:0	R/W	0	YI Source height is Y+1

6.4.5.7 0x0098 TV Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	LS_XO Width is LS_XO+1
15:12	/	/	/
11:0	R/W	0	LS_YO Width is LS_YO+1 LS_YO = TV_YI

6.4.5.8 0x009C TV Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TV_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	TV_XO Width is TV_XO+1
15:12	/	/	/
11:0	R/W	0	TV_YO Height is TV_YO+1

6.4.5.9 0x00A0 TV Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

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Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
28:16	R/W	0	HT Horizontal Total Time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0	HBP Horizontal Back Porch Thbp = (HBP +1) * Thdclk

6.4.5.10 0x00A4 TV Basic Timing Register4 (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0	VT Vertical Total Time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0	VBP Vertical Back Porch (in HD line) Tvbp = (VBP +1) * Th

6.4.5.11 0x00A8 TV Basic Timing Register5 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TV_BASIC5_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0	HSPW Horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	VSPW Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th VT/2 > (VSPW+1)

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6.4.5.12 0x0088 TV SYNC Signal Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0	IO3_INV 0: Not invert 1: Invert
26	R/W	0	IO2 INV 0: Not invert 1: Invert
25	R/W	0	IO1_INV 0: Not invert 1: Invert
24	R/W	0	IO0_INV 0: Not invert 1: Invert
23:0	/	/	/

6.4.5.13 0x008C TV ISYNC Signal IO Control Register (Default Value: 0x0F00_0000)

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable
26	R/W	1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable
25	R/W	1	IO1_OUTPUT_TRI_EN 1: Disable 0: Enable
24	R/W	1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable
23:0	/	/	/

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6.4.5.14 0x00FC TV Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TV_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0	TV_FIFO_UNDER_FLOW
29	/	/	/
28	R	0	TV_FIELD_POLARITY 0: Second field 1: First field
27:12	/	/	/
13	R/W	0	LINE_BUF _BYPASS 0: Used 1: Bypass
12	/	/	/
11:0	R	0	TV_CURRENT_LINEQUE

6.4.5.15 0x0100 TV CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TV_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	CEU_EN 0: Bypass 1: Enable
30:0	/	/	/

6.4.5.16 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10) TV CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/

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Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0	CEU_COEF_MUL_VALUE 1.CEU_Coef_Mul_Value only can be 0 or 1 2. REG Map: N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb
7:0	/	/	/

6.4.5.17 0x0140+N*0x04 (N=0,1,2) TV CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0,1,2)			Register Name: TV_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	CEU_COEF _RANGE_MIN Unsigned 12bit value, range of [0,4095]
15:12	/	/	/
11:0	R/W	0	CEU COEF _RANGE_MAX Unsigned 12bit value, range of [0,4095]

6.4.5.18 0x01F0 TV Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0	SAFE_PERIOD_FIFO_NUM
15:4	R/W	0	SAFE_PERIOD_LINE
3	/	/	/

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Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0	SAFE_PERIOD_MODE 0: Unsafe 1: Safe 2: Safe at LINE_BUF_CURR_NUM > SAFE_PERIOD_FIFO_NUM 3: Safe at 2 and safe at sync active 4: Safe at line

6.4.5.19 0x0300 TV Fill Data Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TV_FILL_EN 0: Bypass 1: Enable
30:0	/	/	/

6.4.5.20 0x0304+N*0x0C (N=0,1,2) TV Fill Data Begin Register (Default Value: 0x0000_0000)

Offset: 0x0304+N*0x0C (N=0,1,2)			Register Name: TV_FILL_BEGIN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	FILL_BEGIN

6.4.5.21 0x0308+N*0x0C (N=0,1,2) TV Fill Data End Register (Default Value: 0x0000_0000)

Offset: 0x0308+N*0x0C (N=0,1,2)			Register Name: TV_FILL_END_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	FILL_END

6.4.5.22 0x030C+N*0x0C (N=0~2) TV Fill Data Value Register (Default Value: 0x0000_0000)

Offset: 0x030C+N*0x0C (N=0~2)			Register Name: TV_FILL_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	FILL_VALUE bit31~0

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6.4.5.23 0x0328 TV Fill Data2 Value Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: TV_FILL_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0	0x318 FILL_VALUE bit47~bit32
15:0	R/W	0	0x30C FILL_VALUE bit47~bit32

6.4.5.24 0x032C TV Fill Data3 Value Register (Default Value: 0x0000_0000)

Offset: 0x032C			Register Name: TV_FILL_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0	0x324 Fill_Value bit47~bit32

6.4.5.25 0x0330 TCON Data IO Polarity Control 0 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: TV_DATA_IO_POL0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	R/Cb CHANNEL DATA_INV bit [11:0] 0: Normal polarity 1: Invert the specify output
15:12	/	/	/
11:0	R/W	0	G/Y CHANNEL DATA_INV bit [11:0] 0: Normal polarity 1: Invert the specify output

6.4.5.26 0x0334 TCON Data IO Polarity Control 1 (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: TV_DATA_IO_POL1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	B/Cr CHANNEL DATA_INV bit [11:0] 0: Normal polarity 1: Invert the specify output
15:0	/	/	/

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6.4.5.27 0x0338 TCON Data IO Enable Control 0 (Default Value: 0x0fff_0fff)

Offset: 0x0338			Register Name: TV_DATA_IO_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xfff	R/Cb CHANNEL DATA_OUTPUT_TRI_EN 1: Disable 0: Enable
15:12	/	/	/
11:0	R/W	0xfff	G/Y CHANNEL DATA_OUTPut_TRI_EN 1: Disable 0: Enable

6.4.5.28 0x033C TCON Data IO Enable Control 1 (Default Value: 0x0fff_0000)

Offset: 0x033C			Register Name: TV_DATA_IO_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xfff	B/Cr CHANNEL DATA_OUTPUT_TRI_EN 1: Disable 0: Enable
15:0	/	/	/

6.4.5.29 0x0340 TV Pixeldepth Mode Control Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0	COLORBAR PIXELDEPTH MODE This bit is only valid when colorbar outputs. 0: 8-bit mode Transmits colorbar pattern of 8-bit mode, when the source is internal colorbar. 1: 10-bit mode Transmits colorbar pattern of 10-bit mode, when the source is internal colorbar. 2: 12-bit mode Transmits colorbar pattern of 12-bit mode, when the source is internal colorbar. 3: Reserved

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6.5 HDMI

6.5.1 Overview

The High Definition Multimedia Interface (HDMI) is a wired digital interconnect that replaces the analog SCART connection. HDMI can transfer uncompressed video, audio, and data using a single cable.

The system architecture of HDMI consists of sources (transmitter) and sinks (receiver). The HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA Data Display Channel (DDC). The DDC is used for configuration and status exchange between a single source and a single sink. The optional CEC protocol provides high-level control functions between all of the various audiovisual products in a user's environment.

The HDMI includes the following features:

- One HDMI2.0 TX interface, supporting HDCP1.4
- Supports 3840x2160, 1920x1080, and 1280x720 resolution
- Up to 4K@60fps for 2D display and up to 4K@30fps for 3D display
- Supports several data formats including RGB888, YUV444, YUV422, and YUV420
- Supports I2S, 192 kHz sampling rate, 8 sound channels
- Supports up to 3840x2160@60 10bit input, 3 Data lanes, 6 Gbit/s per lane for YUV422
- Supports DDC/CEC, 5 V tolerant voltage

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7 Video Input Interfaces

7.1 CSIC

7.1.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface and store the data in memory directly.

The CSIC includes the following features:

- MIPI CSI supports the following
  - 8M@30fps RAW12 2F-WDR, size up to 3264(H) x 2448(V)
  - 4+ 4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI Interface
    - MIPI CSI2 V1.1
    - MIPI DPHY V1.1
    - 2.0 Gbit/s per lane
  - Crop function
  - Frame-rate decreasing via software
- Parallel CSI supports the following
  - 16-bit digital camera interface
  - 8/10/12/16-bit width
  - BT.656, BT.601, BT.1120 interface
  - Dual Data Rate (DDR) sample mode with pixel clock up to 148.5MHz
  - ITU-R BT.656 up to 4*720P@30fps
  - TU-R BT.1120 up to 4*1080P@30fps
- BK supports the following:
  - 6-lane BK and BK0-3 supports 4-lane time-multiplexing
  - 6 DMA controllers for 6 video stream storage
    - Conversion of interlaced input to progressive output
    - Data conversion supports: YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
    - Horizontal and vertical flip
- BK doesn't support anti-aliasing and noise reduction

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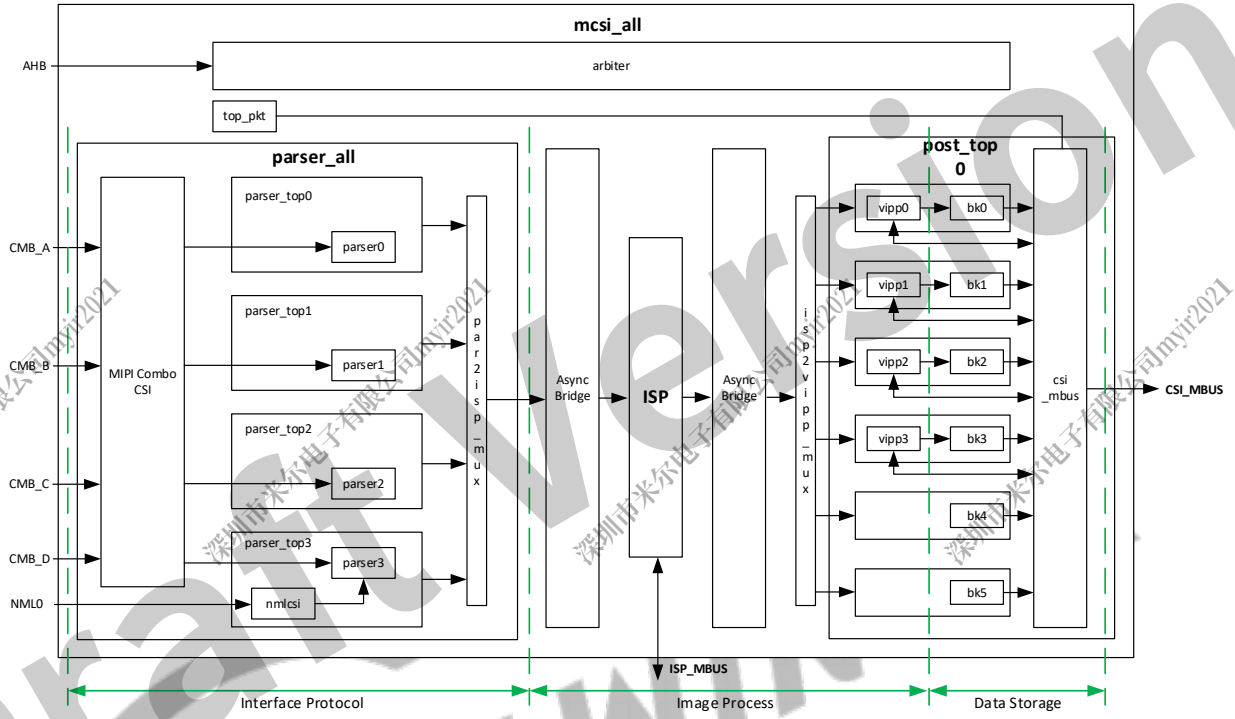
7.1.2 Block Diagram

The following figure shows block diagram of the CSIC.

Figure 7-1 CSIC Block Diagram



7.1.3 Functional Description

7.1.3.1 External Signals

Table 7-1 CSIC External Signals

Signal Name	Description	Type
MIPI CSI		
MCSIA-D0P	MIPI CSI Controller A Data0 Positive Signal	AI
MCSIA-D0N	MIPI CSI Controller A Data0 Negative Signal	AI
MCSIA-D1P	MIPI CSI Controller A Data1 Positive Signal	AI
MCSIA-D1N	MIPI CSI Controller A Data1 Negative Signal	AI
MCSIA-CKP	MIPI CSI Controller A Clock Positive Signal	AI
MCSIA-CKN	MIPI CSI Controller A Clock Negative Signal	AI
MCSI0-MCLK	Master Clock for MIPI Sensor	O
MCSIB-D0P	MIPI CSI Controller B Data0 Positive Signal	AI
MCSIB-D0N	MIPI CSI Controller B Data0 Negative Signal	AI
MCSIB-D1P	MIPI CSI Controller B Data1 Positive Signal	AI
MCSIB-D1N	MIPI CSI Controller B Data1 Negative Signal	AI
MCSIB-CKP	MIPI CSI Controller B Clock Positive Signal	AI
MCSIB-CKN	MIPI CSI Controller B Clock Negative Signal	AI

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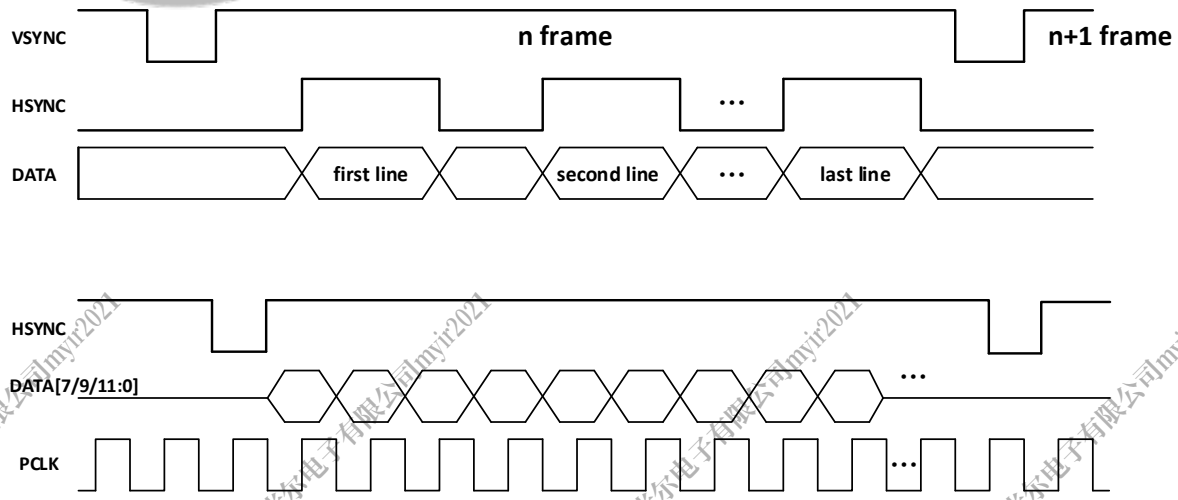
Signal Name	Description	Type
MCSI1-MCLK	Master Clock for MIPI Sensor	O
MCSIC-D0P	MIPI CSI Controller C Data0 Positive Signal	AI
MCSIC-D0N	MIPI CSI Controller C Data0 Negative Signal	AI
MCSIC-D1P	MIPI CSI Controller C Data1 Positive Signal	AI
MCSIC-D1N	MIPI CSI Controller C Data1 Negative Signal	AI
MCSIC-CKP	MIPI CSI Controller C Clock Positive Signal	AI
MCSIC-CKN	MIPI CSI Controller C Clock Negative Signal	AI
MCSI2-MCLK	Master Clock for MIPI Sensor	O
MCSID-D0P	MIPI CSI Controller D Data0 Positive Signal	AI
MCSID-D0N	MIPI CSI Controller D Data0 Negative Signal	AI
MCSID-D1P	MIPI CSI Controller D Data1 Positive Signal	AI
MCSID-D1N	MIPI CSI Controller D Data1 Negative Signal	AI
MCSID-CKP	MIPI CSI Controller D Clock Positive Signal	AI
MCSID-CKN	MIPI CSI Controller D Clock Negative Signal	AI
MCSI3-MCLK	Master Clock for MIPI Sensor	O
CSI-SM-HS	MIPI CSI Slave Mode Horizontal SYNC	O
CSI-SM-VS	MIPI CSI Slave Mode Vertical SYNC	O
Parallel CSI		
NCSI-PCLK	Parallel CSI Pixel Clock	I
NCSI-MCLK	Parallel CSI Master Clock	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI-D[15:0]	Parallel CSI Data Bit	I

7.1.3.2 CSIC Input Timing

The following figure shows the timing of 8bit CMOS Sensor Interface, in this figure clock active at the rising edge, VSYNC valid at positive, HSYNC valid at positive.

Figure 7-2 8-bit DC Sensor Interface Timing



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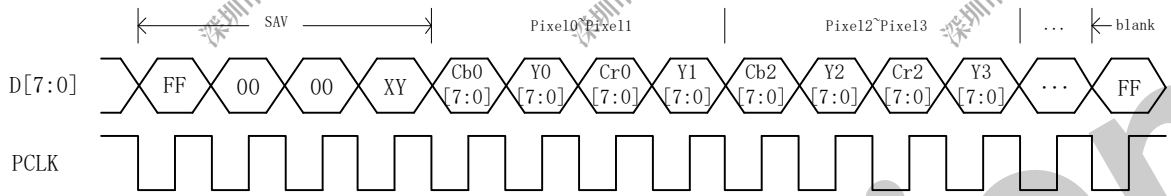
The following figure shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT.656).

Figure 7-3 8-bit YCbCr4:2:2 with Embedded Syncs (BT.656)



The following table shows the header code of BT.656.

Table 7-2 BT.656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

The following table shows the Header Data Bit Definition of BT.656.

Table 7-3 BT.656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

7.1.3.3 CSIC FIFO Distribution

Table 7-4 CSIC FIFO Distribution

Input format	YUV422/YUV420		Raw
Output format	Planar	UV combined	Raw
FIFO0	Y	Y	All pixels data
FIFO1	Cb (U)	CbCr (UV)	-
FIFO2	Cr (V)	-	-

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7.1.3.4 Pixel Format Arrangement

The following figures show the Pixel Format Arrangement.

Figure 7-4 RAW-8 Format

Raw data 3[7:0]	Raw data 2[7:0]	Raw data 1[7:0]	Raw data 0[7:0]

MSB LSB

Figure 7-5 Y Format

Y 3[7:0]	Y 2[7:0]	Y 1[7:0]	Y 0[7:0]

MSB LSB

Figure 7-6 UV-Combined Format

V/U 1[7:0]	U/V 1[7:0]	V/U 0[7:0]	U/V 0[7:0]

MSB LSB

7.1.3.5 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

- For YUV422 format, pixel unit is a YU/YV combination.
- For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
- For Bayer and RAW format, pixel unit is a R/G/B single component.

7.1.3.6 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of Y0U0Y1V1 will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of Y1U0Y0V1 will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

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7.1.4 Programming Guidelines

7.1.4.1 Key Points for Async Bridge Configuration

- If ISP uses work clock with lower frequency than that of parser and post.

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1'b1 to enable async bridge

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1'b1 to make CSI parser work in CSI clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1'b1 to make CSI post work in CSI clock.

- If ISP uses work clock with the same frequency as parser and post

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1'b0 to disable and bypass async bridge.

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1'b0 to make CSI parser work in ISP core clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1'b0 to make CSI post work in ISP core clock.

7.1.4.2 Configuration Notes

- The CCU_CLK_GATING_DISABLE bit (bit [31]) of CCU_CLK_MODE_REG register is configured as 0 by default, that is, the clock in CSIC CCU is gated off by default.
- The MCSI_POST_CLK_MODE bit (bit [1]) and MCSI_PARSER_CLK_MODE bit (bit [0]) of CCU_CLK_MODE_REG register are configured as 1 by default, that is, CSI post and CSI parser work in CSI clock by default.
- The sequence of CSI reset, CSIC clock enable, and PPU power-on is as follows:

  CSIC reset -> PPU power-on -> CSIC clock enable (including: ISP_Clock, CSI Clock, ISP MCLK, CSI MCLK, CSI BUS GATING, and CSI Master0/1/2/3 Clock)
- There are two soft reset bits for MBUS:

Table 7-5 Soft Reset bits for MBUS

Bits	Regsiters	Description
MISP_MBUS_RST (bit [8], high active)	CCU_ISP_CLK_EN_REG	Reset the MBUS interface logic circuit in ISP.
MCSI_POST0_MBUS_RST (bit [20], high active)	CSIC_CCU_POST0_CLK_EN_REG	Reset the MBUS interface logic circuit in POST0.

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7.1.5 Register List

There are four groups of registers in CSIC.

Module Name	Base Address
CSIC_CCU	0x05800000
CSIC_TOP	0x05800800
CSIC_PHY	
PHY COMMON	0x05810000
PHYA DIGITAL LAYER	0x05810100
PHYB DIGITAL LAYER	0x05810200
PHYC DIGITAL LAYER	0x05810300
PHYD DIGITAL LAYER	0x05810400
PORT0 PAYLOAD LAYER	0x05811000
PORT1 PAYLOAD LAYER	0x05811400
PORT2 PAYLOAD LAYER	0x05811800
PORT3 PAYLOAD LAYER	0x05811C00
CSIC_ PARSER	
CSIC_PARSER0	0x05820000
CSIC_PARSER1	0x05821000
CSIC_PARSER2	0x05822000
CSIC_PARSER3	0x05823000
CSIC_DMA	
CSIC_DMA0	0x05830000
CSIC_DMA1	0x05831000
CSIC_DMA2	0x05832000
CSIC_DMA3	0x05833000
CSIC_DMA4	0x05834000
CSIC_DMA5	0x05835000

7.1.5.1 CSIC_CCU Register List

Module Name	Base Address
CSIC_CCU	0x05800000

Register Name	Offset	Description
CSIC_CCU_CLK_MODE_REG	0x0000	CSIC CCU Clock Mode Register
CSIC_CCU_PARSER_CLK_EN_REG	0x0004	CSIC CCU Parser Clock Enable Register
CSIC_CCU_POST0_CLK_EN_REG	0x000C	CSIC CCU Post0 Clock Enable Register
CSIC_CCU_POST0_CLK_EN_SUP_REG	0x0010	CSIC CCU Post0 Clock Enable Sup Register
CSIC_CCU_CHFREQ_CLK_CTRL_REG	0x0014	CSIC CCU Chfreq Clock Control Register

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7.1.5.2 CSIC_TOP Register List

Module Name	Base Address
CSIC_TOP	0x05800800

Register Name	Offset	Description
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_ISP2_INPUT0_SEL_REG	0x0050	CSIC ISP2 Input0 Select Register
CSIC_ISP2_INPUT1_SEL_REG	0x0054	CSIC ISP2 Input1 Select Register
CSIC_ISP2_INPUT2_SEL_REG	0x0058	CSIC ISP2 Input2 Select Register
CSIC_ISP2_INPUT3_SEL_REG	0x005C	CSIC ISP2 Input3 Select Register
CSIC_ISP3_INPUT0_SEL_REG	0x0060	CSIC ISP3 Input0 Select Register
CSIC_ISP3_INPUT1_SEL_REG	0x0064	CSIC ISP3 Input1 Select Register
CSIC_ISP3_INPUT2_SEL_REG	0x0068	CSIC ISP3 Input2 Select Register
CSIC_ISP3_INPUT3_SEL_REG	0x006C	CSIC ISP3 Input3 Select Register
CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG	0x0070	CSIC ISP Bridge Buffer Maxuse Counter Clear Register
CSIC_ISP0_BRG01_BUF_MAXUSE_CNT_REG	0x0074	CSIC ISP0 Bridge01 Buffer Maxuse Counter Register
CSIC_ISP0_BRG23_BUF_MAXUSE_CNT_REG	0x0078	CSIC ISP0 Bridge23 Buffer Maxuse Counter Register
CSIC_ISP0_BRG_INT_EN_REG	0x0084	CSIC ISP0 Bridge Interrupt Enable Register
CSIC_ISP0_BRG_INT_PD_REG	0x008C	CSIC ISP0 Bridge Interrupt Pending Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_DMA4_INPUT_SEL_REG	0x00B0	CSIC DMA4 Input Select Register
CSIC_DMA5_INPUT_SEL_REG	0x00B4	CSIC DMA5 Input Select Register

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Register Name	Offset	Description
CSIC_BIST_CTRL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_ADDR_REG	0x00E4	CSIC BIST Start Address Register
CSIC_BIST_END_ADDR_REG	0x00E8	CSIC BIST End Address Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_CHFREQ_CFG0_REG	0x0108	CSIC Change Frequency Configuration 0 Register
CSIC_CHFREQ_CFG1_REG	0x010C	CSIC Change Frequency Configuration 1 Register
CSIC_CHFREQ_OBS_REG	0x0110	CSIC Change Frequency Observation Register
CSIC_CHFREQ_INT_REG	0x0114	CSIC Change Frequency Interrupt Register
CSIC_CHFREQ_DBG_OBS_REG	0x0118	CSIC Change Frequency Debug Observation Register
CSIC_FEATURE_LIST_REG	0x01F0	CSIC Feature List Register

7.1.5.3 CSIC_PHY Register List

PHY COMMON

Module Name	Base Address
PHY COMMON	0x05810000
PHYA DIGITAL LAYER	0x05810100
PHYB DIGITAL LAYER	0x05810200
PHYC DIGITAL LAYER	0x05810300
PHYD DIGITAL LAYER	0x05810400
PORT0 PAYLOAD LAYER	0x05811000
PORT1 PAYLOAD LAYER	0x05811400
PORT2 PAYLOAD LAYER	0x05811800
PORT3 PAYLOAD LAYER	0x05811C00

Register Name	Offset	Description
PHY_TOP_CTL_REG	0x0000	PHY Top Control Register
PHY_TRESCAL_REG	0x0004	PHY Terminal Resistor Calibration Register

PHY DIGITAL LAYER

Module Name	Base Address
PHYA DIGITAL LAYER	0x05810100
PHYB DIGITAL LAYER	0x05810200
PHYC DIGITAL LAYER	0x05810300

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PHYD DIGITAL LAYER	0x05810400

Register Name	Offset	Description
PHY_CTL_REG	0x0000	PHY Control Register
PHY_EQ_REG	0x0004	PHY Equalization Register
PHY_OFSCAL_REG0	0x0008	PHY Offset Calibration Register0
PHY_OFSCAL_REG1	0x000C	PHY Offset Calibration Register1
PHY_OFSCAL_REG2	0x0010	PHY Offset Calibration Register2
PHY_DESKEW_REG0	0x0014	PHY Deskew Register0
PHY_DESKEW_REG1	0x0018	PHY Deskew Register1
PHY_DESKEW_REG2	0x001C	PHY Deskew Register2
PHY_TERM_CTL_REG	0x0020	PHY Terminal Control Register
PHY_HS_CTL_REG	0x0024	PHY High Speed Control Register
PHY_S2P_CTL_REG	0x0028	PHY Serial To Parallel Control Register
PHY_MIPIRX_CTL_REG	0x002C	PHY MIPIRX Control Register
PHY_MIPIRX_SYNC_TIMEOUT_REG	0x0030	PHY MIPIRX Synchronization Timeout Register
PHY_FREQ_CNT _REG	0x0034	PHY Frequency Counter Register
PHY_MIPI_LP_TIMEOUT_REG	0x0038	PHY MIPI LP Timeout Register
PHY_MIPI_ULPSEXIT_REG0	0x0040	PHY MIPI ULPSEXIT Register0
PHY_INT_EN_REG	0x0080	PHY Interrupt Enable Register
PHY_INT_PD_REG	0x0084	PHY Interrupt Pending Register

PORT PAYLOAD LAYER

Module Name	Base Address
PORT0 PAYLOAD LAYER	0x05811000
PORT1 PAYLOAD LAYER	0x05811400
PORT2 PAYLOAD LAYER	0x05811800
PORT3 PAYLOAD LAYER	0x05811C00

Register Name	Offset	Description
PORT_CTL_REG	0x0000	PORT Control Register
PORT_LANE_MAP_REG0	0x0004	PORT Lane Mapping Register0
PORT_WDR_MODE_REG	0x000C	PORT WDR Mode Register
PORT_FID_SEL_REG	0x0010	PORT Frame ID Select Register
PORT_MIPI_CFG_REG	0x0100	PORT MIPI Configuration Register
PORT_MIPI_NO_UNPAK_NUM_REG	0x0104	PORT MIPI No Unpacket Number Register
PORT_MIPI_DI_REG	0x0108	PORT MIPI Data Identity Register
PORT_MIPI_USER_DT_REG	0x010C	PORT MIPI User Data Type Register

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Register Name	Offset	Description
PORT_MIPI_CH0_DT_TRIG_EN_REG	0x0110	PORT MIPI Channel0 Data Type Trigger Register
PORT_MIPI_CH0_INT_EN_REG	0x0114	PORT MIPI Channel0 Interrupt Enable Register
PORT_MIPI_CH0_INT_PD_REG	0x0118	PORT MIPI Channel0 Interrupt Pending Register
PORT_MIPI_CH0_PH_REG	0x011C	PORT MIPI Channel0 Packet Header Register
PORT_MIPI_CH0_ECC_REG	0x0120	PORT MIPI Channel0 ECC Register
PORT_MIPI_CH0_CKSUM_REG	0x0124	PORT MIPI Channel0 Checksum Register
PORT_MIPI_CH0_FRM_NUM_REG	0x0128	PORT MIPI Channel0 Frame Number Register
PORT_MIPI_CH0_LINE_NUM_REG	0x012C	PORT MIPI Channel0 Line Number Register
PORT_MIPI_CH1_DT_TRIG_EN_REG	0x0130	PORT MIPI Channel1 Data Type Trigger Register
PORT_MIPI_CH1_INT_EN_REG	0x0134	PORT MIPI Channel1 Interrupt Enable Register
PORT_MIPI_CH1_INT_PD_REG	0x0138	PORT MIPI Channel1 Interrupt Pending Register
PORT_MIPI_CH1_PH_REG	0x013C	PORT MIPI Channel1 Packet Header Register
PORT_MIPI_CH1_ECC_REG	0x0140	PORT MIPI Channel1 ECC Register
PORT_MIPI_CH1_CKSUM_REG	0x0144	PORT MIPI Channel1 Checksum Register
PORT_MIPI_CH1_FRM_NUM_REG	0x0148	PORT MIPI Channel1 Frame Number Register
PORT_MIPI_CH1_LINE_NUM_REG	0x014C	PORT MIPI Channel1 Line Number Register
PORT_MIPI_CH2_DT_TRIG_EN_REG	0x0150	PORT MIPI Channel2 Data Type Trigger Register
PORT_MIPI_CH2_INT_EN_REG	0x0154	PORT MIPI Channel2 Interrupt Enable Register
PORT_MIPI_CH2_INT_PD_REG	0x0158	PORT MIPI Channel2 Interrupt Pending Register
PORT_MIPI_CH2_PH_REG	0x015C	PORT MIPI Channel2 Packet Header Register
PORT_MIPI_CH2_ECC_REG	0x0160	PORT MIPI Channel2 ECC Register
PORT_MIPI_CH2_CKSUM_REG	0x0164	PORT MIPI Channel2 Checksum Register
PORT_MIPI_CH2_FRM_NUM_REG	0x0168	PORT MIPI Channel2 Frame Number Register
PORT_MIPI_CH2_LINE_NUM_REG	0x016C	PORT MIPI Channel2 Line Number Register
PORT_MIPI_CH3_DT_TRIG_EN_REG	0x0170	PORT MIPI Channel3 Data Type Trigger Register
PORT_MIPI_CH3_INT_EN_REG	0x0174	PORT MIPI Channel3 Interrupt Enable Register
PORT_MIPI_CH3_INT_PD_REG	0x0178	PORT MIPI Channel3 Interrupt Pending Register
PORT_MIPI_CH3_PH_REG	0x017C	PORT MIPI Channel3 Packet Header Register

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Register Name	Offset	Description
PORT_MIPI_CH3_ECC_REG	0x0180	PORT MIPI Channel3 ECC Register
PORT_MIPI_CH3_CKSUM_REG	0x0184	PORT MIPI Channel3 Checksum Register
PORT_MIPI_CH3_FRM_NUM_REG	0x0188	PORT MIPI Channel3 Frame Number Register
PORT_MIPI_CH3_LINE_NUM_REG	0x018C	PORT MIPI Channel3 Line Number Register
PORT_MIPI_LANE_ERR_INT_EN_REG	0x01F0	PORT MIPI Lane Error Interrupt Register
PORT_MIPI_LANE_ERR_INT_PD_REG	0x01F4	PORT MIPI Lane Error Interrupt Pending Register

7.1.5.4 CSIC_PARSER Register List

Module Name	Base Address
CSIC_PARSER0	0x05820000
CSIC_PARSER1	0x05821000
CSIC_PARSER2	0x05822000
CSIC_PARSER3	0x05823000

Register Name	Offset	Description
CSIC_PRS_EN_REG	0x0000	CSIC Parser Enable Register
CSIC_PRS_NCSIC_IF_CFG_REG	0x0004	CSIC Parser NCSIC Interface Configuration Register
CSIC_PRS_CAP_REG	0x000C	CSIC Parser Capture Register
CSIC_PRS_SIGNAL_STA_REG	0x0010	CSIC Parser Signal Status Register
CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	CSIC Parser NCSIC BT656 Header Configuration Register
CSIC_PRS_CAP_FRM_MSK_0_REG	0x0018	CSIC Parser Capture Frame Mask 0 Register
CSIC_PRS_CAP_FRM_MSK_1_REG	0x001C	CSIC Parser Capture Frame Mask 1 Register
CSIC_PRS_CH0_IN_DMSK_PERIOD_REG	0x0020	CSIC Parser Channel_0 Input Dmask Setting Register
CSIC_PRS_CH0_INFMT_REG	0x0024	CSIC Parser Channel_0 Input Format Register
CSIC_PRS_CH0_OUTPUT_HSIZE_REG	0x0028	CSIC Parser Channel_0 Output Horizontal Size Register
CSIC_PRS_CH0_OUTPUT_VSIZE_REG	0x002C	CSIC Parser Channel_0 Output Vertical Size Register
CSIC_PRS_CH0_INPUT_PARA0_REG	0x0030	CSIC Parser Channel_0 Input Parameter0 Register

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Register Name	Offset	Description
CSIC_PRS_CH0_INPUT_PARA1_REG	0x0034	CSIC Parser Channel_0 Input Parameter1 Register
CSIC_PRS_CH0_INPUT_PARA2_REG	0x0038	CSIC Parser Channel_0 Input Parameter2 Register
CSIC_PRS_CH0_INPUT_PARA3_REG	0x003C	CSIC Parser Channel_0 Input Parameter3 Register
CSIC_PRS_CH0_INT_EN_REG	0x0040	CSIC Parser Channel_0 Interrupt Enable Register
CSIC_PRS_CH0_INT_STA_REG	0x0044	CSIC Parser Channel_0 Interrupt Status Register
CSIC_PRS_CH0_LINE_TIME_REG	0x0048	CSIC Parser Channel_0 Line Time Register
CSIC_PRS_CH0_FRM_PRE_MSK_REG	0x004C	CSIC Parser Channel_0 Frame Pre Mask Setting Register
CSIC_PRS_CH1_IN_DMSK_PERIOD_REG	0x0120	CSIC Parser Channel_1 Input Dmask Setting Register
CSIC_PRS_CH1_INFMT_REG	0x0124	CSIC Parser Channel_1 Input Format Register
CSIC_PRS_CH1_OUTPUT_HSIZE_REG	0x0128	CSIC Parser Channel_1 Output Horizontal Size Register
CSIC_PRS_CH1_OUTPUT_VSIZE_REG	0x012C	CSIC Parser Channel_1 Output Vertical Size Register
CSIC_PRS_CH1_INPUT_PARA0_REG	0x0130	CSIC Parser Channel_1 Input Parameter0 Register
CSIC_PRS_CH1_INPUT_PARA1_REG	0x0134	CSIC Parser Channel_1 Input Parameter1 Register
CSIC_PRS_CH1_INPUT_PARA2_REG	0x0138	CSIC Parser Channel_1 Input Parameter2 Register
CSIC_PRS_CH1_INPUT_PARA3_REG	0x013C	CSIC Parser Channel_1 Input Parameter3 Register
CSIC_PRS_CH1_INT_EN_REG	0x0140	CSIC Parser Channel_1 Interrupt Enable Register
CSIC_PRS_CH1_INT_STA_REG	0x0144	CSIC Parser Channel_1 Interrupt Status Register
CSIC_PRS_CH1_LINE_TIME_REG	0x0148	CSIC Parser Channel_1 Line Time Register
CSIC_PRS_CH1_FRM_PRE_MSK_REG	0x014C	CSIC Parser Channel_1 Frame Pre Mask Setting Register
CSIC_PRS_CH2_IN_DMSK_PERIOD_REG	0x0220	CSIC Parser Channel_2 Input Dmask Setting Register
CSIC_PRS_CH2_INFMT_REG	0x0224	CSIC Parser Channel_2 Input Format Register
CSIC_PRS_CH2_OUTPUT_HSIZE_REG	0x0228	CSIC Parser Channel_2 Output Horizontal Size Register
CSIC_PRS_CH2_OUTPUT_VSIZE_REG	0x022C	CSIC Parser Channel_2 Output Vertical Size Register

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Register Name	Offset	Description
CSIC_PRS_CH2_INPUT_PARA0_REG	0x0230	CSIC Parser Channel_2 Input Parameter0 Register
CSIC_PRS_CH2_INPUT_PARA1_REG	0x0234	CSIC Parser Channel_2 Input Parameter1 Register
CSIC_PRS_CH2_INPUT_PARA2_REG	0x0238	CSIC Parser Channel_2 Input Parameter2 Register
CSIC_PRS_CH2_INPUT_PARA3_REG	0x023C	CSIC Parser Channel_2 Input Parameter3 Register
CSIC_PRS_CH2_INT_EN_REG	0x0240	CSIC Parser Channel_2 Interrupt Enable Register
CSIC_PRS_CH2_INT_STA_REG	0x0244	CSIC Parser Channel_2 Interrupt Status Register
CSIC_PRS_CH2_LINE_TIME_REG	0x0248	CSIC Parser Channel_2 Line Time Register
CSIC_PRS_CH2_FRM_PRE_MSK_REG	0x024C	CSIC Parser Channel_2 Frame Pre Mask Setting Register
CSIC_PRS_CH3_IN_DMSK_PERIOD_REG	0x0320	CSIC Parser Channel_3 Input Dmask Setting Register
CSIC_PRS_CH3_INFMT_REG	0x0324	CSIC Parser Channel_3 Input Format Register
CSIC_PRS_CH3_OUTPUT_HSIZE_REG	0x0328	CSIC Parser Channel_3 Output Horizontal Size Register
CSIC_PRS_CH3_OUTPUT_VSIZE_REG	0x032C	CSIC Parser Channel_3 Output Vertical Size Register
CSIC_PRS_CH3_INPUT_PARA0_REG	0x0330	CSIC Parser Channel_3 Input Parameter0 Register
CSIC_PRS_CH3_INPUT_PARA1_REG	0x0334	CSIC Parser Channel_3 Input Parameter1 Register
CSIC_PRS_CH3_INPUT_PARA2_REG	0x0338	CSIC Parser Channel_3 Input Parameter2 Register
CSIC_PRS_CH3_INPUT_PARA3_REG	0x033C	CSIC Parser Channel_3 Input Parameter3 Register
CSIC_PRS_CH3_INT_EN_REG	0x0340	CSIC Parser Channel_3 Interrupt Enable Register
CSIC_PRS_CH3_INT_STA_REG	0x0344	CSIC Parser Channel_3 Interrupt Status Register
CSIC_PRS_CH3_LINE_TIME_REG	0x0348	CSIC Parser Channel_3 Line Time Register
CSIC_PRS_CH3_FRM_PRE_MSK_REG	0x034C	CSIC Parser Channel_3 Frame Pre Mask Setting Register
CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	CSIC Parser NCSIC RX Signal0 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG	0x050C	CSIC Parser NCSIC RX Signal3 Delay Adjust Register

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Register Name	Offset	Description
CSIC_PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG	0x0510	CSIC Parser NCSIC RX Signal4 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	CSIC Parser NCSIC RX Signal5 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	CSIC Parser NCSIC RX Signal6 Delay Adjust Register
CSIC_PRS_SYNC_EN_REG	0x0520	CSIC Parser SYNC EN Register
CSIC_PRS_SYNC_CFG_REG	0x0524	CSIC Parser SYNC CFG Register
SIC_PRS_VS_WAIT_N_REG	0x0528	CSIC Parser VS WAIT N Register
CSIC_PRS_VS_WAIT_M_REG	0x052C	CSIC Parser VS WAIT M Register
CSIC_PRS_XSYNC_ENABLE_REG	0x0540	CSIC Parser XSYNC ENABLE Register
CSIC_PRS_XVS_PERIOD_REG	0x0544	CSIC Parser XVS Period Register
CSIC_PRS_XHS_PERIOD_REG	0x0548	CSIC Parser XHS Period Register
CSIC_PRS_XVS_LENGTH_REG	0x054C	CSIC Parser XVS LENGTH Register
CSIC_PRS_XHS_LENGTH_REG	0x0550	CSIC Parser XHS LENGTH Register
CSIC_PRS_SYNC_DLY_REG	0x0554	CSIC Parser SYNC DELAY Register

7.1.5.5 CSIC_DMA Register List

NOTE

There is only one channel (CH0) in CSIC_DMA4 and CSIC_DMA5.

Module Name	Base Address
CSIC_DMA0	0x05830000
CSIC_DMA1	0x05831000
CSIC_DMA2	0x05832000
CSIC_DMA3	0x05833000
CSIC_DMA4	0x05834000
CSIC_DMA5	0x05835000

Register Name	Offset	Description
CSIC_DMA_TOP_REG	0x0000	CSIC DMA TOP Register
CSIC_DMA_MUL_CH_CFG_REG	0x0004	CSIC DMA Multi-Channel Configuration Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0010	CSIC DMA Frame Rate Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0014	CSIC DMA Accumulated and Internal Clock Counter Register
CSIC_DMA_FS_FRM_CNT_REG	0x0020	CSIC DMA Fsync Frame Counter Register

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Register Name	Offset	Description
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_VE_FRM_CNT_REG	0x0050	CSIC DMA VE Frame Counter Value Register
CSIC_DMA_VE_LINE_CNT_REG	0x0054	CSIC DMA VE Line Counter Value Register
CSIC_DMA_VE_CUR_FRM_ADDR_REG	0x0058	CSIC DMA VE Current Frame Address Register
CSIC_DMA_VE_LAST_FRM_ADDR_REG	0x005C	CSIC DMA VE Last Frame Address Register
CSIC_DMA_FIFO_STAT_REG	0x0080	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x0084	CSIC DMA FIFO Threshold Register
CSIC_DMA_TOP_INT_EN_REG	0x0100	CSIC DMA TOP Interrupt Enable Register
CSIC_DMA_TOP_INT_STA_REG	0x0104	CSIC DMA TOP Interrupt Status Register
CSIC_DMA_VER_REG	0x01F0	CSIC DMA Version Register
CSIC_DMA_FEATURE_REG	0x01F4	CSIC DMA Feature List Register
CSIC_DMA_CH0_EN_REG	0x0200	CSIC DMA Channel0 Enable Register
CSIC_DMA_CH0_CFG_REG	0x0204	CSIC DMA Channel0 Configuration Register
CSIC_DMA_CH0_FRM_LOST_CNT_REG	0x0208	CSIC DMA Channel0 Frame Lost Counter Register
CSIC_DMA_CH0_FRM_MSK_CFG_REG	0x020C	CSIC DMA Channel0 Frame Mask Configuration Register
CSIC_DMA_CH0_HSIZE_REG	0x0210	CSIC DMA Channel0 Horizontal Size Register
CSIC_DMA_CH0_VSIZE_REG	0x0214	CSIC DMA Channel0 Vertical Size Register
CSIC_DMA_CH0_VCROP_CFG_REG	0x0218	CSIC DMA Channel0 Vertical Crop Mode Register
CSIC_DMA_CH0_F0_BUFA_REG	0x0220	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH0_F0_BUFA_RESULT_REG	0x0224	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F1_BUFA_REG	0x0228	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH0_F1_BUFA_RESULT_REG	0x022C	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F2_BUFA_REG	0x0230	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH0_F2_BUFA_RESULT_REG	0x0234	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH0_BUF_LEN_REG	0x0238	CSIC DMA Channel0 Buffer Length Register
CSIC_DMA_CH0_FLIP_SIZE_REG	0x023C	CSIC DMA Channel0 Flip Size Register

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Register Name	Offset	Description
CSIC_DMA_CH0_CAP_STA_REG	0x024C	CSIC DMA Channel0 Capture Status Register
CSIC_DMA_CH0_INT_EN_REG	0x0250	CSIC DMA Channel0 Interrupt Enable Register
CSIC_DMA_CH0_INT_STA_REG	0x0254	CSIC DMA Channel0 Interrupt Status Register
CSIC_DMA_CH0_LINE_CNT_REG	0x0258	CSIC DMA Channel0 Line Counter Register
CSIC_DMA_CH0_ABN_FRM_NUM_REG	0x025C	CSIC DMA Channel0 Abnormal Frame Number Register
CSIC_DMA_CH0_LINE_STAT_REG	0x0268	CSIC DMA Channel0 Line Statistic Register
CSIC_DMA_CH0_PCLK_STAT_REG	0x0270	CSIC DMA Channel0 PCLK Statistic Register
CSIC_DMA_CH0_ABN_MSK_REG	0x0298	CSIC DMA Channel0 Abnormal Mask Register
CSIC_DMA_CH0_PIXELS_ADD_EN_REG	0x029C	CSIC DMA Channel0 Pixels Add Enable Register
CSIC_DMA_CH0_PIXELS_ADD_VAL_REG	0x02A0	CSIC DMA Channel0 Pixels Add Value Register
The following resgisters are only for DMA0-DMA3.		
CSIC_DMA_CH1_EN_REG	0x0400	CSIC DMA Channel1 Enable Register
CSIC_DMA_CH1_CFG_REG	0x0404	CSIC DMA Channel1 Configuration Register
CSIC_DMA_CH1_FRM_LOST_CNT_REG	0x0408	CSIC DMA Channel1 Frame Lost Counter Register
CSIC_DMA_CH1_FRM_MSK_CFG_REG	0x040C	CSIC DMA Channel1 Frame Mask Configuration Register
CSIC_DMA_CH1_HSIZE_REG	0x0410	CSIC DMA Channel1 Horizontal Size Register
CSIC_DMA_CH1_VSIZE_REG	0x0414	CSIC DMA Channel1 Vertical Size Register
CSIC_DMA_CH1_VCROP_CFG_REG	0x0418	CSIC DMA Channel1 Vertical Crop Mode Register
CSIC_DMA_CH1_F0_BUFA_REG	0x0420	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH1_F0_BUFA_RESULT_REG	0x0424	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F1_BUFA_REG	0x0428	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH1_F1_BUFA_RESULT_REG	0x042C	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F2_BUFA_REG	0x0430	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH1_F2_BUFA_RESULT_REG	0x0434	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH1_BUF_LEN_REG	0x0438	CSIC DMA Channel1 Buffer Length Register
CSIC_DMA_CH1_FLIP_SIZE_REG	0x043C	CSIC DMA Channel1 Flip Size Register
CSIC_DMA_CH1_CAP_STA_REG	0x044C	CSIC DMA Channel1 Capture Status Register
CSIC_DMA_CH1_INT_EN_REG	0x0450	CSIC DMA Channel1 Interrupt Enable Register

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Register Name	Offset	Description
CSIC_DMA_CH1_INT_STA_REG	0x0454	CSIC DMA Channel1 Interrupt Status Register
CSIC_DMA_CH1_LINE_CNT_REG	0x0458	CSIC DMA Channel1 Line Counter Register
CSIC_DMA_CH1_ABN_FRM_NUM_REG	0x045C	CSIC DMA Channel1 Abnormal Frame Number Register
CSIC_DMA_CH1_LINE_STAT_REG	0x0468	CSIC DMA Channel1 Line Statistic Register
CSIC_DMA_CH1_PCLK_STAT_REG	0x0470	CSIC DMA Channel1 PCLK Statistic Register
CSIC_DMA_CH1_ABN_MSK_REG	0x0498	CSIC DMA Channel1 Abnormal Mask Register
CSIC_DMA_CH1_PIXELS_ADD_EN_REG	0x049C	CSIC DMA Channel1 Pixels Add Enable Register
CSIC_DMA_CH1_PIXELS_ADD_VAL_REG	0x04A0	CSIC DMA Channel1 Pixels Add Value Register
CSIC_DMA_CH2_EN_REG	0x0600	CSIC DMA Channel2 Enable Register
CSIC_DMA_CH2_CFG_REG	0x0604	CSIC DMA Channel2 Configuration Register
CSIC_DMA_CH2_FRM_LOST_CNT_REG	0x0608	CSIC DMA Channel2 Frame Lost Counter Register
CSIC_DMA_CH2_FRM_MSK_CFG_REG	0x060C	CSIC DMA Channel2 Frame Mask Configuration Register
CSIC_DMA_CH2_HSIZE_REG	0x0610	CSIC DMA Channel2 Horizontal Size Register
CSIC_DMA_CH2_VSIZE_REG	0x0614	CSIC DMA Channel2 Vertical Size Register
CSIC_DMA_CH2_VCROP_CFG_REG	0x0618	CSIC DMA Channel2 Vertical Crop Mode Register
CSIC_DMA_CH2_F0_BUFA_REG	0x0620	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH2_F0_BUFA_RESULT_REG	0x0624	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F1_BUFA_REG	0x0628	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH2_F1_BUFA_RESULT_REG	0x062C	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F2_BUFA_REG	0x0630	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH2_F2_BUFA_RESULT_REG	0x0634	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH2_BUF_LEN_REG	0x0638	CSIC DMA Channel2 Buffer Length Register
CSIC_DMA_CH2_FLIP_SIZE_REG	0x063C	CSIC DMA Channel2 Flip Size Register
CSIC_DMA_CH2_CAP_STA_REG	0x064C	CSIC DMA Channel2 Capture Status Register
CSIC_DMA_CH2_INT_EN_REG	0x0650	CSIC DMA Channel2 Interrupt Enable Register
CSIC_DMA_CH2_INT_STA_REG	0x0654	CSIC DMA Channel2 Interrupt Status Register
CSIC_DMA_CH2_LINE_CNT_REG	0x0658	CSIC DMA Channel2 Line Counter Register

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Register Name	Offset	Description
CSIC_DMA_CH2_ABN_FRM_NUM_REG	0x065C	CSIC DMA Channel2 Abnormal Frame Number Register
CSIC_DMA_CH2_LINE_STAT_REG	0x0668	CSIC DMA Channel2 Line Statistic Register
CSIC_DMA_CH2_PCLK_STAT_REG	0x0670	CSIC DMA Channel2 PCLK Statistic Register
CSIC_DMA_CH2_ABN_MSK_REG	0x0698	CSIC DMA Channel2 Abnormal Mask Register
CSIC_DMA_CH2_PIXELS_ADD_EN_REG	0x069C	CSIC DMA Channel2 Pixels Add Enable Register
CSIC_DMA_CH2_PIXELS_ADD_VAL_REG	0x06A0	CSIC DMA Channel2 Pixels Add Value Register
CSIC_DMA_CH3_EN_REG	0x0800	CSIC DMA Channel3 Enable Register
CSIC_DMA_CH3_CFG_REG	0x0804	CSIC DMA Channel3 Configuration Register
CSIC_DMA_CH3_FRM_LOST_CNT_REG	0x0808	CSIC DMA Channel3 Frame Lost Counter Register
CSIC_DMA_CH3_FRM_MSK_CFG_REG	0x080C	CSIC DMA Channel3 Frame Mask Configuration Register
CSIC_DMA_CH3_HSIZE_REG	0x0810	CSIC DMA Channel3 Horizontal Size Register
CSIC_DMA_CH3_VSIZE_REG	0x0814	CSIC DMA Channel3 Vertical Size Register
CSIC_DMA_CH3_VCROP_CFG_REG	0x0818	CSIC DMA Channel3 Vertical Crop Mode Register
CSIC_DMA_CH3_F0_BUFA_REG	0x0820	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH3_F0_BUFA_RESULT_REG	0x0824	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F1_BUFA_REG	0x0828	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH3_F1_BUFA_RESULT_REG	0x082C	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F2_BUFA_REG	0x0830	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH3_F2_BUFA_RESULT_REG	0x0834	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH3_BUF_LEN_REG	0x0838	CSIC DMA Channel3 Buffer Length Register
CSIC_DMA_CH3_FLIP_SIZE_REG	0x083C	CSIC DMA Channel3 Flip Size Register
CSIC_DMA_CH3_CAP_STA_REG	0x084C	CSIC DMA Channel3 Capture Status Register
CSIC_DMA_CH3_INT_EN_REG	0x0850	CSIC DMA Channel3 Interrupt Enable Register
CSIC_DMA_CH3_INT_STA_REG	0x0854	CSIC DMA Channel3 Interrupt Status Register
CSIC_DMA_CH3_LINE_CNT_REG	0x0858	CSIC DMA Channel3 Line Counter Register
CSIC_DMA_CH3_ABN_FRM_NUM_REG	0x085C	CSIC DMA Channel3 Abnormal Frame Number Register

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Register Name	Offset	Description
CSIC_DMA_CH3_LINE_STAT_REG	0x0868	CSIC DMA Channel3 Line Statistic Register
CSIC_DMA_CH3_PCLK_STAT_REG	0x0870	CSIC DMA Channel3 PCLK Statistic Register
CSIC_DMA_CH3_ABN_MSK_REG	0x0898	CSIC DMA Channel3 Abnormal Mask Register
CSIC_DMA_CH3_PIXELS_ADD_EN_REG	0x089C	CSIC DMA Channel3 Pixels Add Enable Register
CSIC_DMA_CH3_PIXELS_ADD_VAL_REG	0x08A0	CSIC DMA Channel3 Pixels Add Value Register

7.1.6 CSIC CCU Register Description

7.1.6.1 0x0000 CSIC CCU Clock Mode Register (Default Value:0x0000_0003)

Offset: 0x0000			Register Name: CCU_CLK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CCU_CLK_GATING_DISABLE 0: CCU Clock Gating Registers(0x0004-0x0010) effect 1:CCU Clock Gating Registers(0x0004-0x0010) not effect
30:2	/	/	/
1	R/W	0x1	MCSI_POST_CLK_MODE 0: CSI Post works in ISP core clock 1: CSI Post works in CSI clock
0	R/W	0x1	MCSI_PARSER_CLK_MODE 0: CSI Parser works in ISP core clock 1: CSI Parser works in CSI clock

7.1.6.2 0x0004 CSIC CCU Parser Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE 0: Combo0 clock disable 1: Combo0 clock enable
7:4	/	/	/
3	R/W	0x0	MCSI_PARSER3_CLK_ENABLE 0: CSI Parser3 clock disable 1: CSI Parser3 clock enable

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Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	MCSI_PARSER2_CLK_ENABLE 0: CSI Parser2 clock disable 1: CSI Parser2 clock enable
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE Parser0 clock gating 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

7.1.6.3 0x0008 CSIC CCU ISP Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x0008			Register Name: CCU_ISP_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MISP_MBUS_RST 0: ISP0 MBUS reset de-assert 1: ISP0 MBUS reset assert
7:5	/	/	/
4	R/W	0x0	MISP0_BRIDGE_CLK_ENABLE 0: ISP0 bridge clock disable 1: ISP0 bridge clock enable
3:1	/	/	/
0	R/W	0x0	MISP0_CLK_ENABLE 0: ISP0 clock disable 1: ISP0 clock enable

7.1.6.4 0x000C CSIC CCU Post0 Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	MCSI_POST0_MBUS_RST 0: POST0 MBUS reset de-assert 1: POST0 MBUS reset assert
19:17	/	/	/

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Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	MCSI_POST0_CLK_ENABLE Post0 clock gating 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0: VIPP1 clock disable 1: VIPP1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE 0: VIPP0 clock disable 1: VIPP0 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE 0: BK3 clock disable 1: BK3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE BK1 clock gating 0: BK1 clock disable 1: BK1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE BK0 clock gating 0: BK0 clock disable 1: BK0 clock enable, when MCSI_POST0_CLK_ENABLE is 1

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7.1.6.5 0x0010 CSIC CCU Post0 Clock Enable Sup Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_CCU_POST0_CLK_EN_SUP_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	MCSI_BK5_CLK_ENABLE BK5 clock gating 0: BK5 clock disable 1: BK5 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
0	R/W	0x0	MCSI_BK4_CLK_ENABLE BK4 clock gating 0: BK4 clock disable 1: BK4 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1

7.1.6.6 0x0014 CSIC CCU Chfreq Clock Control Register (Default Value:0x0000_1700)

Offset: 0x0014			Register Name: CSIC_CCU_CHFREQ_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x00	FACTOR_N Factor N= FACTOR_N +1. FACTOR_N is from 0 to 31
15:13	/	/	/
12:8	R/W	0x17	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31
7:1	/	/	/
0	R/W	0x0	CHFREQ_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CHFREQ_CLK = Clock Source/M/N. Clock Source is clk24m.

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7.1.7 CSIC TOP Register Description

7.1.7.1 0x0000 CSIC TOP Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ISP_BRIDGE_EN Enable Async Bridge from parser to ISP and ISP to post, when ISP uses different clock source from csi_top_clk 0: Disable 1: Enable
2:0	/	/	/

7.1.7.2 0x0004 CSIC Pattern Generation Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software writes this bit to “1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to “0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

7.1.7.3 0x0008 CSIC Pattern Control Register (Default Value:0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

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Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 101: NCSIC3 110: COMBO others: Reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH Pattern Generator output data width 00:8bit 01:10bit 10:12bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000: MIPI 1-lane 0001: MIPI 2-lane 0010: MIPI 3-lane 0011: MIPI 4-lane 0100:NCSIC with max 12-bit data ({field,vsyn,hsyn,1'b0,data[11:0]}) 0101:NCSIC with max 16-bit data ({12'h0,field,vsyn,hsyn,1'b0,data[15:0]}) 0110:NCSIC with max 24-bit data ({field,vsyn,hsyn,5'h0,data[23:0]}) 0111: Reserved 1000:BT656 8 bits' width 1001:BT656 16 bits' width 1010:BT656 24 bits' width 1011: Reserved 1100: BAYER 12 bits for ISPFE 1101: UYVY422 12 bits for ISPFE 1110: UYVY420 12 bits for ISPFE 1111:Reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

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7.1.7.4 0x0010 CSIC_PTN_VBLANK_CYCLE Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PTN_VBLANK_CYCLE
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PTN_VBLANK_CYCLE Set clock cycles between two pattern as vblank

7.1.7.5 0x0020 CSIC Pattern Generation Length Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

7.1.7.6 0x0024 CSIC Pattern Generation Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

7.1.7.7 0x0028 CSIC Pattern ISP Size Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

7.1.7.8 0x0030 CSIC ISP0 Input0 Select Register (Default Value:0x0000_0000)

Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	ISP0 Input0 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.9 0x0034 CSIC ISP0 Input1 Select Register (Default Value:0x0000_0001)

Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x1	ISP0 Input1 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.10 0x0038 CSIC ISP0 Input2 Select Register (Default Value:0x0000_0002)

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x2	ISP0 Input2 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.11 0x003C CSIC ISP0 Input3 Select Register (Default Value:0x0000_0003)

Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x3	ISP0 Input3 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.12 0x0040 CSIC ISP1 Input0 Select Register (Default Value:0x0000_0004)

Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x4	ISP1 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.13 0x0044 CSIC ISP1 Input1 Select Register (Default Value:0x0000_0005)

Offset :0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x5	ISP1 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.14 0x0048 CSIC ISP1 Input2 Select Register (Default Value:0x0000_0006)

Offset :0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x6	ISP1 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.15 0x004C CSIC ISP1 Input3 Select Register (Default Value:0x0000_0007)

Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x7	ISP1 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.16 0x0050 CSIC ISP2 Input0 Select Register(Default Value:0x0000_0008)

Offset :0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x8	ISP2 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.17 0x0054 CSIC ISP2 Input1 Select Register(Default Value:0x0000_0009)

Offset :0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x9	ISP2 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.18 0x0058 CSIC ISP2 Input2 Select Register(Default Value:0x0000_000a)

Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xa	ISP2 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.19 0x005C CSIC ISP2 Input3 Select Register(Default Value:0x0000_000b)

Offset :0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xb	ISP2 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.20 0x0060 CSIC ISP3 Input0 Select Register(Default Value:0x0000_000c)

Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xc	ISP3 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.21 0x0064 CSIC ISP3 Input1 Select Register(Default Value:0x0000_000d)

Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xd	ISP3 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.22 0x0068 CSIC ISP3 Input2 Select Register(Default Value:0x0000_000e)

Offset :0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xe	ISP3 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.23 0x006C CSIC ISP3 Input3 Select Register(Default Value:0x0000_000f)

Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xf	ISP3 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.24 0x0070 CSIC ISP Bridge Buffer Maxuse Counter Clear Register (Default Value:0x0000_0000)

Offset :0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ISP0_BRG3_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
2	R/W	0x0	ISP0_BRG2_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
1	R/W	0x0	ISP0_BRG1_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
0	R/W	0x0	ISP0_BRG0_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear

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7.1.7.25 0x0074 CSIC ISP0 Bridge01 Buffer Maxuse Counter Register (Default Value:0x0000_0000)

Offset :0x0074			Register Name: CSIC_ISP0_BRG01_BUF_MAXUSE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	ISP0_BRG1_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG0_BUF_MAXUSE_CNT

7.1.7.26 0x0078 CSIC ISP0 Bridge23 Buffer Maxuse Counter Register (Default Value:0x0000_0000)

Offset :0x0078			Register Name: CSIC_ISP0_BRG23_BUF_MAXUSE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	ISP0_BRG3_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG2_BUF_MAXUSE_CNT

7.1.7.27 0x0084 CSIC ISP0 Bridge Interrupt Enable Register (Default Value:0x0000_0000)

Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x0	ISP0_BRG3_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge3 Slow to Fast Side
26	R/W	0x0	ISP0_BRG2_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge2 Slow to Fast Side
25	R/W	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:20	/	/	/
19	R/W	0x0	ISP0_BRG3_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge3 Fast to Slow Side
18	R/W	0x0	ISP0_BRG2_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge2 Fast to Slow Side

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Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:12	/	/	/
11	R/W	0x0	ISP0_BRG3_BUF_OV_INT_EN ISP0 Bridge3 Buffer overflow interrupt enable
10	R/W	0x0	ISP0_BRG2_BUF_OV_INT_EN ISP0 Bridge2 Buffer overflow interrupt enable
9	R/W	0x0	ISP0_BRG1_BUF_OV_INT_EN ISP0 Bridge1 Buffer overflow interrupt enable
8	R/W	0x0	ISP0_BRG0_BUF_OV_INT_EN ISP0 Bridge0 Buffer overflow interrupt enable
7:4	/	/	/
3	R/W	0x0	ISP0_BRG3_RS_INT_EN ISP0 Bridge3 Read clock too slow interrupt enable
2	R/W	0x0	ISP0_BRG2_RS_INT_EN ISP0 Bridge2 Read clock too slow interrupt enable
1	R/W	0x0	ISP0_BRG1_RS_INT_EN ISP0 Bridge1 Read clock too slow interrupt enable
0	R/W	0x0	ISP0_BRG0_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable

7.1.7.28 0x008C CSIC ISP0 Bridge Interrupt Pending Register (Default Value:0x0000_0000)

Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W1C	0x0	ISP0_BRG3_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge3 Slow to Fast Side
26	R/W1C	0x0	ISP0_BRG2_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge2 Slow to Fast Side
25	R/W1C	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side

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Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:20	/	/	/
19	R/W1C	0x0	ISP0_BRG3_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge3 Fast to Slow Side
18	R/W1C	0x0	ISP0_BRG2_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge2 Fast to Slow Side
17	R/W1C	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W1C	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:12	/	/	/
11	R/W1C	0x0	ISP0_BRG3_BUF_OV_INT_PD ISP0 Bridge3 Buffer overflow interrupt pending
10	R/W1C	0x0	ISP0_BRG2_BUF_OV_INT_PD ISP0 Bridge2 Buffer overflow interrupt pending
9	R/W1C	0x0	ISP0_BRG1_BUF_OV_INT_PD ISP0 Bridge1 Buffer overflow interrupt pending
8	R/W1C	0x0	ISP0_BRG0_BUF_OV_INT_PD ISP0 Bridge0 Buffer overflow interrupt pending
7:4	/	/	/
3	R/W1C	0x0	ISP0_BRG3_RS_INT_PD ISP0 Bridge3 Read clock too slow interrupt pending
2	R/W1C	0x0	ISP0_BRG2_RS_INT_PD ISP0 Bridge2 Read clock too slow interrupt pending
1	R/W1C	0x0	ISP0_BRG1_RS_INT_PD ISP0 Bridge1 Read clock too slow interrupt pending
0	R/W1C	0x0	ISP0_BRG0_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending

7.1.7.29 0x00A0 CSIC DMA0 Input Select Register (Default Value:0x0000_0000)

Offset :0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA0 input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.30 0x00A4 CSIC DMA1 Input Select Register (Default Value:0x0000_0000)

Offset :0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA1 input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.31 0x00A8 CSIC DMA2 Input Select Register (Default Value:0x0000_0000)

Offset :0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA2 input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.32 0x00AC CSIC DMA3 Input Select Register (Default Value:0x0000_0000)

Offset :0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA3 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 **Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.**

7.1.7.33 0x00B0 CSIC DMA4 Input Select Register (Default Value:0x0000_0000)

Offset :0x00B0			Register Name: CSIC_DMA4_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x00B0			Register Name: CSIC_DMA4_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA4 input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.34 0x00B4 CSIC DMA5 Input Select Register (Default Value:0x0000_0000)

Offset :0x00B4			Register Name: CSIC_DMA5_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset :0x00B4			Register Name: CSIC_DMA5_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA5 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.35 0x00E0 CSIC BIST Control Register (Default Value:0x0000_0200)

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0:NO effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle
9	R	0x1	BIST_STOP BIST STOP 0: Running 1:Stop

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Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
8	R	0x0	BIST_BUSY BIST Busy 0: IDLE 1:Busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select
4	R/W	0x0	BIST_ADDR_MODE_SEL BIST Address Mode Select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write Data Pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST Enable. A positive will trigger the BIST to start.

7.1.7.36 0x00E4 CSIC BIST Start Address Register (Default Value:0x0000_0000)

Offset: 0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST Start Address BIST Start Address. It is 32-bit aligned.

7.1.7.37 0x00E8 CSIC BIST End Address Register (Default Value:0x0000_0000)

Offset: 0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST END Address BIST END Address. It is 32-bit aligned.

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7.1.7.38 0x00EC CSIC BIST Data Mask Register (Default Value:0x0000_0000)

Offset: 0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0: Unmask 1:Mask

7.1.7.39 0x00F0 CSIC MBUS REQ MAX Register (Default Value:0x000f_0f0f)

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:21	R	0x000	Reserved
20:16	R/W	0x0f	MISP_MEM_REQ_MAX (no use actually, fixed as 16) Maximum of request commands for the master granted in MISP_MEM arbiter is N+1.
15:5	/	/	/
4:0	R/W	0x0f	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

7.1.7.40 0x0100 CSIC Multi-Frame Mode Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	MULF_STATUS Multi-Frame Mode Status indicates each DMA in frame done pending or not
23:16	/	/	/
15:8	R/W	0x0	MULF_CS Chip Selection for Multi-Frame Mode indicates which DMA is in selected
7:1	/	/	/
0	R/W	0x0	MULF_EN Multi-Frame Mode Enable

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7.1.7.41 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	MULF_ERR_PD Multi-Frame Mode Frame Error Interrupt Pending
16	R/W1C	0x0	MULF_DONE_PD Multi-Frame Mode Frame Done Interrupt Pending
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN Multi-Frame Mode Frame Error Interrupt Enable
0	R/W	0x0	MULF_DONE_EN Multi-Frame Mode Frame Done Interrupt Enable

7.1.7.42 0x0108 CSIC Change Frequency Configuration 0 Register (Default Value:0x0001_0000)

Offset: 0x0108			Register Name: CSIC_CHFREQ_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0001	CHFREQ_PAR2ISP_SEL Chfreq_par2isp select. Each bit corresponds to one channel. When the channel has data stream passing through, the corresponding bit must be set to 1. [19:16]->par2isp0 ch3, ch2, ch1, ch0 [23:20]->par2isp1 ch3, ch2, ch1, ch0 [27:24]->par2isp2 ch3, ch2, ch1, ch0 [31:28]->par2isp3 ch3,ch2,ch1,ch0
15:6	/	/	/
5	R/W	0x0	CHFREQ_BK_DONE_SRC Chfreq_bk done source select. 0: Select bk_frm_end as source 1: Select bk_frm_done as source
4	R/W	0x0	CHFREQ_PULSE_CNT_SCLR_EN Chfreq_pulse Cent Self-Clear Enable 0: Disable pulse cnt self clear 1: Enable pulse cnt self clear
3	R/W	0x0	CHFREQ_RDY_MASK 0: Unmask 1: Mask assert, keep chfreq_rdy output as 0

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Offset: 0x0108			Register Name: CSIC_CHFREQ_CFG0_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CHFREQ_SELECT Chfreq_rdy output source select 0: New implementation 1: Old implementation
1	R/W	0x0	CHFREQ_ALLOW Chfreq Allow Signal 0: Keep chfreq_rdy output as 0 1: Allow chfreq logic when CHFREQ_EN is asserted or all of bk*_en, mvipp*_en, and isp_en are set as 0, CHFREQ_ALLOW will not take effect.
0	R/W	0x0	CHFREQ_RST Soft reset for chfreq logic. 0: Assert 1:De-assert

7.1.7.43 0x010C CSIC Change Frequency Configuration 1 Register (Default Value:0x0000_0064)

Offset: 0x010C			Register Name: CSIC_CHFREQ_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x0000	CHFREQ_WAIT_DONE_TIME The time between hardware chfreq frm_done assert and mcsi chfrq_rdy assert. Take one chfreq_clk cycle as the unit, which is 1 us by default.
15:0	R/W	0x0064	CHFREQ_DDR_TIME The time for DDR to complete frequency change. Take one chfreq_clk cycle as a unit, which is 1 us by default.

7.1.7.44 0x0110 CSIC Change Frequency Observation Register (Default Value:0x0000_0000)

Offset: 0x0110			Register Name: CSIC_CHFREQ_OBS_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0000	CHFREQ_FRM_DONE_TIME The time for frm done after frm_end, measured by hardware. Take one chfreq_clk cycle as the unit, which by default is 1 us.

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Offset: 0x0110			Register Name: CSIC_CHFREQ_OBS_REG
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0000	CHFREQ_VBLANK_LENGTH Vblank length measured by hardware. Take one chfreq_clk cycle as the unit, which by default is 1 us.

7.1.7.45 0x0114 CSIC Change Frequency Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0114			Register Name: CSIC_CHFREQ_INT_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	CHFREQ_FRM_DONE_NUM_ERR_PD Change Frequency Frame Done Number Error Interrupt Pending
17	R/W1C	0x0	CHFREQ_FRM_END_NUM_ERR_PD Change Frequency Frame End Number Error Interrupt Pending
16	R/W1C	0x0	CHFREQ_FRM_STR_NUM_ERR_PD Change Frequency Frame Start Number Error Interrupt Pending
15:3	/	/	/
2	R/W	0x0	CHFREQ_FRM_DONE_NUM_ERR_EN Change Frequency Frame Done Number Error Interrupt Enable
1	R/W	0x0	CHFREQ_FRM_END_NUM_ERR_EN Change Frequency Frame End Number Error Interrupt Enable
0	R/W	0x0	CHFREQ_FRM_STR_NUM_ERR_EN Change Frequency Frame Start Number Error Interrupt Enable

7.1.7.46 0x0118 CSIC Change Frequency Debug Observation Register (Default Value:0x0000_2101)

Offset: 0x0118			Register Name: CSIC_CHFREQ_DBG_OBS_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	CHFREQ_RSTN_T
26	R	0x0	ISP_RSTN_T
25	R	0x0	PAR_RSTN_T
24	R	0x0	POST_RSTN_T
23	R	0x0	ISP_EN_POST_S

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Offset: 0x0118			Register Name: CSIC_CHFREQ_DBG_OBS_REG
Bit	Read/Write	Default/Hex	Description
22:18	R	0x0	FRM_DONE_SRC_NUM
17:13	R	0x1	FRM_STR_SRC_NUM
12:8	R	0x1	FRM_END_SRC_NUM
7	R	0x0	POST_EN_S
6	R	0x0	ISP_EN_S
5	R	0x0	CHFREQ_ALLOW_S
4	R	0x0	FIRST_FRM_END_RECEIVED
3	R	0x0	VBLANK_LENGTH_VALID
2	R	0x0	IN_VBLANK
1	R	0x0	FRM_DONE_TIME_VALID
0	R	0x1	CHFREQ_RDY

7.1.7.47 0x01F0 CSIC Feature List Register (Default Value:0x4411_4600)

Offset: 0x01F0			Register Name: CSIC_FEATURE_LIST_REG
Bit	Read/Write	Default/Hex	Description
31:28	R	0x4	PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x4	MCSI_NUM Only can be read when version register read enable is on.
23:20	R	0x1	NCSI_NUM Only can be read when version register read enable is on.
19:16	R	0x1	ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x6	DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

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7.1.8 CSIC_PHY COMMON Register Description

7.1.8.1 0x0000 PHY Top Control Register (Default Value: 0x006_0500)

Offset:0x0000			Register Name: PHY_TOP_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:29	R/W	0x0	PHY_LINK_MODE PHY Link Selection 2'b00: 4 x 2-lane Links 2'b01: 2 x 2-lane + 1 x 4-lane(phya+phyb) Link 2'b10: 2 x 2-lane + 1 x 4-lane(phyc+phyd) Link 2'b11: 2 x 4-lane(phya+phyb, phyc+phyd) Link
28:27	/	/	/
26:24	R/W	0x0	PRBS_SEL PRBS Test Interface Selection 0x0: PHYA PRBS 0x1: PHYB PRBS 0x2: PHYC PRBS 0x3: PHYD PRBS Other: Reserved
23:12	/	/	/
11:10	R/W	0x1	PHY_VREF_0P2 PHY 0.2V Terminal Resistor Reference Voltage Fine Trimming Every step is 25 mV.
9:8	R/W	0x1	PHY_VREF_0P9 PHY 0.9V LDO Reference Voltage Fine Trimming Every step is 50 mV.
7:4	/	/	/
3	R/W	0x0	PHY_LVLDO_EN PHY 0.9V LDO Enable (High Active)
2	R/W	0x0	PHY_VREF_EN PHY Reference Voltage Enable
1	R/W	0x0	PHY_RSTN PHY Analog Layer Digital Circuit Reset (Low Active)
0	R/W	0x0	PHY_PWDNZ PHY Analog Layer Power Reset (Low Active)

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7.1.8.2 0x0004 PHY Terminal Resistor Calibration Register (Default Value: 0x0000_00a5)

Offset:0x0004			Register Name: PHY_TRESCAL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R	0x0	PHY_TRESCAL_RESULT PHY Terminal Resistor Calibration Result In automatic calibration mode, the result is automatic calibration output value. In software calibration mode, the result is the value of PHY0_TRESCAL_SET bit.
15:9	/	/	/
8:4	R/W	0xa	PHY_TRESCAL_SET PHY Terminal Resistor Software Calibration Set Value
3	R	0x0	PHY_TRESCAL_FLAG PHY Terminal Resistor Calibration Flag In automatic calibration mode, when the value of this bit is 1, the automatic calibration is completed. This bit is fixed as 1 in software calibration mode.
2	R/W	0x1	PHY_TRESCAL_RESETN PHY Terminal Resistor Calibration Reset This bit is only valid for automatic calibration, low active.
1	R/W	0x0	PHY_TRESCAL_SOFT PHY Terminal Resistor Software Calibration Enable (High Active)
0	R/W	0x1	PHY_TRESCAL_AUTO PHY Terminal Resistor Automatic Calibration Enable (High Active)

7.1.9 CSIC_PHY DIGITAL LAYER Register Description

7.1.9.1 0x0000 PHY Control Register (Default Value: 0x0004_0000)

Offset:0x0000			Register Name: PHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PHY0_WORK_MODE 0: Every lane works in MIPI mode.
27	/	/	/

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Offset:0x0000			Register Name: PHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	PHY0_IBIAS_EN PHY0 Reference Current Enable (High Active)
25:20	/	/	/
19	R/W	0x0	PHY0_VCM PHY0 Common Voltage Selection 0: 200mV（MIPI） 1: Reserved
18:16	R/W	0x4	PHY0_HS_REFI Obtain faster speed of every lane by adjusting PHY0 HSRX reference current. The larger the value of this bit, the faster the speed of every lane.
15:13	/	/	/
12	R/W	0x0	PHY0_LP_REFI Adjust the threshold voltage window size by adjusting LPRX reference current, which is able to filter LP noise signals effectively.
11:9	/	/	/
8	R/W	0x0	PHY_LANECK_EN PHY Clock Lane Enable
7:6	/	/	/
5:4	R/W	0x0	PHY_LANEDT_EN PHY Data Lane0-1 Enable
3:1	/	/	/
0	R/W	0x0	PHY_EN PHY Digital Layer Enable (High Active)

7.1.9.2 0x0004 PHY Equalization Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: PHY_EQ_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	PHY_EQ_LANECK0 PHY clock lane0 comparator equalization compensation value
23:20	/	/	/
19:18	R/W	0x0	PHY_EQ_LANED1 PHYC data lane1 comparator equalization compensation value

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Offset:0x0004			Register Name: PHY_EQ_REG
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	PHY_EQ_LANED0 PHY data lane0 comparator equalization compensation value
15:5	/	/	/
4:4	R/W	0x0	PHY_EQ_CK_EN PHY clock lane comparator equalization enable (high active)
3:0	R/W	0x0	PHY_EQ_DT_EN PHY data lane0-1 comparator equalization enable (high active) Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: reserved

7.1.9.3 0x0008 PHY Offset Calibration Register0 (Default Value: 0x0010_0010)

Offset:0x0008			Register Name: PHY_OFSCAL_REG0
Bit	Read/Write	Default/Hex	Description
31:39	/	/	/
28	R	0x0	PHY0_OFSCAL_FLAG PHY0 Offset Calibration Flag In automatic calibration mode, when the value of this bit is 1, the automatic calibration is completed. This bit is fixed as 1 in software calibration mode.
27:21	/	/	/
20	R/W	0x1	PHY0_OFSCAL_RESETN PHY0 Offset Calibration Reset The comparator offset of every lane restarts to calibrate after reset. **Note: This bit is only valid for automatic calibration mode.**
19:13	/	/	/
12	R/W	0x0	PHY0_OFSCAL_SOFT PHY0 offset software calibration enable (high active)
7:6	/	/	/
4	R/W	0x1	PHY_OFSCAL_AUTO PHY0 offset automatic calibration enable (high active)

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Offset:0x0008			Register Name: PHY_OFSCAL_REG0
Bit	Read/Write	Default/Hex	Description
3:0	/	/	/

7.1.9.4 0x000C PHY Offset Calibration Register1 (Default Value: 0x0120_0000)

Offset: 0x000C			Register Name: PHY_OFSCAL_REG1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R/W	0x12	PHY0_OFSCAL_SET PHY0 offset software calibration set value
19:0	/	/	/

7.1.9.5 0x0010 PHY Offset Calibration Register2(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PHY_OFSCAL_REG2
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R	0x0	PHY0_OFSCAL_RESULT PHY0 offset calibration result In automatic calibration mode, the result is automatic calibration output value. In software calibration mode, the result is the value of PHY0_OFSCAL_SET bit.
19:0	/	/	/

7.1.9.6 0x0014 PHY Deskew Register0 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: PHY_DESKEW_REG0
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	PHY0_DESKEW_STEP PHY0 data lane initial deskew step precision 00: Every step is 1. 01: Every step is 2. 10: Every step is 4. 11: Reserved
7:6	/	/	/
5:4	R/W	0x0	PHY_DESKEW_PERIOD_EN PHY data lane0-1 period deskew automatic delay enable (high active)

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Offset: 0x0014			Register Name: PHY_DESKEW_REG0
Bit	Read/Write	Default/Hex	Description
3:2	/	/	/
1:0	R/W	0x0	PHY_DESKEW_EN PHY data lane0-1 deskew automatic delay enable (high active)

7.1.9.7 0x0018 PHY Deskew Register1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PHY_DESKEW_REG1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R/W	0x0	PHY_DESKEW_LANECK0_SET PHY clock lane0 delay
19:10	/	/	/
9:5	R/W	0x0	PHY_DESKEW_LANED1_SET PHY data lane1 delay This bit is valid when PHY_DESKEW_EN[1] =1.
4:0	R/W	0x0	PHY_DESKEW_LANED0_SET PHY data lane0 delay This bit is valid when PHY_DESKEW_EN[0] =0.

7.1.9.8 0x001C PHY Deskew Register2(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PHY_DESKEW_REG2
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
24:20	R	0x0	PHY_DESKEW_LANECK0_RESULT PHY clock lane0 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK0_SET bit.
19:10	/	/	/
9:5	R	0x0	PHY_DESKEW_LANED1_RESULT PHY data lane1 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK1_SET bit, when PHY_DESKEW_EN[1] =1.
4:0	R	0x0	PHY_DESKEW_LANED0_RESULT PHY data lane0 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK0_SET bit, when PHY_DESKEW_EN[0] =0.

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7.1.9.9 0x0020 PHY Terminal Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PHY_TERM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_TERM_EN_DLY These bits are to set the delay of every clock lane and data lane from high-speed RX (LP11-LP01-LP00) request is received to the terminal resistor is enabled in hardware auto-enable mode. These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:5	/	/	/
4	R/W	0x0	PHY_TERMCK_EN PHY Clock Lane Terminal Resistor Software Enable 0: Hardware auto-enable 1: Software enable
3:0	R/W	0x0	PHY_TERMDT_EN PHY Data Lane 0-1 Terminal Resistor Software Enable 0: Hardware auto-enable 1: Software enable Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved

7.1.9.10 0x0024 PHY High Speed Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PHY_HS_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_HS_DLY These bits are to set the delay of every clock lane and data lane from high-speed RX (LP11-LP01-LP00) request is received to the high-speed comparator is enabled in hardware auto-enable mode. These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:13	/	/	/

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Offset: 0x0024			Register Name: PHY_HS_CTL_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	PHY_HSCK_POLAR PHY Clock Lane HSRX Signal Inversion 0: HSRX Signal is not inverse. 1: HSRX Signal is inverse.
11:8	R/W	0x0	PHY_HSDT_POLAR PHY Data Lane0-1 HSRX Signal Inversion 0: HSRX Signal is not inverse. 1: HSRX Signal is inverse.
7:5	/	/	/
4	R/W	0x0	PHY_HSCK_EN PHY Clock Lane High-Speed Mode Software Enable (High Active) 0: Hardware auto-enable 1: Software enable
3:0	R/W	0x0	PHY_HSDT_EN PHY Data Lane0-1 High-Speed Mode Software Enable (High Active) 0: Hardware auto-enable 1: Software enable Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved

7.1.9.11 0x0028 PHY Serial to Parallel Control Register (Default Value: 0x0000_0A00)

Offset: 0x0028			Register Name: PHY_S2P_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_S2P_DLY These bits are to set the delay of every data lane from high-speed RX request is received to the S2P circuit is enabled in hardware auto-enable mode (HS_Settle). These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:10	/	/	/

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Offset: 0x0028			Register Name: PHY_S2P_CTL_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x2	PHY0_S2P_WIDTH PHY0 S2P Circuit Output Width 00: 2 bits 01: 4 bits 1X: 8 bits
7:4	/	/	/
3:0	R/W	0x0	PHY_S2P_EN PHY Data Lane0-1 S2P Circuit Software Enable 0: Hardware auto-enable 1: Software enable Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved

7.1.9.12 0x002C PHY MIPIRX Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PHY_MIPIRX_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PHY0_MIPILP_DBC_EN PHY0 LPRX Debounce Circuit Enable (High Active)
15:13	/	/	/
12	R/W	0x0	PHY_MIPI_LPCK_EN PHY Clock Lane LPRX Enable 0: Disable LPRX 1: Enable LPRX
11:8	R/W	0x0	PHY_MIPI_LPDT_EN PHY Data Lane 0-1 LPRX Enable 0: Disable LPRX 1: Enable LPRX Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved
7:5	/	/	/
4	R/W	0x0	PHY0_MIPIHS_8B9B 0: No 8B9B decoding when receiving bytes in PHY0 MIPI high-speed mode. 1: 8B9B decoding when receiving bytes in PHY0 MIPI high-speed mode.

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Offset: 0x002C			Register Name: PHY_MIPIRX_CTL_REG
Bit	Read/Write	Default/Hex	Description
3	/	/	/
2	R/W	0x0	PHY0_MIPIHS_SYNC_MODE 0: The Sync-Sequence must be 0xb8 in PHY0 MIPI high-speed mode. 1: The Sync-Sequence allows 1-bit difference from 0xb8 in PHY0 MIPI high-speed mode.
1	/	/	/
0	R/W	0x0	PHY0_MIPIHS_ENDIAN This bit is to set which one of the big-endian and little-endian to receive data in PHY0 MIPI high-speed mode. 0: LSB First 1: MSB First

7.1.9.13 0x0030 PHY MIPIRX Synchronization Timeout Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PHY_MIPIRX_SYNC_TIMEOUT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_MIPIHS_SYNC_TOSET The PHY_NOSYNC_ERR_D0_PD bit and PHY_NOSYNC_ERR_D1_PD bit will generate interrupts when the Sync-Sequence (0xb8) is unable to be detected after PHY0 data lane switching from LP mode to HS mode for a period of time configured by this bit. The unit is 16 byte_clk cycles.
15:1	/	/	/
0	R/W	0x0	PHY0_MIPIHS_SYNC_TOEN PHY0 data lane HS Sync-Sequence Detection Time Out Enable (High Active)

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7.1.9.14 0x0034 PHY Frequency Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PHY_FREQ_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PHY_FREQ_CNT The value of these bits is the number of cmb_clk cycle during 1000 PHY byte clk cycles, which is used for byte clk frequency conversion of PHY0 or PHY1. The unit is cmb_clk cycle.
15:1	/	/	/
0	R/W	0x0	PHY0_FREQ_EN PHY0 byte_clk frequency detection enable (high active)

7.1.9.15 0x0038 PHY MIPI LP Timeout Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PHY_MIPI_LP_TIMEOUT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_MIPI_LP_TIMEOUT_SET By default, the LP value will be refreshed when PHY0 MIPI LP signal bounce occurs. After enabling PHY0_MIPI_LP_TIMEOUT_EN bit, even if the signal bounce does not occur, the LP value will be refreshed after the time set by this bit. The unit is cmb_clk cycle.
15:1	/	/	/
0	R/W	0x0	PHY0_MIPI_LP_TIMEOUT_EN By default, the LP value will be refreshed when PHY0 MIPI LP signal bounce occurs. After enabling this bit, even if the signal bounce does not occur, the LP value will be refreshed after the time set by the PHY0_MIPI_LP_TIMEOUT_SET bit.

7.1.9.16 0x0040 PHY MIPI ULPSEXIT Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PHY_MIPI_ULPSEXIT_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY0_MIPI_ULPS_EN Enter ULPS status after the ULPS instruction is detected by PHY0 lane.

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Offset: 0x0040			Register Name: PHY_MIPI_ULPSEXIT_REG0
Bit	Read/Write	Default/Hex	Description
30:20	/	/	/
19:0	R/W	0x0	PHY0_MIPI_ULPSEXIT PHY0 lane needs to keep detecting Mark 1 signal for a certain period of time before exiting ULPS status. The unit is cmb_clk cycle.

7.1.9.17 0x0080 PHY Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PHY_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PHY_LP_CK0_CMD_EN PHY Clock Lane0 Interrupt Enable An interrupt is to be generated after recognizable LP commands are received by PHY clock lane0.
15:14	/	/	/
13	R/W	0x0	PHY_LP_D1_CMD_EN PHY Data Lane1 Interrupt Enable An interrupt is to be generated after recognizable LP commands are received by PHY data lane1.
12	R/W	0x0	PHY_LP_D0_CMD_EN PHY Data Lane0 Interrupt Enable An interrupt is to be generated after recognizable LP commands are received by PHY data lane0.
11:10	/	/	/
9	R/W	0x0	PHY_NOSYNC_ERR_D1_EN PHY Sync-Sequence Error Interrupt Enable An interrupt is to be generated, if the Sync-Sequence is unable to be detected a period of time after data lane1 is switched from LP mode to HS mode.
8	R/W	0x0	PHY_NOSYNC_ERR_D0_EN PHY Sync-Sequence Error Interrupt Enable An interrupt is to be generated, if the Sync-Sequence is unable to be detected a period of time after data lane0 is switched from LP mode to HS mode.
7:6	/	/	/

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Offset: 0x0080			Register Name: PHY_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PHY_SYNC_ERR_D1_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane1 Sync-Sequence.
4	R/W	0x0	PHY_SYNC_ERR_D0_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane0 Sync-Sequence.
3:2	/	/	/
1	R/W	0x0	PHY_SOTDET_D1_EN Generate an interrupt after the Sync-Sequence is detected in Data lane1.
0	R/W	0x0	PHY_SOTDET_D0_EN Generate an interrupt after the Sync-Sequence is detected in Data lane0.

7.1.9.18 0x0084 PHY Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: PHY_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1C	0x0	PHY_LP_CK0_CMD_PD Generate an interrupt after PHY clock lane0 receives recognizable LP commands.
15:14	/	/	/
13	R/W1C	0x0	PHY_LP_D1_CMD_PD Generate an interrupt after PHY clock lane1 receives recognizable LP commands.
12	R/W1C	0x0	PHY_LP_D0_CMD_PD Generate an interrupt after PHY data lane0 receives recognizable LP commands.
11:10	/	/	/
9	R/W1C	0x0	PHY_NOSYNC_ERR_D1_PD Generate an interrupt when the Sync-Sequence is unable to be detected a period of time after data lane1 is switched from LP mode to HS mode.
8	R/W1C	0x0	PHY_NOSYNC_ERR_D0_PD Generate an interrupt when the Sync-Sequence is unable to be detected a period of time after data lane0 is switched from LP mode to HS mode.

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Offset: 0x0084			Register Name: PHY_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
7:6	/	/	/
5	R/W1C	0x0	PHY_SYNC_ERR_D1_PD Generate an interrupt when 1-bit error is detected in the data lane1 Sync-Sequence.
4	R/W1C	0x0	PHY_SYNC_ERR_D0_PD Generate an interrupt when 1-bit error is detected in the data lane0 Sync-Sequence.
3:2	/	/	/
1	R/W1C	0x0	PHY_SOTDET_D1_PD Generate an interrupt after the Sync-Sequence is detected in data lane1.
0	R/W1C	0x0	PHY_SOTDET_D0_PD Generate an interrupt after the Sync-Sequence is detected in data lane0.

7.1.10 CSIC_PHY PORT PAYLOAD LAYER Register Description

7.1.10.1 0x0000 PORT Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: PORT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT_OUT_NUM 0: Output 1 data every valid 1: Output 2 data every valid
30:18	/	/	/
17:16	R/W	0x0	PORT_CHANNEL_NUM 0: 1 channel 1: 2 channels 2: 3 channels 3: 4 channels
15:12	/	/	/
11:8	R/W	0x0	PORT_LANE_NUM MIPI: 1-4 PORT0 and PORT2 support maximum 4 lanes. PORT1 and PORT3 support maximum 2 lanes.
7:6	/	/	/
5:4	R/W	0x0	PORT_WORK_MODE 00: PORT channels work in MIPI mode. 01: Reserved
3:1	/	/	/

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Offset: 0x0000			Register Name: PORT_CTL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PORT_EN PORT Channel Enable (High Active)

7.1.10.2 0x0004 PORT Lane Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0x0	PORT_LANE3_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE3 0x1: Set lane1 (PHYA lane1) as PORT LANE3 0x4: Set lane4 (PHYB lane0) as PORT LANE3 0x5: Set lane5 (PHYB lane1) as PORT LANE3 0x8: Set lane8 (PHYC lane0) as PORT LANE3 0x9: Set lane9 (PHYC lane1) as PORT LANE3 0xc: Set lane12 (PHYD lane0) as PORT LANE3 0xd: Set lane13 (PHYD lane1) as PORT LANE3
11:8	R/W	0x0	PORT_LANE2_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE2 0x1: Set lane1 (PHYA lane1) as PORT LANE2 0x4: Set lane4 (PHYB lane0) as PORT LANE2 0x5: Set lane5 (PHYB lane1) as PORT LANE2 0x8: Set lane8 (PHYC lane0) as PORT LANE2 0x9: Set lane9 (PHYC lane1) as PORT LANE2 0xc: Set lane12 (PHYD lane0) as PORT LANE2 0xd: Set lane13 (PHYD lane1) as PORT LANE2
7:4	R/W	0x0	PORT_LANE1_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE1 0x1: Set lane1 (PHYA lane1) as PORT LANE1 0x4: Set lane4 (PHYB lane0) as PORT LANE1 0x5: Set lane5 (PHYB lane1) as PORT LANE1 0x8: Set lane8 (PHYC lane0) as PORT LANE1 0x9: Set lane9 (PHYC lane1) as PORT LANE1 0xc: Set lane12 (PHYD lane0) as PORT LANE1 0xd: Set lane13 (PHYD lane1) as PORT LANE1

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Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PORT_LANE0_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE0 0x1: Set lane1 (PHYA lane1) as PORT LANE0 0x4: Set lane4 (PHYB lane0) as PORT LANE0 0x5: Set lane5 (PHYB lane1) as PORT LANE0 0x8: Set lane8 (PHYC lane0) as PORT LANE0 0x9: Set lane9 (PHYC lane1) as PORT LANE0 0xc: Set lane12 (PHYD lane0) as PORT LANE0 0xd: Set lane13 (PHYD lane1) as PORT LANE0

7.1.10.3 0x000C PORT WDR Mode Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PORT_WDR_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PORT_WDR_MODE 0x0: Normal mode, No WDR, MIPI VC, or MIPIDT. 0x2: Pixel data mode, distinguish the multi-channel WDR/HR images through the first pixel data of each line. others：Reserved

7.1.10.4 0x0010 PORT Frame ID Select Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PORT_FID_SEL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT_FID_MODE 0: Identify the Frame in bit cs mode. For example, identify Frame0 when FID [0] =1, identify Frame1 when FID [1] =1. 1: Identify the Frame in bit value mode. For example, identify Frame0 when FID [0] =0, identify Frame1 when FID [0] =1.
30:20	/	/	/

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Offset: 0x0010			Register Name: PORT_FID_SEL_REG
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	PORT_FID_MAP_EN FID Mapping Enable Bit19: FID3_MAP_EN Bit18: FID2_MAP_EN Bit17: FID1_MAP_EN Bit16: FID0_MAP_EN
15:12	R/W	0x0	PORT_FID3_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID3 in the first pixel data of every line.
11:8	R/W	0x0	PORT_FID2_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID2 in the first pixel data of every line.
7:4	R/W	0x0	PORT_FID1_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID1 in the first pixel data of every line.
3:0	R/W	0x0	PORT_FID0_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID0 in the first pixel data of every line.

7.1.10.5 0x0100 PORT MIPI Configuration Register (Default Value: 0x4920_0000)

Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:26	R/W	0x12	MIPI_REAR_EMB_DTYPE MIPI Rear Embedded Data Type Value
25:20	R/W	0x12	MIPI_FRONT_EMB_DTYPE MIPI Front Embedded Data Type Value
19	R/W	0x0	MIPI_EMB_MAP The MIPI received embedded data is output in a certain format. 0: Output in the pixel format of the corresponding channel. 1: Output in RAW8 format.
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Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	MIPI_YUV_SEQ MIPI YUV Format Transmission Sequence 00: YUYV 01: YVYU 10: UYVY 11: VYUY
15:10	/	/	/
9	R/W	0x0	MIPI_FRAME_SYNC_ONLY_FS MIPI Frame Synchronization only for Frame Start 0: No support 1: Support
8	R/W	0x0	MIPI_LINE_SYNC_EN MIPI Line Synchronization Enable 0: Generate line sync signals based on long packets 1: Generate line sync signals based on short packets
7	R/W	0x0	MIPI_PL_BITORD MIPI RX Payload Bit Sequence 0: LSb First 1: MSb First
6	R/W	0x0	MIPI_PH_BITORD MIPI Packet Header Bit Sequence (for ECC checksum) 0: LSb First, for example, {WC [15:8], WC[7:0], DI[7:0]} 1: MSb First, for example,{WC[8:15],WC[0:7], DI[0:7]}
5:4	R/W	0x0	MIPI_PH_BYTEORD MIPI Packet Header Byte Sequence (for ECC check) 0: {WCH, WCL, DI} 1: {DI, WCH, WCL} 2: {WCL, WCH, DI} 3: {DI,WCL,WCH}
3	R/W	0x0	MIPI_USER_DEF_EN MIPI USER Define Data Type Enable
2	R/W	0x0	EMBED_EN embed data receiving enable and output in the pixel format of the corresponding channel.

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Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	MIPI_NO_UNPACK_ALL **MIPI_UNPACK_EN=0**: Receive data directly without unpacking. **MIPI_NO_UNPACK_ALL=0**: Only receive effective high-speed data without unpacking and output them from PORT Channel0 in RAW8 format. **MIPI_NO_UNPACK_ALL =1**: Receive rxhs_active, rxhs_valid, and rxhs_data[7:0] simultaneously as RX data and output them from PORT Channel0 in {2'h0，rxhs_active, rxhs_valid, rxhs_data[7:0]} sequence in RAW12 format.
0	R/W	0x0	MIPI_UNPACK_EN MIPI CSI2 Protocol Unpack Enable

7.1.10.6 0x0104 PORT MIPI No Unpacket Number Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: PORT_MIPI_NO_UNPAK_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0x0	MIPI_NO_UNPAK_NUM_REG This bit indicates the number of received raw data. The unit is pixel component.

7.1.10.7 0x0108 PORT MIPI Data Identity Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PORT_MIPI_DI_REG
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	MIPI_CH3_VC MIPI Channel3 VC Number Set
29:24	R/W	0x0	MIPI_CH3_DT MIPI Channel3 Data Type Set
23:22	R/W	0x0	MIPI_CH2_VC MIPI channel2 VC Number Set
21:16	R/W	0x0	MIPI_CH2_DT MIPI Channel2 Data Type Set
15:14	R/W	0x0	MIPI_CH1_VC MIPI Channel1 VC Number Set

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Offset: 0x0108			Register Name: PORT_MIPI_DI_REG
Bit	Read/Write	Default/Hex	Description
13:8	R/W	0x0	MIPI_CH1_DT MIPI Channel1 Data Type Set
7:6	R/W	0x0	MIPI_CH0_VC MIPI channel0 VC Number Set
5:0	R/W	0x0	MIPI_CH0_DT MIPI Channel0 Data Type Set/Real Mapping of USER Define Data Type

7.1.10.8 0x010C PORT MIPI User Data Type Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PORT_MIPI_USER_DT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_USER3_DT_EN Channel3 MIPI USER Define Data Type Enable
30	/	/	/
29:24	R/W	0x0	MIPI_USER3_DT Channel3 MIPI USER Define Data Type This bit is to identify the data belonging to channel3, which is unpacked into the data type set by the MIPI_CH3_DT bit following CSI2 protocol.
23	R/W	0x0	MIPI_USER2_DT_EN Channel2 MIPI USER Define Data Type Enable
22	/	/	/
21:16	R/W	0x0	MIPI_USER2_DT Channel2 MIPI USER Define Data Type This bit is to identify the data belonging to channel2, which is unpacked into the data type set by the MIPI_CH2_DT bit following CSI2 protocol.
15	R/W	0x0	MIPI_USER1_DT_EN Channel1 MIPI USER Define Data Type Enable
14	/	/	/
13:8	R/W	0x0	MIPI_USER1_DT Channel1 MIPI USER Define Data Type This bit is to identify the data belonging to channel1, which is unpacked into the data type set by the MIPI_CH1_DT bit following CSI2 protocol.

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Offset: 0x010C			Register Name: PORT_MIPI_USER_DT_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	MIPI_USER0_DT_EN Channel0 MIPI USER Define Data Type
6	/	/	/
5:0	R/W	0x0	MIPI_USER0_DT Channel0 MIPI USER Define Data Type This bit is to identify the data belonging to channel0, which is unpacked into the data type set by the MIPI_CH0_DT bit following CSI2 protocol.

7.1.10.9 0x0110 PORT MIPI Channel0 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled

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Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled

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Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.10 0x0114 PORT MIPI Channel0 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PORT_MIPI_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable

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Offset: 0x0114			Register Name: PORT_MIPI_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

7.1.10.11 0x0118 PORT MIPI Channel0 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PORT_MIPI_CH0_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt

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Offset: 0x0118			Register Name: PORT_MIPI_CH0_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.12 0x011C PORT MIPI Channel0 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PORT_MIPI_CH0_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.13 0x0120 PORT MIPI Channel0 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PORT_MIPI_CH0_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/

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Offset: 0x0120			Register Name: PORT_MIPI_CH0_ECC_REG
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.14 0x0124 PORT MIPI Channel0 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PORT_MIPI_CH0_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.15 0x0128 PORT MIPI Channel0 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PORT_MIPI_CH0_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.16 0x012C PORT MIPI Channel0 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PORT_MIPI_CH0_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

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7.1.10.17 0x0130 PORT MIPI Channel1 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled

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Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/

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Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.18 0x0134 PORT MIPI Channel1 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: PORT_MIPI_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable

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Offset: 0x0134			Register Name: PORT_MIPI_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

7.1.10.19 0x0138 PORT MIPI Channel1 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: PORT_MIPI_CH1_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt

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Offset: 0x0138			Register Name: PORT_MIPI_CH1_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.20 0x013C PORT MIPI Channel1 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PORT_MIPI_CH1_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.21 0x0140 PORT MIPI Channel1 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PORT_MIPI_CH1_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.22 0x0144 PORT MIPI Channel1 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PORT_MIPI_CH1_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum

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Offset: 0x0144			Register Name: PORT_MIPI_CH1_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.23 0x0148 PORT MIPI Channel1 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PORT_MIPI_CH1_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.24 0x014C PORT MIPI Channel1 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PORT_MIPI_CH1_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.25 0x0150 PORT MIPI Channel2 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.

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Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled

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Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

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7.1.10.26 0x0154 PORT MIPI Channel2 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: PORT_MIPI_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

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7.1.10.27 0x0158 PORT MIPI Channel2 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PORT_MIPI_CH2_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.28 0x015C PORT MIPI Channel2 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PORT_MIPI_CH2_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel

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Offset: 0x015C			Register Name: PORT_MIPI_CH2_PH_REG
Bit	Read/Write	Default/Hex	Description
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.29 0x0160 PORT MIPI Channel2 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PORT_MIPI_CH2_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.30 0x0164 PORT MIPI Channel2 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PORT_MIPI_CH2_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.31 0x0168 PORT MIPI Channel2 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PORT_MIPI_CH2_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.32 0x016C PORT MIPI Channel2 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: PORT_MIPI_CH2_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x016C			Register Name: PORT_MIPI_CH2_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.33 0x0170 PORT MIPI Channel3 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field polarity 0: positive (frm num [0] =1 indicate odd, =0 indicate even) 1: negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled

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Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled

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Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.34 0x0174 PORT MIPI Channel3 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PORT_MIPI_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable

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Offset: 0x0174			Register Name: PORT_MIPI_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

7.1.10.35 0x0178 PORT MIPI Channel3 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PORT_MIPI_CH3_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt

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Offset: 0x0178			Register Name: PORT_MIPI_CH3_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.36 0x017C PORT MIPI Channel3 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PORT_MIPI_CH3_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.37 0x0180 PORT MIPI Channel3 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PORT_MIPI_CH3_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

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7.1.10.38 0x0184 PORT MIPI Channel3 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: PORT_MIPI_CH3_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.39 0x0188 PORT MIPI Channel3 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: PORT_MIPI_CH3_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.40 0x018C PORT MIPI Channel3 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x018C			Register Name: PORT_MIPI_CH3_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.41 0x01F0 PORT MIPI Lane Error Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: PORT_MIPI_LANE_ERR_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0x0	MIPI_LANE_ACT_NO_VLD_INT_EN Data lane0-3 receive no valid data when act high interrupt enable
3:0	R/W	0x0	MIPI_LANE_FIFO_OVERFLOW_INT_EN Data lane0-3 FIFO overflow interrupt enable

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7.1.10.42 0x01F4 PORT MIPI Lane Error Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: PORT_MIPI_LANE_ERR_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W1C	0x0	MIPI_LANE_ACT_NO_VLD_INT_PD Data lane0-3 receive no valid data when act high interrupt
3:0	R/W1C	0x0	MIPI_LANE_FIFO_OVERFLOW_INT_PD Data lane0-3 FIFO overflow interrupt

7.1.11 CSIC_PARSER Register Description

7.1.11.1 0x0000 CSIC Parser Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/
16	R/W	0x0	NCSIC_EN NCSI Controller Enable 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN NCSI Pixel Clock Gating 0: Gate pclk input 1:Enable pclk input
14:4	/	/	/
3:2	R/W	0x0	PRS_CH_MODE Parser channel mode 00: Parser output channel 0-3 corresponding from input channel 0-3 01: Parser output channel 0-3 all from input channel 0 10: Parser output channel0 and 2 from input channel 0, output channel1 and 3 from input channel 1 11: Reserved

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Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PRS_MODE Parser Mode 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN Parser Enable 0: Reset and disable the parser module 1: Enable the parser module

7.1.11.2 0x0004 CSIC Parser NCSIC Interface Configuration Register (Default Value:0x0105_0080)

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER YUV420 Input Line Order 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30	R/W	0x0	ONLY_ACT_CARE 1:only care V active period
29	R/W	0x0	YUV422_SEP When input format is YUV422 16bit or Bt1120, set this bit to transfer YU,YV(2 components for each clock cycle) to Y,U,Y,V(1 component for each clock cycle)
28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode, the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:20	R/W	0x0	SRC_TYPE Bit 20-23 corresponding to the Source types for channel0-3 0: Progressed 1: Interlaced
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: Negative (field=0 indicate odd, field=1 indicate even) 1: Positive (field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)

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Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
18	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	FIELD_DT_MODE only valid when CSI_IF is YUV and source type is interlaced 00:by both field and vsync 01:by field 10:by vsync 11:reserved
13	R/W	0x0	DDR_SAMPLE_MODE_EN Dual Data Rate Sample Mode Enable 0: Disable 1:Enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D [11:4] will be rearranged to D [11:2] +2’b0 at the actual CSI data bus according to these sequences: 00: 6’bx+D [9:8], D [7:0] 01: D [9:2], 6’bx+D [1:0] 10: D [7:0], D [9:8] +6’bx 11: D[7:0], 6’bx+D[9:8]

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Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
10:8	R/W	0x0	IF_DATA_WIDTH Input Data Width 000: 8-bit data bus 001: 10-bit data bus 010: 12-bit data bus 011: 8+2bit data bus 100: 2x8/16bit data bus 101:14-bit data bus 110:20-bit data bus, only for packet generator 111:24 bit data bus, only for packet generator
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	/	/	/

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Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	CSI_IF YUV (separate syncs): 00000: YUYV422/YUV420 or RAW (All data in one data bus) 00001: 2x8 bit YUYV422 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16bit BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16bit BT656(BT1120 like) 2 channels (All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16bit BT656(BT1120 like) 4 channels (All data interleaved in one data bus) Others: Reserved

7.1.11.3 0x0008 CSIC Parser MCSIC Interface Configuration Register (Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/

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Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0X2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5:0	/	/	/

7.1.11.4 0x000C CSIC Parser Capture Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH3_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_1_REG bit [31:16]. Show an example as following. When CH3_FPS_DS_PRD is configured as 4’d6, CSIC_PRS_CAP_FRM_MSK_1_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CAP_FRM_MSK_1_REG bit[22:16] is configured as 7’b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

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Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/WAC	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.
23:22	/	/	/
21:18	R/W	0x0	CH2_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH2_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_1_REG bit [15:0]. Show an example as following. When CH2_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_1_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_PRS_CAP_FRM_MSK_1_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

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Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	R/WAC	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.
15:14	/	/	/
13:10	R/W	0x0	CH1_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH1_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_0_REG bit [31:16]. Show an example as following. When CH1_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_0_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CAP_FRM_MSK_0_REG bit[22:16] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

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Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	R/WAC	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.
7:6	/	/	/
5:2	R/W	0x0	CH0_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH0_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_0_REG bit [15:0]. Show an example as following. When CH0_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_0_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_PRS_CAP_FRM_MSK_0_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

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Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/WAC	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.

7.1.11.5 0x0010 CSIC Parser Signal Status Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	FIFO_FULL Indicates the NCSI IN Async FIFO FULL 0: Not Full 1:Full
30:28	R	0x0	PCLK_CNT Indicates the NCSI Pclk is toggle or not
27	R	0x0	VSYNC_STA Indicates the NCSI Vsync Signal status 0: Low 1:High
26	R	0x0	HSYNC_STA Indicates the NCSI Hsync Signal status 0: Low 1:High
25	R	0x0	FIELD_STA Indicates the NCSI Field Signal status 0: Low 1:High

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Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
24	R	0x0	DATA_VALID_STA Indicates the NCSI Data Valid Signal status(n=0-15), MSB for D15, LSB for D0 0: Low 1: High
23:0	R	0x0	DATA_STA Indicates the NCSI Data Signal status(n=0-15), MSB for D15, LSB for D0 0: Low 1: High

7.1.11.6 0x0014 CSIC Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

7.1.11.7 0x0018 CSIC Parser Capture Frame Mask 0 Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: CSIC_PRS_CAP_FRM_MSK_0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CH1_FRAME_DATA_MASK Only [CH1_FPS_DS_PRD+16:16] are valid

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Offset: 0x0018			Register Name: CSIC_PRS_CAP_FRM_MSK_0_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	CH0_FRAME_DATA_MASK Only [CH0_FPS_DS_PRD:0] are valid

7.1.11.8 0x001C CSIC Parser Capture Frame Mask 1 Register (Default Value:0x0000_0000)

Offset: 0x001C			Register Name: CSIC_PRS_CAP_FRM_MSK_1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CH3_FRAME_DATA_MASK Only [CH3_FPS_DS_PRD+16:16] are valid
15:0	R/W	0x0	CH2_FRAME_DATA_MASK Only [CH2_FPS_DS_PRD:0] are valid

7.1.11.9 0x0020 CSIC Parser Channel_0 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PRS_CH0_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH0 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH0_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH0_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH0_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

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7.1.11.10 0x0024 CSIC Parser Channel_0 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0024			Register Name: CSIC_PRS_CH0_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

7.1.11.11 0x0028 CSIC Parser Channel_0 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0028			Register Name: CSIC_PRS_CH0_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

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7.1.11.12 0x002C CSIC Parser Channel_0 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x002C			Register Name: CSIC_PRS_CH0_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.13 0x0030 CSIC Parser Channel_0 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_PRS_CH0_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 0 0: Progress 1: Interlace

7.1.11.14 0x0034 CSIC Parser Channel_0 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_PRS_CH0_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

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7.1.11.15 0x0038 CSIC Parser Channel_0 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: CSIC_PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.16 0x003C CSIC Parser Channel_0 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: CSIC_PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.17 0x0040 CSIC Parser Channel_0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	IN_VB_CHG_INT_EN
5	R/W	0x0	IN_Y_CHG_INT_EN
4	R/W	0x0	IN_HB_CHG_INT_EN
3	R/W	0x0	IN_X_CHG_INT_EN
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable

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Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.18 0x0044 CSIC Parser Channel_0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	IN_VB_CHG_PD
5	R/W1C	0x0	IN_Y_CHG_PD
4	R/W1C	0x0	IN_HB_CHG_PD
3	R/W1C	0x0	IN_X_CHG_PD
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

7.1.11.19 0x0048 CSIC Parser Channel_0 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_PRS_CH0_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

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7.1.11.20 0x004C CSIC Parser Channel_0 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x004C			Register Name: CSIC_PRS_CH0_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN This bit needs to be set after configurating FRM_PRE_MSK_NUM bit. 0: Disable frame pre mask 1: Enable frame pre mask

7.1.11.21 0x0120 CSIC Parser Channel_1 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0120			Register Name: CSIC_PRS_CH1_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0120			Register Name: CSIC_PRS_CH1_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH1 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH1_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH1_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH1_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.22 0x0124 CSIC Parser Channel_1 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0124			Register Name: CSIC_PRS_CH1_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid. Pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

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7.1.11.23 0x0128 CSIC Parser Channel_1 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0128			Register Name: CSIC_PRS_CH1_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.24 0x012C CSIC Parser Channel_1 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x012C			Register Name: CSIC_PRS_CH1_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.25 0x0130 CSIC Parser Channel_1 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0130			Register Name: CSIC_PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0130			Register Name: CSIC_PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 1 0: Progress 1:Interlace

7.1.11.26 0x0134 CSIC Parser Channel_1 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0134			Register Name: CSIC_PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.27 0x0138 CSIC Parser Channel_1 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0138			Register Name: CSIC_PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.28 0x013C CSIC Parser Channel_1 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.29 0x0140 CSIC Parser Channel_1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.30 0x0144 CSIC Parser Channel_1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0144			Register Name: CSIC_PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

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7.1.11.31 0x0148 CSIC Parser Channel_1 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0148			Register Name: CSIC_PRS_CH1_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle.
15:0	R	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle.

7.1.11.32 0x014C CSIC Parser Channel_1 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x014C			Register Name: CSIC_PRS_CH1_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN This bit needs to be set after configuring FRM_PRE_MSK_NUM bit. 0: Disable frame pre mask 1: Enable frame pre mask

7.1.11.33 0x0220 CSIC Parser Channel_2 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: CSIC_PRS_CH2_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0220			Register Name: CSIC_PRS_CH2_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH2 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH2_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH2_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH2_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.34 0x0224 CSIC Parser Channel_2 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0224			Register Name: CSIC_PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

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7.1.11.35 0x0228 CSIC Parser Channel_2 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0228			Register Name: CSIC_PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.36 0x022C CSIC Parser Channel_2 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.37 0x0230 CSIC Parser Channel_2 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_PRS_CH2_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0230			Register Name: CSIC_PRS_CH2_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 2 0: Progress 1: Interlace

7.1.11.38 0x0234 CSIC Parser Channel_2 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_PRS_CH2_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.39 0x0238 CSIC Parser Channel_2 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.40 0x023C CSIC Parser Channel_2 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x023C			Register Name: CSIC_PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x023C			Register Name: CSIC_PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.41 0x0240 CSIC Parser Channel_2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0240			Register Name: CSIC_PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.42 0x0244 CSIC Parser Channel_2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

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7.1.11.43 0x0248 CSIC Parser Channel_2 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0248			Register Name: CSIC_PRS_CH2_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle.
15:0	R	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle.

7.1.11.44 0x024C CSIC Parser Channel_2 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x024C			Register Name: CSIC_PRS_CH2_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN Should be set after configuring FRM_PRE_MSK_NUM 0: disable frame pre mask 1: enable frame pre mask

7.1.11.45 0x0320 CSIC Parser Channel_3 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0320			Register Name: CSIC_PRS_CH3_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0320			Register Name: CSIC_PRS_CH3_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH3 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH3_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH3_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH3_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.46 0x0324 CSIC Parser Channel_3 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0324			Register Name: CSIC_PRS_CH3_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

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7.1.11.47 0x0328 CSIC Parser Channel_3 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0328			Register Name: CSIC_PRS_CH3_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.48 0x032C CSIC Parser Channel_3 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x032C			Register Name: CSIC_PRS_CH3_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.49 0x0330 CSIC Parser Channel_3 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0330			Register Name: CSIC_PRS_CH3_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0330			Register Name: CSIC_PRS_CH3_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 3 0: Progress 1:Interlace

7.1.11.50 0x0334 CSIC Parser Channel_3 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0334			Register Name: CSIC_PRS_CH3_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.51 0x0338 CSIC Parser Channel_3 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0338			Register Name: CSIC_PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.52 0x033C CSIC Parser Channel_3 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x033C			Register Name: CSIC_PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x033C			Register Name: CSIC_PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.53 0x0340 CSIC Parser Channel_3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.54 0x0344 CSIC Parser Channel_3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0344			Register Name: CSIC_PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

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7.1.11.55 0x0348 CSIC Parser Channel_3 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0348			Register Name: CSIC_PRS_CH3_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

7.1.11.56 0x034C CSIC Parser Channel_3 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x034C			Register Name: CSIC_PRS_CH3_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN This bit needs to be set after the FRM_PRE_MSK_NUM bit is configured. 0: Disable frame pre mask 1: Enable frame pre mask

7.1.11.57 0x0500 CSIC Parser NCSIC RX Signal0 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	FILED_DLY 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	VSYNC_DLY 32 Step for adjust, 1 step = 0.2ns

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Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
15:13	/	/	/
12:8	R/W	0x0	HSYNC_DLY 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	PCLK_DLY 32 Step for adjust, 1 step = 0.2ns

7.1.11.58 0x050C CSIC Parser NCSIC RX Signal3 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.59 0x0510 CSIC Parser NCSIC RX Signal4 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns

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Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.60 0x0514 CSIC Parser NCSIC RX Signal5 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.61 0x0518 CSIC Parser NCSIC RX Signal6 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

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7.1.11.62 0X0520 CSIC Parser SYNC EN Register (Default Value:0x0000_0000)

Offset :0X0520			Register Name: CSIC_PRS_SYNC_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
19:16	R/W	0x0	VSYNC_MODE Input vsync signal Source select 0: Vsync signals all from 1 parser 1: Vsync signals from 2 parser 2: Vsync signals from 4 parser others: Reserved
15:12	/	/	/
11:8	R/W	0x0	VSYNC_SEL Generate sync signal Benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	VSYNC_USED Parser input vsync signal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	FSYNC_OUT_SEL Parser sent sync signal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	FSYNC_MODE Parser sync signal source select 0: From outside 1: Generate by self
0	R/W	0x0	FSYNC_FUN_EN Enable Parser sent sync signal 0: Disable 1: Enable

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7.1.11.63 0X0524 CSIC Parser SYNC CFG Register (Default Value:0x0000_0000)

Offset :0X0524			Register Name: CSIC_PRS_SYNC_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	FSYNC_PUL_WID Sync signal pulse width $N*T_{24M}$ $N*T_{24M} \geqslant 4*Tpclk$
15:0	R/W	0x0	FYSNC_DISTANCE The interval of two sync signal

7.1.11.64 0X0528 CSIC Parser VS WAIT N Register (Default Value:0x0000_0000)

Offset :0X0528			Register Name: CSIC_PRS_VS_WAIT_N_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come, the max wait time.

7.1.11.65 0X052C CSIC Parser VS WAIT M Register (Default Value:0x0000_0000)

Offset :0X052C			Register Name: CSIC_PRS_VS_WAIT_M_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode, sync comes at the different time, these bits indicate the max wait time.

7.1.11.66 0X0540 CSIC Parser XSYNC ENABLE Register (Default Value:0x0000_0000)

Offset: 0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0x0	XVS_TO_XHS_T The period of XHS delay to XVS, ${XVS_TO_XHS_T}+1 master clock cycles, no more than XHS_LEN
7:5	/	/	/
4	R/W	0x0	XVS_XHS_OUT_SEL When sensor works in slave mode, this bit select XVS and XHS to output. 0: XHS0, XVS0 1: XHS1,XVS1

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Offset: 0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	XVS_POL When sensor works in slave mode, this bit set polarity of XVS. 0: Negative 1: Positive
2	R/W	0x0	XHS_POL When sensor works in slave mode, this bit set polarity of XHS. 0: Negative 1: Positive
1	R/W	0x0	XVS_OUT_EN When sensor works in slave mode, this bit enables output XVS to sensor 0: Disable 1: Enable
0	R/W	0x0	XHS_OUT_EN When sensor works in slave mode, this bit enables output XHS to sensor 0: Disable 1: Enable

7.1.11.67 0X0544 CSIC Parser XVS Period Register (Default Value:0x0000_0000)

Offset: 0X0544			Register Name: CSIC_PRS_XVS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_T The period of XVS signal, ${XVS_T}+2 master clock cycles

7.1.11.68 0X0548 CSIC Parser XHS Period Register (Default Value:0x0000_0000)

Offset: 0X0548			Register Name: CSIC_PRS_XHS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_T The period of XHS signal, ${XHS_T}+2 master clock cycles

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7.1.11.69 0X054C CSIC Parser XVS LENGTH Register (Default Value:0x0000_0000)

Offset: 0X054C			Register Name: CSIC_PRS_XVS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_LEN The valid length of XVS signal, ${XVS_LEN}+1 master clock cycles

7.1.11.70 0X0550 CSIC Parser XHS LENGTH Register (Default Value:0x0000_0000)

Offset: 0X0550			Register Name: CSIC_PRS_XHS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_LEN The valid length of XHS signal, ${XHS_LEN}+1 master clock cycles

7.1.11.71 0X0554 CSIC Parser SYNC DELAY Register (Default Value:0x0000_0000)

Offset: 0X0554			Register Name: CSIC_PRS_SYNC_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SYNC_DLY The XHS/XVS will sent after, ${SYNC_DLY}+1 master clock cycles, no more than XVS_LEN

7.1.12 CISC_DMA Register Description

7.1.12.1 0x0000 CSIC DMA TOP Register (Default Value:0x7000_0000)

Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_EN CSIC DMA Version Register Read Enable: 0: Disable 1: Enable
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: hardware 1: software

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Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x1	BUF_LENGTH_CFG_MODE buffer length set by software or calculated by hardware 0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:17	/	/	/
16	R/W	0x0	FRM_END_SEL 0: Select mcsi_bk_frm_end_in 1: Select dma_frm_end
15	/	/	/
14:13	R/W	0x0	VE_ONLINE_CH_SEL Select BK Channel for VE Online handshake
12	R/W	0x0	VE_ONLINE_HANDSHAKE_EN Set this bit to Enable frame and line counter for VE online handshake
11:10	/	/	/
9:8	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if hflip is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes(not Support For DMA1\2\3)
7	/	/	/
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FS_FRM_CNT_EN When BK_TOP_EN enable, this bit set 1 indicate the Frame counter start to add. 0: Disable 1: Enable
4:3	/	/	/

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Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	FRM_RATE_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	FRM_RATE_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN Module Enable 0: Disable 1: Enable

7.1.12.2 0x0004 CSIC DMA Multi-Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R	0x0	CUR_OUT_CH When Multi-Channel enable, this field indicates the Current Output Channel ID
19:18	/	/	/
17:16	R	0x0	CUR_IN_CH When Multi-Channel enable, this field indicates the Current Input Channel ID
15:1	/	/	/
0	R/W	0x0	MUL_CH_EN DMA off-line multi-channel enable 0: disable 1: enable

7.1.12.3 0x0010 CSIC DMA Frame Rate Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0010			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
23:0	R	0x0	FRM_RATE_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

7.1.12.4 0x0014 CSIC DMA Accumulated and Internal Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

7.1.12.5 0x0020 CSIC DMA Fsync Frame Counter Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	FS_FRM_CNT_CLR When the bit set to 1,Frame cnt clear to 0
30:16	R/W	0x0	FS_FRM_CNT_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$

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Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
15	/	/	/
14:0	R	0x0	FS_FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the reg full ,it cleared to 0 . When parser sent a sync signal, it clear to 0

7.1.12.6 0x0040 CSIC DMA Video Input Timeout Threshold0 Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH0 Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , Time Unit is a 12M clock period.

7.1.12.7 0x0044 CSIC DMA Video Input Timeout Threshold1 Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH1 Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

7.1.12.8 0x0048 CSIC DMA Video Input Timeout Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
23:0	R	0x0	VI_TCNT_VAL Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

7.1.12.9 0x0050 CSIC DMA VE Frame Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_VE_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	FRM_DONE_CNT Indicates How Many Frame which Stored in DDR
15:8	/	/	/
7:0	R	0x0	FRM_ST_CNT Indicates the Frame Number which is Storing

7.1.12.10 0x0054 CSIC DMA VE Line Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_VE_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_DONE_CNT Indicates How Many Line which Stored in DDR
15:14	/	/	/
13:0	R	0x0	LINE_ST_CNT Indicates the Line Number which is Storing

7.1.12.11 0x0058 CSIC DMA VE Current Frame Address Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_VE_CUR_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_FRM_ADDR Indicates the FIFO0 Address Which Current Frame is Storing

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7.1.12.12 0x005C CSIC DMA VE Last Frame Address Register (Default Value:0x0000_0000)

Offset: 0x005C			Register Name: CSIC_DMA_VE_LAST_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LAST_FRM_ADDR Indicates the FIFO0 Address Which Last Frame is Stored

7.1.12.13 0x0080 CSIC DMA FIFO Statistic Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone. Unit is byte.

7.1.12.14 0x0084 CSIC DMA FIFO Threshold Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change. Unit is byte.

7.1.12.15 0x0100 CSIC DMA TOP Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_DMA_TOP_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time.
1	R/W	0x0	CLR_FS_FRM_CNT_INT_EN Set a INT When Clear FS Frame cnt.
0	R/W	0x0	FS_PUL_INT_EN Set an INT when a Fsync signal received

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7.1.12.16 0x0104 CSIC DMA TOP Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_DMA_TOP_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time
1	R/W1C	0x0	CLR_FRAME_CNT_INT_PD Set a INT When Clear FS Frame cnt.
0	R/W1C	0x0	FS_PUL_INT_PD Set an INT when a Fsync signal received

7.1.12.17 0x01F0 CSIC DMA Version Register (Default Value:0x0014_0100)

Offset: 0x01F0			Register Name: CSIC_DMA_VER_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:12	R	0x140	VER_BIG_VER Big Version of hardware circuit. Only can be read when version register read enable is on.
11:0	R	0x100	VER_SMALL_VER Small Version of hardware circuit. Only can be read when version register read enable is on.

7.1.12.18 0x01F4 CSIC DMA Feature List Register (Default Value:0x0000_0040)

Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R	0x4	DMA0_CHNUM Channel numbers (note: for DMA0-DMA3, DMA0/1/2/3_CHNUM=4; for DMA4-DMA5, DMA4/5_CHNUM=1)
3:2	/	/	/
1	R	0x0	DMA0_EMBEDDED_LBC LBC Feature Existence 0: No Embedded LBC 1: Embedded LBC

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Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	DMA0_EMBEDDED_FBC FBC Feature Existence 0: No Embedded FBC 1: Embedded FBC

7.1.12.19 0x0200 CSIC DMA Channel0 Enable Register (Default Value:0x0000_0000)

Offset: 0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:1	/	/	/
0	R/W	0x0	CAP_EN Video in Capture Enable 0: Disable 1: Enable

7.1.12.20 0x0204 CSIC DMA Channel0 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

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19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output

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Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved

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Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames …… 15: 16 frames CH0 FPS_DS_PRD should be used together with CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[15:0]. For example, when CH0 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH0_FRM_MSK_CFG_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.21 0x0208 CSIC DMA Channel0 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

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7.1.12.22 0x020C CSIC DMA Channel0 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x020C			Register Name: CSIC_DMA_CH0_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.23 0x0210 CSIC DMA Channel0 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0210			Register Name: CSIC_DMA_CH0_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.24 0x0214 CSIC DMA Channel0 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0214			Register Name: CSIC_DMA_CH0_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

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7.1.12.25 0x0218 CSIC DMA Channel0 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0218			Register Name: CSIC_DMA_CH0_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.26 0x0220 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: CSIC_DMA_CH0_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.27 0x0224 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register (Default 0x0224 Value:0x0000_0000)

Offset: 0x0224			Register Name: CSIC_DMA_CH0_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address FIFO. Only used for debug.

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7.1.12.28 0x0228 CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0228			Register Name: CSIC_DMA_CH0_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

7.1.12.29 0x022C CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x022C			Register Name: CSIC_DMA_CH0_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address FIFO. Only used for debug.

7.1.12.30 0x0230 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_DMA_CH0_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.31 0x0234 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_DMA_CH0_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address FIFO. Only used for debug.

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7.1.12.32 0x0238 CSIC DMA Channel0 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0238			Register Name: CSIC_DMA_CH0_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.33 0x023C CSIC DMA Channel0 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x023C			Register Name: CSIC_DMA_CH0_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.34 0x024C CSIC DMA Channel0 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/

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Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.35 0x0250 CSIC DMA Channel0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing

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Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN Vsync Flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this IRQ come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO_OF_INT_EN FIFO Overflow The bit is set when the FIFO occurs an overflow.
1	R/W	0x0	FD_INT_EN Frame Done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

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Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.36 0x0254 CSIC DMA Channel0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used

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Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

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7.1.12.37 0x0258 CSIC DMA Channel0 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0258			Register Name: CSIC_DMA_CH0_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user, when internal line counter reach the set value, the LC_PD will set.

7.1.12.38 0x025C CSIC DMA Channel0 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.39 0x0268 CSIC DMA Channel0 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0268			Register Name: CSIC_DMA_CH0_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current hsync.
15:0	/	/	/

7.1.12.40 0x0270 CSIC DMA Channel0 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/

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Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.41 0x0298 CSIC DMA Channel0 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

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Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

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7.1.12.42 0x029C CSIC DMA Channel0 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x029C			Register Name: CSIC_DMA_CH0_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels' miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.43 0x02A0 CSIC DMA Channel0 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x02A0			Register Name: CSIC_DMA_CH0_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

7.1.12.44 0x0400 CSIC DMA Channel1 Enable Register (Default Value:0x0000_0000)

Offset: 0x0400			Register Name: CSIC_DMA_CH1_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:1	/	/	/
0	R/W	0x0	CAP_EN Video in Capture Enable 0: Disable 1: Enable

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7.1.12.45 0x0404 CSIC DMA Channel1 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

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19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output

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Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved

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Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames ..... 15: 16 frames Note: CH1 FPS_DS_PRD should be used together with CSIC_DMA_CH1_FRM_MSK_CFG_REG bit [15:0]. For example, when CH1 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH1_FRM_MSK_CFG_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_DMA_CH1_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.46 0x0408 CSIC DMA Channel1 Frami Lost Counter Register (Default Value:0x0001_0000)

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

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7.1.12.47 0x040C CSIC DMA Channel1 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x040C			Register Name: CSIC_DMA_CH1_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.48 0x0410 CSIC DMA Channel1 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0410			Register Name: CSIC_DMA_CH1_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.49 0x0414 CSIC DMA Channel1 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0414			Register Name: CSIC_DMA_CH1_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

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7.1.12.50 0x0418 CSIC DMA Channel1 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0418			Register Name: CSIC_DMA_CH1_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.51 0x0420 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0420			Register Name: CSIC_DMA_CH1_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.52 0x0424 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0424			Register Name: CSIC_DMA_CH1_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

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7.1.12.53 0x0428 CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0428			Register Name: CSIC_DMA_CH1_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

7.1.12.54 0x042C CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x042C			Register Name: CSIC_DMA_CH1_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.55 0x0430 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0430			Register Name: CSIC_DMA_CH1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.56 0x0434 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0434			Register Name: CSIC_DMA_CH1_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

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7.1.12.57 0x0438 CSIC DMA Channel1 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0438			Register Name: CSIC_DMA_CH1_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.58 0x043C CSIC DMA Channel1 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x043C			Register Name: CSIC_DMA_CH1_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.59 0x044C CSIC DMA Channel1 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/

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Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.60 0x0450 CSIC DMA Channel1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)

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Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

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Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.61 0x0454 CSIC DMA Channel1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready

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Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

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7.1.12.62 0x0458 CSIC DMA Channel1 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0458			Register Name: CSIC_DMA_CH1_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

7.1.12.63 0x045C CSIC DMA Channel1 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.64 0x0468 CSIC DMA Channel1 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0468			Register Name: CSIC_DMA_CH1_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

7.1.12.65 0x0470 CSIC DMA Channel1 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0470			Register Name: CSIC_DMA_CH1_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.

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Offset: 0x0470			Register Name: CSIC_DMA_CH1_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.66 0x0498 CSIC DMA Channel1 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0498			Register Name: CSIC_DMA_CH1_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

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Offset: 0x0498			Register Name: CSIC_DMA_CH1_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.67 0x049C CSIC DMA Channel1 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x049C			Register Name: CSIC_DMA_CH1_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x049C			Register Name: CSIC_DMA_CH1_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.68 0x04A0 CSIC DMA Channel1 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x04A0			Register Name: CSIC_DMA_CH1_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

7.1.12.69 0x0600 CSIC DMA Channel2 Enable Register (Default Value:0x0000_0000)

Offset: 0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:1	/	/	/
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

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7.1.12.70 0x0604 CSIC DMA Channel2 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

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19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output

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Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved

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Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames ..... 15: 16 frames Note: CH2 FPS_DS_PRD should be used together with CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH2 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.71 0x0608 CSIC DMA Channel2 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

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7.1.12.72 0x060C CSIC DMA Channel2 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x060C			Register Name: CSIC_DMA_CH2_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.73 0x0610 CSIC DMA Channel2 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0610			Register Name: CSIC_DMA_CH2_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.74 0x0614 CSIC DMA Channel2 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

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7.1.12.75 0x0618 CSIC DMA Channel2 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0618			Register Name: CSIC_DMA_CH2_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.76 0x0620 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0620			Register Name: CSIC_DMA_CH2_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.77 0x0624 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0624			Register Name: CSIC_DMA_CH2_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

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7.1.12.78 0x0628 CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0628			Register Name: CSIC_DMA_CH2_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

7.1.12.79 0x062C CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x062C			Register Name: CSIC_DMA_CH2_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.80 0x0630 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0630			Register Name: CSIC_DMA_CH2_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.81 0x0634 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0634			Register Name: CSIC_DMA_CH2_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

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7.1.12.82 0x0638 CSIC DMA Channel2 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0638			Register Name: CSIC_DMA_CH2_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.83 0x063C CSIC DMA Channel2 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x063C			Register Name: CSIC_DMA_CH2_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.84 0x064C CSIC DMA Channel2 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x064C			Register Name: CSIC_DMA_CH2_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/

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Offset: 0x064C			Register Name: CSIC_DMA_CH2_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.85 0x0650 CSIC DMA Channel2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)

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Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

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Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.86 0x0654 CSIC DMA Channel2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready

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Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

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7.1.12.87 0x0658 CSIC DMA Channel2 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0658			Register Name: CSIC_DMA_CH2_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

7.1.12.88 0x065C CSIC DMA Channel2 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.89 0x0668 CSIC DMA Channel2 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0668			Register Name: CSIC_DMA_CH2_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

7.1.12.90 0x0670 CSIC DMA Channel2 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0670			Register Name: CSIC_DMA_CH2_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.

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Offset: 0x0670			Register Name: CSIC_DMA_CH2_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.91 0x0698 CSIC DMA Channel2 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

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Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.92 0x069C CSIC DMA Channel2 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x069C			Register Name: CSIC_DMA_CH2_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x069C			Register Name: CSIC_DMA_CH2_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.93 0x06A0 CSIC DMA Channel2 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x06A0			Register Name: CSIC_DMA_CH2_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

7.1.12.94 0x0800 CSIC DMA Channel3 Enable Register (Default Value:0x0000_0000)

Offset: 0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

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7.1.12.95 0x0804 CSIC DMA Channel3 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

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19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output

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Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved

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Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames ..... 15: 16 frames Note: CH3 FPS_DS_PRD should be used together with CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH3 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.96 0x0808 CSIC DMA Channel3 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

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7.1.12.97 0x080C CSIC DMA Channel3 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x080C			Register Name: CSIC_DMA_CH3_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.98 0x0810 CSIC DMA Channel3 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0810			Register Name: CSIC_DMA_CH3_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.99 0x0814 CSIC DMA Channel3 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0814			Register Name: CSIC_DMA_CH3_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

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7.1.12.1000x0818 CSIC DMA Channel3 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0818			Register Name: CSIC_DMA_CH3_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.1010x0820 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0820			Register Name: CSIC_DMA_CH3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.1020x0824 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0824			Register Name: CSIC_DMA_CH3_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

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7.1.12.1030x0828 CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0828			Register Name: CSIC_DMA_CH3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address in DMA mode.

7.1.12.1040x082C CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x082C			Register Name: CSIC_DMA_CH3_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.1050x0830 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0830			Register Name: CSIC_DMA_CH3_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.1060x0834 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0834			Register Name: CSIC_DMA_CH3_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

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7.1.12.107 0x0838 CSIC DMA Channel3 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0838			Register Name: CSIC_DMA_CH3_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.108 0x083C CSIC DMA Channel3 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x083C			Register Name: CSIC_DMA_CH3_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.109 0x084C CSIC DMA Channel3 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/

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Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.1100x0850 CSIC DMA Channel3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)

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Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

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Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.1110x0854 CSIC DMA Channel3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready

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Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

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7.1.12.1120x0858 CSIC DMA Channel3 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0858			Register Name: CSIC_DMA_CH3_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

7.1.12.1130x085C CSIC DMA Channel3 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

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Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.1140x0868 CSIC DMA Channel3 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0868			Register Name: CSIC_DMA_CH3_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

7.1.12.1150x0870 CSIC DMA Channel3 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0870			Register Name: CSIC_DMA_CH3_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.

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Offset: 0x0870			Register Name: CSIC_DMA_CH3_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.1160x0898 CSIC DMA Channel3 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0898			Register Name: CSIC_DMA_CH3_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

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Offset: 0x0898			Register Name: CSIC_DMA_CH3_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.1170x089C CSIC DMA Channel3 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x089C			Register Name: CSIC_DMA_CH3_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x089C			Register Name: CSIC_DMA_CH3_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.1180x08A0 CSIC DMA Channel3 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x08A0			Register Name: CSIC_DMA_CH3_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

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8 Interfaces

8.1 CIR Receiver (CIR_RX)

8.1.1 Overview

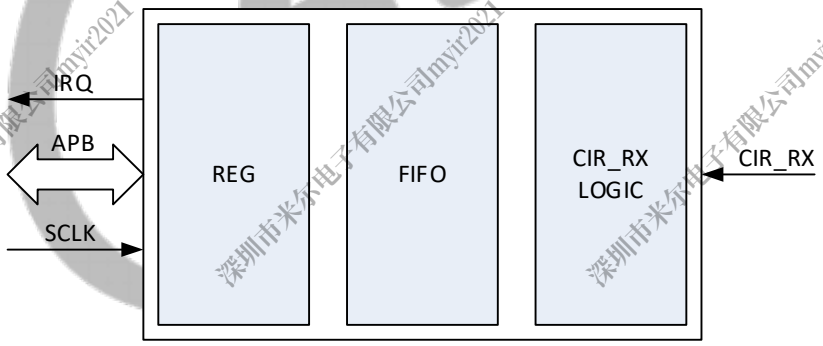
The Consumer Infrared (CIR) receiver captures pulse from the IR Receiver module and uses the Run-Length Code (RLC) to encode the pulse.

The CIR receiver has the following features:

- One CIR_RX interface in CPUX domain and one CIR_RX interface in CPUS domain
- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz
- Supports interrupt and DMA mode

8.1.2 Block Diagram

Figure 8-1 CIR Receiver Block Diagram



The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal, the rest 7 bits are used for the length of RLC. The maximum length of the RLC is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

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8.1.3 Functional Description

8.1.3.1 External Signals

The following table describes the external signals of CIR Receiver.

Table 8-1 CIR Receiver External Signals

Signal Name	Description	Type
IR-RX	Consumer Infrared Receiver	I
S-IR-RX	Consumer infrared receiver	I

8.1.3.2 Clock Sources

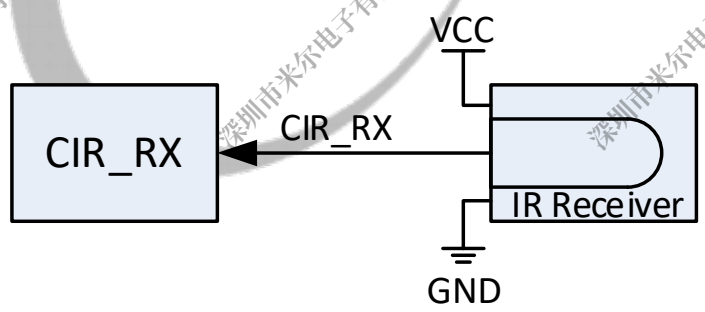
The following table describes the clock sources of CIR Receiver.

Table 8-2 CIR Receiver Clock Sources

Clock Sources	Description	Module
CIR_RX		
CLK32K	By default, CLK32K is 32.768 kHz.	CCU
HOSC	By default, HOSC is 24 MHz.	CCU
S_CIRRX		
CLK32K	By default, CLK32K is 32.768 kHz.	PRCM
CLK24M	By default, CLK24M is 24 MHz.	PRCM

8.1.3.3 Typical Application

Figure 8-2 CIR Receiver Application Diagram



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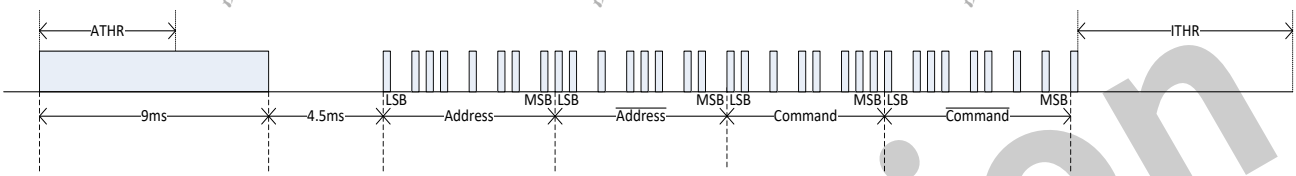
8.1.3.4 NEC Protocol Format

Figure 8-3 NEC Protocol



The CIR receiver module is a timer with a capture function.

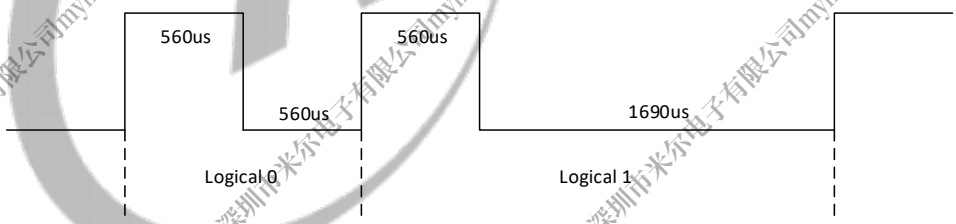
When CIR_RX signals satisfy the Active Threshold (ATHR), the CIR receiver can start to capture. In the process, the signal is ignored if the pulse width of the signal is less than NTHR. When CIR_RX signals satisfy ITHR (Idle Threshold), the capture process is stopped and the Receiver Packet End interrupt is generated, then the Receiver Packet End Flag is asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of the Run-Length Code. The MSB bit of a byte is the polarity of pulse, and the rest 7 bits is pulse width by taking Sample Clock as a basic unit. This is the code form of the RLC-Byte. When the level changes or the pulse width counter overflows, the RLC-Byte is buffered to FIFO. The CIR_RX module receives the infrared signals transmitted by the infrared remote control, the software decodes the signals.

8.1.3.5 Operating Mode

Sample Clock

Figure 8-4 Logical '0' and Logical '1' of NEC Protocol



For NEC protocol, a logical "1" takes 2.25 ms (560 us+1680 us) to transmit, while a logical "0" is only half of that, being 1.12 ms (560 us+560 us).

For example, if the sample clock is 31.25 kHz, a sample cycle is 32 us, then 18 sample cycles are 560 us. So the RLC of 560 us low level is 0x12 (b'00010010), the RLC of 560 us high level is 0x92 (b'10010010). Then a logical "1" takes code 0x12 (b'00010010) and code 0xb5 (b'10110101) to transmit, a logical "0" takes code 0x12 and code 0x92 to transmit.

Active Threshold (ATHR)

When the CIR receiver is in Idle state, if the electrical level of the IR-RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then the CIR receiver takes the

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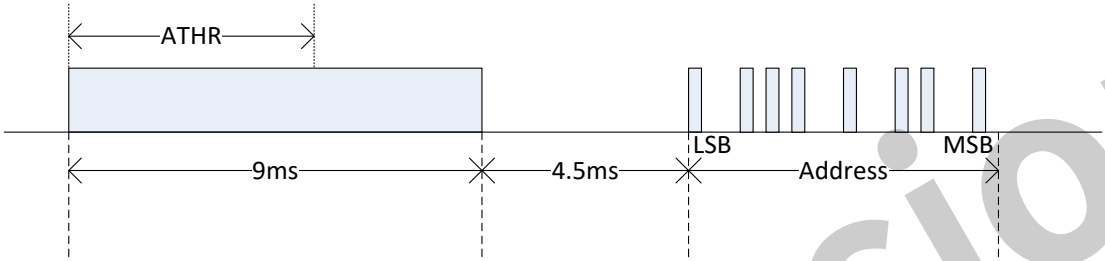
starting of the signal as a lead code, and the CIR receiver turns into an active state and starts to capture IR-RX signals.

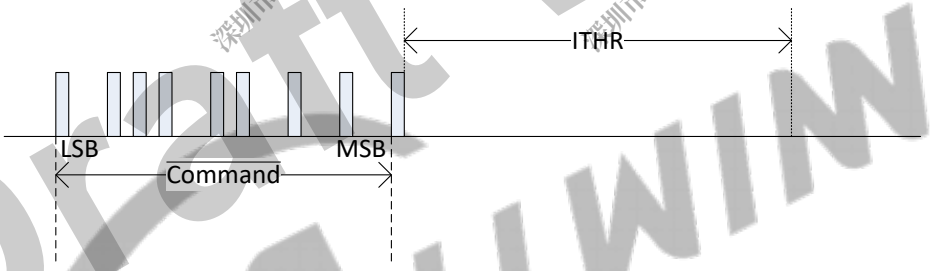
Figure 8-5 ATHR Definition



Idle Threshold (ITHR)

If the electrical level of IR-RX signals has no change, and the duration reaches this threshold, then the CIR receiver enters into Idle state and ends this capture.

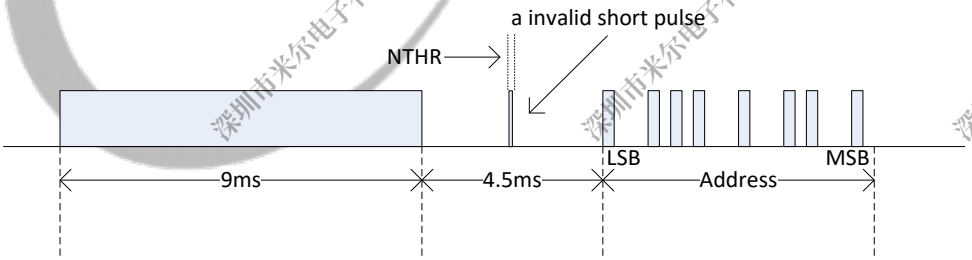
Figure 8-6 ITHR Definition



Noise Threshold (NTHR)

In the capture process, the pulse is ignored if the pulse width is less than the Noise Threshold.

Figure 8-7 NTHR Definition



Active Pulse Accept Mode (APAM)

The APAM is used to fit the type of lead code. If a pulse does not fit the type of lead code, it is not regarded as a lead code even if the pulse width reaches ATHR.

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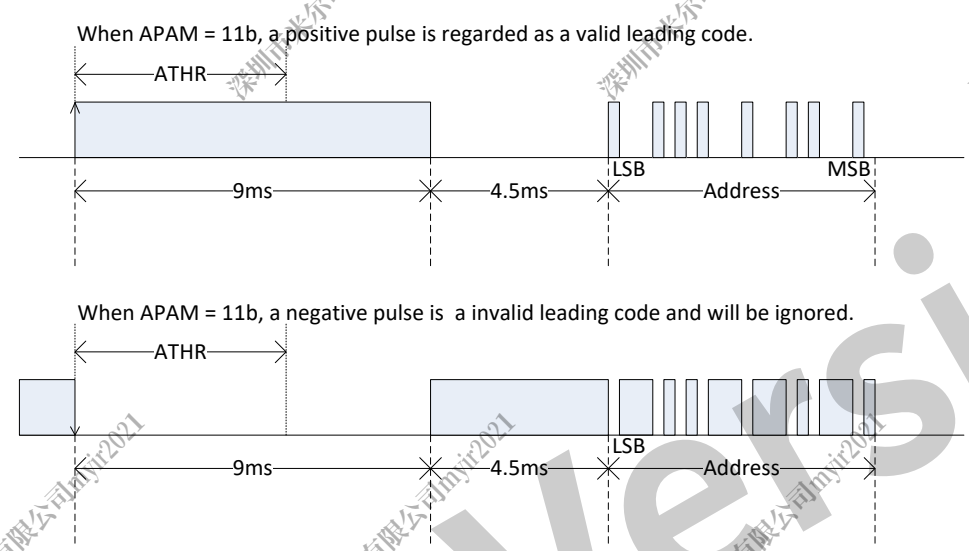
Figure 8-8 APAM Definition



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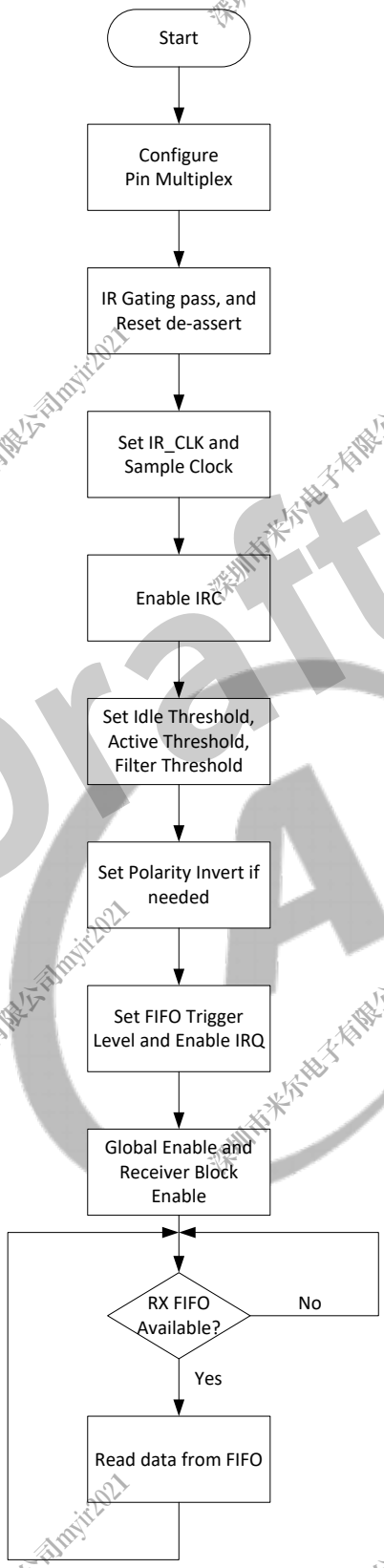
8.1.4 Programming Guidelines

Figure 8-9 CIR Receiver Process



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8.1.5 Register List

Module Name	Base Address
S_CIRRX	0x0704 0000
CIR_RX	0x0200 5000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Receiver Control Register
CIR_RXCTL	0x0010	CIR Receiver Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_CONFIG	0x0034	CIR Receiver Configure Register
CIR_STORE0	0x0080	CIR Receiver Store Register0
CIR_STORE1	0x0084	CIR Receiver Store Register1
CIR_STORE2	0x0088	CIR Receiver Store Register2
CIR_STORE3	0x008C	CIR Receiver Store Register3

8.1.6 Register Description

8.1.6.1 0x0000 CIR Receiver Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	Read/Write	Default/HEX	Description
31:8	/	/	/
7:6	R/W	0x0	APAM Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code. 10: Only negative pulse is valid as a leading code. 11: Only positive pulse is valid as a leading code.
5:4	R/W	0x0	CEN CIR ENABLE 00-10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable

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Offset: 0x0000			Register Name: CIR_CTL
Bit	Read/Write	Default/HEX	Description
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

8.1.6.2 0x0010 CIR Receiver Configure Register (Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXCTL
Bit	Read/Write	Default/HEX	Description
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert. 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

8.1.6.3 0x0020 CIR Receiver FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	Read/Write	Default/HEX	Description
31:8	/	/	/
7:0	R	0x0	RBF Receiver Byte FIFO

8.1.6.4 0x002C CIR Receiver Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	Read/Write	Default/HEX	Description
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1

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Offset: 0x002C			Register Name: CIR_RXINT
Bit	Read/Write	Default/HEX	Description
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

8.1.6.5 0x0030 CIR Receiver Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	Read/Write	Default/HEX	Description
31:15	/	/	/
14:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1-byte available data in RX FIFO 2: 2-byte available data in RX FIFO ... 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0x0: Idle 0x1: busy

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Offset: 0x0030			Register Name: CIR_RXSTA
Bit	Read/Write	Default/HEX	Description
6:5	/	/	/
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a '1'.
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7'b0000,000 and 8'b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a '1'.
0	R/W1C	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a '1'.

8.1.6.6 0x0034 CIR Receiver Configure Register (Default Value: 0x0000_1828)

Offset: 0x0034			Register Name: CIR_CONFIG
Bit	Read/Write	Default/HEX	Description
31	/	/	/
30:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0x0:ATHR in Unit of (Sample Clock) 0x1:ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1) *(ATHC? Sample Clock: 128*Sample Clock)).

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Offset: 0x0034			Register Name: CIR_CONFIG
Bit	Read/Write	Default/HEX	Description
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU. When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.
7:2	R/W	0xa	NTHR Noise Threshold for CIR When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware. 0: all samples are recorded into RX FIFO 1: If the signal is only one sample duration, it is taken as noise and discarded. 2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded. … 61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.
1:0	R/W	0x0	SCS Sample Clock Select for CIR

SCS2	SCS[1]	SCS[0]	Sample Clock
0	0	0	IR_CLK/64
0	0	1	IR_CLK /128
0	1	0	IR_CLK /256
0	1	1	IR_CLK /512
1	0	0	IR_CLK
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

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8.1.6.7 0x0080 CIR Receiver Store Register0 (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_STORE0
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV0 Receiver Store Value 0

8.1.6.8 0x0084 CIR Receiver Store Register1 (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CIR_STORE1
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV1 Receiver Store Value 1

8.1.6.9 0x0088 CIR Receiver Store Register2 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: CIR_STORE2
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV2 Receiver Store Value 2

8.1.6.10 0x008C CIR Receiver Store Register3 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: CIR_STORE3
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV3 Receiver Store Value 3

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8.2 CIR Transmitter (CIR_TX)

8.2.1 Overview

The CIR transmitter (CIR_TX) can transfer arbitrary waves which can be modulated with configurable carrier waves such as 38 kHz. CIR_TX only uses lower 8 bits of the 32-bit registers. CIR_TX stores a 16-bit number in 2 registers, where one register contains the higher 8 bits while the other contains the lower 8 bits.

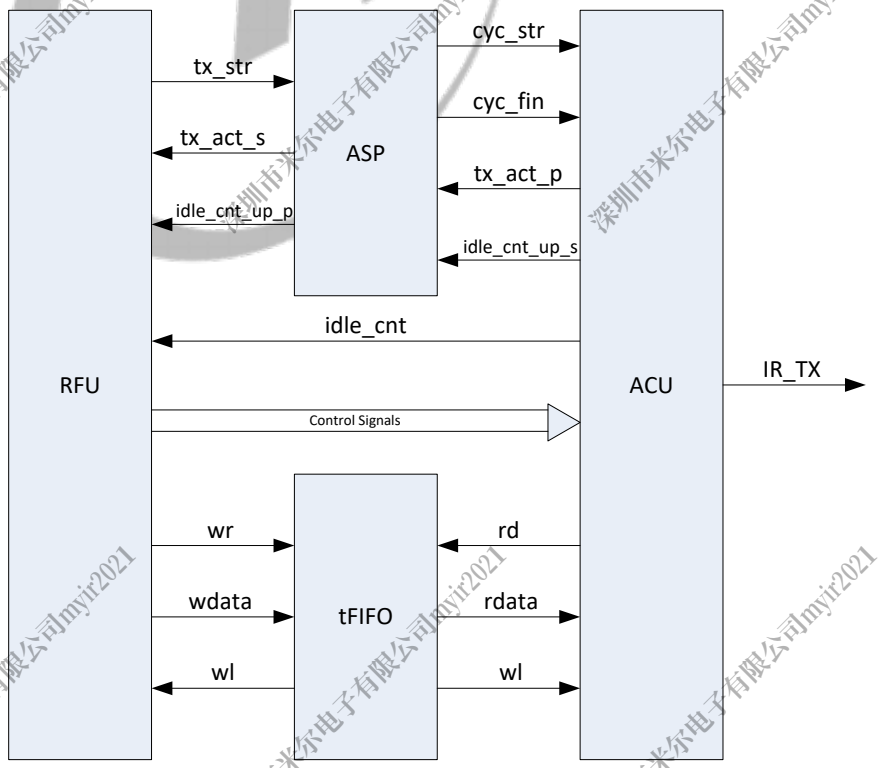
The CIR_TX has the following features:

- One CIR_TX interface in CPUX domain
- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Full physical layer implementation
- Arbitrary wave generator
- Configurable carrier frequency
- Handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer
- Supports Interrupts and DMA

8.2.2 Block Diagram

The following figure shows a block diagram of the CIR_TX.

Figure 8-10 CIR_TX Block Diagram



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8.2.3 Functional Description

8.2.3.1 External Signals

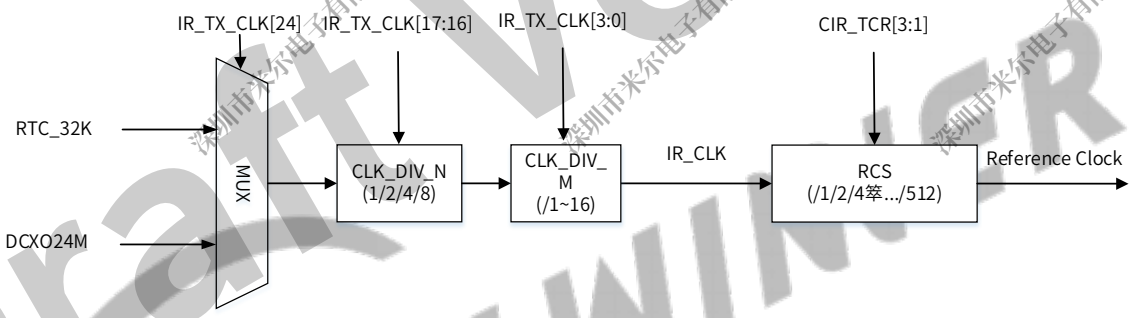
The following table describes the external signals of CIR_TX.

Table 8-3 CIR_TX External Signals

Signal Name	Description	Type
IR-TX	Consumer Infrared Receiver	I

8.2.3.2 Clock Sources

Figure 8-11 CIR_TX Clock Description



8.2.3.3 Function Implementation

The CIR_TX is used to generate a waveform of arbitrary length, arbitrary shape, and no high-speed requirement, and it can change the data into the high-/low-level sequence of a certain length. Every transmitting data is in bytes, the Bit[7] of a byte means whether the level of a transmitting wave is high or low, the Bit[6:0] is the length of this wave. If the current transmitting frequency-division is 1, 0x88 is a high level of 8 cycles, 0x08 is a low level of 8 cycles. If the current transmitting frequency-division is 4, 0x88 is a high level of 32 cycles, 0x08 is a low level of 32 cycles.

The CIR_TX has two transmission modes: non-cycle transmission, and cycle transmission.

The non-cycle transmission is to transmit all the data in TX_FIFO until the FIFO is empty.

The cycle transmission is to transmit all the data in TX_FIFO, after the transmission completion, wait for a certain time to recover the data in TX_FIFO and then send it until a stop signal is detected. The data recovery in FIFO is implemented by clearing the read pointer.

8.2.3.4 Timing Diagram

The IR remote control contains many protocols designed by different manufacturers. Here to NEC protocol as an example, the CIR_TX module uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote-control applications. A message

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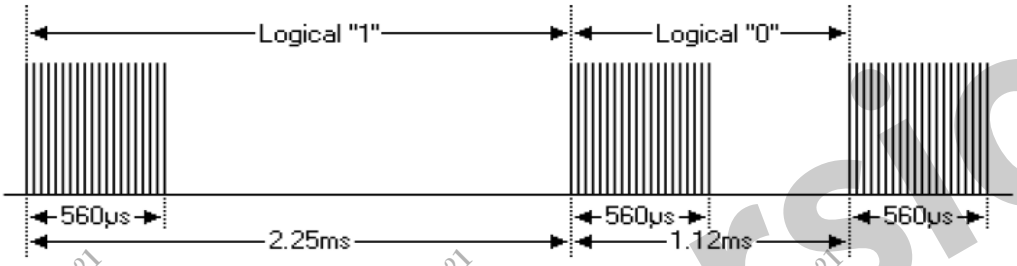
is started by a 9 ms AGC burst, which is used to set the gain of the earlier CIR receivers. This AGC burst is then followed by a 4.5 ms space, which is then followed by the address and command.

Bit definition: the logical “1” takes 2.25 ms to transmit, while a logical “0” is only 1.12 ms.

Figure 8-12 Definitions of Logical “1” and Logical “0”



Timing for a message:

Figure 8-13 CIR Message Timing Diagram

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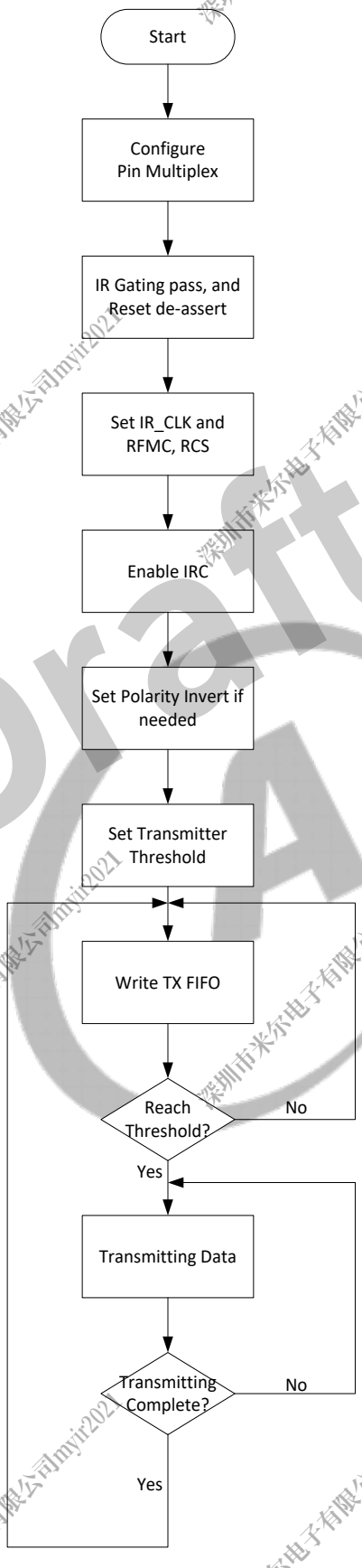
8.2.4 Programming Guidelines

Figure 8-14 CIR Transmitter Process



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8.2.5 Register List

Module Name	Base Address
CIR_TX	0x0200 3000

Register Name	Offset	Description
CIR_TGLR	0x0000	CIR Transmit Global Register
CIR_TMCR	0x0004	CIR Transmit Modulation Control Register
CIR_TCR	0x0008	CIR Transmit Control Register
CIR_IDC_H	0x000C	CIR Transmit Idle Duration Threshold Register
CIR_IDC_L	0x0010	CIR Transmit Idle Duration Threshold Register
CIR_TICR_H	0x0014	CIR Transmit Idle Counter Register
CIR_TICR_L	0x0018	CIR Transmit Idle Counter Register
CIR_TEL	0x0020	CIR TX FIFO empty Level Register
CIR_TXINT	0x0024	CIR Transmit Interrupt Control Register
CIR_TAC	0x0028	CIR Transmit FIFO Available Counter Register
CIR_TXSTA	0x002C	CIR Transmit Status Register
CIR_TXT	0x0030	CIR Transmit Threshold Register
CIR_DMA	0x0034	CIR DMA Control Register
CIR_TXFIFO	0x0080	CIR Transmit FIFO Data Register

8.2.6 Register Description

8.2.6.1 0x0000 CIR Transmitter Global Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_TGLR
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0x0	IMS Internal Modulation Select 0: the transmitting signal is not modulated 1: the transmitting signal is modulated internally
6:5	R/W	0x0	DRMC Duty ratio of modulated carrier is high level /low level. 0: low level is the one time of high level 1: low level is the two times of high level 2: low level is the three times of high level 3: reserved
4:3	/	/	/

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Offset: 0x0000			Register Name: CIR_TGLR
Bit	Read/Write	Default	Description
2	R/W	0x0	TPPI Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
1	R/W	0x0	TR Transmit Reset When this bit is set, the transmitting is reset. The FIFO will be flush, the TIC filed and CSS field will be clean during Transmit Reset. This field will automatically clean when the Transmit Reset is finished, and the CIR transmitter will state Idle.
0	R/W	0x0	TXEN Transmit Block Enable 0: Disable the CIR Transmitter 1: Enable the CIR Transmitter

8.2.6.2 0x0004 CIR Transmitter Modulation Control Register (Default Value:0x0000_009E)

Offset: 0x0004			Register Name: CIR_TMCR
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x9E	RFMC Reference Frequency of modulated carrier. Reference Frequency of modulated carrier based on a division of a fixed functional clock(FCLK). The range of the modulated carrier is usually 30KHZ to 60KHz.The most consumer electronics is 38KHz. The default modulated carrier is 38KHz when FCLK is 12MHz. RFMC= FCLK/((N+1)*(DRMC+2)).

8.2.6.3 0x0008 CIR Transmitter Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CIR_TCR
Bit	Read/Write	Default	Description
31:8	/	/	/

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Offset: 0x0008			Register Name: CIR_TCR
Bit	Read/Write	Default	Description
7	R/W	0x0	CSS Cyclical Pulse Start/Stop Control Start to transmit when set to '1', 0: Stop when cleared to '0'. From start to stop, all data in FIFO must be transmitted. 1: Start.
6:4	/	/	/
3:1	R/W	0x0	RCS Reference Clock Select for CIR Transmit 000: CIR Transmit reference clock is ir_clk 001: CIR Transmit reference clock is ir_clk/2 010: CIR Transmit reference clock is ir_clk/4 011: CIR Transmit reference clock is ir_clk/8 100: CIR Transmit reference clock is ir_clk/64 101: CIR Transmit reference clock is ir_clk/128 110: CIR Transmit reference clock is ir_clk/256 111: CIR Transmit reference clock is ir_clk/512
0	R/W	0x0	TTS Type of the transmission signal 0: The transmitting wave is single non-cyclical pulse. 1: The transmitting wave is cyclical short-pulse.

8.2.6.4 0x000C CIR Transmitter Idle Duration Counter Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CIR_IDC_H
Bit	Read/Write	Default	Description
31:8	/	/	/
3:0	R/W	0x0	IDC_H Idle Duration Counter threshold (High 4 bit) Idle Duration = 128*IDC*Ts (IDC = 0-4095)

8.2.6.5 0x0010 CIR Transmitter Idle Duration Counter Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CIR_IDC_L
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	IDC_L Idle Duration Counter threshold (Low 8 bit) Idle Duration = 128*IDC*Ts (IDC = 0-4095)

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8.2.6.6 0x0014 CIR Transmitter Idle Counter Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CIR_TICR_H
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x0	TIC_H Transmit Idle Counter_H (High 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

8.2.6.7 0x0018 CIR Transmitter Idle Counter Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CIR_TICR_L
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x0	TIC_L Transmit Idle Counter_L (Low 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

8.2.6.8 0x0020 CIR Transmitter FIFO Empty Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_TEL
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	TEL TX FIFO empty Level for DRQ and IRQ. TRIGGER_LEVEL = TEL + 1

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8.2.6.9 0x0024 CIR Transmitter Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CIR_TXINT
Bit	Read/Write	Default	Description
31:3	/	/	/
2	R/W	0x0	DRQ_EN TX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails.
1	R/W	0x0	TAI_EN TX FIFO Available Interrupt Enable 0: Disable 1:Enable
0	R/W	0x0	TPEI_EN Transmit Packet End Interrupt Enable for Cyclical Pulse 0: Disable 1: Enable TUI_EN Transmitter FIFO under run Interrupt Enable for Non-cyclical Pulse 0: Disable 1: Enable

8.2.6.10 0x0028 CIR Transmitter FIFO Available Counter Register (Default Value: 0x0000_0080)

Offset: 0x0028			Register Name: CIR_TAC
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x80	TAC TX FIFO Available Space Counter 0x00: No available space in TX FIFO 0x01: 1-byte available space in TX FIFO 0x02: 2-byte available space in TX FIFO ... 0x80: 128 byte available space in TX FIFO

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8.2.6.11 0x002C CIR Transmitter Status Register (Default Value: 0x0000_0002)

Offset: 0x002C			Register Name: CIR_TXSTA
Bit	Read/Write	Default	Description
31:4	/	/	/
3	R	0x0	STCT Status of CIR Transmitter 0x0: Idle 0x1: Active This bit will automatically set when the controller begins transmit the data in the FIFO. The "1" will last when the data in the FIFO. It will automatically be cleaned to "0" when all data in the FIFO is transmitted. The bit is for debug. Output Level of Idle state determined by level of the last data output.
2	R	0x0	DRQ DMA Request Flag When set to '1', the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails. This bit is for debug.
1	R/W	0x1	TAI TX FIFO Available Interrupt Flag 0: TX FIFO not available by its level 1: TX FIFO available by its level This bit can be cleared by software writing '1'.
0	R/W	0x0	TPE Transmitter Packet End Flag for Cyclical Pulse 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed TUR Transmitter FIFO Under Run Flag for Non-cyclical Pulse 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a '1'.

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8.2.6.12 0x0030 CIR Transmitter Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_TXT
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	NCTT Non-cyclical Pulse Transmit Threshold The controller will trigger transmitting the data in the FIFO when the data byte number has reaches the Transmit Threshold set in this field.

8.2.6.13 0x0034 CIR Transmitter DMA Control Register (Default Value: 0x0000_00A5)

Offset: 0x0034			Register Name: CIR_DMA_CTL
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0xA5	DMA Handshake configuration 0xA5: DMA wait cycle mode 0xEA: DMA handshake mode

8.2.6.14 0x0080 CIR Transmitter FIFO Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_TXFIFO
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	W	0x0	Transmit Byte FIFO When the transmitting is trigger, the data in the FIFO will be transmitted until the data number has been transmitted finished.

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8.3 GAMC0

8.3.1 Overview

The Gigabit Medium Access Controller (GMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000 Mbit/s external PHY with RMII/RGMII interface in full-duplex and half-duplex modes. The internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors.

The GMAC has the following features:

- One GMAC interface (GMAC) for connecting external Ethernet PHY
- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operations
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
  - Supports linked-list descriptor list structure
  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
  - Comprehensive status reporting for normal operation and transfers with errors
- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies

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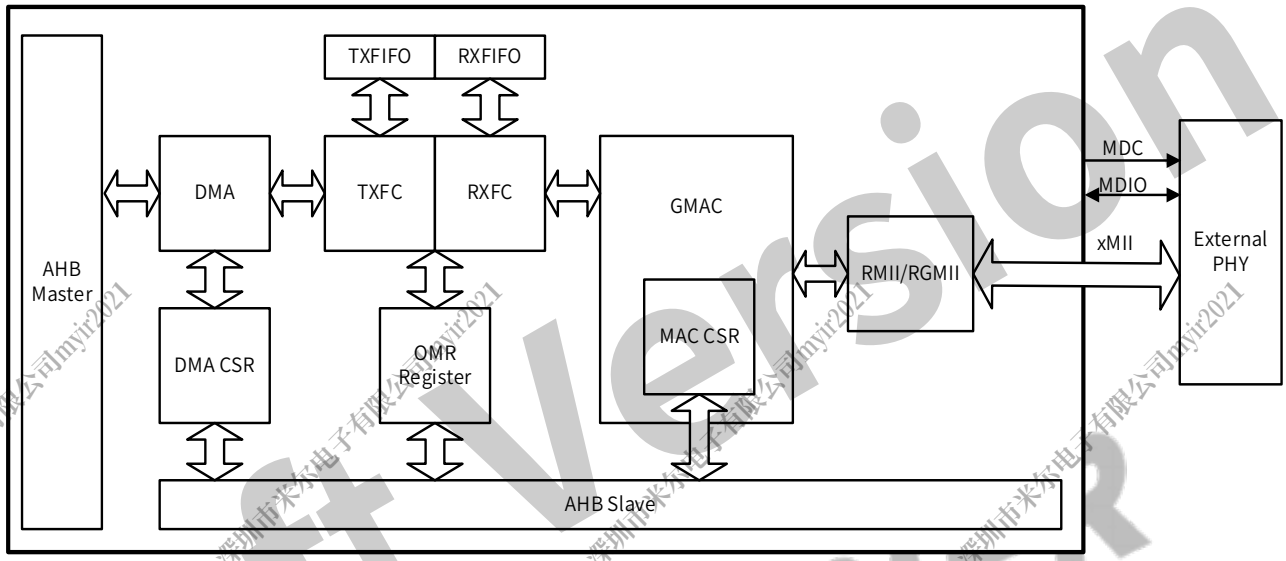
8.3.2 Block Diagram

The following figure shows the block diagram of GMAC.

Figure 8-158-16 GMAC Block Diagram



8.3.3 Functional Description

8.3.3.1 External Signals

The following table describes the pin list of GMAC.

Table 8-4 GMAC External Siganls

Signal Name	Description	Type
RGMII0-RXD0/RMII0-RXD0	RGMII/RMII Receive Data0	I
RGMII0-RXD1/RMII0-RXD1	RGMII/RMII Receive Data1	I
RGMII0-RXD2/RMII0-NULL	RGMII Receive Data2	I
RGMII0-RXD3/RMII0-NULL	RGMII Receive Data3	I
RGMII0-RXCK/ RMII0-NULL	RGMII Receive Clock	I
RGMII0-RXCTRL/RMII0-CRS-DV	RGMII Receive Control/RMII Carrier Sense Receive Data Valid	I
RGMII0-CLKIN/RMII0-RXER	RGMII Transmit Clock from External/RMII Receive Error	I
RGMII0-TXD0/RMII0-TXD0	RGMII/RMII Transmit Data0	O
RGMII0-TXD1/RMII0-TXD1	RGMII/RMII Transmit Data1	O
RGMII0-TXD2/RMII0-NULL	RGMII Transmit Data2	O
RGMII0-TXD3/RMII0-NULL	RGMII Transmit Data3	O
RGMII0-TXCK/RMII0-TXCK	RGMII/RMII Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII0-TXCTRL/RMII0-TXEN	RGMII Transmit Control/RMII Transmit Enable	O

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Signal Name	Description	Type
RGMII0-MDC	RGMII Management Data Clock	O
RGMII0-MDIO	RGMII Management Data Input/ Output	I/O
RGMII0-EPHY-25M	25 MHz Output for GMAC PHY	O

8.3.3.2 Clock Sources

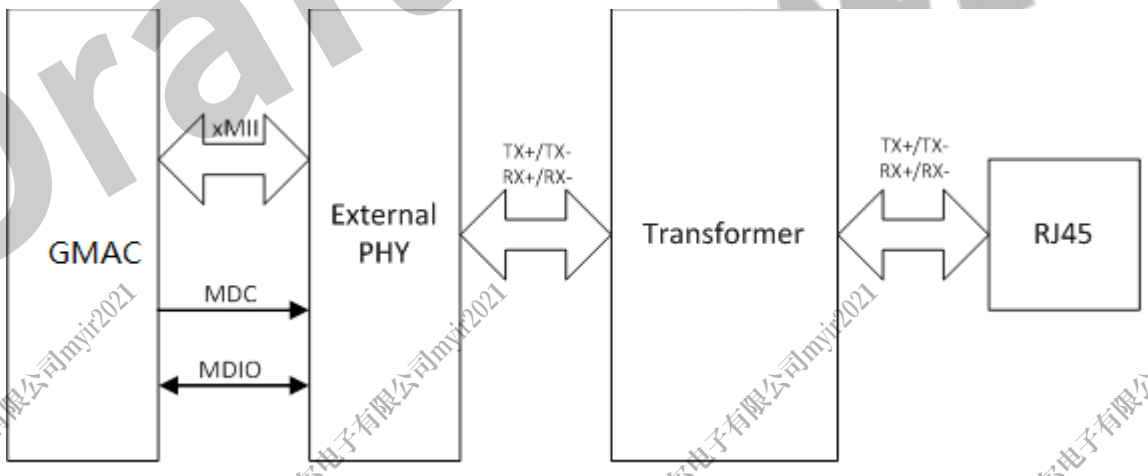
GMAC has two clock sources. The following table describes the clock sources of the GMAC.

Table 8-5 GMAC Clock Sources

Clock Sources	Description	Module
AHB	Bus clock. The bus frequency is 200 MHz.	CCU
GMAC_25M	GMAC 25M clock. The default value is 25 MHz.	

8.3.3.3 Typical Application

Figure 8-178-18 GMAC Typical Application



8.3.3.4 GMAC RX/TX Descriptor

The internal DMA of GMAC transfers data between host memory and internal RX/TX FIFO by a linked list of descriptors. Each descriptor consists of four words and contains some necessary information to transfer TX and RX frames. The following figure shows the descriptor list structure. The address of each descriptor must be 32-bit aligned.

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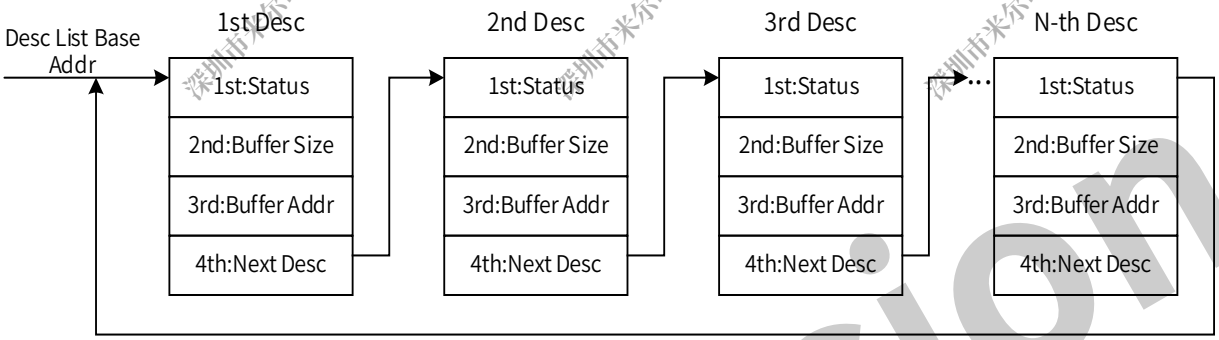
Figure 8-198-20 GMAC RX/TX Descriptor List



8.3.3.5 TX Descriptor

1st Word of TX Descriptor

Bits	Description
31	TX_DESC_CTL When set, the current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in the buffer of the current descriptor are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of the header for the transmitted frame is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of the transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of the payload for the transmitted frame is wrong.
11	Reserved
10	TX_CRS_ERR When set, the carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of a collision after the contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of the TX FIFO underflow error.

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Bits	Description
0	TX_DEFER When set in Half-Duplex mode, the GMAC defers the frame transmission.

2nd Word of TX Descriptor

Bits	Description
31	TX_INT_CTL When it is set and the current frame has been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When it is set, the current descriptor is the last one of the current frame.
29	FIR_DESC When it is set, the current descriptor is the first one of the current frame.
28:27	CHECKSUM_CTL These bits control to insert checksum in the transmit frame.
26	CRC_CTL When it is set, the CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of the buffer specified by the current descriptor.

3rd Word of TX Descriptor

Bits	Description
31:0	BUF_ADDR The address of the buffer specified by the current descriptor.

4th Word of TX Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of the next descriptor. It must be 32-bit aligned.

8.3.3.6 RX Descriptor

1st Word of RX Descriptor

Bits	Description
31	RX_DESC_CTL When it is set, the current descriptor can be used by DMA. This bit is cleared by DMA when the complete frame is received or the buffer of the current descriptor is full.
30	RX_DAF_FAIL When it is set, the current frame does not pass the DA filter.

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Bits	Description
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for the current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of the received frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When it is set, the current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When it is set, the current fame does not pass the SA filter.
12	Reserved
11	RX_OVERFLOW_ERR When it is set, a buffer overflow error occurred and the current frame is wrong.
10	Reserved
9	FIR_DESC When it is set, the current descriptor is the first descriptor of the current frame.
8	LAST_DESC When it is set, the current descriptor is the last descriptor of the current frame.
7	RX_HEADER_ERR When it is set, the checksum of the frame header is wrong.
6	RX_COL_ERR When it is set, there is a late collision during the reception in half-duplex mode.
5	Reserved
4	RX_LENGTH_ERR When it is set, the length of the current frame is wrong.
3	RX_PHY_ERR When it is set, the receive error signal from PHY is asserted during the reception.
2	Reserved
1	RX_CRC_ERR When it is set, the CRC field of the received frame is wrong.
0	RX_PAYLOAD_ERR When it is set, the checksum or length of the payload for the received frame is wrong.

2nd Word of RX Descriptor

Bits	Description
31	RX_INT_CTL When it is set and a frame has been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of the buffer is specified by the current descriptor.

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3rd Word of RX Descriptor

Bits	Description
31:0	BUF_ADDR The address of the buffer specified by the current descriptor.

4th Word of RX Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of the next descriptor. This field must be 32-bit aligned.

8.3.4 Programming Guidelines

8.3.4.1 GMAC System Configuration

Perform the following steps:

Step 1 Write 0 to GMAC_BGR_REG[bit16] to assert the module reset.

Step 2 Write 1 to GMAC_BGR_REG[bit16] to deassert the module reset.

Step 3 Write 1 to GMAC_BGR_REG[bit0] to enable the bus clock of the module.

Step 4 Configure the pin interfaces of GMAC by setting GPIO module.

Step 5 Configure to set the transmission clock source of RGMII/RMII.

- For RGMII RXCLK/CLK125M:

In RGMII mode, in addition to the configuration of the transmission clock source, it is generally necessary to adjust the timing by configuring the transmission clock delay, reception clock delay, transmission clock reverse, reception clock reverse.

- Write 0 to the bit [13] and write 1 to the bit [2] to select the RGMII interface.
- If selecting RXCLK as the clock source of RGMII, write 2 to the bit [1:0]; if selecting CLK125M as the clock source of RGMII, write 1 to the bit [1:0].
- Write 0 to the bit [3], write 0 to the bit [4], write 31 to the bit [9:5], and write 7 to the bit [12:10] to transmit the reception sequence adjustment.

- For RMII TXCLK:

- Write 1 to the bit [13] and write 0 to the bit [2] to select the RMII interface.
- Write 0 to the bit [0] to select TXCLK as the clock source of RMII.

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The configuration value of GMAC_EPHY_CLK_REG0 can refer to the following table.

Table 8-6 GMAC_EPHY_CLK_REG0 Configuration Value

GMAC_EPHY _CLK_REG0	PHY_SEL	RMII_EN	ETXDC	ERXDC	ERXIE	ETXIE	RMII/RGMII	ETCS
	Bit15	Bit13	Bit[12:10]	Bit[9:5]	Bit4	Bit3	Bit2	Bit[1:0]
RGMII	0	0	7	31	0	0	1	1/2
RMII	0	1	0	0	0	0	0	0

8.3.4.2 GMAC Initialization

Step 1 Write 1 to GMAC_BASIC_CTL1[bit0] to perform the software reset.

Step 2 Write 1 to GMAC_BASIC_CTL1[bit1] to set the DMA priority of TX/RX.

Step 3 Configure GMAC_TX_CTL1 and GMAC_RX_CTL1 to set the configuration of DMA TX and DMA RX.

Step 4 Configure GMAC_INT_EN to set the corresponding interrupts and shield the needless interrupts.

Step 5 Configure GMAC_TX_DMA_LIST and GMAC_RX_DMA_LIST to set the first address of the TX descriptor and the RX descriptor, respectively.

Step 6 Configure GMAC_TX_CTL0 and GMAC_RX_CTL0 to set the TX and RX parameters. Configure GMAC_BASIC_CTL0 to set the speed, duplex mode, loopback configuration. (If enabled the auto-negotiation, the configuration is performed as a result of the negotiation)

Step 7 Configure GMAC_RX_FRM_FLT to set the RX frame filter.

Step 8 Configure GMAC_TX_FLOW_CTL and GMAC_RX_CTL0 to set the control mechanism of TX and RX.

Step 9 Clear all interrupt flags.

Step 10 Write 1 to GMAC_TX_CTL0[bit31] and write 1 to GMAC_RX_CTL0[bit31] to enable the TX and RX functions.

8.3.5 Register List

Module Name	Base Address
GMAC	0x04500000

Register Name	Offset	Description
GMAC_BASIC_CTL0	0x0000	GMAC Basic Control Register0
GMAC_BASIC_CTL1	0x0004	GMAC Basic Control Register1

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Register Name	Offset	Description
GMAC_INT_STA	0x0008	GMAC Interrupt Status Register
GMAC_INT_EN	0x000C	GMAC Interrupt Enable Register
GMAC_TX_CTL0	0x0010	GMAC Transmit Control Register0
GMAC_TX_CTL1	0x0014	GMAC Transmit Control Register1
GMAC_TX_FLOW_CTL	0x001C	GMAC Transmit Flow Control Register
GMAC_TX_DMA_DESC_LIST	0x0020	GMAC Transmit Descriptor List Address Register
GMAC_RX_CTL0	0x0024	GMAC Receive Control Register0
GMAC_RX_CTL1	0x0028	GMAC Receive Control Register1
GMAC_RX_DMA_DESC_LIST	0x0034	GMAC Receive Descriptor List Address Register
GMAC_RX_FRM_FLT	0x0038	GMAC Receive Frame Filter Register
GMAC_RX_HASH0	0x0040	GMAC Hash Table Register0
GMAC_RX_HASH1	0x0044	GMAC Hash Table Register1
GMAC_MII_CMD	0x0048	GMAC Management Interface Command Register
GMAC_MII_DATA	0x004C	GMAC Management Interface Data Register
GMAC_ADDR_HIGH0	0x0050	GMAC MAC Address High Register0
GMAC_ADDR_LOW0	0x0054	GMAC MAC Address Low Register0
GMAC_ADDR_HIGHN	0x0050+0x08*N (N=1–7)	GMAC MAC Address High Register N (N=1–7)
GMAC_ADDR_LOWN	0x0054+0x08*N (N=1–7)	GMAC MAC Address Low Register N (N=1–7)
GMAC_TX_DMA_STA	0x00B0	GMAC Transmit DMA Status Register
GMAC_TX_CUR_DESC	0x00B4	GMAC Current Transmit Descriptor Register
GMAC_TX_CUR_BUF	0x00B8	GMAC Current Transmit Buffer Address Register
GMAC_RX_DMA_STA	0x00C0	GMAC Receive DMA Status Register
GMAC_RX_CUR_DESC	0x00C4	GMAC Current Receive Descriptor Register
GMAC_RX_CUR_BUF	0x00C8	GMAC Current Receive Buffer Address Register
GMAC_RGMII_STA	0x00D0	GMAC RGMII Status Register

8.3.6 Register Description

8.3.6.1 0x0000 GMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GMAC_BASIC_CTL0
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0000			Register Name: GMAC_BASIC_CTL0
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x0	SPEED GMAC Working Speed 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK GMAC Loopback Mode for Test 0: Disable 1: Enable
0	R/W	0x0	DUPLEX GMAC Transfer Mode 0: Half-duplex 1: Full-duplex

8.3.6.2 0x0004 GMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: GMAC_BASIC_CTL1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA Priority 0: Same priority 1: RX priority is over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset All clock inputs must be valid before soft reset. This bit is cleared internally when the reset operation is completed fully. Before writing any register, this bit should read a 0.

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8.3.6.3 0x0008 GMAC Interrupt Status Register (Default Value: 0x4000_0000)

Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	R	0x2000	Reserved
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First Data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, the length of the received frame is greater than 2048 bytes (10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, the RX DMA cannot acquire the next RX descriptor and RX DMA FSM is suspended. The ownership of the next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when the RX_DMA_START is written or the next receive frame is coming.

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Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains running.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Total interrupt pending which the frame is transmitted to FIFO 0: No Pending 1: Pending Write '1' to clear it.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire the next TX descriptor and the TX DMA FSM is suspended. The ownership of the next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to TX_DMA_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.

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Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.

8.3.6.4 0x000C GMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: GMAC_INT_EN
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable

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Offset: 0x000C			Register Name: GMAC_INT_EN
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

8.3.6.5 0x0010 GMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GMAC_TX_CTL0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disabled, the transmission will continue until the current transmission finishes.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

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8.3.6.6 0x0014 GMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GMAC_TX_CTL1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0.
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission 1: Start and run TX DMA
29:11	/	/	/
10:8	R/W	0x0	TX_TH Threshold value of TX DMA FIFO When TX_MD is 0, the transmission starts when the frame size in TX DMA FIFO is greater than the threshold. In addition, the full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX starts after the TX DMA FIFO bytes is greater than the TX_TH 1: TX starts after the TX DMA FIFO is located a full frame
0	R/WAC	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO 0: Enable 1: Disable

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8.3.6.7 0x001C GMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: GMAC_TX_FLOW_CTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After the transmission is completed, this bit will be cleared automatically. Before writing TX_FLOW_CTRL register, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic re-transmission of the pause frame. The threshold values should be always less than PAUSE_TIME.
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate the Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

8.3.6.8 0x0020 GMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GMAC_TX_DMA_LIST
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_DESC_LIST The base address of the transmission descriptor list It must be 32-bit aligned.

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8.3.6.9 0x0024 GMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GMAC_RX_CTL0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2048 bytes (JUMBO_FRM_EN==0) Up to 10240 bytes (JUMBO_FRM_EN==1) 1: Up to 16384 bytes Any bytes after that is cut off.
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length of field value is less than or equal to 1500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with the address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decodes the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

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8.3.6.10 0x0028 GMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GMAC_RX_CTL1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RX_DMA_START When set, the RX DMA will work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finishing the received current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable, base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/

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Offset: 0x0028			Register Name: GMAC_RX_CTL1
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 Only valid when RX_MD == 0, the full frames with a length less than the threshold are transferred automatically.
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When the bit is set to 1, it indicates forward undersized frames with no error and length less than 64 bytes.
1	R/W	0x0	RX_MD Receive Mode 0: RX starts to read after the RX DMA FIFO byte is greater than RX_TH 1: RX starts to read after the RX DMA FIFO is located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when the receive descriptors/buffers are unavailable 1: Disable

8.3.6.11 0x0034 GMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GMAC_RX_DMA_LIST
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_DESC_LIST The base address of the received descriptor list It must be 32-bit aligned.

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8.3.6.12 0x0038 GMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GMAC_RX_FRM_FLT
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive all
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when passing the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set 0: By comparing the DA field in DA MAC address registers 1: According to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: By comparing the DA field in DA MAC address registers 1: According to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of the SA filter. In addition, if the SA field of the received frame does not match the values in SA MAC address registers, drop this frame.

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Offset: 0x0038			Register Name: GMAC_RX_FRM_FLT
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass frames whose SA field matches SA MAC address registers 1: Pass frames whose SA field does not match SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it passes the address register filter or the hash filter (set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter (pass or fail) in the receive status word

8.3.6.13 0x0040 GMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: GMAC_RX_HASH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for the received frame filter.

8.3.6.14 0x0044 GMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: GMAC_RX_HASH1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for the received frame filter.

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8.3.6.15 0x0048 GMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: GMAC_MII_CMD
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divider Ratio The MDC Clock is divided from the AHB clock. 000: 16 001: 32 010: 64 011: 128 Others: Reserved
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/WAC	0x0	MII_BUSY MII Status 0: Writing 0 is no valid, and reading 0 indicates the read/write operation is finished 1: Writing 1 starts the read/write operation, and reading 1 indicates busy.

8.3.6.16 0x004C GMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: GMAC_MII_DATA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

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8.3.6.17 0x0050 GMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: GMAC_ADDR_HIGH0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16 bits of the 1st MAC address.

8.3.6.18 0x0054 GMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: GMAC_ADDR_LOW0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

8.3.6.19 0x0050+0x08*N GMAC MAC Address High Register N (Default Value: 0x0000_FFFF)

Offset: 0x0050+0x08*N (N=1~7)			Register Name: GMAC_ADDR_HIGHN
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: Used to compare with the destination address of the received frame 1: Used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of the MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH The upper 16 bits of the MAC address.

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8.3.6.20 0x0054+0x08*N GMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x08*N (N=1~7)			Register Name: GMAC_ADDR_LOWN
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32 bits of MAC address N (N: 1–7).

8.3.6.21 0x00B0 GMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: GMAC_TX_DMA_STA
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, when reset or disable TX DMA 001: RUN_FETCH_DESC, fetching TX DMA descriptor 010: RUN_WAIT_STA, waiting for the status of TX frame 011: RUN_TRANS_DATA, passing the frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, closing TX descriptor 110: SUSPEND, TX descriptor is unavailable or TX DMA FIFO underflow

8.3.6.22 0x00B4 GMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: GMAC_TX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TX_DMA_CUR_DESC The address of current transmit descriptor.

8.3.6.23 0x00B8 GMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: GMAC_TX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TX_DMA_CUR_BUF The address of current transmit DMA buffer.

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8.3.6.24 0x00C0 GMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: GMAC_RX_DMA_STA
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, when reset or disable RX DMA 001: RUN_FETCH_DESC, fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, waiting for the frame 100: SUSPEND, RX descriptor is unavailable 101: RUN_CLOSE_DESC, closing RX descriptor 110: Reserved 111: RUN_TRANS_DATA, passing the frame from host memory to RX DMA FIFO

8.3.6.25 0x00C4 GMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: GMAC_RX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DMA_CUR_DESC The address of current receive descriptor

8.3.6.26 0x00C8 GMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: GMAC_RX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DMA_CUR_BUF The address of current receive DMA buffer

8.3.6.27 0x00D0 GMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: GMAC_RGMII_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of the RGMII interface 0: Down 1: Up

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Offset: 0x00D0			Register Name: GMAC_RGMII_STA
Bit	Read/Write	Default/Hex	Description
2:1	R	0x0	RGMII_LINK_SPD The link speed of the RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of the RGMII interface 0: Half-Duplex 1: Full-Duplex

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8.4 GMAC1

8.4.1 Overview

The GMAC (QOS) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2015 standard.

The GMAC has the following features:

- One GMAC interface (GMAC1) for connecting to external Ethernet PHY
- Compliant with the IEEE 802.3-2015 standard
- IEEE 1588-2008 for precision networked clock synchronization, support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008
- Supports 10/100/1000 Mbit/s data transfer rates
- Supports RMII/RGMII PHY interface
- AMBA4 AXI master interface with 64-bit data transfer
- Supports both full-duplex and half-duplex operation
- Full-duplex flow control
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Source Address field and VLAN insertion or replacement, Double VLAN
- Transmit TCP/IP Checksum Offload
- Supports a variety of flexible address filtering modes (include Hash filter function)
- Optimization for packet-oriented DMA transfers with frame delimiters
  - Supports linked-list descriptor list structure
  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention: each descriptor can transfer up to 32 KB of data
  - Comprehensive status reporting for normal operation and transfers with errors
- Supports 4KB TXFIFO for transmission packets and 8KB RXFIFO for reception packets
- Supports 16 Descriptors Descriptor Pre-fetch cache for TX DMA and RX DMA
- Programmable interrupt options for different operational conditions
- Supports MDIO Interface for PHY device configuration and management
- Configurable big-endian and little-endian mode for Transmit and Receive paths
- Supports statistics on the received and transmitted packets
- Supports split header

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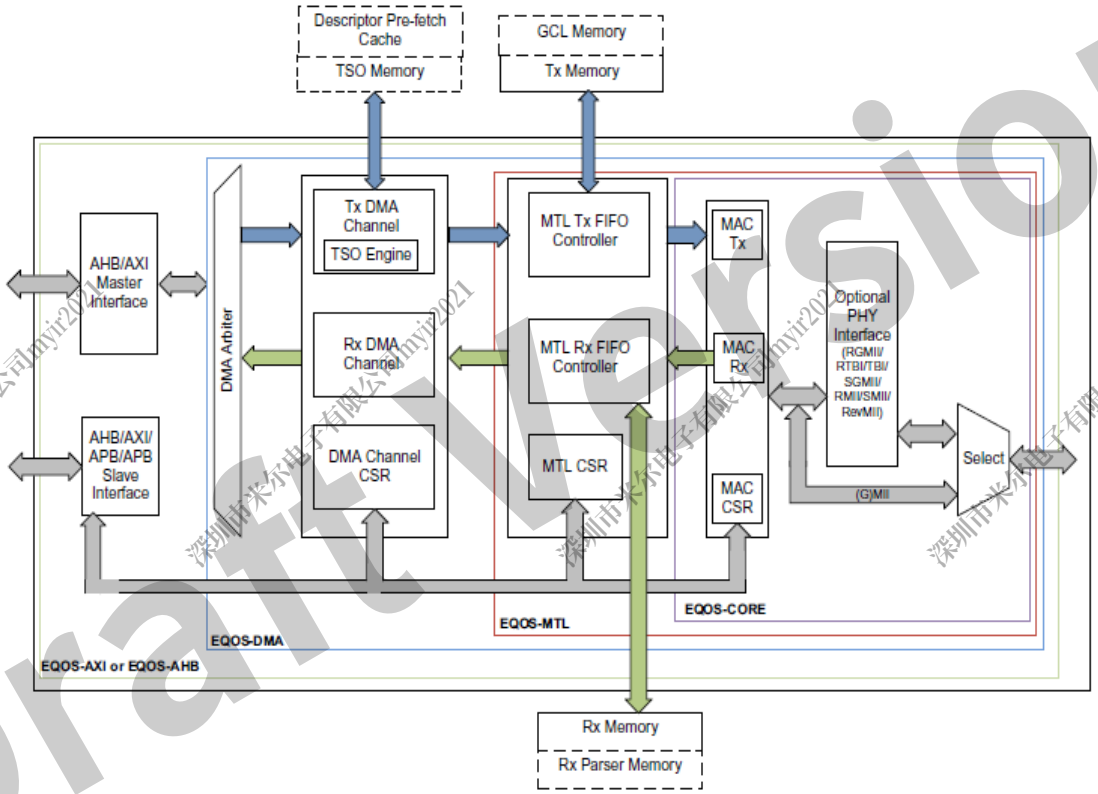
8.4.2 Block Diagram

The following figure shows the block diagram of the GMAC.

Figure 8-21 GMAC Block Diagram



The following table describes the components of the GMAC.

Table 8-7 GMAC Components

Components	Description
Interfaces	• AHB slave interface The 32-bit AHB slave interface provides access to the DMA, MTL, and MAC CSR space. • AXI master interface The DMA controller interfaces with the application through the AMBA4 AXI interface. The AMBA4 AXI bus interface provides the characteristics to support highly-effective data traffic throughput. • PHY interface The PHY interface can be configured to GMII/MII RGMII and RMII.
DMA	One DMA Channel has independent Transmit (TX) and Receive (RX) engines, and a CSR space. The TX engine transfers data from the system memory to the device port (MTL), whereas the Rx engine transfers data from the device port to the system memory. The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention.

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Components	Description
MTL	The MAC Transaction Layer (MTL) provides the FIFO memory interface to buffer and regulate the packets between the application system memory and the MAC. It also enables the data to be transferred between the application clock and MAC clock domains. One MTL queue. The MTL layer has two data paths: Transmit path and Receive Path.
MAC	The MAC supports many interfaces towards the PHY chip.

8.4.3 Functional Description

8.4.3.1 External Signals

The following table describes the external signals of the GMAC.

Table 8-8 GMAC External Signals

Signal Name	Description	Type
RGMII1-RXD0/RMII1-RXD0	RGMII1/RMII1 Receive Data0	I
RGMII1-RXD1/RMII1-RXD1	RGMII1/RMII1 Receive Data1	I
RGMII1-RXD2/RMII1-NULL	RGMII1 Receive Data2	I
RGMII1-RXD3/RMII1-NULL	RGMII1 Receive Data3	I
RGMII1-RXCK/ RMII1-NULL	RGMII1 Receive Clock	I
RGMII1-RXCTL/RMII1-CRS-DV	RGMII1 Receive Control/RMII1 Carrier Sense Receive Data Valid	I
RGMII1-CLKIN/RMII1-RXER	RGMII1 Transmit Clock from External/RMII1 Receive Error	I
RGMII1-TXD0/RMII1-TXD0	RGMII1/RMII1 Transmit Data0	O
RGMII1-TXD1/ RMII1-TXD1	RGMII1 Transmit Data1	O
RGMII1-TXD2/RMII1-NULL	RGMII1 Transmit Data2	O
RGMII1-TXD3/RMII1-NULL	RGMII1 Transmit Data3	O
RGMII1-TXCK/RMII1-TXCK	RGMII1/RMII1 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII1-TXCTL/RMII1-TXEN	RGMII1 Transmit Control/RMII1 Transmit Enable	O
RGMII1-MDC	RGMII1 Management Data Clock	O
RGMII1-MDIO	RGMII1 Management Data Input/ Output	I/O
RGMII1-EPHY-25M	25 MHz Output for GMAC PHY	O

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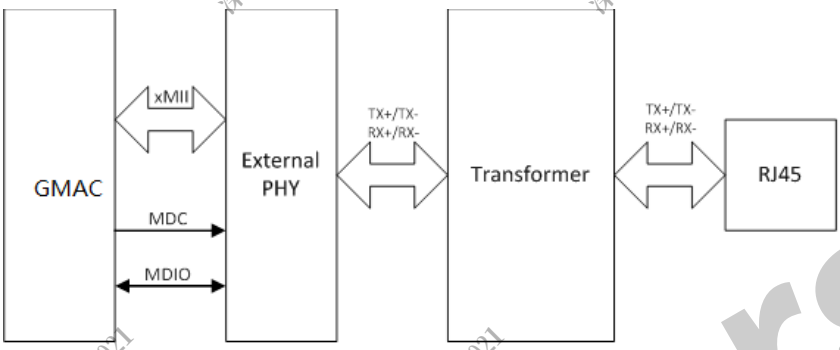
8.4.3.2 Typical Application

Figure 8-22 Typical Application



8.4.3.3 Source Address and VLAN Insertion, Replacement, or Deletion

The source address (SA) and VLAN fields are TX packet-related control information that are provided as part of the control word through ATI interfaces. GMAC supports the feature to insert or replace the source address based on the information in the MAC Address Registers, and also the feature to insert, replace or delete the VLAN fields (VLAN Type and VLAN Tag) based on the setting of the VLTI bit in the MAC_VLAN_Incl register. The SA insertion or replacement feature for all Transmit packets or selective packets. Similarly, the VLAN insertion, replacement, or deletion feature for all TX packets or selective packets.

8.4.3.4 External Memory for Descriptor Cache

GMAC supports external memory for descriptor cache. The external memory (SPRAM) is used to store the prefetched descriptors of all the DMAs active in the controller. Each DMA (TX or Rx) is allocated space to cache 16 descriptors (256 bytes). So, the DMA can read the prefetched descriptors without the bus access latency. After the prefetched descriptors are completely utilized, that is, when the descriptor cache is empty, a new request is placed for another burst of descriptors on AXI/AHB bus, when DMA requests for a new descriptor.

8.4.3.5 Packet Filtering

GMAC support Source Address or Destination Address Filtering and VLAN tag perfect filtering.

The Address Filtering Module of the MAC checks the source address (SA) and destination address (DA) fields of each incoming packet. The MAC supports 32 MAC addresses for perfect filtering and 64-bit hash table for Hash filter mode.

In VLAN tag perfect filtering, the MAC compares the VLAN tag of received packet and provides the VLAN packet status to the application. Based on the programmed mode, the MAC compares the lower 12 bits or all 16 bits of received VLAN tag to determine the perfect match.

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8.4.3.6 MAC Management Counters

The GMAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application. The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets.

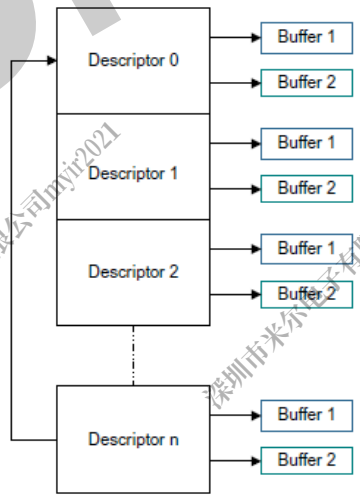
8.4.3.7 Descriptors

The DMA in the Ethernet subsystem transfers data based on a linked list of descriptors. The application creates the descriptors in the system memory. The GMAC supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted.
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted.

The GMAC supports the ring structure for DMA descriptor. Each normal descriptor contains two buffers and two address pointers.

Figure 8-23 Descriptor Ring Structure



In Ring structure, the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process. The descriptors up to one location less than the one indicated by the descriptor

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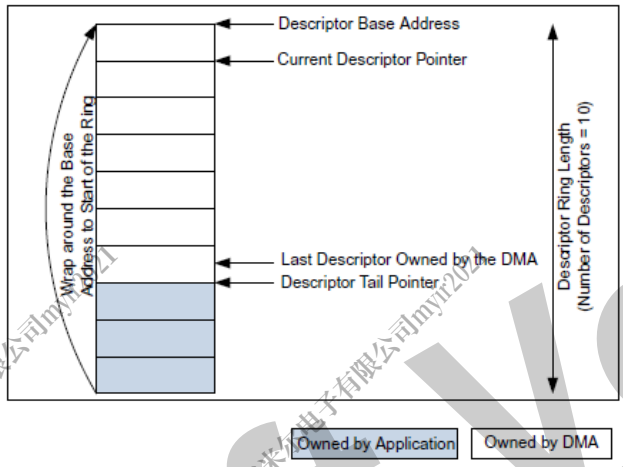
tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

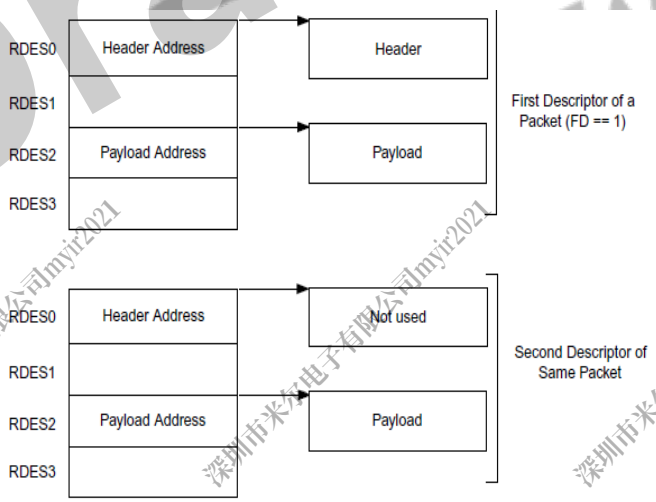
Current Descriptor Pointer == Descriptor Tail Pointer;

Figure 8-24 DMA Descriptor Ring



GMAC supports splitting the incoming receive packet header such that the header and the payload are stored in different buffers (buffer-1 and buffer-2) in the system memory.

Figure 8-25 Descriptors with Split Header Feature



Transmit Descriptor

Transmit Normal descriptor has two formats: Read format and Write-Back format.

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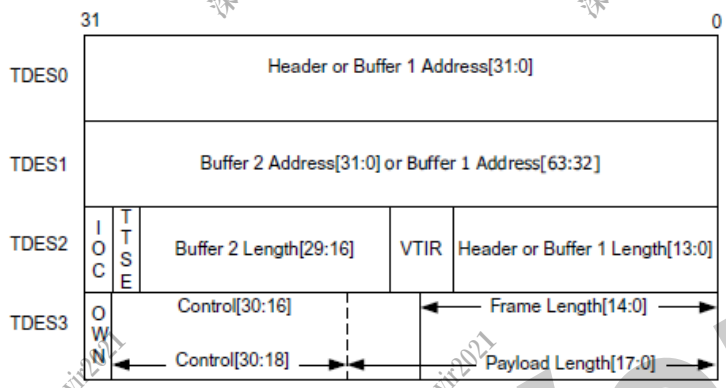
- Transmit Normal Descriptor (Read Format)

Figure 8-26 Transmit Descriptor Read Format



Bit	Name	Description
TDES0 Normal Descriptor (Read Format)		
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TmSO Header Address pointer when the following bits are set: • TSE bit of TDES3 • FD bit of TDES3
TDES1 Normal Descriptor (Read Format)		
31: 0	BUF2AP	Buffer 2 or Buffer 1 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment. In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16- bit of the Buffer 1 Address Pointer.
TDES2 Normal Descriptor (Read Format)		
31	IOC	Interrupt on Completion This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE/TMWD	Transmit Timestamp Enable or External TSO Memory Write Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set. If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet.
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length.

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Bit	Name	Description
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: 2'b00: Do not add a VLAN tag. 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the VLAN packets. 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets. These bits are valid when the Enable SA and VLAN Insertion on TX option is selected while configuring the core.
13:0	HL or B1L	Header Length or Buffer 1 Length For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.
TDES3 Normal Descriptor (Read Format)		
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.

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Bit	Name	Description
27:26	CPC	CRC Pad Control This field controls the CRC and Pad Insertion for TX packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits [27:26]: 2'b00: CRC and Pad Insertion The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. 2'b01: CRC Insertion (Disable Pad Insertion) The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. 2'b10: Disable CRC Insertion The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. 2'b11: CRC Replacement The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. This field is valid only for the first descriptor. **Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.**

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Bit	Name	Description
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits [24:23]: 2'b00: Do not include the source address 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. 2'b11: Reserved These bits are valid in the EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations when the Enable SA and VLAN Insertion on TX option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set. This field is valid only for the first descriptor.
22:19	SLOTNU Mor THL	SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels. THL: TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor.
18	TSE	TCP Segmentation Enable When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE [1:0] bit of the DMA_CH(#i) _Tx_Control register. This bit is valid only if the FD bit is set.

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Bit	Name	Description
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length These bits control the checksum calculation and insertion. The following list describes the bit encoding: 2'b00: Checksum Insertion Disabled. 2'b01: Only IP header checksum calculation and insertion are enabled. 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core.
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not include Ethernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOT enabled, value written into this field is not used when TSE = 0.

- Transmit Normal Descriptor (Write-Back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet.

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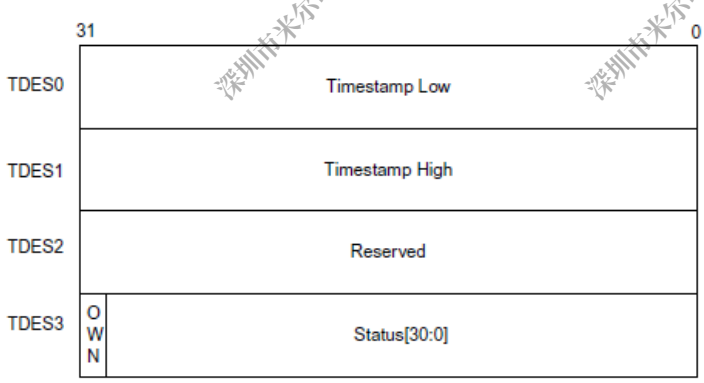
Figure 8-27 Transmit Context Descriptor



Bit	Name	Description
TDES0 Normal Descriptor (Write Format)		
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set.
TDES1Normal Descriptor (Write Format)		
31: 0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.
TDES2 Normal Descriptor (Write Format)		
31:0	/	Reserved
TDES3 Normal Descriptor (Write Format)		
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. The DMA clears this bit when it completes the packet transmission. After the write-back is complete, this bit is set to 'b0.
30	CTXT	Context Type This bit should be set to 'b0 for Normal descriptor.
29	FD	First Descriptor This bit indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor This bit is set 'b1 for last descriptor of a packet. The DMA writes the status fields only in the last descriptor of the packet.

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Bit	Name	Description
27:24	/	Reserved
23	DE	Descriptor Error Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be: ● Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet. ● All 1s ● CTXT is set to 1 along with LD or FD bits set to 1. **Note:** ● **When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA sets the TI bit in the DMA_CH#_Status register.** ● **Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.**
22:18	/	Reserved
17	TTSS	TX Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. **Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by GMAC.**

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Bit	Name	Description
15	ES	Error Summary This bit indicates the logical OR of the following bits: TDES3[0]: IP Header Error TDES3[14]: Jabber Timeout TDES3[13]: Packet Flush TDES3[12]: Payload Checksum Error TDES3[11]: Loss of Carrier TDES3[10]: No Carrier TDES3[9]: Late Collision TDES3[8]: Excessive Collision TDES3[3]: Excessive Deferral TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set.
14	JT	Jabber Timeout Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC_Configuration register is not set.
13	FF	Packet Flushed Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved.
11	LoC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.

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Bit	Name	Description
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted.
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits' times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ● The DMA encountered an empty Transmit Buffer while transmitting the packet. ● The application filled the MTL TX FIFO slower than the MAC transmit rate. The transmission process enters the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register.
1	DB	Deferred Bit This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.

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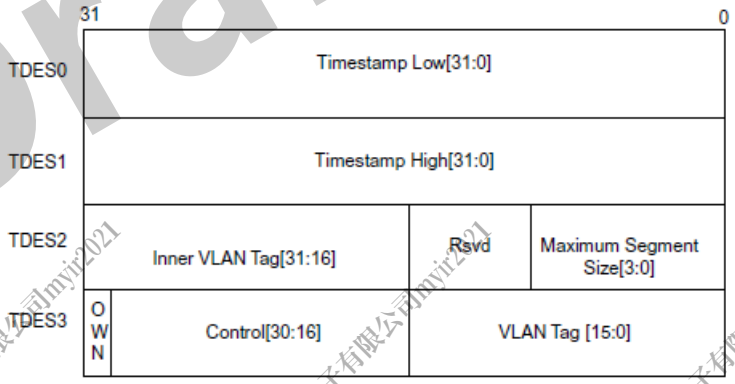
Bit	Name	Description
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when TX Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload. In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error.

- Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

Figure 8-28 Transmit Context Descriptor



Bit	Name	Description
TDES0 Context Descriptor		
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

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Bit	Name	Description
TDES1 Context Descriptor		
31: 0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.
TDES2 Context Descriptor		
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	/	Reserved
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.
TDES3 Context Descriptor		
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.
30	CTXT	Context Type This bit should be set to 1'b1 for Context descriptor.
29:28	/	Reserved
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMS SV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.
25:24	/	Reserved

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Bit	Name	Description
23	CDE	Context Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the context descriptor. Context Descriptor Errors can be: ● Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet. ● All 1s. ● CD, LD, and FD bits set to 1. Note: ● When the Context Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA sets the TI bit in the DMA_CH#_Status register. ● Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent. ● This error is categorized as an abnormal event; recovery is only by issuing a software reset (DMA stopping-reconfiguring-restarting recovery mechanism is not supported).
22:20	Rsvd	Reserved
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: ● 2'b00: Do not add the inner VLAN tag. ● 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. ● 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_In-ner_VLAN_Incl register or context descriptor. ● 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames. These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected.

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Bit	Name	Description
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset.

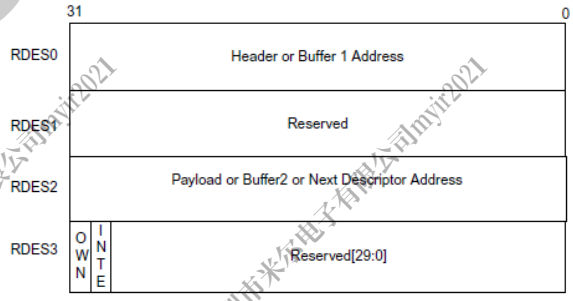
Receive Descriptor

All RX descriptors are prepared by the software and given to the DMA as "Normal" Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA closes the descriptor with the corresponding packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)".

- Receive Normal Descriptor (Read Format)

The read format for a Receive Normal descriptor is made up of a header or Buffer 1 address, reserved field, payload or Buffer 2 or Next Descriptor address, a 30-bit reserved filed, OWN bit, and an interrupt bit.

Figure 8-29 Receive Normal Descriptor (Read Format)



Bit	Name	Description
RDES0 Normal Descriptor (Read Format)		
31:0	BUF1AP	Header or Buffer 1 Address Pointer When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet.

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Bit	Name	Description
RDES1 Normal Descriptor (Read Format)		
31: 0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.
RDES2 Normal Descriptor (Read Format)		
31: 0	BUF2A P	Buffer 2 Address Pointer These bits indicate the physical address of Buffer 2. When the SPH bit of the DMA_CH#_Control register is set, the buffer address pointer must be bus width-aligned, that is, RDES2[3:0, 2:0, or 1:0] = 0 corresponding to 128, 64, or 32 bus width. LSBs are ignored internally.
RDES3 Normal Descriptor (Read Format)		
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ● The DMA completes the packet reception. ● The buffers associated with the descriptor are full.
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Rsvd	Reserved
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:16	Rsvd	Reserved
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Rsvd	Reserved
15:0	BUF2A P	Buffer2 Address Pointer In the 64 bit addressing mode, this field contains the most-significant 16 bits of the Buffer2 address pointer. Otherwise, this field is reserved.

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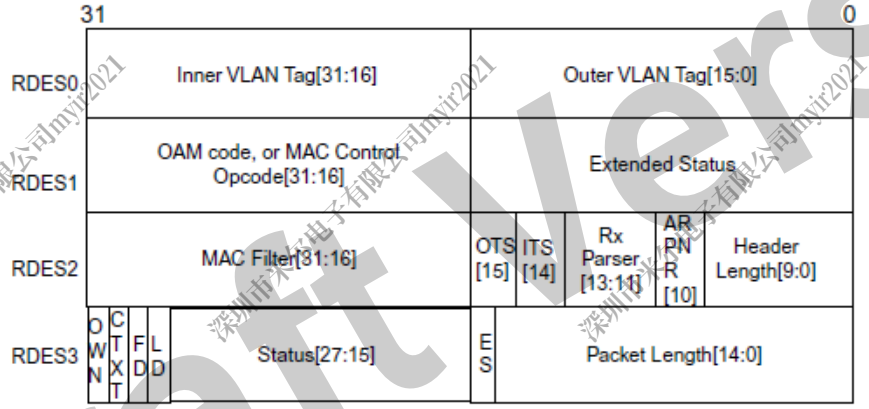
Bit	Name	Description
24	BUF1V	Buffer 1 Address Valid
23:1 6	Rsvd	Reserved
15:0	BUF2A P	Buffer2 Address Pointer In the 64 bit addressing mode, this field contains the most-significant 16 bits of the Buffer2 address pointer. Otherwise, this field is reserved.

- Receive Normal Descriptor (Write-Back Format)

Figure 8-30 Receive Normal Descriptor (Write-Back Format)



Bit	Name	Description
RDES0 Normal Descriptor (Write-Back Format)		
31:1 6	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set. This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.
RDES1 Normal Descriptor (Write-Back Format)		
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode The bits[15:8] of RDES3 contains the subtype and bits [7:0] contains the code.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.

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Bit	Name	Description
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal descriptor for a packet.
13	PV	PTP Version This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: 0000: No PTP message received 0001: SYNC (all clock types) 0010: Follow_Up (all clock types) 0011: Delay_Req (all clock types) 0100: Delay_Resp (all clock types) 0101: Pdelay_Req (in peer-to-peer transparent clock) 0110: Pdelay_Resp (in peer-to-peer transparent clock) 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) 1000: Announce 1001: Management 1010: Signaling 1011–1110: Reserved 1111: PTP packet with Reserved message type These bits are available only when you select the Timestamp feature.
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ● The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ● The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ● The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP. Bit 15 (ES) of RDES3 is not set when this bit is set.

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Bit	Name	Description
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error When this bit is set, it indicates either of the following: ● The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes. ● The IP datagram version is not consistent with the Ethernet Type value. ● Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
2:0	PT	Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): 3'b000: Unknown type or IP/AV payload not processed 3'b001: UDP 3'b010: TCP 3'b011: ICMP 3'b110: AV Tagged Data Packet 3'b111: AV Tagged Control Packet 3'b101: AV Untagged Control Packet 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

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Bit	Name	Description
RDES2 Normal Descriptor (Write-Back Format)		
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: 000: Filter 0 001: Filter 1 010: Filter 2 011: Filter 3 100: Filter 4 101: Filter 5 110: Filter 6 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter. **Note: This status is not available when Flexible RX Parser is enabled.**
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ● Layer 3 fields are not enabled and all enabled Layer 4 fields match. ● All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29]. **Note: This status is not available when Flexible RX Parser is enabled.**
27	L3FM	Layer 3 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ● All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed. ● All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29]. **Note: This status is not available when Flexible RX Parser is enabled.**

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Bit	Name	Description
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register. **Note: This status is not available when Flexible RX Parser is enabled.**
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hash value. **Note: This status is not available when Flexible RX Parser is enabled.**
17	DAF/RXPI	Destination Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error. **Note: When this bit is set, ES bit of RDES3 is also set.**
16	SAF/RXP D	SA Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser. **Note: When this bit is set, ES bit of RDES3 is also set.**
15	OTS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter. This bit is valid only when DWC_EQOS_ERVFE is not enabled. If DWC_EQOS_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS). This bit is valid for both Single and Double VLAN Tagged frames
14	ITS	Inner VLAN Tag Filter Status (ITS) This bit is valid only when DWC_EQOS_ERVFE is enabled. This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled. For more information, see the Filter Status topic.

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Bit	Name	Description
13:11	RxParser	3'b000: RX Parser filter passed 3'b001: Packet rejected in Rx Parser 3'b010: Rx Parser overflow errors 3'b011: Incomplete Rx parsing of the packet 3'b100: AF = 1, RF = 1, Bypass 3'b101: RA = 1 and L2 filter fails (Rx parser bypass) 3'b110: Reserved 3'b111: Incomplete parsing due to ECC error
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time). This bit is reserved when the Enable IPv4 ARP Offload option is not selected.
9:0	HL	L3/L4 Header Length This field contains the length of the header of the packet split by the MAC at L3 or L4 header boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1). The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header. This field is valid when the Enable Split Header Feature option is selected.
RDES3 Normal Descriptor (Write-Back Format)		
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ● The DMA completes the packet reception ● The buffers associated with the descriptor are full

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Bit	Name	Description
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} 2'b00: Intermediate Descriptor 2'b01: First Descriptor 2'b10: Reserved 2'b11: Descriptor Error (due to all 1s) **Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data. Receive DMA sets the CDE field of the DMA_CH#_Status register but does not the RI field even when IOC field is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.**
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last Descriptor When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.

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Bit	Name	Description
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). **Note: Giant packet indicates only the packet length. It does not cause any packet truncation.**
22	RWT	Receive Watchdog Timeout When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. **Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial packets are dropped completely in Rx FIFO.**
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: 3'b000: The packet is a length packet 3'b001: The packet is a type packet. 3'b011: The packet is a ARP Request packet type 3'b100: The packet is a type packet with VLAN Tag 3'b101: The packet is a type packet with Double VLAN Tag 3'b110: The packet is a MAC Control packet type 3'b111: The packet is a OAM packet type 3'b010: Reserved

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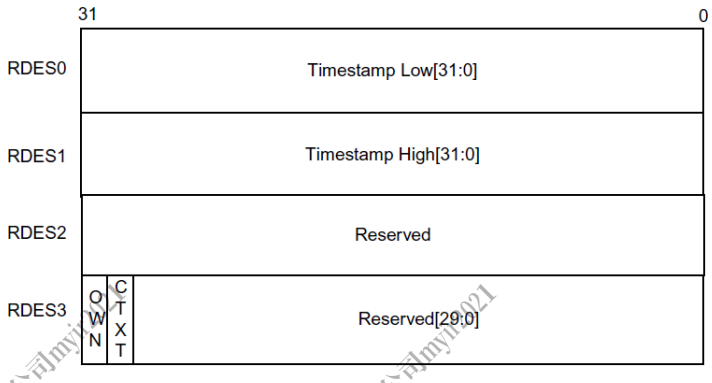
Bit	Name	Description
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: RDES3[24]: CRC Error RDES3[19]: Dribble Error RDES3[20]: Receive Error RDES3[22]: Watchdog Timeout RDES3[21]: Overflow Error RDES3[23]: Giant Packet RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled. This field is valid only when the LD bit of RDES3 is set.
14:0	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

- Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Figure 8-31 Receive Context Descriptor



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Bit	Name	Description
RDES0 Context Descriptor		
31: 0	RTSL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.
RDES1 Context Descriptor		
31: 0	RTSH	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt.
RDES2 Context Descriptor		
31:0	/	Reserved
RDES3 Context Descriptor		
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ● The DMA completes the packet reception. ● The buffers associated with the descriptor are full.
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2'b11 to indicate a descriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} 2'b00: Reserved 2'b01: Reserved 2'b10: Context Descriptor 2'b11: Descriptor Error **Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA sets the CDE bit in DMA_CH#_Status register but does not set the RI field even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.**
29	DE	Descriptor Error See the CTXT bit description for details of using theDE bit along with CTXT bit.

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Bit	Name	Description
28:0	/	Reserved

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8.5 General Purpose ADC (GPADC)

8.5.1 Overview

The General Purpose ADC (GPADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection. This ADC is a type of successive approximation register (SAR) A/D converter.

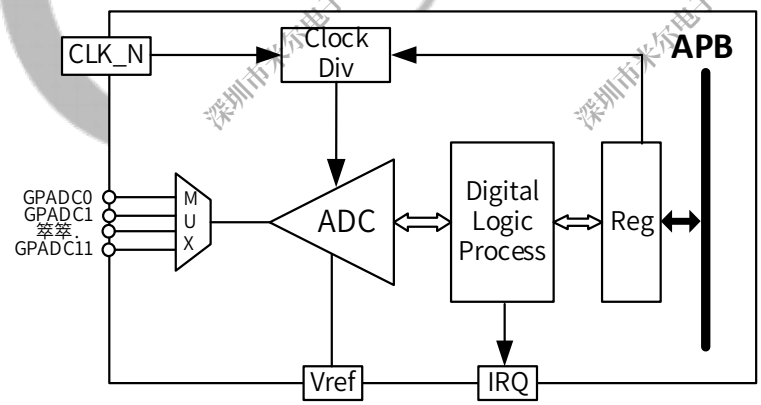
The GPADC has the following features:

- 24-ch successive approximation register (SAR) analog-to-digital converter (ADC)
  - GPADC_CTRL0: 12 channels
  - GPADC_CTRL1: 12 channels
- 64 FIFO depth of data register
- 12-bit sampling resolution and 10-bit precision
- Power reference voltage: VCC-ADC, analog input voltage range: 0 to VCC-ADC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode
- Input voltage: 0 V to 1.8 V

8.5.2 Block Diagram

The following table shows the block diagram of the GPADC_CTRL0 and the block diagram of GPADC_CTR1 is the same.

Figure 8-32 GPADC_CTRL0 Block Diagram



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8.5.3 Functional Description

8.5.3.1 External Signals

The following table describes the external signals of the GPADC.

Table 8-9 GPADC External Signals

Signal Name	Description	Type
ADCIN0	External Resistor and Capacitor Input	AI
ADCIN1	External Resistor and Capacitor Input	AI
PGAOUT0	External Resistor and Capacitor Output	AO
PGAOUT1	External Resistor and Capacitor Output	AO
GND-ADC	Analog Ground	G
VCM-ADC	External Capacitor Connection	A I/O
VREFP-ADC	GPADC Reference Voltage (Positive)	P
VREFN-ADC	GPADC Reference Voltage (Negative)	P
VCC-ADC	Power Supply for GPADC	P
GPADC_CTRL0		
GPADC0	General Purpose ADC Input Channel 0/ BROM Boot Select in GPADC_CTRL0	AI
GPADC1	General Purpose ADC Input Channel 1 in GPADC_CTRL0	AI
GPADC2	General Purpose ADC Input Channel 2 in GPADC_CTRL0	AI
GPADC3	General Purpose ADC Input Channel 3 in GPADC_CTRL0	AI
GPADC4	General Purpose ADC Input Channel 4 in GPADC_CTRL0	AI
GPADC5	General Purpose ADC Input Channel 5 in GPADC_CTRL0	AI
GPADC6	General Purpose ADC Input Channel 6 in GPADC_CTRL0	AI
GPADC7	General Purpose ADC Input Channel 7 in GPADC_CTRL0	AI
GPADC8	General Purpose ADC Input Channel 8 in GPADC_CTRL0	AI
GPADC9	General Purpose ADC Input Channel 9 in GPADC_CTRL0	AI
GPADC10	General Purpose ADC Input Channel 10 in GPADC_CTRL0	AI
GPADC11	General Purpose ADC Input Channel 11 in GPADC_CTRL0	AI
GPADC_CTRL1		
GPADC12	General Purpose ADC Input Channel 0 in GPADC_CTRL1	AI
GPADC13	General Purpose ADC Input Channel 1 in GPADC_CTRL1	AI
GPADC14	General Purpose ADC Input Channel 2 in GPADC_CTRL1	AI
GPADC15	General Purpose ADC Input Channel 3 in GPADC_CTRL1	AI
GPADC16	General Purpose ADC Input Channel 4 in GPADC_CTRL1	AI
GPADC17	General Purpose ADC Input Channel 5 in GPADC_CTRL1	AI
GPADC18	General Purpose ADC Input Channel 6 in GPADC_CTRL1	AI
GPADC19	General Purpose ADC Input Channel 7 in GPADC_CTRL1	AI
GPADC20	General Purpose ADC Input Channel 8 in GPADC_CTRL1	AI
GPADC21	General Purpose ADC Input Channel 9 in GPADC_CTRL1	AI
GPADC22	General Purpose ADC Input Channel 10 in GPADC_CTRL1	AI

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Signal Name	Description	Type
GPADC23	General Purpose ADC Input Channel 11 in GPADC_CTRL1	AI

8.5.3.2 Clock Sources

The GPADC has one clock source. The following table describes the clock source for GPADC. Users can see section 2.7 Clock Controller Unit (CCU) for clock setting, configuration, and gating information.

Table 8-10 GPADC Clock Sources

Clock Sources	Description	module
HOSC	The default frequency is 24 MHz	CCU

8.5.3.3 GPADC Work Mode

- Single conversion mode

The GPADC completes one conversion in a specified channel, the converted data is updated at the data register of the corresponding channel.

- Continuous conversion mode

The GPADC has continuous conversion in a specified channel until the software stops, the converted data is updated at the data register of the corresponding channel.

- Burst conversion mode

The GPADC samples and converts in a specified channel, and sequentially stores the results in FIFO.

8.5.3.4 Clock and Timing Requirements

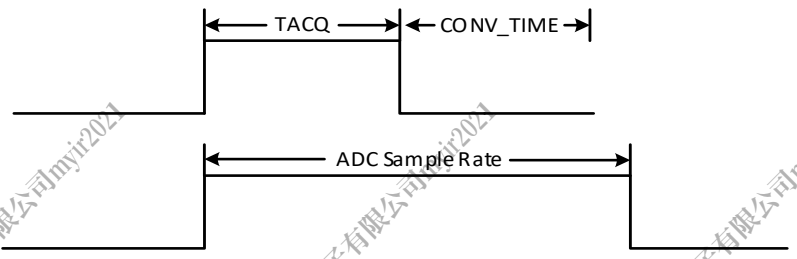
CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/(24MHz/13Cycles) =0.542 (us)

TACQ (ADC acquiring time) > 10RC (R is output impedance of ADC sample circuit, C = 6.4 pF)

ADC Sample Frequency > TACQ+CONV_TIME

Figure 8-33 GPADC Clock and Timing Requirement



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8.5.3.5 GPADC Calculate Formula

GPADC calculate formula: GPADC_DATA = Vin/VREF*4095

Where:

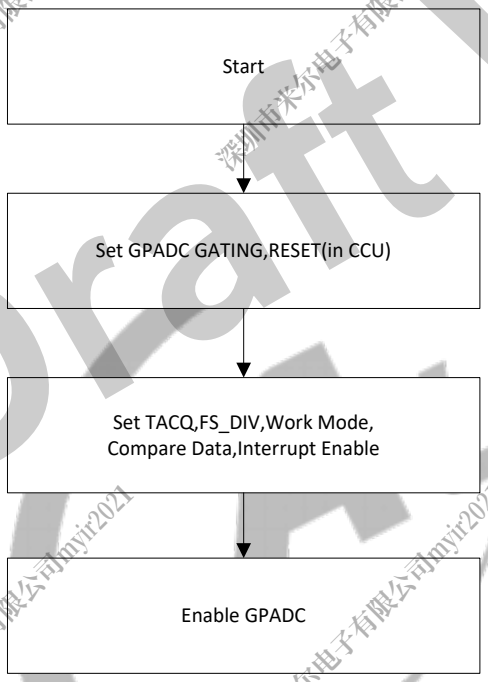
VREF = 1.8 V

8.5.4 Programming Guidelines

8.5.4.1 Initializing GPADC

The GPADC initial process is as follows.

Figure 8-34 GPADC Initial Process



Query Mode

Take channel0 for example:

Step 1 Write 0x1 to the bit [16] of GPADC_BGR_REG to dessert reset.

Step 2 Write 0x1 to the bit [0] of GPADC_BGR_REG to enable the GPADC clock.

Step 3 Write 0x2F to the bit [15:0] of GP_SR_CON to set the acquiring time of ADC.

Step 4 Write 0x1DF to the bit [31:16] of GP_SR_CON to set the ADC sample frequency divider.

Step 5 Write 0x2 to the bit [19:18] of GP_CTRL to set the continuous conversion mode.

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Step 6 (Optional) If you need to configure the sampling frequency for each channel, follow these steps:

a) Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency set in step4 is multiplied by this value to get the actual sampling frequency. For detailed configuration information, please refer to section 8.5.4.2 Configuring Sampling Frequency.

b) Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0.

Step 7 Write 0x1 to the bit [0] of GP_CS_EN to enable the analog input channel.

Step 8 Write 0x1 to the bit [16] of GP_CTRL to enable the ADC function.

Step 9 Read the bit [0] of GP_DATA_INTS, if the bit is 1, then data conversion is complete.

Step 10 Read the bit [11:0] of GP_CH0_DATA, and calculate voltage value based on GPADC formula.

Interrupt Mode

Take channel0 for example:

Step 1 Write 0x1 to the bit [16] of GPADC_BGR_REG to dessert reset.

Step 2 Write 0x1 to the bit [0] of GPADC_BGR_REG to enable the GPADC clock.

Step 3 Write 0x2F to the bit [15:0] of GP_SR_CON to set the acquiring time of ADC.

Step 4 Write 0x1DF to the bit [31:16] of GP_SR_CON to set the ADC sample frequency divider.

Step 5 Write 0x2 to the bit [19:18] of GP_CTRL to set the continuous conversion mode.

Step 6 (Optional) If you need to configure the sampling frequency for each channel, follow these steps:

a) Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency set in step4 is multiplied by this value to get the actual sampling frequency. For detailed configuration information, please refer to section 8.5.4.2 Configuring Sampling Frequency.

b) Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0. Write 0x1 to the bit [0] of GP_CS_EN to enable the analog input channel.

Step 7 Write 0x1 to the bit [0] of GP_DATA_INTC to enable the GPADC data interrupt.

Step 8 Set the GIC module based on the IRQ 93.

Step 9 Put interrupt handler address into interrupt vector table based on the IRQ 93.

Step 10 Write 0x1 to the bit16 of GP_CTRL to enable the ADC function.

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Step 11 Read the bit [11:0] of GP_CH0_DATA from the interrupt handler, calculate voltage value based on GPADC formula.

8.5.4.2 Configuring Sampling Frequency

The sampling frequency is only configurable in continue conversion mode. Note that the sampling frequency for each channel is only able to be configured as a multiple of 32 kHz and the total sampling frequency (sum of the sampling frequency of each channel) should be less than or equal to 1 MHz.

The sampling frequency configuration steps are as follows.

Step 1 If GPADC function is enabled, Configure the ADC_EN bit (bit [16]) of GP_CTRL (offset: 0x0004) register to disable ADC function.

Step 2 Configure the FS_DIV bit (bit [31:16]) of GP_SR_CON (offset: 0x0000) register to set the initial sampling frequency of each channel.

Step 3 Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency is multiplied by this value to get the actual sampling frequency.

NOTE

All GPADC channels should be configured simultaneously.

The following are the all available sampling frequencies for each channel and corresponding GP_SMP_TMS values.

Table 8-11 GP_SMP_TMS Value Corresponding to Each Sampling Frequency

Sampling frequency	GP_SMP_TMS Value	Sampling frequency	GP_SMP_TMS Value
32 kHz	1	544 kHz	17
64 kHz	2	576 kHz	18
96 kHz	3	608 kHz	19
128 kHz	4	640 kHz	20
160 kHz	5	672 kHz	21
192 kHz	6	704 kHz	22
224 kHz	7	736 kHz	23
256 kHz	8	768 kHz	24
288 kHz	9	800 kHz	25
320 kHz	10	832 kHz	26
352 kHz	11	864 kHz	27
384 kHz	12	896 kHz	28
416 kHz	13	928 kHz	29
448 kHz	14	960 kHz	30

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Sampling frequency	GP_SMP_TMS Value	Sampling frequency	GP_SMP_TMS Value
480 kHz	15	992 kHz	31
512 kHz	16	/	/

Step 4 Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0.

Step 5 Configure the ADC_EN bit (bit [16]) of GP_CTRL (offset: 0x0004) register to enable ADC function.

8.5.5 Register List

Module Name	Base Address
GPADC_CTRL0	0x02009000
GPADC_CTRL1	0x02009C00

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register
GP_CH2_CMP_DATA	0x0048	GPADC CH2 Compare Data Register
GP_CH3_CMP_DATA	0x004C	GPADC CH3 Compare Data Register
GP_CH4_CMP_DATA	0x0050	GPADC CH4 Compare Data Register
GP_CH5_CMP_DATA	0x0054	GPADC CH5 Compare Data Register
GP_CH6_CMP_DATA	0x0058	GPADC CH6 Compare Data Register
GP_CH7_CMP_DATA	0x005C	GPADC CH7 Compare Data Register
GP_CH8_CMP_DATA	0x0060	GPADC CH8 Compare Data Register
GP_CH9_CMP_DATA	0x0064	GPADC CH9 Compare Data Register
GP_CH10_CMP_DATA	0x0068	GPADC CH10 Compare Data Register
GP_CH11_CMP_DATA	0x006C	GPADC CH11 Compare Data Register

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Register Name	Offset	Description
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register
GP_CH2_DATA	0x0088	GPADC CH2 Data Register
GP_CH3_DATA	0x008C	GPADC CH3 Data Register
GP_CH4_DATA	0x0090	GPADC CH4 Data Register
GP_CH5_DATA	0x0094	GPADC CH5 Data Register
GP_CH6_DATA	0x0098	GPADC CH6 Data Register
GP_CH7_DATA	0x009C	GPADC CH7 Data Register
GP_CH8_DATA	0x00A0	GPADC CH8 Data Register
GP_CH9_DATA	0x00A4	GPADC CH9 Data Register
GP_CH10_DATA	0x00A8	GPADC CH10 Data Register
GP_CH11_DATA	0x00AC	GPADC CH11 Data Register
GP_SMP_TMS0	0x00C0	GPADC Sampling Times0 Register Description
GP_SMP_TMS1	0x00C4	GPADC Sampling Times1 Register Description
GP_SMP_TMS2	0x00C8	GPADC Sampling Times2 Register Description
GP_SMP_BYP	0x00D0	GPADC Channel Sample Rate Setting Bypass Register Description
GP_COMP_EN	0x00FC	GPADC Reference Voltage Source Select Register

8.5.6 Register Description

8.5.6.1 0x0000 GPADC Sample Rate Configure Register Description (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	Read/Write	Default/Hex	Description
31: 16	R/W	0x1DF	FS_DIV ADC Sample Frequency Divider CLK_IN/(n+1) Default value: 50K
15:0	R/W	0x2F	TACQ ADC Acquiring Time (n+1)/CLK_IN Default value: 2 us

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8.5.6.2 0x0004 GPADC Control Register Description (Default Value: 0x0080_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	ADC_FIRST_DLY ADC First Convert Delay setting ADC conversion of each channel is delayed by N samples.
23	R/W	0x1	ADC_AUTOCALI_EN ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias Adjust the bandwidth of the ADC amplifier.
19:18	R/W	0x0	GP_MODE GPADC Work Mode 00: Single conversion mode 01: Single-cycle conversion mode 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: start Calibration, it is clear to 0 after calibration
16	R/W	0x0	ADC_EN ADC Function Enable Before the bit is enabled, configure ADC parameters including the work mode and channel number, etc. 0: Disable 1: Enable When selecting a single conversion mode, the bit can be cleared automatically after the switch is completed.
15:0	/	/	/

8.5.6.3 0x0008 GPADC Compare and Select Enable Register Description (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

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Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	ADC_CH11_CMP_EN Channel 11 Compare Enable 0: Disable 1: Enable
26	R/W	0x0	ADC_CH10_CMP_EN Channel 10 Compare Enable 0: Disable 1: Enable
25	R/W	0x0	ADC_CH9_CMP_EN Channel 9 Compare Enable 0: Disable 1: Enable
24	R/W	0x0	ADC_CH8_CMP_EN Channel 8 Compare Enable 0: Disable 1: Enable
23	R/W	0x0	ADC_CH7_CMP_EN Channel 7 Compare Enable 0: Disable 1: Enable
22	R/W	0x0	ADC_CH6_CMP_EN Channel 6 Compare Enable 0: Disable 1: Enable
21	R/W	0x0	ADC_CH5_CMP_EN Channel 5 Compare Enable 0: Disable 1: Enable
20	R/W	0x0	ADC_CH4_CMP_EN Channel 4 Compare Enable 0: Disable 1: Enable
19	R/W	0x0	ADC_CH3_CMP_EN Channel 3 Compare Enable 0: Disable 1: Enable
18	R/W	0x0	ADC_CH2_CMP_EN Channel 2 Compare Enable 0: Disable 1: Enable

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Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable 0: Disable 1: Enable
15:12	/	/	/
11	R/W	0x0	ADC_CH11_SELECT Analog input channel 11 Select 0: Disable 1: Enable
10	R/W	0x0	ADC_CH10_SELECT Analog input channel 10 Select 0: Disable 1: Enable
9	R/W	0x0	ADC_CH9_SELECT Analog input channel 9 Select 0: Disable 1: Enable
8	R/W	0x0	ADC_CH8_SELECT Analog input channel 8 Select 0: Disable 1: Enable
7	R/W	0x0	ADC_CH7_SELECT Analog input channel 7 Select 0: Disable 1: Enable
6	R/W	0x0	ADC_CH6_SELECT Analog input channel 6 Select 0: Disable 1: Enable
5	R/W	0x0	ADC_CH5_SELECT Analog input channel 5 Select 0: Disable 1: Enable
4	R/W	0x0	ADC_CH4_SELECT Analog input channel 4 Select 0: Disable 1: Enable

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Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	ADC_CH3_SELECT Analog input channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CH2_SELECT Analog input channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CH1_SELECT Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x0	ADC_CH0_SELECT Analog input channel 0 Select 0: Disable 1: Enable

8.5.6.4 0x000C GPADC FIFO Interrupt Control Register Description (Default Value: 0x0000_1F00)

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	FIFO_DATA_DRQ_EN ADC FIFO Date DRQ Enable 0: Disable 1: Enable
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/

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Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	Read/Write	Default/Hex	Description
4	R/WAC	0x0	FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self-clear to '0'.
3:0	/	/	/

8.5.6.5 0x0010 GPADC FIFO Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING. ADC FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
16	R/W1C	0x0	FIFO_DATA_PENDING. ADC FIFO Data Available Pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt
15:14	/	/	/
13:8	R	0x0	RXA_CNT. ADC FIFO available Sample Word Counter
7:0	/	/	/

8.5.6.6 0x0014 GPADC FIFO Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	GP_FIFO_DATA GPADC Data in FIFO

8.5.6.7 0x0018 GPADC Calibration Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GP_CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

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Offset: 0x0018			Register Name: GP_CDATA
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x000	GP_CDATA GPADC Calibration Data

8.5.6.8 0x0020 GPADC Data Low Interrupt Configure Register Description (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W	0x0	CH11_LOW_IRQ_EN Channel 11 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	CH10_LOW_IRQ_EN Channel 10 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	CH9_LOW_IRQ_EN Channel 9 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	CH8_LOW_IRQ_EN Channel 8 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
7	R/W	0x0	CH7_LOW_IRQ_EN Channel 7 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
6	R/W	0x0	CH6_LOW_IRQ_EN Channel 6 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	CH5_LOW_IRQ_EN Channel 5 Voltage Low Available Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	CH4_LOW_IRQ_EN Channel 4 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	CH3_LOW_IRQ_EN Channel 3 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_LOW_IRQ_EN Channel 2 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_LOW_IRQ_EN Channel 1 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_LOW_IRQ_EN Channel 0 Voltage Low Available Interrupt Enable 0: Disable 1: Enable

8.5.6.9 0x0024 GPADC Data High Interrupt Configure Register Description (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W	0x0	CH11_HIG_IRQ_EN Channel 11 Voltage High Available Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	CH10_HIG_IRQ_EN Channel 10 Voltage High Available Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	CH9_HIG_IRQ_EN Channel 9 Voltage High Available Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	CH8_HIG_IRQ_EN Channel 8 Voltage High Available Interrupt Enable 0: Disable 1: Enable
7	R/W	0x0	CH7_HIG_IRQ_EN Channel 7 Voltage High Available Interrupt Enable 0: Disable 1: Enable
6	R/W	0x0	CH6_HIG_IRQ_EN Channel 6 Voltage High Available Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	CH5_HIG_IRQ_EN Channel 5 Voltage High Available Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CH4_HIG_IRQ_EN Channel 4 Voltage High Available Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	CH3_HIG_IRQ_EN Channel 3 Voltage High Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_HIG_IRQ_EN Channel 2 Voltage High Available Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CH1_HIG_IRQ_EN Channel 1 Voltage High Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_HIG_IRQ_EN Channel 0 Voltage High Available Interrupt Enable 0: Disable 1: Enable

8.5.6.10 0x0028 GPADC DATA Interrupt Configure Register Description (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W	0x0	CH11_DATA_IRQ_EN Channel 11 Data Available Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	CH10_DATA_IRQ_EN Channel 10 Data Available Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	CH9_DATA_IRQ_EN Channel 9 Data Available Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	CH8_DATA_IRQ_EN Channel 8 Data Available Interrupt Enable 0: Disable 1: Enable
7	R/W	0x0	CH7_DATA_IRQ_EN Channel 7 Data Available Interrupt Enable 0: Disable 1: Enable
6	R/W	0x0	CH6_DATA_IRQ_EN Channel 6 Data Available Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	CH5_DATA_IRQ_EN Channel 5 Data Available Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CH4_DATA_IRQ_EN Channel 4 Data Available Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	CH3_DATA_IRQ_EN Channel 3 Data Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_DATA_IRQ_EN Channel 2 Data Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_DATA_IRQ_EN Channel 1 Data Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_DATA_IRQ_EN Channel 0 Data Available Interrupt Enable 0: Disable 1: Enable

8.5.6.11 0x0030 GPADC Data Low Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W1C	0x0	CH11_LOW_PENGDING Channel 11 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

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Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
10	R/W1C	0x0	CH10_LOW_PENGDING Channel 10 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
9	R/W1C	0x0	CH9_LOW_PENGDING Channel 9 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
8	R/W1C	0x0	CH8_LOW_PENGDING Channel 8 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
7	R/W1C	0x0	CH7_LOW_PENGDING Channel 7 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
6	R/W1C	0x0	CH6_LOW_PENGDING Channel 6 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
5	R/W1C	0x0	CH5_LOW_PENGDING Channel 5 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

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Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	CH4_LOW_PENGDING Channel 4 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
3	R/W1C	0x0	CH3_LOW_PENGDING Channel 3 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_LOW_PENGDING Channel 2 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_LOW_PENGDING Channel 1 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_LOW_PENGDING Channel 0 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

8.5.6.12 0x0034 GPADC Data High Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

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Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	CH11_HIG_PENGDING Channel 11 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 11 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
10	R/W1C	0x0	CH10_HIG_PENGDING Channel 10 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 10 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
9	R/W1C	0x0	CH9_HIG_PENGDING Channel 9 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 9 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
8	R/W1C	0x0	CH8_HIG_PENGDING Channel 8 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 8 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
7	R/W1C	0x0	CH7_HIG_PENGDING Channel 7 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 7 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
6	R/W1C	0x0	CH6_HIG_PENGDING Channel 6 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 6 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

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Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	CH5_HIG_PENGDING Channel 5 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 5 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
4	R/W1C	0x0	CH4_HIG_PENGDING Channel 4 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 4 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
3	R/W1C	0x0	CH3_HIG_PENGDING Channel 3 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_HIG_PENGDING Channel 2 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_HIG_PENGDING Channel 1 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_HIG_PENGDING Channel 0 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

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8.5.6.13 0x0038 GPADC Data Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W1C	0x0	CH11_DATA_PENGDING Channel 11 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 11 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
10	R/W1C	0x0	CH10_DATA_PENGDING Channel 10 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 10 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
9	R/W1C	0x0	CH9_DATA_PENGDING Channel 9 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 9 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
8	R/W1C	0x0	CH8_DATA_PENGDING Channel 8 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 8 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
7	R/W1C	0x0	CH7_DATA_PENGDING Channel 7 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 7 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
6	R/W1C	0x0	CH6_DATA_PENGDING Channel 6 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 6 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

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Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	CH5_DATA_PENGDING Channel 5 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 5 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
4	R/W1C	0x0	CH4_DATA_PENGDING Channel 4 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 4 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
3	R/W1C	0x0	CH3_DATA_PENGDING Channel 3 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_DATA_PENGDING Channel 2 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_DATA_PENGDING Channel 1 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_DATA_PENGDING Channel 0 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

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8.5.6.14 0x0040 GPADC CH0 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0040			Register Name: GP_CH0_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

8.5.6.15 0x0044 GPADC CH1 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0044			Register Name: GP_CH1_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

8.5.6.16 0x0048 GPADC CH2 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0048			Register Name: GP_CH2_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH2_CMP_HIG_DATA Channel 2 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH2_CMP_LOW_DATA Channel 2 Voltage Low Value

8.5.6.17 0x004C GPADC CH3 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x004C			Register Name: GP_CH3_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH3_CMP_HIG_DATA Channel 3 Voltage High Value
15:12	/	/	/

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Offset: 0x004C			Register Name: GP_CH3_CMP_DATA
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x400	CH3_CMP_LOW_DATA Channel 3 Voltage Low Value

8.5.6.18 0x0050 GPADC CH4 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0050			Register Name: GP_CH4_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH4_CMP_HIG_DATA Channel 4 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH4_CMP_LOW_DATA Channel 4 Voltage Low Value

8.5.6.19 0x0054 GPADC CH5 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0054			Register Name: GP_CH5_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH5_CMP_HIG_DATA Channel 5 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH5_CMP_LOW_DATA Channel 5 Voltage Low Value

8.5.6.20 0x0058 GPADC CH6 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0058			Register Name: GP_CH6_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH6_CMP_HIG_DATA Channel 6 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH6_CMP_LOW_DATA Channel 6 Voltage Low Value

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8.5.6.21 0x005C GPADC CH7 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x005C			Register Name: GP_CH7_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH7_CMP_HIG_DATA Channel 7 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH7_CMP_LOW_DATA Channel 7 Voltage Low Value

8.5.6.22 0x0060 GPADC CH8 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0060			Register Name: GP_CH8_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH8_CMP_HIG_DATA Channel 8 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH8_CMP_LOW_DATA Channel 8 Voltage Low Value

8.5.6.23 0x0064 GPADC CH9 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0064			Register Name: GP_CH9_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH9_CMP_HIG_DATA Channel 9 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH9_CMP_LOW_DATA Channel 9 Voltage Low Value

8.5.6.24 0x0068 GPADC CH10 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0068			Register Name: GP_CH10_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH10_CMP_HIG_DATA Channel 10 Voltage High Value
15:12	/	/	/

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Offset: 0x0068			Register Name: GP_CH10_CMP_DATA
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x400	CH10_CMP_LOW_DATA Channel 10 Voltage Low Value

8.5.6.25 0x006C GPADC CH11 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x006C			Register Name: GP_CH11_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH11_CMP_HIG_DATA Channel 11 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH11_CMP_LOW_DATA Channel 11 Voltage Low Value

8.5.6.26 0x0080 GPADC CH0 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GP_CH0_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

8.5.6.27 0x0084 GPADC CH1 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

8.5.6.28 0x0088 GPADC CH2 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: GP_CH2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH2_DATA Channel 2 Data

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8.5.6.29 0x008C GPADC CH3 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: GP_CH3_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH3_DATA Channel 3 Data

8.5.6.30 0x0090 GPADC CH4 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: GP_CH4_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH4_DATA Channel 4 Data

8.5.6.31 0x0094 GPADC CH5 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: GP_CH5_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH5_DATA Channel 5 Data

8.5.6.32 0x0098 GPADC CH6 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: GP_CH6_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH6_DATA Channel 6 Data

8.5.6.33 0x009C GPADC CH7 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: GP_CH7_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH7_DATA Channel 7 Data

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8.5.6.34 0x00A0 GPADC CH8 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: GP_CH8_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH8_DATA Channel 8 Data

8.5.6.35 0x00A4 GPADC CH9 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: GP_CH9_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH9_DATA Channel 9 Data

8.5.6.36 0x00A8 GPADC CH10 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: GP_CH10_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH10_DATA Channel 10 Data

8.5.6.37 0x00AC GPADC CH11 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: GP_CH11_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH11_DATA Channel 11 Data

8.5.6.38 0x00C0 GPADC Sampling Times0 Register Description (Default Value 0x0000_0000)

Offset: 0x00C0			Register Name: GP_SMP_TMS0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x00C0			Register Name: GP_SMP_TMS0
Bit	Read/Write	Default/Hex	Description
29:24	R/W	0x0	GP_ CH3_SMP_TMS GPADC Channel 3 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other:reserved
23：22	/	/	/
21:16	R/W	0x0	GP_ CH2_SMP_TMS GPADC Channel 2 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
15：14	/	/	/
13:8	R/W	0x0	GP_ CH1_SMP_TMS GPADC Channel 1 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
7:6	/	/	/
5:0	R/W	0x0	GP_ CH0_SMP_TMS GPADC Channel 0 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved

8.5.6.39 0x00C4 GPADC Sampling Times1 Source Select Register Description (Default Value 0x0000_0000)

Offset: 0x00C4			Register Name: GP_SMP_TMS1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x00C4			Register Name: GP_SMP_TMS1
Bit	Read/Write	Default/Hex	Description
29:24	R/W	0x0	GP_ CH7_SMP_TMS GPADC Channel 7 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
23：22	/	/	/
21:16	R/W	0x0	GP_ CH6_SMP_TMS GPADC Channel 6 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
15：14	/	/	/
13:8	R/W	0x0	GP_ CH5_SMP_TMS GPADC Channel 5 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
7:6	/	/	/
5:0	R/W	0x0	GP_ CH4_SMP_TMS GPADC Channel 4 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved

8.5.6.40 0x00C8 GPADC Sampling Times2 Source Select Register Description (Default Value 0x0000_0000)

Offset: 0x00C8			Register Name: GP_SMP_TMS2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x00C8			Register Name: GP_SMP_TMS2
Bit	Read/Write	Default/Hex	Description
29:24	R/W	0x0	GP_ CH11_SMP_TMS GPADC Channel 11 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
23：22	/	/	/
21:16	R/W	0x0	GP_ CH10_SMP_TMS GPADC Channel 10 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
15：14	/	/	/
13:8	R/W	0x0	GP_ CH9_SMP_TMS GPADC Channel 9 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
7:6	/	/	/
5:0	R/W	0x0	GP_ CH8_SMP_TMS GPADC Channel 8 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved

8.5.6.41 0x00D0 GPADC Channel Sample Rate Setting Bypass Register Description (Default Value 0x00D0 0x0000_0001)

Offset: 0x00D0			Register Name: GP_SMP_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x00D0			Register Name: GP_SMP_BYP
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	GP_ CH_SMP_BYP GPADC Channel Sample Rate Setting Bypass Register 0: Enable sampling rate setting 1: Disable sampling rate setting

8.5.6.42 0x00FC GPADC Reference Voltage Source Select Register Description (Default Value 0x0000_0001)

Offset: 0x00FC			Register Name: GP_RVLT_SEL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	GP_RVLT_SEL GPADC Reference Voltage Source Selector 0: External LDO 1: Internal LDO

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8.6 GPIO

8.6.1 Overview

The general purpose input/output (GPIO) is one of the blocks controlling the chip multiplexing pins. The T527 supports 12 groups of GPIO pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

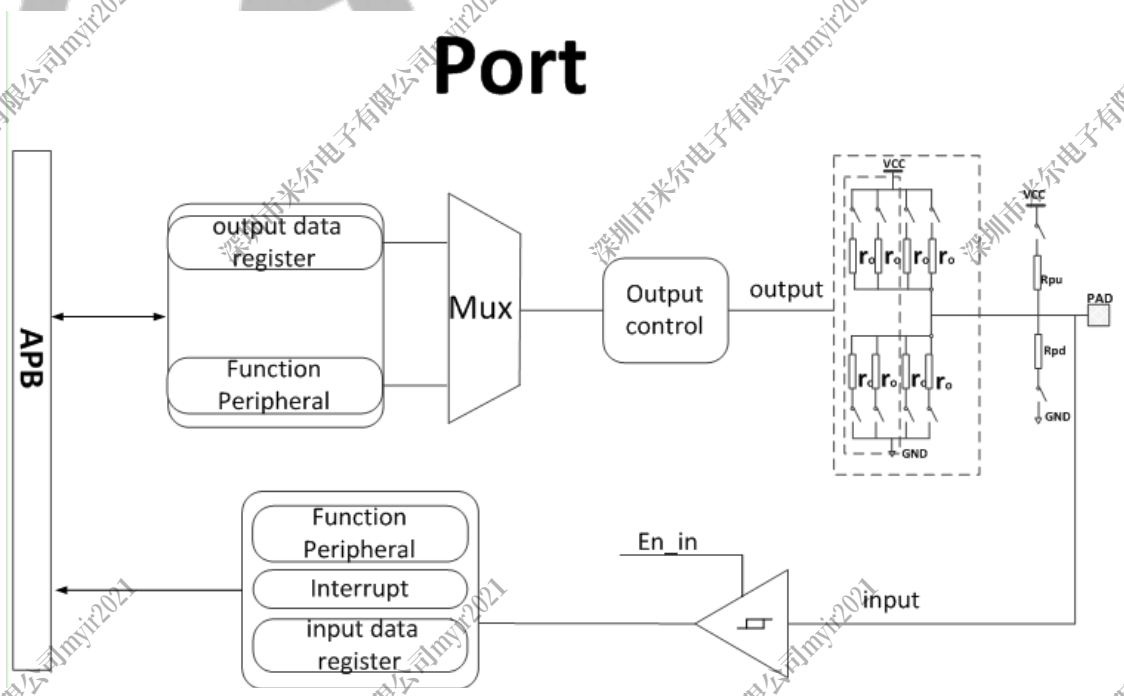
The GPIO has the following features:

- 12 groups of ports (PB, PC, PD, PE, PF, PG, PH, PI, PJ, PK, PL, PM)
- Software control for each signal pin
- Data input (capture)/output (drive)
- Each GPIO peripheral can produce an interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 203 interrupts
- Configurable interrupt edges

8.6.2 Block Diagram

The following figure shows the block diagram of the GPIO.

Figure 8-35 GPIO Block Diagram



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The GPIO consists of the digital part (GPIO, external interface) and IO analog part (output buffer, dual pull down, pad). The digital part can select the output interface by the MUX switch; the analog part can configure pull up/down and buffer strength.

When executing GPIO read state, the GPIO reads the current level of the pin into the internal register bus. When not executing GPIO read state, the external pin and the internal register bus are off-status, which is high-impedance.

8.6.3 Functional Description

8.6.3.1 Multi-function Port

The T527 includes 203 multi-functional input/output port pins. There are 12 ports as listed below.

Table 8-12 Multi-function Port

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Typical Power Supply
PB	15	Schmitt	CMOS	UART/TWI/ OWA/I2S/ SPI/JTAG/PWM/LCD/HDMI/CAN	3.3 V
PC	17	Schmitt	CMOS	NAND/SDC/SPI/SPIFC	3.3 V/1.8 V
PD	24	Schmitt	CMOS	LCD/PWM/LVDS/SPI/DSI/UART/PWM	3.3 V/1.8 V
PE	16	Schmitt	CMOS	MCSI/TWI/UART/PLL_LOCK_DBG /PWM/I2S/ SPI/LEDC/ LCD/NCSI	3.3 V/1.8 V
PF	7	Schmitt	CMOS	SDC /JTAG/UART/I2S	3.3 V/1.8 V
PG	15	Schmitt	CMOS	SDC/UART/PCIE/I2S	3.3 V/1.8 V
PH	20	Schmitt	CMOS	TWI/UART/DMIC/CIR/ SPI/I2S/LEDC/OWA/RGMII0/RMII0/PCIE	3.3 V
PI	17	Schmitt	CMOS	TWI/UART/SPI/IRRX/OWA/DMIC/PWM/I2S/CAN	3.3 V/1.8 V
PJ	28	Schmitt	CMOS	UART/TWI/SPI/RGMII1/RMII1	3.3 V/1.8 V
PK	24	Schmitt	CMOS	MCSI /TWI/UART/PWM/NCSI	3.3V/1.8 V
PL	14	Schmitt	CMOS	CIR/JTAG/TWI/UART/PWM /JTAG/I2S/DMIC/SPI	3.3 V/1.8 V
PM	6	Schmitt	CMOS	UARY/TWI/PWM/CIR/JTAG	3.3 V/1.8 V

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8.6.3.2 GPIO Multiplex Function

Table 8-13 to Table 8-24 show the multiplex function pins of the T527.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function7 to Function13 are reserved.

Table 8-13 PB Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PB0	I/O	UART2-TX	SPI2-CS0	JTAG-MS	LCD0-D0	PWM6	PB-EINT0
PB1	I/O	UART2-RX	SPI2-CLK	JTAG-CK	LCD0-D1	PWM7	PB-EINT1
PB2	I/O	UART2-RTS	SPI2-MOSI	JTAG-DO	LCD0-D8	CAN-TX0	PB-EINT2
PB3	I/O	UART2-CTS	SPI2-MISO	JTAG-DI	LCD0-D9	CAN-RX0	PB-EINT3
PB4	I/O	TWI1-SCK	I2S0-MCLK		PWM8	HDMI-SCL	PB-EINT4
PB5	I/O	TWI1-SDA	I2S0-BCLK		PWM9	HDMI-SDA	PB-EINT5
PB6	I/O		I2S0-LRCK		PWM10	HDMI-CEC	PB-EINT6
PB7	I/O	OWA-IN	I2S0-DOUT0	I2S0-DIN1	LCD0-D16	PWM11	PB-EINT7
PB8	I/O	OWA-OUT	I2S0-DIN0	I2S0-DOUT1	LCD0-D17	PWM0	PB-EINT8
PB9	I/O	UART0-TX	TWI0-SCK		I2S0-DIN2	I2S0-DOUT2	PB-EINT9
PB10	I/O	UART0-RX	TWI0-SDA	PWM1	I2S0-DIN3	I2S0-DOUT3	PB-EINT10
PB11	I/O	TWI5-SCK	UART7-RTS	SPI1-CS0	PWM2		PB-EINT11
PB12	I/O	TWI5-SDA	UART7-CTS	SPI1-CLK	PWM3		PB-EINT12
PB13	I/O	TWI4-SCK	UART7-TX	SPI1-MOSI	PWM4		PB-EINT13
PB14	I/O	TWI4-SDA	UART7-RX	SPI1-MISO	PWM5		PB-EINT14

Table 8-14 PC Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PC0	I/O	NAND-WE	SDC2-DS				PC-EINT0
PC1	I/O	NAND-ALE	SDC2-RST				PC-EINT1
PC2	I/O	NAND-CLE		SPI0-MOSI	SPIF-MOSI		PC-EINT2
PC3	I/O	NAND-CE1		SPI0-CS0	SPIF-CS0		PC-EINT3
PC4	I/O	NAND-CE0		SPI0-MISO	SPIF-MISO		PC-EINT4
PC5	I/O	NAND-RE	SDC2-CLK				PC-EINT5
PC6	I/O	NAND-RB0	SDC2-CMD				PC-EINT6
PC7	I/O	NAND-RB1		SPI0-CS1	SPIF-DQS		PC-EINT7
PC8	I/O	NAND-DQ7	SDC2-D3		SPIF-D7		PC-EINT8
PC9	I/O	NAND-DQ6	SDC2-D4		SPIF-D6		PC-EINT9
PC10	I/O	NAND-DQ5	SDC2-D0		SPIF-D5		PC-EINT10
PC11	I/O	NAND-DQ4	SDC2-D5		SPIF-D4		PC-EINT11
PC12	I/O	NAND-DQS		SPI0-CLK	SPIF-CLK		PC-EINT12
PC13	I/O	NAND-DQ3	SDC2-D1				PC-EINT13
PC14	I/O	NAND-DQ2	SDC2-D6				PC-EINT14
PC15	I/O	NAND-DQ1	SDC2-D2	SPI0-WP	SPIF-WP		PC-EINT15
PC16	I/O	NAND-DQ0	SDC2-D7	SPI0-HOLD	SPIF-HOLD		PC-EINT16

Table 8-15 PD Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PD0	I/O	LCD0-D2	LVDS0-D0P	DSI0-D0P	PWM0		PD-EINT0
PD1	I/O	LCD0-D3	LVDS0-D0N	DSI0-D0N	PWM1		PD-EINT1
PD2	I/O	LCD0-D4	LVDS0-D1P	DSI0-D1P	PWM2		PD-EINT2
PD3	I/O	LCD0-D5	LVDS0-D1N	DSI0-D1N	PWM3		PD-EINT3
PD4	I/O	LCD0-D6	LVDS0-D2P	DSI0-CKP	PWM4		PD-EINT4
PD5	I/O	LCD0-D7	LVDS0-D2N	DSI0-CKN	PWM5		PD-EINT5
PD6	I/O	LCD0-D10	LVDS0-CKP	DSI0-D2P	PWM6		PD-EINT6
PD7	I/O	LCD0-D11	LVDS0-CKN	DSI0-D2N	PWM7		PD-EINT7
PD8	I/O	LCD0-D12	LVDS0-D3P	DSI0-D3P	PWM8		PD-EINT8
PD9	I/O	LCD0-D13	LVDS0-D3N	DSI0-D3N	PWM9		PD-EINT9
PD10	I/O	LCD0-D14	LVDS1-D0P	DSI1-D0P	PWM10	SPI1-CS0/DBI-CSX	PD-EINT10
PD11	I/O	LCD0-D15	LVDS1-D0N	DSI1-D0N	PWM11	SPI1-CLK/DBI-SCLK	PD-EINT11
PD12	I/O	LCD0-D18	LVDS1-D1P	DSI1-D1P	PWM12	SPI1-MOSI/DBI-SDO	PD-EINT12

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Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PD13	I/O	LCD0-D19	LVDS1-D1N	DSI1-D1N	PWM13	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PD-EINT13
PD14	I/O	LCD0-D20	LVDS1-D2P	DSI1-CKP	PWM14	UART3-TX	PD-EINT14
PD15	I/O	LCD0-D21	LVDS1-D2N	DSI1-CKN	PWM15	UART3-RX	PD-EINT15
PD16	I/O	LCD0-D22	LVDS1-CKP	DSI1-D2P	PWM16	UART3-RTS	PD-EINT16
PD17	I/O	LCD0-D23	LVDS1-CKN	DSI1-D2N	PWM17	UART3-CTS	PD-EINT17
PD18	I/O	LCD0-CLK	LVDS1-D3P	DSI1-D3P	PWM18	UART4-TX	PD-EINT18
PD19	I/O	LCD0-DE	LVDS1-D3N	DSI1-D3N	PWM19	UART4-RX	PD-EINT19
PD20	I/O	LCD0-HSYNC	PWM2	UART2-TX	UART7-RTS	UART4-RTS	PD-EINT20
PD21	I/O	LCD0-VSYNC	PWM3	UART2-RX	UART7-CTS	UART4-CTS	PD-EINT21
PD22	I/O	PWM1	SPI1-HOLD/DBI-DCX/DBI-WRX	UART2-RTS	UART7-TX	TWI0-SCK	PD-EINT22
PD23	I/O	PWM0	SPI1-WP/DBI-TE	UART2-CTS	UART7-RX	TWI0-SDA	PD-EINT23

Table 8-16 PE Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PE0	I/O	MCSI0-MCLK					PE-EINT0
PE1	I/O	TWI2-SCK	UART4-TX				PE-EINT1
PE2	I/O	TWI2-SDA	UART4-RX				PE-EINT2
PE3	I/O	TWI3-SCK	UART4-RTS				PE-EINT3
PE4	I/O	TWI3-SDA	UART4-CTS				PE-EINT4
PE5	I/O	MCSI1-MCLK		I2S2-MCLK	LEDC		PE-EINT5
PE6	I/O			I2S2-BCLK	LCD0-TRIG	NCSI-D8	PE-EINT6
PE7	I/O			I2S2-LRCK	LCD1-TRIG	NCSI-D9	PE-EINT7
PE8	I/O			I2S2-DOUT0	LCD2-TRIG	NCSI-D10	PE-EINT8
PE9	I/O			I2S2-DIN0		NCSI-D11	PE-EINT9
PE10	I/O	MCSI3-MCLK	PWM3			NCSI-D12	PE-EINT10
PE11	I/O	TWI1-SCK	UART5-RTS	SPI2-CS0	UART6-TX	NCSI-D13	PE-EINT11
PE12	I/O	TWI1-SDA	UART5-CTS	SPI2-CLK	UART6-RX	NCSI-D14	PE-EINT12
PE13	I/O	TWI4-SCK	UART5-TX	SPI2-MOSI	UART6-RTS	CSI0-XVS-FSYNC	PE-EINT13
PE14	I/O	TWI4-SDA	UART5-RX	SPI2-MISO	UART6-CTS	CSI1-XVS-FSYNC	PE-EINT14
PE15	I/O	MCSI2-MCLK	PWM2			NCSI-D15	PE-EINT15

Table 8-17 PF Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PF0	I/O	SDC0-D1	JTAG-MS		I2S3-DIN0	I2S3-DOUT1	PF-EINT0
PF1	I/O	SDC0-D0	JTAG-DI		I2S3-DOUT0	I2S3-DIN1	PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX		I2S3-DIN2	I2S3-DOUT2	PF-EINT2
PF3	I/O	SDC0-CMD	JTAG-DO		I2S3-LRCK		PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX		I2S3-DIN3	I2S3-DOUT3	PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK		I2S3-BCLK		PF-EINT5
PF6	I/O				I2S3-MCLK		PF-EINT6

Table 8-18 PG Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PG0	I/O	SDC1-CLK					PG-EINT0
PG1	I/O	SDC1-CMD					PG-EINT1
PG2	I/O	SDC1-D0	PCIE0-PERSTN				PG-EINT2
PG3	I/O	SDC1-D1	PCIE0-WAKEN				PG-EINT3
PG4	I/O	SDC1-D2	PCIE0-CLKREQN				PG-EINT4
PG5	I/O	SDC1-D3					PG-EINT5
PG6	I/O	UART1-TX					PG-EINT6
PG7	I/O	UART1-RX					PG-EINT7
PG8	I/O	UART1-RTS					PG-EINT8
PG9	I/O	UART1-CTS					PG-EINT9
PG10	I/O		I2S1-MCLK				PG-EINT10
PG11	I/O		I2S1-BCLK				PG-EINT11
PG12	I/O		I2S1-LRCK				PG-EINT12
PG13	I/O		I2S1-DOUT0	I2S1-DIN1			PG-EINT13
PG14	I/O		I2S1-DIN0	I2S1-DOUT1			PG-EINT14

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Table 8-19 PH Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PH0	I/O	TWI0-SCK			RGMII0-RXD1/RMII0-RXD1		PH-EINT0
PH1	I/O	TWI0-SDA			RGMII0-RXD0/RMII0-RXD0		PH-EINT1
PH2	I/O	TWI1-SCK		I2S2-DIN3	RGMII0-RXCTL/RMII0-CRS-DV	I2S2-DOUT3	PH-EINT2
PH3	I/O	TWI1-SDA	IR-TX	I2S2-DIN2	RGMII0-CLKIN/RMII0-RXER	I2S2-DOUT2	PH-EINT3
PH4	I/O	UART3-TX	SPI1-CS0		RGMII0-TXD1/RMII0-TXD1		PH-EINT4
PH5	I/O	UART3-RX	SPI1-CLK	LEDC	RGMII0-TXD0/RMII0-TXD0		PH-EINT5
PH6	I/O	UART3-RTS	SPI1-MOSI	OWA-IN	RGMII0-TXCK/RMII0-TXCK		PH-EINT6
PH7	I/O	UART3-CTS	SPI1-MISO	OWA-OUT	RGMII0-TXCTL/RMII0-TXEN		PH-EINT7
PH8	I/O	DMIC-CLK	SPI2-CS0	I2S2-MCLK	I2S2-DIN2		PH-EINT8
PH9	I/O	DMIC-DATA0	SPI2-CLK	I2S2-BCLK	RGMII0-MDC		PH-EINT9
PH10	I/O	DMIC-DATA1	SPI2-MOSI	I2S2-LRCK	RGMII0-MDIO		PH-EINT10
PH11	I/O	DMIC-DATA2	SPI2-MISO	I2S2-DOUT0	I2S2-DIN1	PCIE0-PERSTN	PH-EINT11
PH12	I/O	DMIC-DATA3	TWI3-SCK	I2S2-DIN0	I2S2-DOUT1	PCIE0-WAKEN	PH-EINT12
PH13	I/O		TWI3-SDA	I2S3-MCLK	RGMII0-EPHY-25M		PH-EINT13
PH14	I/O			I2S3-BCLK	RGMII0-RXD3/RMII0-NULL		PH-EINT14
PH15	I/O			I2S3-LRCK	RGMII0-RXD2/RMII0-NULL		PH-EINT15
PH16	I/O		I2S3-DOUT0	I2S3-DIN1	RGMII0-RXCK/RMII0-NULL	CLK-FANOUT0	PH-EINT16
PH17	I/O		I2S3-DOUT1	I2S3-DIN0	RGMII0-TXD3/RMII0-NULL		PH-EINT17
PH18	I/O	IR-TX	I2S3-DOUT2	I2S3-DIN2	RGMII0-TXD2/RMII0-NULL		PH-EINT18
PH19	I/O	IR-RX	I2S3-DOUT3	I2S3-DIN3	LEDC	PCIE0-CLKREQN	PH-EINT19

Table 8-20 PI Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PI0	I/O	TWI4-SCK	UART4-TX	PWM1	I2S2-DIN3	I2S2-DOUT3	PI-EINT0
PI1	I/O	TWI4-SDA	UART4-RX	PWM2	I2S2-DIN2	I2S2-DOUT2	PI-EINT1
PI2	I/O	UART5-TX	SPI1-CS0	PWM3	I2S2-BCLK		PI-EINT2
PI3	I/O	UART5-RX	SPI1-CLK	PWM4	I2S2-LRCK		PI-EINT3
PI4	I/O	UART5-RTS	SPI1-MOSI	PWM5	I2S2-DOUT0	I2S2-DIN1	PI-EINT4
PI5	I/O	UART5-CTS	SPI1-MISO	PWM6	I2S2-DIN0	I2S2-DOUT1	PI-EINT5
PI6	I/O	UART6-TX	UART4-RTS	PWM7	SPI2-CS0		PI-EINT6
PI7	I/O	UART6-RX	UART4-CTS	PWM8	SPI2-CLK		PI-EINT7
PI8	I/O	TWI5-SCK	IR-RX	PWM9	SPI2-MOSI		PI-EINT8
PI9	I/O	TWI5-SDA	DMIC-DATA2	PWM10			PI-EINT9
PI10	I/O	OWA-OUT	DMIC-DATA1	PWM11	I2S2-MCLK		PI-EINT10
PI11	I/O	UART3-TX	DMIC-DATA0	PWM12			PI-EINT11
PI12	I/O	UART3-RX		PWM13	SPI2-MISO		PI-EINT12
PI13	I/O	UART6-CTS	DMIC-DATA3	PWM14	I2S2-MCLK		PI-EINT13
PI14	I/O	UART6-RTS	DMIC-CLK	PWM15			PI-EINT14
PI15	I/O	UART3-RTS	TWI2-SCK	PWM16	CAN-TX0		PI-EINT15
PI16	I/O	UART3-CTS	TWI2-SDA	PWM17	CAN-RX0		PI-EINT16

Table 8-21 PJ Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PJ0	I/O	LCD1-D0	LVDS2-D0P		RGMII1-RXD1/RMII1-RXD1		PJ-EINT0
PJ1	I/O	LCD1-D1	LVDS2-D0N		RGMII1-RXD0/RMII1-RXD0		PJ-EINT1
PJ2	I/O	LCD1-D2	LVDS2-D1P		RGMII1-RXCTL/RMII1-CRS-DV		PJ-EINT2
PJ3	I/O	LCD1-D3	LVDS2-D1N		RGMII1-CLKIN/RMII1-RXER		PJ-EINT3
PJ4	I/O	LCD1-D4	LVDS2-D2P		RGMII1-TXD1/RMII1-TXD1		PJ-EINT4
PJ5	I/O	LCD1-D5	LVDS2-D2N		RGMII1-TXD0/RMII1-TXD0		PJ-EINT5
PJ6	I/O	LCD1-D6	LVDS2-CKP		RGMII1-TXCK/RMII1-TXCK		PJ-EINT6
PJ7	I/O	LCD1-D7	LVDS2-CKN		RGMII1-TXCTL/RMII1-TXEN		PJ-EINT7
PJ8	I/O	LCD1-D8	LVDS2-D3P		RGMII1-MDC		PJ-EINT8
PJ9	I/O	LCD1-D9	LVDS2-D3N		RGMII1-MDIO		PJ-EINT9
PJ10	I/O	LCD1-D10	LVDS3-D0P		RGMII1-EPHY-25M		PJ-EINT10
PJ11	I/O	LCD1-D11	LVDS3-D0N		RGMII1-RXD3/RMII1-NULL		PJ-EINT11
PJ12	I/O	LCD1-D12	LVDS3-D1P		RGMII1-RXD2/RMII1-NULL		PJ-EINT12
PJ13	I/O	LCD1-D13	LVDS3-D1N		RGMII1-RXCK/RMII1-NULL		PJ-EINT13
PJ14	I/O	LCD1-D14	LVDS3-D2P		RGMII1-TXD3/RMII1-NULL		PJ-EINT14
PJ15	I/O	LCD1-D15	LVDS3-D2N		RGMII1-TXD2/RMII1-NULL		PJ-EINT15
PJ16	I/O	LCD1-D16	LVDS3-CKP				PJ-EINT16
PJ17	I/O	LCD1-D17	LVDS3-CKN				PJ-EINT17

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Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PJ18	I/O	LCD1-D18	LVDS3-D3P				PJ-EINT18
PJ19	I/O	LCD1-D19	LVDS3-D3N				PJ-EINT19
PJ20	I/O	LCD1-D20	UART2-TX	UART3-RTS	SPI0-CS0		PJ-EINT20
PJ21	I/O	LCD1-D21	UART2-RX	UART3-CTS	SPI0-CLK		PJ-EINT21
PJ22	I/O	LCD1-D22	UART2-RTS	UART3-TX	SPI0-MOSI		PJ-EINT22
PJ23	I/O	LCD1-D23	UART2-CTS	UART3-RX	SPI0-MISO		PJ-EINT23
PJ24	I/O	LCD1-CLK	TWI4-SCK	UART4-TX	SPI0-CS1		PJ-EINT24
PJ25	I/O	LCD1-DE	TWI4-SDA	UART4-RX	SPI0-WP		PJ-EINT25
PJ26	I/O	LCD1-HSYNC	TWI5-SCK	UART4-RTS	SPI0-HOLD		PJ-EINT26
PJ27	I/O	LCD1-VSYNC	TWI5-SDA	UART4-CTS			PJ-EINT27

Table 8-22 PK Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PK0	I/O	MCSIA-D0N					PK-EINT0
PK1	I/O	MCSIA-D0P					PK-EINT1
PK2	I/O	MCSIA-D1N					PK-EINT2
PK3	I/O	MCSIA-D1P					PK-EINT3
PK4	I/O	MCSIA-CKN	TWI2-SCK				PK-EINT4
PK5	I/O	MCSIA-CKP	TWI2-SDA				PK-EINT5
PK6	I/O	MCSIB-D0N					PK-EINT6
PK7	I/O	MCSIB-D0P					PK-EINT7
PK8	I/O	MCSIB-D1N					PK-EINT8
PK9	I/O	MCSIB-D1P					PK-EINT9
PK10	I/O	MCSIB-CKN	TWI3-SCK				PK-EINT10
PK11	I/O	MCSIB-CKP	TWI3-SDA				PK-EINT11
PK12	I/O	MCSIC-D0N	UART7-TX	TWI4-SCK	NCSI-PCLK		PK-EINT12
PK13	I/O	MCSIC-D0P	UART7-RX	TWI4-SDA	NCSI-MCLK		PK-EINT13
PK14	I/O	MCSIC-D1N	UART7-RTS	UART5-RTS	NCSI-HSYNC		PK-EINT14
PK15	I/O	MCSIC-D1P	UART7-CTS	UART5-CTS	NCSI-VSYNC		PK-EINT15
PK16	I/O	MCSIC-CKN	TWI5-SCK	UART5-TX	NCSI-D0		PK-EINT16
PK17	I/O	MCSIC-CKP	TWI5-SDA	UART5-RX	NCSI-D1		PK-EINT17
PK18	I/O	MCSID-D0N	MCSI0-MCLK	UART6-TX	NCSI-D2		PK-EINT18
PK19	I/O	MCSID-D0P	TWI2-SCK	UART6-RX	NCSI-D3		PK-EINT19
PK20	I/O	MCSID-D1N	TWI2-SDA	UART6-RTS	NCSI-D4		PK-EINT20
PK21	I/O	MCSID-D1P	MCSI1-MCLK	UART6-CTS	NCSI-D5		PK-EINT21
PK22	I/O	MCSID-CKN	TWI3-SCK	PWM6	NCSI-D6		PK-EINT22
PK23	I/O	MCSID-CKP	TWI3-SDA	PWM7	NCSI-D7		PK-EINT23

Table 8-23 PL Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PL0	I/O	S-TWI0-SCK					PL-EINT0
PL1	I/O	S-TWI0-SDA					PL-EINT1
PL2	I/O	S-UART0-TX	S-UART1-TX	S-PWM2			PL-EINT2
PL3	I/O	S-UART0-RX	S-UART1-RX	S-PWM3			PL-EINT3
PL4	I/O	S-JTAG-MS	S-CAN-TX0	S-PWM4	S-I2S0-BCLK		PL-EINT4
PL5	I/O	S-JTAG-CK	S-CAN-RX0	S-PWM5	S-I2S0-LRCK	S-DMIC-DATA3	PL-EINT5
PL6	I/O	S-JTAG-DO	S-PWM6	S-I2S0-DIN1	S-I2S0-DOUT0	S-DMIC-DATA2	PL-EINT6
PL7	I/O	S-JTAG-DI	S-PWM7	S-I2S0-DOUT1	S-I2S0-DIN0	S-DMIC-DATA1	PL-EINT7
PL8	I/O	S-TWI1-SCK		S-RJTAG-MS	S-I2S0-MCLK	S-DMIC-DATA0	PL-EINT8
PL9	I/O	S-TWI1-SDA		S-RJTAG-CK	S-PWM1	S-DMIC-CLK	PL-EINT9
PL10	I/O	S-PWM0		S-RJTAG-DO	S-DMIC-DATA0	S-SPI0-CS0	PL-EINT10
PL11	I/O	S-IR-RX		S-RJTAG-DI	S-DMIC-DATA1	S-SPI0-CLK	PL-EINT11
PL12	I/O	S-TWI2-SCK	S-PWM8	S-UART0-TX	S-DMIC-DATA2	S-SPI0-MOSI	PL-EINT12
PL13	I/O	S-TWI2-SDA	S-PWM9	S-UART0-RX	S-DMIC-DATA3	S-SPI0-MISO	PL-EINT13

Table 8-24 PM Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PM0	I/O	S-UART0-TX	S-UART1-TX	S-PWM2			PM-EINT0
PM1	I/O	S-UART0-RX	S-UART1-RX	S-PWM3			PM-EINT1
PM2	I/O	S-TWI1-SCK	S-RJTAG-MS	S-PWM6			PM-EINT2
PM3	I/O	S-TWI1-SDA	S-RJTAG-CK	S-PWM7			PM-EINT3
PM4	I/O	S-PWM8	S-RJTAG-DO	S-TWI2-SCK			PM-EINT4
PM5	I/O	S-IR-RX	S-RJTAG-DI	S-TWI2-SDA	S-PWM9		PM-EINT5

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8.6.3.3 Port Function

The Port Controller supports 120 GPIOs, every GPIO can configure as Input, Output, Function Peripheral, IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 8-25 Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/: non-configure, configuration is invalid

Y: configure

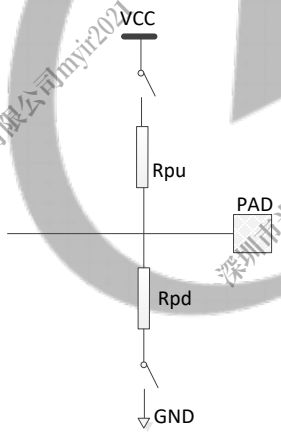
X: Select configuration according to the actual situation

N: Forbid to configure

8.6.3.4 Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

Figure 8-36 Pull up/down Logic



High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, the software configures the switch on Rpu and Rpd as off, and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by resistance, the resistance has a current-limiting function. When pulling up, the switch on Rpu is conducted by software configuration, the IO is pulled up to VCC by Rpu.

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Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is conducted by software configuration, the IO is pulled down to GND by Rpd.

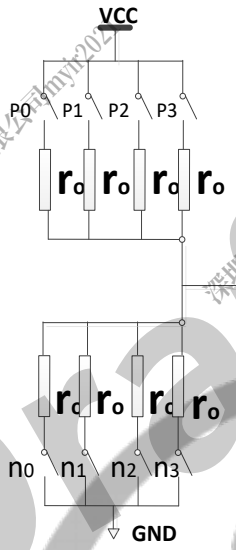
The pull-up/down of each IO is weak pull-up/down.

The setting of pull-down, pull-up, high-impedance is decided by the external circuit.

8.6.3.5 Buffer Strength

Each IO can be set as different buffer strength. The IO buffer diagram is as follows.

Figure 8-37 IO Buffer Strength Diagram



When output high level, the n0, n1, n2, n3 of NMOS is off, the p0, p1, p2, p3 of PMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the p0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the p0, p1, and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, the p0, p1, p2, and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0, p1, p2, p3 of PMOS is off, the n0, n1, n2, n3 of NMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the n0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the n0, n1, and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When the buffer strength is 3, the n0, n1, n2, and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between the output driver circuit and the port is unconnected, the driver configuration is invalid.

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8.6.3.6 Interrupt

Each group IO has an independent interrupt number. The IO within-group uses one interrupt number when one IO generates interrupt, the GPIO pins sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

The interrupt trigger of GPIO supports the following trigger types.

- Positive Edge: When a low level changes to a high level, the interrupt will generate. No matter how long a high level keeps, the interrupt generates only once.
- Negative Edge: When a high level changes to a low level, the interrupt will generate. No matter how long a low level keeps, the interrupt generates only once.
- High Level: Just keep a high level and the interrupt will always generate.
- Low Level: Just keep a low level and the interrupt will always generate.
- Double Edge: Positive and negative edge.

External Interrupt Configure Register is used to configure the trigger type.

The GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using a lower sample clock, to reach the debounce effect because the dither frequency of the signal is higher than the sample frequency.

Set the sample clock source by PIO_INT_CLK_SELECT and the prescale factor by DEB_CLK_PRE_SCALE.

8.6.4 Programming Guidelines

8.6.4.1 Disable

The steps to disable I/O pins are as follows:

Step 1 Write FFFF to the Px_SELECT bit of the Px_CFG register to disable the I/O pins.

Step 2 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins. In this case, the default status of I/O pins is logic-high.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins. In this case, the default status of I/O pins is logic-low.

8.6.4.2 Input

The steps to configure I/O pins as inputs are as follows:

Step 1 Write 0000 to the Px_SELECT bit of the Px_CFG register to enable input function.

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Step 2 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins.

Step 3 Configure the Px_DAT bit of the Px_DAT register to read the pin status.

- If the external input is driven, the value of the Px_DAT bit is the external input value.
- If the external input is not driven, the value of the Px_DAT bit is 1 when the I/O pins are pulled up and is 0 when pins are pulled down.

8.6.4.3 Output

The steps to configure I/O pins as outputs are as follows:

Step 1 Write 0001 to the Px_SELECT bit of the Px_CFG register to enable outputput function.

Step 2 If it is needed to set the buffer strength of the I/O pins, configure the Px_DRV bit of the Px_DRV register.

- When the Px_DRV bit is configured as 00, the buffer strength is the weakest.
- When the Px_DRV bit is configured as 11, the buffer strength is the strongest.
- The default value of the Px_DRV register is 01.

Step 3 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins.

Step 4 Configure the Px_DAT bit of the Px_DAT register to output 1 or 0 to the I/O pins.

- If output function is enabled, the pin status is the same as the corresponding bit.
- If output function is disabled, the value of the Px_DAT bit is 1 when the I/O pins are pulled up and is 0 when pins are pulled down.

8.6.4.4 Interrupt

The steps to configure I/O pins as interrupt pins are as follows:

Step 1 Write 1110 to the Px_SELECT bit of the Px_CFG register to enable interrupt function.

Step 2 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins. in this case, if external pins are not driven, the input level is high by default.

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- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins. In this case, if external pins are not driven, the input level is low by default.

Step 3 Configure the EINTx_CFG bit of Px_INT_CFG register to set the interrupt generation mode.

Step 4 Configure Px_INT_DEB regsiter to set debounce parameters including sample clock source and prescale factor.

Step 5 Write 1 to the EINTx_STATUS bit of the Px_INT_STA register to clear IRQ pending.

Step 6 Write 1 to the EINTx_CTL bit of the Px_INT_CTL register to enable interrupt.

Step 7 After an interrupt is processed, repeat Step5 to clrear IRQ pending and wait for next interrupt operation.

Step 8 Write 0 to the EINTx_CTL bit of the Px_INT_CTL register to disable interrupt function.

8.6.4.5 Multi Function

The steps to configure I/O pins as for function multiplexing are as follows:

Step 1 Configrue the Px_SELECT bit of the Px_CFG register to select the funciton needed.

Step 2 Configure the Px_DRV bit of the Px_DRV register to set buffer strength depending on the characteristic of the selected funciton.

Step 3 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins.
- If external pins are driven, the pin status is the same as the corresponding bit.
- If external pins are not driven, the value of the Px_DAT bit is 1 when the I/O pins are pulled up and 0 when pins are pulled down.

8.6.4.6 Power Configuation

Configuring Group Power Volatge

T527 only supports to set group power voltage in PF ports, which is able to be set as 3.3 V or 1.8V by configuring GPIO_POW_VAL_SET_CTL register. The group power voltage in other ports is un configurable and depended on the peripheral circuit.

Configuring Group Withstand Voltage

Configuring group withstand voltage intends to ensure that the internal withstand circuit voltage is consistent with group voltage. There are two modes, adaptive mode and manual mode, for users. In adaptive mode, the interl withstand circuit will adjust group withstand mode

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automatically depending on the detected GPIO voltage. The default mode is manual mode and it is recommended to choose manual mode in T527.

The following steps describe how to configure group withstand voltage.

- **Adptive Mode**

The following table shows the configuration for registers in adptive mode.

Bit	Register
Px_PWR_MOD_SEL bit = 0	GPIO_POW_MOD_SEL
VCC_Px_WS_VOL_MOD_SEL bit = 0	GPIO_POW_MS_CTL

- **Manual Mode (Recommended)**

Step 1 Before using GPIO, read GPIO_POW_VAL register to obtain current group voltage.

- If the current power supply is 1.8V, continue from Step2.
- If the current power supply is 3.3V, continue from Step4.

Step 2 Read the PB_PWR_VAL bit (bit [1]) of GPIO_POW_VAL register to obtain current group voltage.

Step 3 Configure withstand voltage.

The following table shows the corresponding withstand voltage for each group voltage and corresponding configuration register.

Group Voltage	Withstand Voltage	Bit	Register
1.8V	1.8V	Px_PWR_MOD_SEL bit = 0	GPIO_POW_MOD_SEL
		VCC_Px_WS_VOL_MOD_SEL bit = 1	GPIO_POW_MS_CTL
2.5V	3.3V	Px_PWR_MOD_SEL bit = 1	GPIO_POW_MOD_SEL
3.3V	3.3V	Px_PWR_MOD_SEL bit = 1	GPIO_POW_MOD_SEL

Step 4 After the I/O pins are power-on, repeat Step2 and Step3 to configure withstand voltage according to the actual group voltage.

Step 5 When adjusting group voltage during usage, follow the steps blow to configure withstand voltage.

- If the group voltage is to be switched from 1.8 V to 3.3 V, configure withstand voltage to 3.3 V before switching.
- If the group voltage is to be switched from 3.3 V to 1.8 V, configure withstand voltage to 1.8 V after switching.

8.6.5 Register List

There are two groups of registers for GPIO.

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Module Name	Base Address
GPIO	0x0200 0000
S_GPIO	0x0702 2000

8.6.5.1 GPIO Register List

Module Name	Base Address
GPIO	0x0200 0000

Register Name	Offset	Description
PB_CFG0	0x0030	PB Configure Register 0
PB_CFG1	0x0034	PB Configure Register 1
PB_CFG2	0x0038	PB Configure Register 2
PB_CFG3	0x003C	PB Configure Register 3
PB_DAT	0x0040	PB Data Register
PB_DRV0	0x0044	PB Multi_Driving Register 0
PB_DRV1	0x0048	PB Multi_Driving Register 1
PB_DRV2	0x004C	PB Multi_Driving Register 2
PB_DRV3	0x0050	PB Multi_Driving Register 3
PB_PUL0	0x0054	PB Pull Register 0
PB_PUL1	0x0058	PB Pull Register 1
PC_CFG0	0x0060	PC Configure Register 0
PC_CFG1	0x0064	PC Configure Register 1
PC_CFG2	0x0068	PC Configure Register 2
PC_CFG3	0x006C	PC Configure Register 3
PC_DAT	0x0070	PC Data Register
PC_DRV0	0x0074	PC Multi_Driving Register 0
PC_DRV1	0x0078	PC Multi_Driving Register 1
PC_DRV2	0x007C	PC Multi_Driving Register 2
PC_DRV3	0x0080	PC Multi_Driving Register 3
PC_PUL0	0x0084	PC Pull Register 0
PC_PUL1	0x0088	PC Pull Register 1
PD_CFG0	0x0090	PD Configure Register 0
PD_CFG1	0x0094	PD Configure Register 1
PD_CFG2	0x0098	PD Configure Register 2
PD_CFG3	0x009C	PD Configure Register 3
PD_DAT	0x00A0	PD Data Register
PD_DRV0	0x00A4	PD Multi_Driving Register 0
PD_DRV1	0x00A8	PD Multi_Driving Register 1
PD_DRV2	0x00AC	PD Multi_Driving Register 2
PD_DRV3	0x00B0	PD Multi_Driving Register 3

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Register Name	Offset	Description
PD_PUL0	0x00B4	PD Pull Register 0
PD_PUL1	0x00B8	PD Pull Register 1
PE_CFG0	0x00C0	PE Configure Register 0
PE_CFG1	0x00C4	PE Configure Register 1
PE_CFG2	0x00C8	PE Configure Register 2
PE_CFG3	0x00CC	PE Configure Register 3
PE_DAT	0x00D0	PE Data Register
PE_DRV0	0x00D4	PE Multi_Driving Register 0
PE_DRV1	0x00D8	PE Multi_Driving Register 1
PE_DRV2	0x00DC	PE Multi_Driving Register 2
PE_DRV3	0x00E0	PE Multi_Driving Register 3
PE_PUL0	0x00E4	PE Pull Register 0
PE_PUL1	0x00E8	PE Pull Register 1
PF_CFG0	0x00F0	PF Configure Register 0
PF_CFG1	0x00F4	PF Configure Register 1
PF_CFG2	0x00F8	PF Configure Register 2
PF_CFG3	0x00FC	PF Configure Register 3
PF_DAT	0x0100	PF Data Register
PF_DRV0	0x0104	PF Multi_Driving Register 0
PF_DRV1	0x0108	PF Multi_Driving Register 1
PF_DRV2	0x010C	PF Multi_Driving Register 2
PF_DRV3	0x0110	PF Multi_Driving Register 3
PF_PUL0	0x0114	PF Pull Register 0
PF_PUL1	0x0118	PF Pull Register 1
PG_CFG0	0x0120	PG Configure Register 0
PG_CFG1	0x0124	PG Configure Register 1
PG_CFG2	0x0128	PG Configure Register 2
PG_CFG3	0x012C	PG Configure Register 3
PG_DAT	0x0130	PG Data Register
PG_DRV0	0x0134	PG Multi_Driving Register 0
PG_DRV1	0x0138	PG Multi_Driving Register 1
PG_DRV2	0x013C	PG Multi_Driving Register 2
PG_DRV3	0x0140	PG Multi_Driving Register 3
PG_PUL0	0x0144	PG Pull Register 0
PG_PUL1	0x0148	PG Pull Register 1
PH_CFG0	0x0150	PH Configure Register 0
PH_CFG1	0x0154	PH Configure Register 1
PH_CFG2	0x0158	PH Configure Register 2
PH_CFG3	0x015C	PH Configure Register 3
PH_DAT	0x0160	PH Data Register
PH_DRV0	0x0164	PH Multi_Driving Register 0
PH_DRV1	0x0168	PH Multi_Driving Register 1

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Register Name	Offset	Description
PH_DRV2	0x016C	PH Multi_Driving Register 2
PH_DRV3	0x0170	PH Multi_Driving Register 3
PH_PUL0	0x0174	PH Pull Register 0
PH_PUL1	0x0178	PH Pull Register 1
PI_CFG0	0x0180	PI Configure Register 0
PI_CFG1	0x0184	PI Configure Register 1
PI_CFG2	0x0188	PI Configure Register 2
PI_CFG3	0x018C	PI Configure Register 3
PI_DAT	0x0190	PI Data Register
PI_DRV0	0x0194	PI Multi_Driving Register 0
PI_DRV1	0x0198	PI Multi_Driving Register 1
PI_DRV2	0x019C	PI Multi_Driving Register 2
PI_DRV3	0x01A0	PI Multi_Driving Register 3
PI_PUL0	0x01A4	PI Pull Register 0
PI_PUL1	0x01A8	PI Pull Register 1
PJ_CFG0	0x01B0	PJ Configure Register 0
PJ_CFG1	0x01B4	PJ Configure Register 1
PJ_CFG2	0x01B8	PJ Configure Register 2
PJ_CFG3	0x01BC	PJ Configure Register 3
PJ_DAT	0x01C0	PJ Data Register
PJ_DRV0	0x01C4	PJ Multi_Driving Register 0
PJ_DRV1	0x01C8	PJ Multi_Driving Register 1
PJ_DRV2	0x01CC	PJ Multi_Driving Register 2
PJ_DRV3	0x01D0	PJ Multi_Driving Register 3
PJ_PUL0	0x01D4	PJ Pull Register 0
PJ_PUL1	0x01D8	PJ Pull Register 1
PK_CFG0	0x0500	PK Configure Register 0
PK_CFG1	0x0504	PK Configure Register 1
PK_CFG2	0x0508	PK Configure Register 2
PK_CFG3	0x050C	PK Configure Register 3
PK_DAT	0x0510	PK Data Register
PK_DRV0	0x0514	PK Multi_Driving Register 0
PK_DRV1	0x0518	PK Multi_Driving Register 1
PK_DRV2	0x051C	PK Multi_Driving Register 2
PK_DRV3	0x0520	PK Multi_Driving Register 3
PK_PUL0	0x0524	PK Pull Register 0
PK_PUL1	0x0528	PK Pull Register 1
PB_INT_CFG0	0x0220	PB External Interrupt Configure Register 0
PB_INT_CFG1	0x0224	PB External Interrupt Configure Register 1
PB_INT_CFG2	0x0228	PB External Interrupt Configure Register 2
PB_INT_CFG3	0x022C	PB External Interrupt Configure Register 3
PB_INT_CTL	0x0230	PB External Interrupt Control Register

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Register Name	Offset	Description
PB_INT_STA	0x0234	PB External Interrupt Status Register
PB_INT_DEB	0x0238	PB External Debounce Configure Register
PC_INT_CFG0	0x0240	PC External Interrupt Configure Register 0
PC_INT_CFG1	0x0244	PC External Interrupt Configure Register 1
PC_INT_CFG2	0x0248	PC External Interrupt Configure Register 2
PC_INT_CFG3	0x024C	PC External Interrupt Configure Register 3
PC_INT_CTL	0x0250	PC External Interrupt Control Register
PC_INT_STA	0x0254	PC External Interrupt Status Register
PC_INT_DEB	0x0258	PC External Debounce Configure Register
PD_INT_CFG0	0x0260	PD External Interrupt Configure Register 0
PD_INT_CFG1	0x0264	PD External Interrupt Configure Register 1
PD_INT_CFG2	0x0268	PD External Interrupt Configure Register 2
PD_INT_CFG3	0x026C	PD External Interrupt Configure Register 3
PD_INT_CTL	0x0270	PD External Interrupt Control Register
PD_INT_STA	0x0274	PD External Interrupt Status Register
PD_INT_DEB	0x0278	PD External Debounce Configure Register
PE_INT_CFG0	0x0280	PE External Interrupt Configure Register 0
PE_INT_CFG1	0x0284	PE External Interrupt Configure Register 1
PE_INT_CFG2	0x0288	PE External Interrupt Configure Register 2
PE_INT_CFG3	0x028C	PE External Interrupt Configure Register 3
PE_INT_CTL	0x0290	PE External Interrupt Control Register
PE_INT_STA	0x0294	PE External Interrupt Status Register
PE_INT_DEB	0x0298	PE External Debounce Configure Register
PF_INT_CFG0	0x02A0	PF External Interrupt Configure Register 0
PF_INT_CFG1	0x02A4	PF External Interrupt Configure Register 1
PF_INT_CFG2	0x02A8	PF External Interrupt Configure Register 2
PF_INT_CFG3	0x02AC	PF External Interrupt Configure Register 3
PF_INT_CTL	0x02B0	PF External Interrupt Control Register
PF_INT_STA	0x02B4	PF External Interrupt Status Register
PF_INT_DEB	0x02B8	PF External Debounce Configure Register
PG_INT_CFG0	0x02C0	PG External Interrupt Configure Register 0
PG_INT_CFG1	0x02C4	PG External Interrupt Configure Register 1
PG_INT_CFG2	0x02C8	PG External Interrupt Configure Register 2
PG_INT_CFG3	0x02CC	PG External Interrupt Configure Register 3
PG_INT_CTL	0x02D0	PG External Interrupt Control Register
PG_INT_STA	0x02D4	PG External Interrupt Status Register
PG_INT_DEB	0x02D8	PG External Debounce Configure Register
PH_INT_CFG0	0x02E0	PH External Interrupt Configure Register 0
PH_INT_CFG1	0x02E4	PH External Interrupt Configure Register 1
PH_INT_CFG2	0x02E8	PH External Interrupt Configure Register 2
PH_INT_CFG3	0x02EC	PH External Interrupt Configure Register 3
PH_INT_CTL	0x02F0	PH External Interrupt Control Register

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Register Name	Offset	Description
PH_INT_STA	0x02F4	PH External Interrupt Status Register
PH_INT_DEB	0x02F8	PH External Debounce Configure Register
PI_INT_CFG0	0x0300	PI External Interrupt Configure Register 0
PI_INT_CFG1	0x0304	PI External Interrupt Configure Register 1
PI_INT_CFG2	0x0308	PI External Interrupt Configure Register 2
PI_INT_CFG3	0x030C	PI External Interrupt Configure Register 3
PI_INT_CTL	0x0310	PI External Interrupt Control Register
PI_INT_STA	0x0314	PI External Interrupt Status Register
PI_INT_DEB	0x0318	PI External Debounce Configure Register
PJ_INT_CFG0	0x0320	PJ External Interrupt Configure Register 0
PJ_INT_CFG1	0x0324	PJ External Interrupt Configure Register 1
PJ_INT_CFG2	0x0328	PJ External Interrupt Configure Register 2
PJ_INT_CFG3	0x032C	PJ External Interrupt Configure Register 3
PJ_INT_CTL	0x0330	PJ External Interrupt Control Register
PJ_INT_STA	0x0334	PJ External Interrupt Status Register
PK_INT_CFG0	0x0340	PK External Interrupt Configure Register 0
PK_INT_CFG1	0x0344	PK External Interrupt Configure Register 1
PK_INT_CFG2	0x0348	PK External Interrupt Configure Register 2
PK_INT_CFG3	0x034C	PK External Interrupt Configure Register 3
PK_INT_CTL	0x0350	PK External Interrupt Control Register
PK_INT_STA	0x0354	PK External Interrupt Status Register
PK_INT_DEB	0x0358	PK External Debounce Configure Register
GPIO_POW_MOD_SEL	0x0380	GPIO Group Withstand Voltage Mode Select Register
GPIO_POW_MS_CTL	0x0384	GPIO Group Withstand Voltage Mode Select Control Register
GPIO_POW_VAL	0x0388	GPIO Group Power Value Register
GPIO_POW_VAL_SET_CTL	0x0390	GPIO Group Power Voltage Select Control Register

8.6.5.2 S_GPIO Register List

Module Name	Base Address
S_GPIO	0x0702 2000

Register Name	Offset	Description
PL_CFG0	0x0000	PL Configure Register 0
PL_CFG1	0x0004	PL Configure Register 1
PL_CFG2	0x0008	PL Configure Register 2
PL_CFG3	0x000C	PL Configure Register 3
PL_DAT	0x0010	PL Data Register
PL_DRV0	0x0014	PL Multi_Driving Register 0

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Register Name	Offset	Description
PL_DRV1	0x0018	PL Multi_Driving Register 1
PL_DRV2	0x001C	PL Multi_Driving Register 2
PL_DRV3	0x0020	PL Multi_Driving Register 3
PL_PUL0	0x0024	PL Pull Register 0
PL_PUL1	0x0028	PL Pull Register 1
PM_CFG0	0x0030	PM Configure Register 0
PM_CFG1	0x0034	PM Configure Register 1
PM_CFG2	0x0038	PM Configure Register 2
PM_CFG3	0x003C	PM Configure Register 3
PM_DAT	0x0040	PM Data Register
PM_DRV0	0x0044	PM Multi_Driving Register 0
PM_DRV1	0x0048	PM Multi_Driving Register 1
PM_DRV2	0x004C	PM Multi_Driving Register 2
PM_DRV3	0x0050	PM Multi_Driving Register 3
PM_PUL0	0x0054	PM Pull Register 0
PM_PUL1	0x0058	PM Pull Register 1
PL_INT_CFG0	0x0200	PL External Interrupt Configure Register 0
PL_INT_CFG1	0x0204	PL External Interrupt Configure Register 1
PL_INT_CFG2	0x0208	PL External Interrupt Configure Register 2
PL_INT_CFG3	0x020C	PL External Interrupt Configure Register 3
PL_INT_CTL	0x0210	PL External Interrupt Control Register
PL_INT_STA	0x0214	PL External Interrupt Status Register
PL_INT_DEB	0x0218	PL External Debounce Configure Register
PM_INT_CFG0	0x0220	PM External Interrupt Configure Register 0
PM_INT_CFG1	0x0224	PM External Interrupt Configure Register 1
PM_INT_CFG2	0x0228	PM External Interrupt Configure Register 2
PM_INT_CFG3	0x022C	PM External Interrupt Configure Register 3
PM_INT_CTL	0x0230	PM External Interrupt Control Register
PM_INT_STA	0x0234	PM External Interrupt Status Register
PM_INT_DEB	0x0238	PM External Debounce Configure Register
GPIO_POW_MOD_SEL	0x0340	GPIO Group Withstand Voltage Mode Select Register
GPIO_POW_MS_CTL	0x0344	GPIO Group Withstand Voltage Mode Select Control Register
GPIO_POW_VAL	0x0348	GPIO Group Power Value Register
GPIO_POW_VAL_SET_CTL	0x0350	GPIO Group Power Voltage Select Control Register

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8.6.6 GPIO Register Description

8.6.6.1 0x0030 PB Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0030			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PB7_SELECT PB7 Select 0000: Input 0001: Output 0010: OWA-IN 0011: I2S0-DOUT0 0100: I2S0-DIN1 0101: LCD0-D16 0110: PWM11 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT7 1111: IO Disable
27:24	R/W	0xF	PB6_SELECT PB6 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S0-LRCK 0100: Reserved 0101: PWM10 0110: HDMI-CEC 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT6 1111: IO Disable
23:20	R/W	0xF	PB5_SELECT PB5 Select 0000: Input 0001: Output 0010: TWI1-SDA 0011: I2S0-BCLK 0100: Reserved 0101: PWM9 0110: HDMI-SDA 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT5 1111: IO Disable

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Offset: 0x0030			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PB4_SELECT PB4 Select 0000: Input 0001: Output 0010: TWI1-SCK 0011: I2S0-MCLK 0100: Reserved 0101: PWM8 0110: HDMI-SCL 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT4 1111: IO Disable
15:12	R/W	0xF	PB3_SELECT PB3 Select 0000: Input 0001: Output 0010: UART2-CTS 0011: SPI2-MISO 0100: JTAG-DI 0101: LCD0-D9 0110: CAN-RX0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT3 1111: IO Disable
11:8	R/W	0xF	PB2_SELECT PB2 Select 0000: Input 0001: Output 0010: UART2-RTS 0011: SPI2-MOSI 0100: JTAG-DO 0101: LCD0-D8 0110: CAN-TX0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT2 1111: IO Disable
7:4	R/W	0xF	PB1_SELECT PB1 Select 0000: Input 0001: Output 0010: UART2-RX 0011: SPI2-CLK 0100: JTAG-CK 0101: LCD0-D1 0110: PWM7 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT1 1111: IO Disable

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Offset: 0x0030			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PB0_SELECT PB0 Select 0000: Input 0001: Output 0010: UART2-TX 0011: SPI2-CS 0100: JTAG-MS 0101: LCD0-D0 0110: PWM6 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT0 1111: IO Disable

8.6.6.2 0x0034 PB Configure Register 1 (Default Value: 0x0FFF_FFFF)

Offset: 0x0034			Register Name: PB_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	PB14_SELECT PB14 Select 0000: Input 0001: Output 0010: TWI4-SDA 0011: UART7-RX 0100: SPI1-MISO 0101: PWM5 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT14 1111: IO Disable
23:20	R/W	0xF	PB13_SELECT PB13 Select 0000: Input 0001: Output 0010: TWI4-SCK 0011: UART7-TX 0100: SPI1-MOSI 0101: PWM4 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT13 1111: IO Disable

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Offset: 0x0034			Register Name: PB_CFG1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PB12_SELECT PB12 Select 0000: Input 0001: Output 0010: TWI5-SDA 0011: UART7-CTS 0100: SPI1-CLK 0101: PWM3 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT12 1111: IO Disable
15:12	R/W	0xF	PB11_SELECT PB11 Select 0000: Input 0001: Output 0010: TWI5-SCK 0011: UART7-RTS 0100: SPI1-CS0 0101: PWM2 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT11 1111: IO Disable
11:8	R/W	0xF	PB10_SELECT PB10 Select 0000: Input 0001: Output 0010: UART0-RX 0011: TWI0-SDA 0100: PWM1 0101: I2S0-DIN3 0110: I2S0-DOUT3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT10 1111: IO Disable
7:4	R/W	0xF	PB9_SELECT PB9 Select 0000: Input 0001: Output 0010: UART0-TX 0011: TWI0-SCK 0100: Reserved 0101: I2S0-DIN2 0110: I2S0-DOUT2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT9 1111: IO Disable

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Offset: 0x0034			Register Name: PB_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PB8_SELECT PB8 Select 0000: Input 0001: Output 0010: OWA-OUT 0011: I2S0-DIN0 0100: I2S0-DOUT1 0101: LCD0-D17 0110: PWM0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT8 1111: IO Disable

8.6.6.3 0x0038 PB Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PB_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.4 0x003C PB Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PB_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.5 0x0040 PB Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PB_DAT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	0	PB_DAT PB Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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8.6.6.6 0x0044 PB Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0044			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PB7_DRV PB7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PB6_DRV PB6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PB5_DRV PB5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PB4_DRV PB4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PB3_DRV PB3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PB2_DRV PB2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PB1_DRV PB1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/

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Offset: 0x0044			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	PB0_DRV PB0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.7 0x0048 PB Multi_Driving Register 1 (Default Value: 0x0111_1111)

Offset: 0x0048			Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PB14_DRV PB14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PB13_DRV PB13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PB12_DRV PB12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PB11_DRV PB11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PB10_DRV PB10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PB9_DRV PB9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/

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Offset: 0x0048			Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	PB8_DRV PB8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.8 0x004C PB Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: PB_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.9 0x0050 PB Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: PB_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.10 0x0054 PB Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PB14_PULL PB14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PB13_PULL PB13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PB12_PULL PB12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PB11_PULL PB11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0054			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	PB10_PULL PB10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PB9_PULL PB9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PB8_PULL PB8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PB7_PULL PB7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PB6_PULL PB6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PB5_PULL PB5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PB4_PULL PB4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PB3_PULL PB3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PB2_PULL PB2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PB1_PULL PB1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0054			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PB0_PULL PB0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.11 0x0058 PB Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PB_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.12 0x0060 PC Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0060			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PC7_SELECT PC7 Select 0000: Input 0001: Output 0010: NAND-RB1 0011: Reserved 0100: SPI0-CS1 0101: SPIF-DQS 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT7 1111: IO Disable
27:24	R/W	0xF	PC6_SELECT PC6 Select 0000: Input 0001: Output 0010: NAND-RB0 0011: SDC2-CMD 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT6 1111: IO Disable

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Offset: 0x0060			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PC5_SELECT PC5 Select 0000: Input 0001: Output 0010: NAND-RE 0011: SDC2-CLK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT5 1111: IO Disable
19:16	R/W	0xF	PC4_SELECT PC4 Select 0000: Input 0001: Output 0010: NAND-CE0 0011: Reserved 0100: SPI0-MISO 0101: SPIF-MISO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT4 1111: IO Disable
15:12	R/W	0xF	PC3_SELECT PC3 Select 0000: Input 0001: Output 0010: NAND-CE1 0011: Reserved 0100: SPI0-CS0 0101: SPIF-CS0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT3 1111: IO Disable
11:8	R/W	0xF	PC2_SELECT PC2 Select 0000: Input 0001: Output 0010: NAND-CLE 0011: Reserved 0100: SPI0-MOSI 0101: SPIF-MOSI 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT2 1111: IO Disable

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Offset: 0x0060			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PC1_SELECT PC1 Select 0000: Input 0001: Output 0010: NAND-ALE 0011: SDC2-RST 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT1 1111: IO Disable
3:0	R/W	0xF	PC0_SELECT PC0 Select 0000: Input 0001: Output 0010: NAND-WE 0011: SDC2-DS 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT0 1111: IO Disable

8.6.6.13 0x0064 PC Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0064			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PC15_SELECT PC15 Select 0000: Input 0001: Output 0010: NAND-DQ1 0011: SDC2-D2 0100: SPI0-WP 0101: SPIF-WP 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT15 1111: IO Disable

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Offset: 0x0064			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PC14_SELECT PC14 Select 0000: Input 0001: Output 0010: NAND-DQ2 0011: SDC2-D6 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT14 1111: IO Disable
23:20	R/W	0xF	PC13_SELECT PC13 Select 0000: Input 0001: Output 0010: NAND-DQ3 0011: SDC2-D1 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT13 1111: IO Disable
19:16	R/W	0xF	PC12_SELECT PC12 Select 0000: Input 0001: Output 0010: NAND-DQS 0011: Reserved 0100: SPI0-CLK 0101: SPIF-CLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT12 1111: IO Disable
15:12	R/W	0xF	PC11_SELECT PC11 Select 0000: Input 0001: Output 0010: NAND-DQ4 0011: SDC2-D5 0100: Reserved 0101: SPIF-D4 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT11 1111: IO Disable

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Offset: 0x0064			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PC10_SELECT PC10 Select 0000: Input 0001: Output 0010: NAND-DQ5 0011: SDC2-D0 0100: Reserved 0101: SPIF-D5 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT10 1111: IO Disable
7:4	R/W	0xF	PC9_SELECT PC9 Select 0000: Input 0001: Output 0010: NAND-DQ6 0011: SDC2-D4 0100: Reserved 0101: SPIF-D6 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT9 1111: IO Disable
3:0	R/W	0xF	PC8_SELECT PC8 Select 0000: Input 0001: Output 0010: NAND-DQ7 0011: SDC2-D3 0100: Reserved 0101: SPIF-D7 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT8 1111: IO Disable

8.6.6.14 0x0068 PC Configure Register 2 (Default Value: 0x0000_000F)

Offset: 0x0068			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0068			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PC16_SELECT PC16 Select 0000: Input 0001: Output 0010: NAND-DQ0 0011: SDC2-D7 0100: SPI0-HOLD 0101: SPIF-HOLD 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT16 1111: IO Disable

8.6.6.15 0x006C PC Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: PC_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.16 0x0070 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PC_DAT
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:0	R/W	0	PC_DAT PC Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.17 0x0074 PC Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0074			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x0074			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x1	PC7_DRV PC7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PC6_DRV PC6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PC5_DRV PC5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC4_DRV PC4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC3_DRV PC3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC2_DRV PC2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC1_DRV PC1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PC0_DRV PC0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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8.6.6.18 0x0078 PC Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0078			Register Name: PC_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PC15_DRV PC15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PC14_DRV PC14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PC13_DRV PC13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC12_DRV PC12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC11_DRV PC11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC10_DRV PC10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC9_DRV PC9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/

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Offset: 0x0078			Register Name: PC_DRV1
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	PC8_DRV PC8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.19 0x007C PC Multi_Driving Register 2 (Default Value: 0x0000_0001)

Offset: 0x007C			Register Name: PC_DRV2
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	PC16_DRV PC16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.20 0x0080 PC Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PC_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.21 0x0084 PC Pull Register 0 (Default Value: 0x0000_5140)

Offset: 0x0084			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PC15_PULL PC15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PC14_PULL PC14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PC13_PULL PC13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0084			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	PC12_PULL PC12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PC11_PULL PC11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x1	PC7_PULL PC7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x1	PC6_PULL PC6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PC5_PULL PC5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x1	PC4_PULL PC4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0084			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x0	PC2_PULL PC2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.22 0x0088 PC Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PC_PUL1
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PC16_PULL PC16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.23 0x0090 PD Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0090			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD7_SELECT PD7 Select 0000: Input 0001: Output 0010: LCD0-D11 0011: LVDS0-CKN 0100: DSI0-D2N 0101: PWM7 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT7 1111: IO Disable

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Offset: 0x0090			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PD6_SELECT PD6 Select 0000: Input 0001: Output 0010: LCD0-D10 0011: LVDS0-CKP 0100: DSI0-D2P 0101: PWM6 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT6 1111: IO Disable
23:20	R/W	0xF	PD5_SELECT PD5 Select 0000: Input 0001: Output 0010: LCD0-D7 0011: LVDS0-D2N 0100: DSI0-CKN 0101: PWM5 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT5 1111: IO Disable
19:16	R/W	0xF	PD4_SELECT PD4 Select 0000: Input 0001: Output 0010: LCD0-D6 0011: LVDS0-D2P 0100: DSI0-CKP 0101: PWM4 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT4 1111: IO Disable
15:12	R/W	0xF	PD3_SELECT PD3 Select 0000: Input 0001: Output 0010: LCD0-D5 0011: LVDS0-D1N 0100: DSI0-D1N 0101: PWM3 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT3 1111: IO Disable

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Offset: 0x0090			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PD2_SELECT PD2 Select 0000: Input 0001: Output 0010: LCD0-D4 0011: LVDS0-D1P 0100: DSI0-D1P 0101: PWM2 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT2 1111: IO Disable
7:4	R/W	0xF	PD1_SELECT PD1 Select 0000: Input 0001: Output 0010: LCD0-D3 0011: LVDS0-D0N 0100: DSI0-D0N 0101: PWM1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT1 1111: IO Disable
3:0	R/W	0xF	PD0_SELECT PD0 Select 0000: Input 0001: Output 0010: LCD0-D2 0011: LVDS0-D0P 0100: DSI0-D0P 0101: PWM0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT0 1111: IO Disable

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8.6.6.24 0x0094 PD Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0094			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD15_SELECT PD15 Select 0000: Input 0001: Output 0010: LCD0-D21 0011: LVDS1-D2N 0100: DSI1-CKN 0101: PWM15 0110: UART3-RX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT15 1111: IO Disable
27:24	R/W	0xF	PD14_SELECT PD14 Select 0000: Input 0001: Output 0010: LCD0-D20 0011: LVDS1-D2P 0100: DSI1-CKP 0101: PWM14 0110: UART3-TX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT14 1111: IO Disable
23:20	R/W	0xF	PD13_SELECT PD13 Select 0000: Input 0001: Output 0010: LCD0-D19 0011: LVDS1-D1N 0100: DSI1-D1N 0101: PWM13 0110:SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT13 1111: IO Disable

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Offset: 0x0094			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PD12_SELECT PD12 Select 0000: Input 0001: Output 0010: LCD0-D18 0011: LVDS1-D1P 0100: DSI1-D1P 0101: PWM12 0110: SPI1-MOSI/DBI-SDO 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT12 1111: IO Disable
15:12	R/W	0xF	PD11_SELECT PD11 Select 0000: Input 0001: Output 0010: LCD0-D15 0011: LVDS1-D0N 0100: DSI1-D0N 0101: PWM11 0110: SPI1-CLK/DBI-SCLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT11 1111: IO Disable
11:8	R/W	0xF	PD10_SELECT PD10 Select 0000: Input 0001: Output 0010: LCD0-D14 0011: LVDS1-D0P 0100: DSI1-D0P 0101: PWM10 0110: SPI1-CS/DBI-CSX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT10 1111: IO Disable

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Offset: 0x0094			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PD9_SELECT PD9 Select 0000: Input 0001: Output 0010: LCD0-D13 0011: LVDS0-D3N 0100: DSI0-D3N 0101: PWM9 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT9 1111: IO Disable
3:0	R/W	0xF	PD8_SELECT PD8 Select 0000: Input 0001: Output 0010: LCD0-D12 0011: LVDS0-D3P 0100: DSI0-D3P 0101: PWM8 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT8 1111: IO Disable

8.6.6.25 0x0098 PD Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x0098			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD23_SELECT PD23 Select 0000: Input 0001: Output 0010: PWM0 0011: SPI1-WP/DBI-TE 0100: UART2-CTS 0101: UART7-RX 0110: TWI0-SDA 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT23 1111: IO Disable

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Offset: 0x0098			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PD22_SELECT PD22 Select 0000: Input 0001: Output 0010: PWM1 0011: SPI1-HOLD/DBI-DCX/DBI-WRX 0100: UART2-RTS 0101: UART7-TX 0110: TWI0-SCK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT22 1111: IO Disable
23:20	R/W	0xF	PD21_SELECT PD21 Select 0000: Input 0001: Output 0010: LCD0-VSYNC 0011: PWM3 0100: UART2-RX 0101: UART7-CTS 0110: UART4-CTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT21 1111: IO Disable
19:16	R/W	0xF	PD20_SELECT PD20 Select 0000: Input 0001: Output 0010: LCD0-HSYNC 0011: PWM2 0100: UART2-TX 0101: UART7-RTS 0110: UART4-RTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT20 1111: IO Disable
15:12	R/W	0xF	PD19_SELECT PD19 Select 0000: Input 0001: Output 0010: LCD0-DE 0011: LVDS1-D3N 0100: DSI1-D3N 0101: PWM19 0110: UART4-RX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT19 1111: IO Disable

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Offset: 0x0098			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PD18_SELECT PD18 Select 0000: Input 0001: Output 0010: LCD0-CLK 0011: LVDS1-D3P 0100: DSI1-D3P 0101: PWM18 0110: UART4-TX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT18 1111: IO Disable
7:4	R/W	0xF	PD17_SELECT PD17 Select 0000: Input 0001: Output 0010: LCD0-D23 0011: LVDS1-CKN 0100: DSI1-D2N 0101: PWM17 0110: UART3-CTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT17 1111: IO Disable
3:0	R/W	0xF	PD16_SELECT PD16 Select 0000: Input 0001: Output 0010: LCD0-D22 0011: LVDS1-CKP 0100: DSI1-D2P 0101: PWM16 0110: UART3-RTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT16 1111: IO Disable

8.6.6.26 0x009C PD Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PD_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.27 0x00A0 PD Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	PD_DAT PD Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.28 0x00A4 PD Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00A4			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD7_DRV PD7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD6_DRV PD6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD5_DRV PD5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD4_DRV PD4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/

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Offset: 0x00A4			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x1	PD3_DRV PD3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD2_DRV PD2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD1_DRV PD1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD0_DRV PD0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.29 0x00A8 PD Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00A8			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD15_DRV PD15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD14_DRV PD14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD13_DRV PD13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

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Offset: 0x00A8			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x1	PD12_DRV PD12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD11_DRV PD11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD10_DRV PD10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD9_DRV PD9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD8_DRV PD8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.30 0x00AC PD Multi_Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x00AC			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD23_DRV PD23 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD22_DRV PD22 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/

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Offset: 0x00AC			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x1	PD21_DRV PD21 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD20_DRV PD20 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD19_DRV PD19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD18_DRV PD18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD17_DRV PD17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD16_DRV PD16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.31 0x00B0 PD Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PD_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.32 0x00B4 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PD15_PULL PD15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x00B4			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x0	PD6_PULL PD6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.33 0x00B8 PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PD_PUL1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	R/W	0x0	PD23_PULL PD23 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x00B8			Register Name: PD_PUL1
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x0	PD22_PULL PD22 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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8.6.6.34 0x00C0 PE Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C0			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PE7_SELECT PE7 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-LRCK 0101: LCD1-TRIG 0110: NCSI-D9 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT7 1111: IO Disable
27:24	R/W	0xF	PE6_SELECT PE6 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-BCLK 0101: LCD0-TRIG 0110: NCSI-D8 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT6 1111: IO Disable
23:20	R/W	0xF	PE5_SELECT PE5 Select 0000: Input 0001: Output 0010: MCSI1-MCLK 0011: PLL-LOCK-DBG 0100: I2S2-MCLK 0101: LEDC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT5 1111: IO Disable

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Offset: 0x00C0			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PE4_SELECT PE4 Select 0000: Input 0001: Output 0010: TWI3-SDA 0011: UART4-CTS 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT4 1111: IO Disable
15:12	R/W	0xF	PE3_SELECT PE3 Select 0000: Input 0001: Output 0010: TWI3-SCK 0011: UART4-RTS 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT3 1111: IO Disable
11:8	R/W	0xF	PE2_SELECT PE2 Select 0000: Input 0001: Output 0010: TWI2-SDA 0011: UART4-RX 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT2 1111: IO Disable
7:4	R/W	0xF	PE1_SELECT PE1 Select 0000: Input 0001: Output 0010: TWI2-SCK 0011: UART4-TX 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT1 1111: IO Disable

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Offset: 0x00C0			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PE0_SELECT PE0 Select 0000: Input 0001: Output 0010: MCSI0-MCLK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT0 1111: IO Disable

8.6.6.35 0x00C4 PE Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C4			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PE15_SELECT PE15 Select 0000: Input 0001: Output 0010: MCSI2-MCLK 0011: PWM2 0100: Reserved 0101: Reserved 0110: NCSI-D15 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT15 1111: IO Disable
27:24	R/W	0xF	PE14_SELECT PE14 Select 0000: Input 0001: Output 0010: TWI4-SDA 0011: UART5-RX 0100: SPI2-MISO 0101: UART6-CTS 0110: CSI1-XVS-FSYNC 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT14 1111: IO Disable

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Offset: 0x00C4			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PE13_SELECT PE13 Select 0000: Input 0001: Output 0010: TWI4-SCK 0011: UART5-TX 0100: SPI2-MOSI 0101: UART6-RTS 0110: CSI0-XVS-FSYNC 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT13 1111: IO Disable
19:16	R/W	0xF	PE12_SELECT PE12 Select 0000: Input 0001: Output 0010: TWI1-SDA 0011: UART5-CTS 0100: SPI2-CLK 0101: UART6-RX 0110: NCSI-D14 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT12 1111: IO Disable
15:12	R/W	0xF	PE11_SELECT PE11 Select 0000: Input 0001: Output 0010: TWI1-SCK 0011: UART5-RTS 0100: SPI2-CS0 0101: UART6-TX 0110: NCSI-D13 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT11 1111: IO Disable
11:8	R/W	0xF	PE10_SELECT PE10 Select 0000: Input 0001: Output 0010: MCSI3-MCLK 0011: PWM3 0100: Reserved 0101: Reserved 0110: NCSI-D12 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT10 1111: IO Disable

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Offset: 0x00C4			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PE9_SELECT PE9 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-DIN0 0101: Reserved 0110: NCSI-D11 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT9 1111: IO Disable
3:0	R/W	0xF	PE8_SELECT PE8 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-DOUT0 0101: Reserved 0110: NCSI-D10 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT8 1111: IO Disable

8.6.6.36 0x00C8 PE Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: PE_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.37 0x00CC PE Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PE_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.38 0x00D0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x00D0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0	PE_DAT PE Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.39 0x00D4 PE Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00D4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PE7_DRV PE7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE6_DRV PE6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE5_DRV PE5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE4_DRV PE4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE3_DRV PE3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x00D4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
11:10	/	/	/
9:8	R/W	0x1	PE2_DRV PE2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE1_DRV PE1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE0_DRV PE0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.40 0x00D8 PE Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00D8			Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PE15_DRV PE15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE14_DRV PE14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE13_DRV PE13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE12_DRV PE12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x00D8			Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:12	R/W	0x1	PE11_DRV PE11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE10_DRV PE10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE9_DRV PE9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE8_DRV PE8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.41 0x00DC PE Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x00DC			Register Name: PE_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.42 0x00E0 PE Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PE_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.43 0x00E4 PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PE15_PULL PE15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PE14_PULL PE14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PE13_PULL PE13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x00E4			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x0	PE6_PULL PE6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.44 0x00E8 PE Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PE_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.45 0x00F0 PF Configure Register 0 (Default Value: 0x0FFF_FFFF)

Offset: 0x00F0			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

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Offset: 0x00F0			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PF6_SELECT PF6 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: Reserved 0101: I2S3-MCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT6 1111: IO Disable
23:20	R/W	0xF	PF5_SELECT PF5 Select 0000: Input 0001: Output 0010: SDC0-D2 0011: JTAG-CK 0100: Reserved 0101: I2S3-BCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT5 1111: IO Disable
19:16	R/W	0xF	PF4_SELECT PF4 Select 0000: Input 0001: Output 0010: SDC0-D3 0011: UART0-RX 0100: Reserved 0101: I2S3-DIN3 0110: I2S3-DOUT3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT4 1111: IO Disable
15:12	R/W	0xF	PF3_SELECT PF3 Select 0000: Input 0001: Output 0010: SDC0-CMD 0011: JTAG-DO 0100: Reserved 0101: I2S3-LRCK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT3 1111: IO Disable

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Offset: 0x00F0			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PF2_SELECT PF2 Select 0000: Input 0001: Output 0010: SDC0-CLK 0011: UART0-TX 0100: Reserved 0101: I2S3-DIN2 0110: I2S3-DOUT2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT2 1111: IO Disable
7:4	R/W	0xF	PF1_SELECT PF1 Select 0000: Input 0001: Output 0010: SDC0-D0 0011: JTAG-DI 0100: Reserved 0101: I2S3-DOUT0 0110: I2S3-DIN1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT1 1111: IO Disable
3:0	R/W	0xF	PF0_SELECT PF0 Select 0000: Input 0001: Output 0010: SDC0-D1 0011: JTAG-MS 0100: Reserved 0101: I2S3-DIN0 0110: I2S3-DOUT1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT0 1111: IO Disable

8.6.6.46 0x00F4 PF Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PF_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.47 0x00F8 PF Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PF_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.48 0x00FC PF Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: PF_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.49 0x0100 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R/W	0	PF_DAT PF Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.50 0x0104 PF Multi_Driving Register 0 (Default Value: 0x0111_1111)

Offset: 0x0104			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PF6_DRV PF6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/

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Offset: 0x0104			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x1	PF5_DRV PF5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PF4_DRV PF4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PF3_DRV PF3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PF2_DRV PF2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PF1_DRV PF1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PF0_DRV PF0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.51 0x0108 PF Multi_Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PF_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.52 0x010C PF Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PF_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.53 0x0110 PF Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PF_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.54 0x0114 PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PF_PUL0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0114			Register Name: PF_PUL0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PF0_PULL PF0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.55 0x0118 PF Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PF_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.56 0x0120 PG Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0120			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PG7_SELECT PG7 Select 0000: Input 0001: Output 0010: UART1-RX 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT7 1111: IO Disable
27:24	R/W	0xF	PG6_SELECT PG6 Select 0000: Input 0001: Output 0010: UART1-TX 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT6 1111: IO Disable

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Offset: 0x0120			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PG5_SELECT PG5 Select 0000: Input 0001: Output 0010: SDC1-D3 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT5 1111: IO Disable
19:16	R/W	0xF	PG4_SELECT PG4 Select 0000: Input 0001: Output 0010: SDC1-D2 0011: PCIE0-CLKREQN 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT4 1111: IO Disable
15:12	R/W	0xF	PG3_SELECT PG3 Select 0000: Input 0001: Output 0010: SDC1-D1 0011: PCIE0-WAKEN 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT3 1111: IO Disable
11:8	R/W	0xF	PG2_SELECT PG2 Select 0000: Input 0001: Output 0010: SDC1-D0 0011: PCIE0-PERSTN 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT2 1111: IO Disable

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Offset: 0x0120			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PG1_SELECT PG1 Select 0000: Input 0001: Output 0010: SDC1-CMD 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT1 1111: IO Disable
3:0	R/W	0xF	PG0_SELECT PG0 Select 0000: Input 0001: Output 0010: SDC1-CLK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT0 1111: IO Disable

8.6.6.57 0x0124 PG Configure Register 1 (Default Value: 0x0FFF_FFFF)

Offset: 0x0124			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	PG14_SELECT PG14 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-DIN0 0100: I2S1-DOUT1 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT14 1111: IO Disable

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Offset: 0x0124			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PG13_SELECT PG13 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-DOUT0 0100: I2S1-DIN1 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT13 1111: IO Disable
19:16	R/W	0xF	PG12_SELECT PG12 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-LRCK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT12 1111: IO Disable
15:12	R/W	0xF	PG11_SELECT PG11 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-BCLK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT11 1111: IO Disable
11:8	R/W	0xF	PG10_SELECT PG10 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-MCLK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT10 1111: IO Disable

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Offset: 0x0124			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PG9_SELECT PG9 Select 0000: Input 0001: Output 0010: UART1-CTS 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT9 1111: IO Disable
3:0	R/W	0xF	PG8_SELECT PG8 Select 0000: Input 0001: Output 0010: UART1-RTS 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT8 1111: IO Disable

8.6.6.58 0x0128 PG Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PG_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.59 0x012C PG Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PG_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.60 0x0130 PG Data Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PG_DAT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/

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Offset: 0x0130			Register Name: PG_DAT
Bit	Read/Write	Default/Hex	Description
14:0	R/W	0	PG_DAT PG Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.61 0x0134 PG Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0134			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PG7_DRV PG7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PG6_DRV PG6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PG5_DRV PG5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PG4_DRV PG4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PG3_DRV PG3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x0134			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
11:10	/	/	/
9:8	R/W	0x1	PG2_DRV PG2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PG1_DRV PG1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PG0_DRV PG0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.62 0x0138 PG Multi_Driving Register 1 (Default Value: 0x0111_1111)

Offset: 0x0138			Register Name: PG_DRV1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PG14_DRV PG14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PG13_DRV PG13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PG12_DRV PG12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PG11_DRV PG11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x0138			Register Name: PG_DRV1
Bit	Read/Write	Default/Hex	Description
11:10	/	/	/
9:8	R/W	0x1	PG10_DRV PG10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PG9_DRV PG9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PG8_DRV PG8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.63 0x013C PG Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PG_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.64 0x0140 PG Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PG_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.65 0x0144 PG Pull Register 0 (Default Value: 0x0000_0554)

Offset: 0x0144			Register Name: PG_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PG14_PULL PG14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0144			Register Name: PG_PUL0
Bit	Read/Write	Default/Hex	Description
27:26	R/W	0x0	PG13_PULL PG13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PG10_PULL PG10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x1	PG5_PULL PG5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x1	PG4_PULL PG4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0144			Register Name: PG_PUL0
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x1	PG3_PULL PG3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x1	PG2_PULL PG2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x1	PG1_PULL PG1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.66 0x0148 PG Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PG_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.67 0x0150 PH Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PH7_SELECT PH7 Select 0000: Input 0001: Output 0010: UART3-CTS 0011: SPI1-MISO 0100: OWA-OUT 0101: RGMII0-TXCTL/RMII0-TXEN 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT7 1111: IO Disable

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Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PH6_SELECT PH6 Select 0000: Input 0001: Output 0010: UART3-RTS 0011: SPI1-MOSI 0100: OWA-IN 0101: RGMII0-TXCK/RMII0-TXCK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT6 1111: IO Disable
23:20	R/W	0xF	PH5_SELECT PH5 Select 0000: Input 0001: Output 0010: UART3-RX 0011: SPI1-CLK 0100: LEDC 0101: RGMII0-TXD0/RMII0-TXD0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT5 1111: IO Disable
19:16	R/W	0xF	PH4_SELECT PH4 Select 0000: Input 0001: Output 0010: UART3-TX 0011: SPI1-CS0 0100: Reserved 0101: RGMII0-TXD1/RMII0-TXD1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT4 1111: IO Disable

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Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PH3_SELECT PH3 Select 0000: Input 0001: Output 0010: TWI1-SDA 0011: IR-TX 0100: I2S2-DIN2 0101: RGMII0-CLKIN/RMII0-RXER 0110: I2S2-DOUT2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT3 1111: IO Disable
11:8	R/W	0xF	PH2_SELECT PH2 Select 0000: Input 0001: Output 0010: TWI1-SCK 0011: Reserved 0100: I2S2-DIN3 0101: RGMII0-RXCTL/RMII0-CRS-DV 0110: I2S2-DOUT3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT2 1111: IO Disable
7:4	R/W	0xF	PH1_SELECT PH1 Select 0000: Input 0001: Output 0010: TWI0-SDA 0011: Reserved 0100: Reserved 0101: RGMII0-RXD0/RMII0-RXD0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT1 1111: IO Disable

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Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PH0_SELECT PH0 Select 0000: Input 0001: Output 0010: TWI0-SCK 0011: Reserved 0100: Reserved 0101: RGMII0-RXD1/RMII0-RXD1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT0 1111: IO Disable

8.6.6.68 0x0154 PH Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0154			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PH15_SELECT PH15 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S3-LRCK 0101: RGMII0-RXD2/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT15 1111: IO Disable
27:24	R/W	0xF	PH14_SELECT PH14 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S3-BCLK 0101: RGMII0-RXD3/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT14 1111: IO Disable

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Offset: 0x0154			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PH13_SELECT PH13 Select 0000: Input 0001: Output 0010: Reserved 0011: TWI3-SDA 0100: I2S3-MCLK 0101: RGMII0-EPHY-25M 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT13 1111: IO Disable
19:16	R/W	0xF	PH12_SELECT PH12 Select 0000: Input 0001: Output 0010: DMIC-DATA3 0011: TWI3-SCK 0100: I2S2-DIN0 0101: I2S2-DOUT1 0110: PCIE0-WAKEN 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT12 1111: IO Disable
15:12	R/W	0xF	PH11_SELECT PH11 Select 0000: Input 0001: Output 0010: DMIC-DATA2 0011: SPI2-MISO 0100: I2S2-DOUT0 0101: I2S2-DIN1 0110: PCIE0-PERSTN 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT11 1111: IO Disable
11:8	R/W	0xF	PH10_SELECT PH10 Select 0000: Input 0001: Output 0010: DMIC-DATA1 0011: SPI2-MOSI 0100: I2S2-LRCK 0101: RGMII0-MDIO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT10 1111: IO Disable

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Offset: 0x0154			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PH9_SELECT PH9 Select 0000: Input 0001: Output 0010: DMIC-DATA0 0011: SPI2-CLK 0100: I2S2-BCLK 0101: RGMII0-MDC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT9 1111: IO Disable
3:0	R/W	0xF	PH8_SELECT PH8 Select 0000: Input 0001: Output 0010: DMIC-CLK 0011: SPI2-CS0 0100: I2S2-MCLK 0101: I2S2-DIN2 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT8 1111: IO Disable

8.6.6.69 0x0158 PH Configure Register 2 (Default Value: 0x0000_FFFF)

Offset: 0x0158			Register Name: PH_CFG2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0xF	PH19_SELECT PH19 Select 0000: Input 0001: Output 0010: IR-RX 0011: I2S3-DOUT3 0100: I2S3-DIN3 0101: LEDC 0110: PCIE0-CLKREQN 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT19 1111: IO Disable

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Offset: 0x0158			Register Name: PH_CFG2
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PH18_SELECT PH18 Select 0000: Input 0001: Output 0010: IR-TX 0011: I2S3-DOUT2 0100: I2S3-DIN2 0101: RGMII0-TXD2/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT18 1111: IO Disable
7:4	R/W	0xF	PH17_SELECT PH17 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S3-DOUT1 0100: I2S3-DIN0 0101: RGMII0-TXD3/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT17 1111: IO Disable
3:0	R/W	0xF	PH16_SELECT PH16 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S3-DOUT0 0100: I2S3-DIN1 0101: RGMII0-RXCK/RMII0-NULL 0110: CLK-FANOUT0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT16 1111: IO Disable

8.6.6.70 0x015C PH Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PH_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.71 0x0160 PH Data Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PH_DAT
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0	PH_DAT PH Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.72 0x0164 PH Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0164			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PH7_DRV PH7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PH6_DRV PH6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH5_DRV PH5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH4_DRV PH4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/

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Offset: 0x0164			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x1	PH3_DRV PH3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH2_DRV PH2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH1_DRV PH1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH0_DRV PH0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.73 0x0168 PH Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0168			Register Name: PH_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PH15_DRV PH15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PH14_DRV PH14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH13_DRV PH13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

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Offset: 0x0168			Register Name: PH_DRV1
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x1	PH12_DRV PH12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH11_DRV PH11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH10_DRV PH10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH9_DRV PH9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH8_DRV PH8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.74 0x016C PH Multi_Driving Register 2 (Default Value: 0x0000_1111)

Offset: 0x016C			Register Name: PH_DRV2
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x1	PH19_DRV PH19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH18_DRV PH18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/

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Offset: 0x016C			Register Name: PH_DRV2
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x1	PH17_DRV PH17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH16_DRV PH16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.75 0x0170 PH Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PH_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.76 0x0174 PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PH15_PULL PH15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0174			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	PH10_PULL PH10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0174			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PH0_PULL PH0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.77 0x0178 PH Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PH_PUL1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x0	PH19_PULL PH19 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PH18_PULL PH18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PH17_PULL PH17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PH16_PULL PH16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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8.6.6.78 0x0180 PI Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0180			Register Name: PI_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PI7_SELECT PI7 Select 0000: Input 0001: Output 0010: UART6-RX 0011: UART4-CTS 0100: PWM8 0101: SPI2-CLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT7 1111: IO Disable
27:24	R/W	0xF	PI6_SELECT PI6 Select 0000: Input 0001: Output 0010: UART6-TX 0011: UART4-RTS 0100: PWM7 0101: SPI2-CS 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT6 1111: IO Disable
23:20	R/W	0xF	PI5_SELECT PI5 Select 0000: Input 0001: Output 0010: UART5-CTS 0011: SPI1-MISO 0100: PWM6 0101: I2S2-DIN0 0110: I2S2-DOUT1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT5 1111: IO Disable

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Offset: 0x0180			Register Name: PI_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PI4_SELECT PI4 Select 0000: Input 0001: Output 0010: UART5-RTS 0011: SPI1-MOSI 0100: PWM5 0101: I2S2-DOUT0 0110: I2S2-DIN1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT4 1111: IO Disable
15:12	R/W	0xF	PI3_SELECT PI3 Select 0000: Input 0001: Output 0010: UART5-RX 0011: SPI1-CLK 0100: PWM4 0101: I2S2-LRCK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT3 1111: IO Disable
11:8	R/W	0xF	PI2_SELECT PI2 Select 0000: Input 0001: Output 0010: UART5-TX 0011: SPI1-CS 0100: PWM3 0101: I2S2-BCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT2 1111: IO Disable
7:4	R/W	0xF	PI1_SELECT PI1 Select 0000: Input 0001: Output 0010: TWI4-SDA 0011: UART4-RX 0100: PWM2 0101: I2S2-DIN2 0110: I2S2-DOUT2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT1 1111: IO Disable

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Offset: 0x0180			Register Name: PI_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PI0_SELECT PI0 Select 0000: Input 0001: Output 0010: TWI4-SCK 0011: UART4-TX 0100: PWM1 0101: I2S2-DIN3 0110: I2S2-DOUT3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT0 1111: IO Disable

8.6.6.79 0x0184 PI Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0184			Register Name: PI_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PI15_SELECT PI15 Select 0000: Input 0001: Output 0010: UART3-RTS 0011: TWI2-SCK 0100: PWM16 0101: CAN-TX0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT15 1111: IO Disable
27:24	R/W	0xF	PI14_SELECT PI14 Select 0000: Input 0001: Output 0010: UART6-RTS 0011: DMIC-CLK 0100: PWM15 0101: CAN-RX0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT14 1111: IO Disable

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Offset: 0x0184			Register Name: PI_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PI13_SELECT PI13 Select 0000: Input 0001: Output 0010: UART6-CTS 0011: DMIC-DATA3 0100: PWM14 0101: I2S2-MCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT13 1111: IO Disable
19:16	R/W	0xF	PI12_SELECT PI12 Select 0000: Input 0001: Output 0010: UART3-RX 0011: Reserved 0100: PWM13 0101: SPI2-MISO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT12 1111: IO Disable
15:12	R/W	0xF	PI11_SELECT PI11 Select 0000: Input 0001: Output 0010: UART3-TX 0011: DMIC-DATA0 0100: PWM12 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT11 1111: IO Disable
11:8	R/W	0xF	PI10_SELECT PI10 Select 0000: Input 0001: Output 0010: OWA-OUT 0011: DMIC-DATA1 0100: PWM11 0101: I2S2-MCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT10 1111: IO Disable

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Offset: 0x0184			Register Name: PI_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PI9_SELECT PI9 Select 0000: Input 0001: Output 0010: TWI5-SDA 0011: DMIC-DATA2 0100: PWM10 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT9 1111: IO Disable
3:0	R/W	0xF	PI8_SELECT PI8 Select 0000: Input 0001: Output 0010: TWI5-SCK 0011: JR-RX 0100: PWM9 0101: SPI2-MOSI 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT8 1111: IO Disable

8.6.6.80 0x0188 PI Configure Register 2 (Default Value: 0x0000_000F)

Offset: 0x0188			Register Name: PI_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xF	PI16_SELECT PI16 Select 0000: Input 0001: Output 0010: UART3-CTS 0011: TWI2-SDA 0100: PWM17 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PI-EINT16 1111: IO Disable

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8.6.6.81 0x018C PI Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x018C			Register Name: PI_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.82 0x0190 PI Data Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: PI_DAT
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:0	R/W	0	PI_DAT PI Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.83 0x0194 PI Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0194			Register Name: PI_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PI7_DRV PI7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PI6_DRV PI6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PI5_DRV PI5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

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Offset: 0x0194			Register Name: PI_DRV0
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x1	PI4_DRV PI4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PI3_DRV PI3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PI2_DRV PI2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PI1_DRV PI1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PI0_DRV PI0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.84 0x0198 PI Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0198			Register Name: PI_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PI15_DRV PI15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PI14_DRV PI14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/

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Offset: 0x0198			Register Name: PI_DRV1
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x1	PI13_DRV PI13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PI12_DRV PI12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PI11_DRV PI11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PI10_DRV PI10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PI9_DRV PI9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PI8_DRV PI8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.85 0x019C PI Multi_Driving Register 2 (Default Value: 0x0000_0001)

Offset: 0x019C			Register Name: PI_DRV2
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	PI16_DRV PI16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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8.6.6.86 0x01A0 PI Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x01A0			Register Name: PI_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.87 0x01A4 PI Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x01A4			Register Name: PI_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PI15_PULL PI15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PI14_PULL PI14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PI13_PULL PI13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PI12_PULL PI12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PI11_PULL PI11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PI10_PULL PI10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PI9_PULL PI9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PI8_PULL PI8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x01A4			Register Name: PI_PUL0
Bit	Read/Write	Default/Hex	Description
15:14	R/W	0x0	PI7_PULL PI7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PI6_PULL PI6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PI5_PULL PI5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PI4_PULL PI4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PI3_PULL PI3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PI2_PULL PI2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PI1_PULL PI1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PI0_PULL PI0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.88 0x01A8 PI Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x01A8			Register Name: PI_PUL1
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/

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Offset: 0x01A8			Register Name: PI_PUL1
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PI16_PULL PI16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.89 0x01B0 PJ Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x01B0			Register Name: PJ_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PJ7_SELECT PJ7 Select 0000: Input 0001: Output 0010: LCD1-D7 0011: LVDS2-CKN 0100: Reserved 0101: RGMII1-TXCTL/RMII1-TXEN 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ_EINT7 1111: IO Disable
27:24	R/W	0xF	PJ6_SELECT PJ6 Select 0000: Input 0001: Output 0010: LCD1-D6 0011: LVDS2-CKP 0100: Reserved 0101: RGMII1-TXCK/RMII1-TXCK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT6 1111: IO Disable

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Offset: 0x01B0			Register Name: PJ_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PJ5_SELECT PJ5 Select 0000: Input 0001: Output 0010: LCD1-D5 0011: LVDS2-D2N 0100: Reserved 0101: RGMII1-TXD0/RMII1-TXD0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT5 1111: IO Disable
19:16	R/W	0xF	PJ4_SELECT PJ4 Select 0000: Input 0001: Output 0010: LCD1-D4 0011: LVDS2-D2P 0100: Reserved 0101: RGMII1-TXD1/RMII1-TXD1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT4 1111: IO Disable
15:12	R/W	0xF	PJ3_SELECT PJ3 Select 0000: Input 0001: Output 0010: LCD1-D3 0011: LVDS2-D1N 0100: Reserved 0101: RGMII1-CLKIN/RMII1-RXER 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT3 1111: IO Disable

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Offset: 0x01B0			Register Name: PJ_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PJ2_SELECT PJ2 Select 0000: Input 0001: Output 0010: LCD1-D2 0011: LVDS2-D1P 0100: Reserved 0101: RGMII1-RXCTL/RMII1-CRS-DV 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT2 1111: IO Disable
7:4	R/W	0xF	PJ1_SELECT PJ1 Select 0000: Input 0001: Output 0010: LCD1-D1 0011: LVDS2-D0N 0100: Reserved 0101: RGMII1-RXD0/RMII1-RXD0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT1 1111: IO Disable
3:0	R/W	0xF	PJ0_SELECT PJ0 Select 0000: Input 0001: Output 0010: LCD1-D0 0011: LVDS2-D0P 0100: Reserved 0101: RGMII1-RXD1/RMII1-RXD1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT0 1111: IO Disable

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8.6.6.90 0x01B4 PJ Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x01B4			Register Name: PJ_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PJ15_SELECT PJ15 Select 0000: Input 0001: Output 0010: LCD1-D15 0011: LVDS3-D2N 0100: Reserved 0101: RGMII1-TXD2/RMII1-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT15 1111: IO Disable
27:24	R/W	0xF	PJ14_SELECT PJ14 Select 0000: Input 0001: Output 0010: LCD1-D14 0011: LVDS3-D2P 0100: Reserved 0101: RGMII1-TXD3/RMII1-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT14 1111: IO Disable
23:20	R/W	0xF	PJ13_SELECT PJ13 Select 0000: Input 0001: Output 0010: LCD1-D13 0011: LVDS3-D1N 0100: Reserved 0101: RGMII1-RXCK/RMII1-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT13 1111: IO Disable

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Offset: 0x01B4			Register Name: PJ_CFG1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PJ12_SELECT PJ12 Select 0000: Input 0001: Output 0010: LCD1-D12 0011: LVDS3-D1P 0100: Reserved 0101: RGMII1-RXD2/RMII1-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT12 1111: IO Disable
15:12	R/W	0xF	PJ11_SELECT PJ11 Select 0000: Input 0001: Output 0010: LCD1-D11 0011: LVDS3-D0N 0100: Reserved 0101: RGMII1-RXD3/RMII1-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT11 1111: IO Disable
11:8	R/W	0xF	PJ10_SELECT PJ10 Select 0000: Input 0001: Output 0010: LCD1-D10 0011: LVDS3-D0P 0100: Reserved 0101: RGMII1-EPHY-25M 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT10 1111: IO Disable

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Offset: 0x01B4			Register Name: PJ_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PJ9_SELECT PJ9 Select 0000: Input 0001: Output 0010: LCD1-D9 0011: LVDS2-D3N 0100: Reserved 0101: RGMII1-MDIO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT9 1111: IO Disable
3:0	R/W	0xF	PJ8_SELECT PJ8 Select 0000: Input 0001: Output 0010: LCD1-D8 0011: LVDS2-D3P 0100: Reserved 0101: RGMII1-MDC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT8 1111: IO Disable

8.6.6.91 0x01B8 PJ Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x01B8			Register Name: PJ_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PJ23_SELECT PJ23 Select 0000: Input 0001: Output 0010: LCD1-D23 0011: UART2-CTS 0100: UART3-RX 0101: SPI0-MISO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT23 1111: IO Disable

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Offset: 0x01B8			Register Name: PJ_CFG2
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PJ22_SELECT PJ22 Select 0000: Input 0001: Output 0010: LCD1-D22 0011: UART2-RTS 0100: UART3-TX 0101: SPI0-MOSI 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT22 1111: IO Disable
23:20	R/W	0xF	PJ21_SELECT PJ21 Select 0000: Input 0001: Output 0010: LCD1-D21 0011: UART2-RX 0100: UART3-CTS 0101: SPI0-CLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT21 1111: IO Disable
19:16	R/W	0xF	PJ20_SELECT PJ20 Select 0000: Input 0001: Output 0010: LCD1-D20 0011: UART2-TX 0100: UART3-RTS 0101: SPI0-CS0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT20 1111: IO Disable
15:12	R/W	0xF	PJ19_SELECT PJ19 Select 0000: Input 0001: Output 0010: LCD1-D19 0011: LVDS3-D3N 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT19 1111: IO Disable

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Offset: 0x01B8			Register Name: PJ_CFG2
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PJ18_SELECT PJ18 Select 0000: Input 0001: Output 0010: LCD1-D18 0011: LVDS3-D3P 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT18 1111: IO Disable
7:4	R/W	0xF	PJ17_SELECT PJ17 Select 0000: Input 0001: Output 0010: LCD1-D17 0011: LVDS3-CKN 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT17 1111: IO Disable
3:0	R/W	0xF	PJ16_SELECT PJ16 Select 0000: Input 0001: Output 0010: LCD1-D16 0011: LVDS3-CKP 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT16 1111: IO Disable

8.6.6.92 0x01BC PJ Configure Register 3 (Default Value: 0x0000_FFFF)

Offset: 0x01BC			Register Name: PJ_CFG3
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x01BC			Register Name: PJ_CFG3
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PJ27_SELECT PJ27 Select 0000: Input 0001: Output 0010: LCD1-VSYNC 0011: TWI5-SDA 0100: UART4-CTS 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT27 1111: IO Disable
11:8	R/W	0xF	PJ26_SELECT PJ26 Select 0000: Input 0001: Output 0010: LCD1-HSYNC 0011: TWI5-SCK 0100: UART4-RTS 0101: SPI0-HOLD 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT26 1111: IO Disable
7:4	R/W	0xF	PJ25_SELECT PJ25 Select 0000: Input 0001: Output 0010: LCD1-DE 0011: TWI4-SDA 0100: UART4-RX 0101: SPI0-WP 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT25 1111: IO Disable
3:0	R/W	0xF	PJ24_SELECT PJ24 Select 0000: Input 0001: Output 0010: LCD1-CLK 0011: TWI4-SCK 0100: UART4-TX 0101: SPI0-CS1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT24 1111: IO Disable

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8.6.6.93 0x01C0 PJ Data Register (Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: PJ_DAT
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:0	R/W	0	PJ_DAT PJ Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.94 0x01C4 PJ Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x01C4			Register Name: PJ_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PJ7_DRV PJ7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PJ6_DRV PJ6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PJ5_DRV PJ5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PJ4_DRV PJ4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/

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Offset: 0x01C4			Register Name: PJ_DRV0
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x1	PJ3_DRV PJ3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PJ2_DRV PJ2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PJ1_DRV PJ1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PJ0_DRV PJ0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.95 0x01C8 PJ Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x01C8			Register Name: PJ_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PJ15_DRV PJ15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PJ14_DRV PJ14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PJ13_DRV PJ13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

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Offset: 0x01C8			Register Name: PJ_DRV1
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x1	PJ12_DRV PJ12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PJ11_DRV PJ11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PJ10_DRV PJ10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PJ9_DRV PJ9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PJ8_DRV PJ8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.96 0x01CC PJ Multi_Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x01CC			Register Name: PJ_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PJ23_DRV PJ23 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PJ22_DRV PJ22 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/

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Offset: 0x01CC			Register Name: PJ_DRV2
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x1	PJ21_DRV PJ21 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PJ20_DRV PJ20 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PJ19_DRV PJ19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PJ18_DRV PJ18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PJ17_DRV PJ17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PJ16_DRV PJ16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.97 0x01D0 PJ Multi_Driving Register 3 (Default Value: 0x0000_1111)

Offset: 0x01D0			Register Name: PJ_DRV3
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x1	PJ27_DRV PJ27 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/

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Offset: 0x01D0			Register Name: PJ_DRV3
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x1	PJ26_DRV PJ26 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PJ25_DRV PJ25 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PJ24_DRV PJ24 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.98 0x01D4 PJ Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x01D4			Register Name: PJ_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PJ15_PULL PJ15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PJ14_PULL PJ14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PJ13_PULL PJ13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PJ12_PULL PJ12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PJ11_PULL PJ11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x01D4			Register Name: PJ_PUL0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	PJ10_PULL PJ10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PJ9_PULL PJ9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PJ8_PULL PJ8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PJ7_PULL PJ7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PJ6_PULL PJ6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PJ5_PULL PJ5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PJ4_PULL PJ4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PJ3_PULL PJ3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PJ2_PULL PJ2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PJ1_PULL PJ1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x01D4			Register Name: PJ_PUL0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PJ0_PULL PJ0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.99 0x01D8 PJ Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x01D8			Register Name: PJ_PUL1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:22	R/W	0x0	PJ27_PULL PJ27 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PJ26_PULL PJ26 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PJ25_PULL PJ25 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PJ24_PULL PJ24 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PJ23_PULL PJ23 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PJ22_PULL PJ22 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PJ21_PULL PJ21 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x01D8			Register Name: PJ_PUL1
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	PJ20_PULL PJ20 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PJ19_PULL PJ19 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PJ18_PULL PJ18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PJ17_PULL PJ17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PJ16_PULL PJ16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.100 0x0500 PK Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0500			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK7_SELECT PK7 Select 0000: Input 0001: Output 0010: MCSIB-D0P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT7 1111: IO Disable

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Offset: 0x0500			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PK6_SELECT PK6 Select 0000: Input 0001: Output 0010: MCSIB-D0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT6 1111: IO Disable
23:20	R/W	0xF	PK5_SELECT PK5 Select 0000: Input 0001: Output 0010: MCSIA-CKP 0011: TWI2-SDA 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT5 1111: IO Disable
19:16	R/W	0xF	PK4_SELECT PK4 Select 0000: Input 0001: Output 0010: MCSIA-CKN 0011: TWI2-SCK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT4 1111: IO Disable
15:12	R/W	0xF	PK3_SELECT PK3 Select 0000: Input 0001: Output 0010: MCSIA-D1P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT3 1111: IO Disable

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Offset: 0x0500			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PK2_SELECT PK2 Select 0000: Input 0001: Output 0010: MCSIA-D1N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT2 1111: IO Disable
7:4	R/W	0xF	PK1_SELECT PK1 Select 0000: Input 0001: Output 0010: MCSIA-D0P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT1 1111: IO Disable
3:0	R/W	0xF	PK0_SELECT PK0 Select 0000: Input 0001: Output 0010: MCSIA-D0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT0 1111: IO Disable

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8.6.6.101 0x0504 PK Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0504			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK15_SELECT PK15 Select 0000: Input 0001: Output 0010: MCSIC-D1P 0011: UART7-CTS 0100: UART5-CTS 0101: NCSI-VSYNC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT15 1111: IO Disable
27:24	R/W	0xF	PK14_SELECT PK14 Select 0000: Input 0001: Output 0010: MCSIC-D1N 0011: UART7-RTS 0100: UART5-RTS 0101: NCSI-HSYNC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT14 1111: IO Disable
23:20	R/W	0xF	PK13_SELECT PK13 Select 0000: Input 0001: Output 0010: MCSIC-D0P 0011: UART7-RX 0100: TWI4-SDA 0101: NCSI-MCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT13 1111: IO Disable

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Offset: 0x0504			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PK12_SELECT PK12 Select 0000: Input 0001: Output 0010: MCSIC-D0N 0011: UART7-TX 0100: TWI4-SCK 0101: NCSI-PCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT12 1111: IO Disable
15:12	R/W	0xF	PK11_SELECT PK11 Select 0000: Input 0001: Output 0010: MCSIB-CKP 0011: TWI3-SDA 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT11 1111: IO Disable
11:8	R/W	0xF	PK10_SELECT PK10 Select 0000: Input 0001: Output 0010: MCSIB-CKN 0011: TWI3-SCK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT10 1111: IO Disable
7:4	R/W	0xF	PK9_SELECT PK9 Select 0000: Input 0001: Output 0010: MCSIB-D1P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT9 1111: IO Disable

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Offset: 0x0504			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PK8_SELECT PK8 Select 0000: Input 0001: Output 0010: MCSIB-D1N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT8 1111: IO Disable

8.6.6.102 0x0508 PK Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x0508			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK23_SELECT PK23 Select 0000: Input 0001: Output 0010: MCSID-CKP 0011: TWI3-SDA 0100: PWM7 0101: NCSI-D7 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT23 1111: IO Disable
27:24	R/W	0xF	PK22_SELECT PK22 Select 0000: Input 0001: Output 0010: MCSID-CKN 0011: TWI3-SCK 0100: PWM6 0101: NCSI-D6 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT22 1111: IO Disable

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Offset: 0x0508			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PK21_SELECT PK21 Select 0000: Input 0001: Output 0010: MCSID-D1P 0011: MIPI-MCLK1 0100: UART6-CTS 0101: NCSI-D5 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT21 1111: IO Disable
19:16	R/W	0xF	PK20_SELECT PK20 Select 0000: Input 0001: Output 0010: MCSID-D1N 0011: TWI2-SDA 0100: UART6-RTS 0101: NCSI-D4 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT20 1111: IO Disable
15:12	R/W	0xF	PK19_SELECT PK19 Select 0000: Input 0001: Output 0010: MCSID-D0P 0011: TWI2-SCK 0100: UART6-RX 0101: NCSI-D3 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT19 1111: IO Disable
11:8	R/W	0xF	PK18_SELECT PK18 Select 0000: Input 0001: Output 0010: MCSID-D0N 0011: MIPI-MCLK0 0100: UART6-TX 0101: NCSI-D2 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT18 1111: IO Disable

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Offset: 0x0508			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PK17_SELECT PK17 Select 0000: Input 0001: Output 0010: MCSIC-CKP 0011: TWI5-SDA 0100: UART5-RX 0101: NCSI-D1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT17 1111: IO Disable
3:0	R/W	0xF	PK16_SELECT PK16 Select 0000: Input 0001: Output 0010: MCSIC-CKN 0011: TWI5-SCK 0100: UART5-TX 0101: NCSI-D0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT16 1111: IO Disable

8.6.6.103 0x050C PK Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x050C			Register Name: PK_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.104 0x0510 PK Data Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: PK_DAT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0510			Register Name: PK_DAT
Bit	Read/Write	Default/Hex	Description
23:0	R/W	0	PK_DAT PK Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.6.105 0x0514 PK Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0514			Register Name: PK_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK7_DRV PK7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK6_DRV PK6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK5_DRV PK5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK4_DRV PK4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK3_DRV PK3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x0514			Register Name: PK_DRV0
Bit	Read/Write	Default/Hex	Description
11:10	/	/	/
9:8	R/W	0x1	PK2_DRV PK2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK1_DRV PK1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK0_DRV PK0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.106 0x0518 PK Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0518			Register Name: PK_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK15_DRV PK15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK14_DRV PK14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK13_DRV PK13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK12_DRV PK12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x0518			Register Name: PK_DRV1
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:12	R/W	0x1	PK11_DRV PK11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK10_DRV PK10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK9_DRV PK9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK8_DRV PK8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.107 0x051C PK Multi_Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x051C			Register Name: PK_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK23_DRV PK23 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK22_DRV PK22 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK21_DRV PK21 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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Offset: 0x051C			Register Name: PK_DRV2
Bit	Read/Write	Default/Hex	Description
19:18	/	/	/
17:16	R/W	0x1	PK20_DRV PK20 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK19_DRV PK19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK18_DRV PK18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK17_DRV PK17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK16_DRV PK16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.6.108 0x0520 PK Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: PK_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.109 0x0524 PK Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PK15_PULL PK15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0524			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x0	PK14_PULL PK14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PK13_PULL PK13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PK12_PULL PK12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PK11_PULL PK11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PK10_PULL PK10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PK9_PULL PK9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PK8_PULL PK8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PK7_PULL PK7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PK6_PULL PK6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PK5_PULL PK5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0524			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	PK4_PULL PK4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PK3_PULL PK3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PK2_PULL PK2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PK1_PULL PK1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PK0_PULL PK0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.110 0x0528 PK Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0528			Register Name: PK_PUL1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	R/W	0x0	PK23_PULL PK23 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PK22_PULL PK22 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PK21_PULL PK21 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0528			Register Name: PK_PUL1
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	PK20_PULL PK20 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PK19_PULL PK19 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PK18_PULL PK18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PK17_PULL PK17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PK16_PULL PK16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.6.111 0x0220 PB External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0220			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0220			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.112 0x0224 PB External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PB_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0224			Register Name: PB_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.113 0x0228 PB External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PB_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.114 0x022C PB External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PB_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.115 0x0230 PB External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PB_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable

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Offset: 0x0230			Register Name: PB_INT_CTL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.116 0x0234 PB External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/

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Offset: 0x0234			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0234			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.117 0x0238 PB External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PB_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

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Offset: 0x0238			Register Name: PB_INT_DEB
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.6.6.118 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.119 0x0244 PC External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0244			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.120 0x0248 PC External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PC_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0248			Register Name: PC_INT_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.121 0x024C PC External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: PC_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.122 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable

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Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable

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Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.123 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.124 0x0258 PC External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

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8.6.6.125 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0260			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.126 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: PD_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0264			Register Name: PD_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.127 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.128 0x026C PD External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: PD_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.129 0x0270 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_CTL External INT23 Enable 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable

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Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable

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Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.130 0x0274 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.131 0x0278 PD External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: PD_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

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8.6.6.132 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.133 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.134 0x0288 PE External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: PE_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.135 0x028C PE External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: PE_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.136 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable

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Offset: 0x0290			Register Name: PE_INT_CTL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

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8.6.6.137 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.138 0x0298 PE External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.6.6.139 0x02A0 PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x02A0			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x02A0			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.140 0x02A4 PF External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02A4			Register Name: PF_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.141 0x02A8 PF External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PF_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.142 0x02AC PF External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: PF_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.143 0x02B0 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable

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Offset: 0x02B0			Register Name: PF_INT_CTL
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.144 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_INT_STA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x02B4			Register Name: PF_INT_STA
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.145 0x02B8 PF External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

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8.6.6.146 0x02C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x02C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.147 0x02C4 PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

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Offset: 0x02C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x02C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.148 0x02C8 PG External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02C8			Register Name: PG_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.149 0x02CC PG External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02CC			Register Name: PG_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.150 0x02D0 PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable

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Offset: 0x02D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable

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Offset: 0x02D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.151 0x02D4 PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x02D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x02D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.152 0x02D8 PG External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PG_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

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8.6.6.153 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.154 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.155 0x02E8 PH External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: PH_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x02E8			Register Name: PH_INT_CFG2
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.156 0x02EC PH External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: PH_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.157 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable

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Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable

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Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.158 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.159 0x02F8 PH External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/

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Offset: 0x02F8			Register Name: PH_INT_DEB
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.6.6.160 0x0300 PI External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: PI_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0300			Register Name: PI_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.161 0x0304 PI External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: PI_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0304			Register Name: PI_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.162 0x0308 PI External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: PI_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

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Offset: 0x0308			Register Name: PI_INT_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.163 0x030C PI External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x030C			Register Name: PI_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.6.164 0x0310 PI External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: PI_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable

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Offset: 0x0310			Register Name: PI_INT_CTL
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable

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Offset: 0x0310			Register Name: PI_INT_CTL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.165 0x0314 PI External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: PI_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0314			Register Name: PI_INT_STA
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0314			Register Name: PI_INT_STA
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.166 0x0318 PI External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: PI_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

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8.6.6.167 0x0320 PJ External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: PJ_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0320			Register Name: PJ_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.168 0x0324 PJ External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: PJ_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0324			Register Name: PJ_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.169 0x0328 PJ External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: PJ_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0328			Register Name: PJ_INT_CFG2
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.170 0x032C PJ External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x032C			Register Name: PJ_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x032C			Register Name: PJ_INT_CFG3
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT27_CFG External INT27 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT26_CFG External INT26 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT25_CFG External INT25 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT24_CFG External INT24 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.171 0x0330 PJ External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: PJ_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

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Offset: 0x0330			Register Name: PJ_INT_CTL
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	EINT27_CTL External INT27 Enable 0: Disable 1: Enable
26	R/W	0x0	EINT26_CTL External INT26 Enable 0: Disable 1: Enable
25	R/W	0x0	EINT25_CTL External INT25 Enable 0: Disable 1: Enable
24	R/W	0x0	EINT24_CTL External INT24 Enable 0: Disable 1: Enable
23	R/W	0x0	EINT23_CTL External INT23 Enable 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable

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Offset: 0x0330			Register Name: PJ_INT_CTL
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable

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Offset: 0x0330			Register Name: PJ_INT_CTL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.172 0x0334 PJ External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: PJ_INT_STA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

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Offset: 0x0334			Register Name: PJ_INT_STA
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	EINT27_STATUS External INT27 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
26	R/W	0x0	EINT26_STATUS External INT26 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
25	R/W	0x0	EINT25_STATUS External INT25 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
24	R/W	0x0	EINT24_STATUS External INT24 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
23	R/W	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0334			Register Name: PJ_INT_STA
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0334			Register Name: PJ_INT_STA
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0334			Register Name: PJ_INT_STA
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.173 0x0338 PJ External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: PJ_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

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8.6.6.174 0x0340 PK External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PK_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0340			Register Name: PK_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.175 0x0344 PK External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PK_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0344			Register Name: PK_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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8.6.6.176 0x0348 PK External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0348			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.6.177 0x034C PK External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x034C			Register Name: PK_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.6.178 0x0350 PK External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_CTL External INT23 Enable 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable

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Offset: 0x0350			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable

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Offset: 0x0350			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.6.179 0x0354 PK External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.6.180 0x0358 PK External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: PK_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

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8.6.6.181 0x0380 GPIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0380			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x1	VCCIO_PWR_MOD_SEL VCC_IO POWER MODE Select 1: 3.3V 0: 1.8V
11	/	/	/
10	R/W	0x1	PK_PWR_MOD_SEL PK_POWER MODE Select 1: 3.3V 0: 1.8V If PK_Port Power Source select VCC_IO, this bit is invalid
9	R/W	0x1	PJ_PWR_MOD_SEL PJ_POWER MODE Select 1: 3.3V 0: 1.8V If PJ_Port Power Source select VCC_IO, this bit is invalid
8	R/W	0x1	PI_PWR_MOD_SEL PI_POWER MODE Select 1: 3.3V 0: 1.8V If PI_Port Power Source select VCC_IO, this bit is invalid
7	/	/	/
6	R/W	0x1	PG_PWR_MOD_SEL PG_POWER MODE Select 1: 3.3V 0: 1.8V If PG_Port Power Source select VCC_IO, this bit is invalid
5	R/W	0x1	PF_PWR_MOD_SEL PF_POWER MODE Select 1: 3.3V 0: 1.8V If PF_Port Power Source select VCC_IO, this bit is invalid

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Offset: 0x0380			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
4	R/W	0x1	PE_PWR_MOD_SEL PE_POWER MODE Select 1: 3.3V 0: 1.8V If PE_Port Power Source select VCC_IO, this bit is invalid
3	R/W	0x1	PD_PWR_MOD_SEL PD_POWER MODE Select 1: 3.3V 0: 1.8V If PD_Port Power Source select VCC_IO, this bit is invalid
2	R/W	0x1	PC_PWR_MOD_SEL PC_POWER MODE Select 1: 3.3V 0: 1.8V If PC_Port Power Source select VCC_IO, this bit is invalid
1	R/W	0x1	PB_PWR_MOD_SEL PB_POWER MODE Select 1: 3.3V 0: 1.8V If PB_Port Power Source select VCC_IO, this bit is invalid
0	/	/	/

8.6.6.182 0x0384 GPIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0384			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL VCC_IO Withstand Voltage Mode Select Control 0: Enable 1: Disable
11	/	/	/

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Offset: 0x0384			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	VCC_PK_WS_VOL_MOD_SEL VCC_PK Withstand Voltage Mode Select Control. 0: Enable 1: Disable
9	R/W	0x0	VCC_PJ_WS_VOL_MOD_SEL VCC_PJ Withstand Voltage Mode Select Control 0: Enable 1: Disable
8	R/W	0x0	VCC_PI_WS_VOL_MOD_SEL VCC_PI Withstand Voltage Mode Select Control 0: Enable 1: Disable
7	/	/	/
6	R/W	0x0	VCC_PG_WS_VOL_MOD_SEL VCC_PG Withstand Voltage Mode Select Control 0: Enable 1: Disable
5	R/W	0x0	VCC_PF_WS_VOL_MOD_SEL VCC_PF Withstand Voltage Mode Select Control 0: Enable 1: Disable
4	R/W	0x0	VCC_PE_WS_VOL_MOD_SEL VCC_PE Withstand Voltage Mode Select Control 0: Enable 1: Disable
3	R/W	0x0	VCC_PD_WS_VOL_MOD_SEL VCC_PD Withstand Voltage Mode Select Control 0: Enable 1: Disable
2	R/W	0x0	VCC_PC_WS_VOL_MOD_SEL VCC_PC Withstand Voltage Mode Select Control 0: Enable 1: Disable

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Offset: 0x0384			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	VCC_PB_WS_VOL_MOD_SEL VCC_PB Withstand Voltage Mode Select Control 0: Enable 1: Disable
0	/	/	/

8.6.6.183 0x0388 GPIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0388			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	VCCIO_PWR_VAL VCC_IO Power Value
15:11	/	/	/
10	R	0x0	PK_PWR_VAL PK_Port Power Value 0:3.3V 1:1.8V If PK_Port Power Source select VCC_IO, this bit is invalid
9	R	0x0	PJ_PWR_VAL PJ_Port Power Value 0:3.3V 1:1.8V If PJ_Port Power Source select VCC_IO, this bit is invalid
8	R	0x0	PI_PWR_VAL PI_Port Power Value 0:3.3V 1:1.8V If PI_Port Power Source select VCC_IO, this bit is invalid
7	/	/	/
6	R	0x0	PG_PWR_VAL PG_Port Power Value 0:3.3V 1:1.8V If PG_Port Power Source select VCC_IO, this bit is invalid

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Offset: 0x0388			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
5	R	0x0	PF_PWR_VAL PF_Port Power Value 0:3.3V 1:1.8V If PF_Port Power Source select VCC_IO, this bit is invalid
4	R	0x0	PE_PWR_VAL PE_Port Power Value 0:3.3V 1:1.8V If PE_Port Power Source select VCC_IO, this bit is invalid
3	R	0x0	PD_PWR_VAL PD_Port Power Value 0:3.3V 1:1.8V If PD_Port Power Source select VCC_IO, this bit is invalid
2	R	0x0	PC_PWR_VAL PC_Port Power Value 0:3.3V 1:1.8V If PC_Port Power Source select VCC_IO, this bit is invalid
1	R	0x0	PB_PWR_VAL PB_Port Power Value 0:3.3V 1:1.8V If PB_Port Power Source select VCC_IO, this bit is invalid
0	/	/	/

8.6.6.184 0x0390 GPIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0390			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0390			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control 0: 1.8V 1: 3.3V

8.6.7 S_GPIO Register Description

8.6.7.1 0x0000 PL Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PL7_SELECT PL7 Select 0000: Input 0001: Output 0010: S-JTAG-DI 0011: S-PWM7 0100: S-I2S0-DOUT1 0101: S-I2S0-DIN0 0110: DMIC-DATA1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT7 1111: IO Disable
27:24	R/W	0xF	PL6_SELECT PL6 Select 0000: Input 0001: Output 0010: S-JTAG-DO 0011: S-PWM6 0100: S-I2S0-DIN1 0101: S-I2S0-DOUT0 0110: DMIC-DATA2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT6 1111: IO Disable

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Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PL5_SELECT PL5 Select 0000: Input 0001: Output 0010: S-JTAG-CK 0011: S-CAN-RX0 0100: S-PWM5 0101: S-I2S0-LRCK 0110: DMIC-DATA3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT5 1111: IO Disable
19:16	R/W	0xF	PL4_SELECT PL4 Select 0000: Input 0001: Output 0010: S-JTAG-MS 0011: S-CAN-TX0 0100: S-PWM4 0101: S-I2S0-BCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT4 1111: IO Disable
15:12	R/W	0xF	PL3_SELECT PL3 Select 0000: Input 0001: Output 0010: S-UART0-RX 0011: S-UART1-RX 0100: S-PWM3 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT3 1111: IO Disable
11:8	R/W	0xF	PL2_SELECT PL2 Select 0000: Input 0001: Output 0010: S-UART0-TX 0011: S-UART1-TX 0100: S-PWM2 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT2 1111: IO Disable

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Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PL1_SELECT PL1 Select 0000: Input 0001: Output 0010: S-TWI0-SDA 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT1 1111: IO Disable
3:0	R/W	0xF	PL0_SELECT PL0 Select 0000: Input 0001: Output 0010: S-TWI0-SCK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT0 1111: IO Disable

8.6.7.2 0x0004 PL Configure Register 1 (Default Value: 0x00FF_FFFF)

Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0xF	PL13_SELECT PL13 Select 0000: Input 0001: Output 0010: S-TWI2-SDA 0011: S-PWM9 0100: S-UART0-RX 0101: DMIC-DATA3 0110: S-SPI0-MISO 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT13 1111: IO Disable

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Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PL12_SELECT PL12 Select 0000: Input 0001: Output 0010: S-TWI2-SCK 0011: S-PWM8 0100: S-UART0-TX 0101: DMIC-DATA2 0110: S-SPI0-MOSI 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT12 1111: IO Disable
15:12	R/W	0xF	PL11_SELECT PL11 Select 0000: Input 0001: Output 0010: S-IR-RX 0011: Reserved 0100: S-RJTAG-DI 0101: S-DMIC-DATA1 0110: S-SPI0-CLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT11 1111: IO Disable
11:8	R/W	0xF	PL10_SELECT PL10 Select 0000: Input 0001: Output 0010: S-PWM0 0011: Reserved 0100: S-RJTAG-DO 0101: S-DMIC-DATA0 0110: S-SPI0-CS0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT10 1111: IO Disable
7:4	R/W	0xF	PL9_SELECT PL9 Select 0000: Input 0001: Output 0010: S-TWI1-SDA 0011: Reserved 0100: S-RJTAG-CK 0101: S-PWM1 0110: S-DMIC-CLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT9 1111: IO Disable

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Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PL8_SELECT PL8 Select 0000: Input 0001: Output 0010: S-TWI1-SCK 0011: Reserved 0100: S-RJTAG-MS 0101: S-I2S0-MCLK 0110: S-DMIC-DATA0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT8 1111: IO Disable

8.6.7.3 0x0008 PL Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PL_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.4 0x000C PL Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PL_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.5 0x0010 PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	PL_DAT PL Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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8.6.7.6 0x0014 PL Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PL7_DRV PL7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PL6_DRV PL6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PL5_DRV PL5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PL4_DRV PL4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PL3_DRV PL3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PL2_DRV PL2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PL1_DRV PL1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/

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Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	PL0_DRV PL0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.7.7 0x0018 PL Multi_Driving Register 1 (Default Value: 0x0011_1111)

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PL13_DRV PL13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PL12_DRV PL12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PL11_DRV PL11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PL10_DRV PL10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PL9_DRV PL9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PL8_DRV PL8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

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8.6.7.8 0x001C PL Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PL_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.9 0x0020 PL Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PL_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.10 0x0024 PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x0	PL13_PULL PL13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PL12_PULL PL12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PL11_PULL PL11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PL10_PULL PL10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PL9_PULL PL9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

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Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
15:14	R/W	0x0	PL7_PULL PL7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x1	PL1_PULL PL1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.7.11 0x0028 PL Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PL_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.7.12 0x0030 PM Configure Register 0 (Default Value: 0x00FF_FFFF)

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0xF	PM5_SELECT PM5 Select 0000: Input 0001: Output 0010: S-IR-RX 0011: S-RJTAG-DI 0100: S-TWI2-SDA 0101: S-PWM9 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT5 1111: IO Disable
19:16	R/W	0xF	PM4_SELECT PM4 Select 0000: Input 0001: Output 0010: S-PWM8 0011: S-RJTAG-DO 0100: S-TWI2-SCK 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT4 1111: IO Disable
15:12	R/W	0xF	PM3_SELECT PM3 Select 0000: Input 0001: Output 0010: S-TWI1-SDA 0011: S-RJTAG-CK 0100: S-PWM7 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT3 1111: IO Disable

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Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PM2_SELECT PM2 Select 0000: Input 0001: Output 0010: S-TWI1-SCK 0011: S-RJTAG-MS 0100: S-PWM6 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT2 1111: IO Disable
7:4	R/W	0xF	PM1_SELECT PM1 Select 0000: Input 0001: Output 0010: S-UART0-RX 0011: S-UART1-RX 0100: S-PWM3 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT1 1111: IO Disable
3:0	R/W	0xF	PM0_SELECT PM0 Select 0000: Input 0001: Output 0010: S-UART0-TX 0011: S-UART1-TX 0100: S-PWM2 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT0 1111: IO Disable

8.6.7.13 0x0034 PM Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PM_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.7.14 0x0038 PM Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PM_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.15 0x003C PM Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PM_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.16 0x0040 PM Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PM_DAT
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0	PM_DAT PM Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.6.7.17 0x0044 PM Multi_Driving Register 0 (Default Value: 0x0011_1111)

Offset: 0x0044			Register Name: PM_DRV0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PM5_DRV PM5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

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Offset: 0x0044			Register Name: PM_DRV0
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x1	PM4_DRV PM4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PM3_DRV PM3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PM2_DRV PM2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PM1_DRV PM1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PM0_DRV PM0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.6.7.18 0x0048 PM Multi_Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: PM_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.19 0x004C PM Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: PM_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.7.20 0x0050 PM Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: PM_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.21 0x0054 PM Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PM_PUL0
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:10	R/W	0x0	PM5_PULL PM5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PM4_PULL PM4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PM3_PULL PM3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PM2_PULL PM2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PM1_PULL PM1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PM0_PULL PM0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.6.7.22 0x0058 PM Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PM_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.7.23 0x0200 PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PL_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0200			Register Name: PL_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.7.24 0x0204 PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.7.25 0x0208 PL External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PL_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.26 0x020C PL External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PL_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.27 0x0210 PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable

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Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable

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Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.6.7.28 0x0214 PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_INT_STA
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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Offset: 0x0214			Register Name: PL_INT_STA
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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8.6.7.29 0x0218 PL External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.6.7.30 0x0220 PM External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PM_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

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Offset: 0x0220			Register Name: PM_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.6.7.31 0x0224 PM External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PM_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.6.7.32 0x0228 PM External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PM_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.33 0x022C PM External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PM_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.6.7.34 0x0230 PM External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PM_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

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8.6.7.35 0x0234 PM External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PM_INT_STA
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.6.7.36 0x0238 PM External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PM_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

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Offset: 0x0238			Register Name: PM_INT_DEB
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.6.7.37 0x0340 GPIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0003)

Offset: 0x0340			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VCCIO_PWR_MOD_SEL VCC-IO POWER MODE Select 1: 3.3V 0: 1.8V
11:2	/	/	/
1	R/W	0x1	PM_PWR_MOD_SEL PM_POWER MODE Select 1: 3.3V 0: 1.8V If PM_Port Power Source select VCC-IO, this bit is invalid
0	R/W	0x1	PL_PWR_MOD_SEL PL_POWER MODE Select 1: 3.3V 0: 1.8V If PL_Port Power Source select VCC_IO, this bit is invalid

8.6.7.38 0x0344 GPIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

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Offset: 0x0344			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL VCC_IO Withstand Voltage Mode Select Control 0: Enable 1: Disable
11:2	/	/	/
1	R/W	0x0	VCC_PM_WS_VOL_MOD_SEL VCC_PM Withstand Voltage Mode Select Control 0: Enable 1: Disable
0	R/W	0x0	VCC_PL_WS_VOL_MOD_SEL VCC_PL Withstand Voltage Mode Select Control 0: Enable 1: Disable

8.6.7.39 0x0348 GPIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	VCCIO_PWR_VAL VCC_IO Power Value
15:2	/	/	/
1	R	0x0	PM_PWR_VAL PM_Port Power Value If PM_Port Power Source select VCC_IO, this bit is invalid
0	R	0x0	PL_PWR_VAL PL_Port Power Value If PL_Port Power Source select VCC_IO, this bit is invalid

8.6.7.40 0x0350 GPIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0350			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control 0: 1.8V 1: 3.3V

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8.7 LEDC

8.7.1 Overview

The LEDC is used to control the external LED lamp.

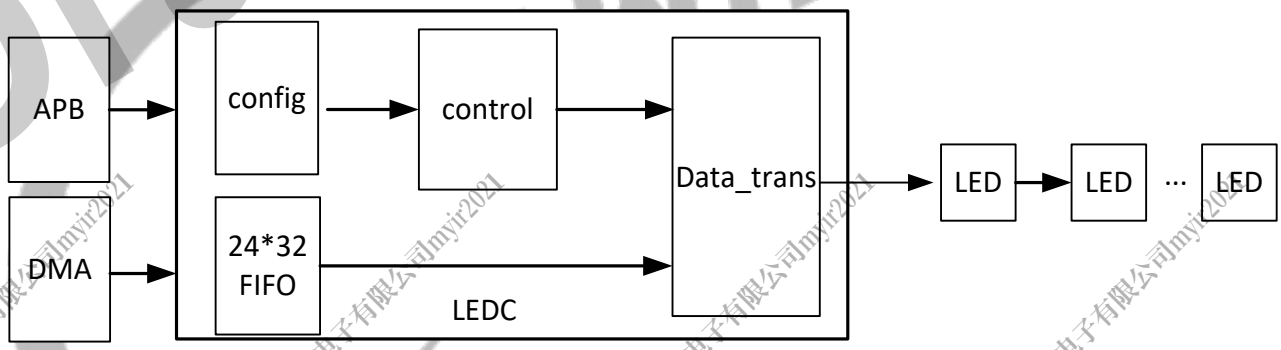
The LEDC has the following features:

- Configurable LED output high-/low-level width
- Configurable LED reset time
- Configurable interval time for packets and frame data
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s
- Configurable RGB display mode

8.7.2 Block Diagram

The following figure shows a block diagram of the LEDC.

Figure 8-38 LEDC Block Diagram



LEDC contains the following sub-blocks:

Table 8-26 LEDC Sub-blocks

Sub-block	Description
config	register configuration
control	LEDC timing control and status control
FIFO	24-bit width x 32 depth
Data_trans	Convert input data to the 0 and 1 characters of LED

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8.7.3 Functional Description

8.7.3.1 External Signals

The following table describes the external signals of the LEDC.

Table 8-27 LEDC External Signals

Signal Name	Description	Type
LEDC	Intelligent Control LED Signal Output	O

8.7.3.2 Clock Sources

The following table describes the clock sources of the LEDC.

Table 8-28 LEDC Clock Sources

Clock Sources	Description	module
HOSC	24 MHz	CCU
PERI0_600M	Peripheral Clock. The default value is 600 MHz	

8.7.3.3 Reset

The following table describes the reset of the LEDC.

Table 8-29 LEDC Reset

Reset signal	Source
LEDC_RST	CCU

8.7.3.4 LEDC Timing

Figure 8-39 LEDC Package Output Timing Diagram

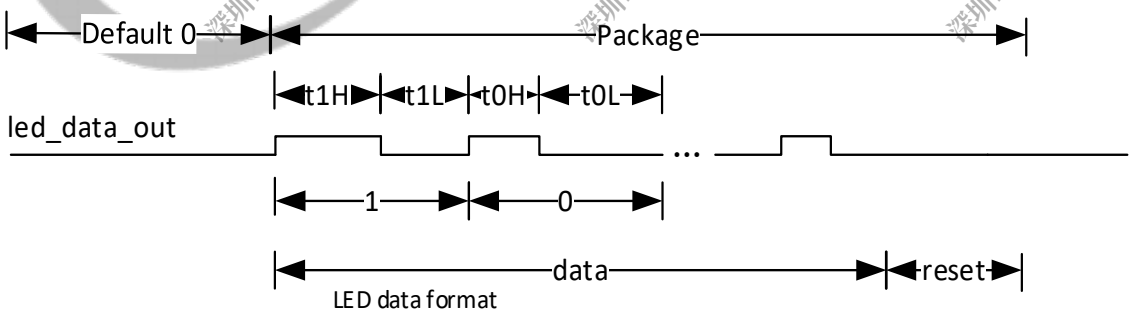

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Figure 8-40 LEDC 1-frame Output Timing Diagram

8.7.3.5 LEDC Input Data Structure

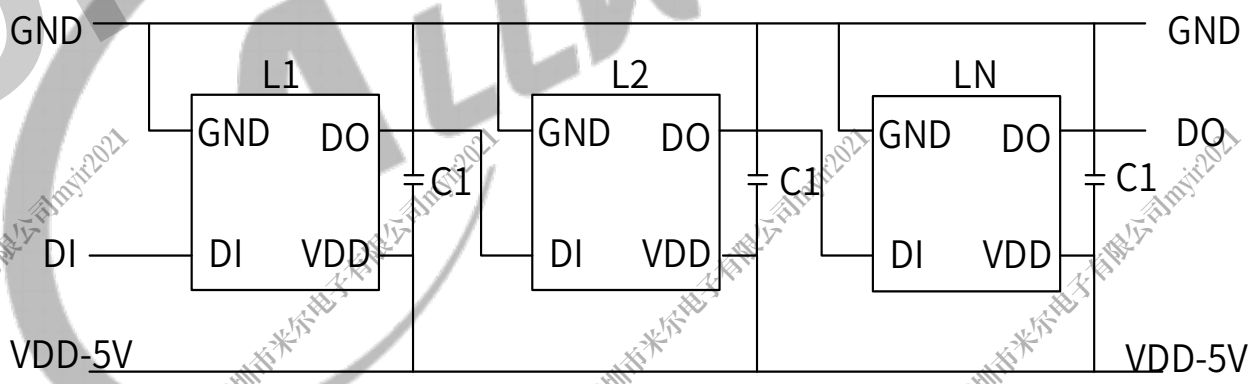
The RGB mode of LEDC data is configurable. By default, the data is sent in GRB order, and the higher bit is transmitted first.

Figure 8-41 LEDC Input Data Structure

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

8.7.3.6 LEDC Typical Circuit

Figure 8-42 LEDC Typical Circuit



C1 is the filter capacitor of LED light, and its value is usually 100 Nf.

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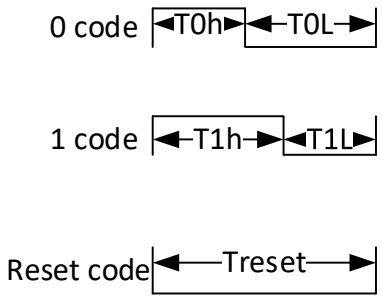
8.7.3.7 LEDC Data Input Code

Figure 8-43 LEDC Data Input Code



8.7.3.8 LEDC Data Transfer Time

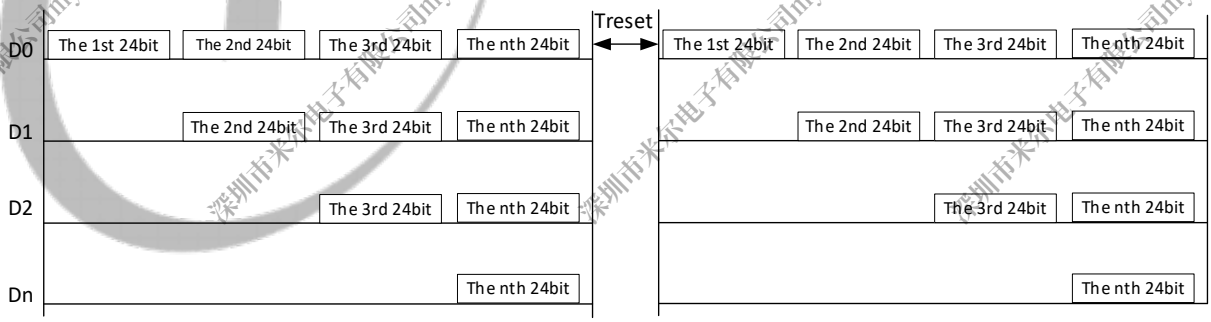
The time parameter of the typical LED specification shows as follows.

Table 8-30 Time Parameters of Typical LED Specification

T0H	0 code, high-level time	220 ns to 380 ns
T0L	0 code, low-level time	580 ns to 1.6 us
T1H	1 code, high-level time	580 ns to 1.6 us
T1L	1 code, low-level time	220 ns to 420 ns
RESET	Frame unit, low-level time	> 280 us

8.7.3.9 LEDC Data Transfer Mode

Figure 8-44 LEDC Data Transfer Mode



8.7.3.10 LEDC Parameter

- PAD rate > 800 kbit/s
- LED number supported: $T_{0\text{-code}}$: 800 ns to 1980 ns, $T_{1\text{-code}}$: 800 ns to 2020 ns

When the LED refresh rate is 30 frame/s, LED number supported is (1 s/30-280 us)/ ((800 ns to 2020 ns) *24) =1023 to 681.

When the LED refresh rate is 60 frame/s, LED number supported is (1 s/60-280 us)/ ((800 ns to 2020 ns) *24) =853 to 337.

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8.7.3.11 LEDC Data Transfer

The LEDC supports DMA data transfer mode or CPU data transfer mode. The DMA data transfer mode is set by LEDC_DMA_EN

- Data transfer in DMA mode

When the valid space of internal FIFO is greater than the setting FIFO free space threshold, the LEDC sends DMA_REQ to require DMA to transfer data from DRAM to LEDC. The maximum data transfer size in DMA mode is 16 words. (The internal FIFO level is 32.)

- Data transfer in CPU mode

When the valid space of internal FIFO is greater than the setting FIFO free space threshold, the LEDC sends LEDC_CPUREQ_INT to require CPU to transfer data to LEDC. The transfer data size in CPU mode is controlled by software. The internal FIFO destination address is 0x06700014. The data width is 32-bit. (The lower 24-bit is valid.)

8.7.3.12 LEDC Interrupt

Module Name	Description
FIFO_OVERFLOW_INT	FIFO overflow interrupt. The data written by external is more than the maximum storage space of LED FIFO, the LEDC will be in data loss state. At this time, software needs to deal with the abnormal situation. The processing mode is as follows. The software can query LED_FIFO_DATA_REG to determine which data has been stored in the internal FIFO of LEDC. The LEDC performs soft_reset operation to refresh all data.
FIFO_CPUREQ_INT	FIFO request CPU data interrupt When FIFO data is less than a threshold, the interrupt will be reported to the CPU.
LEDC_TRANS_FINISH_INT	Data transfer complete interrupt The value indicates that the data configured as total_data_length has been transferred completely.

LEDC interrupt usage scenario:

- CPU mode

The software can enable GLOBAL_INT_EN, FIFO_CPUREQ_INT_EN, WAITDATA_TIMEOUT_INT_EN, FIFO_OVERFLOW_INT_EN, LEDC_TRANS_FINISH_INT_EN, and cooperate with LEDC_FIFO_TRIG_LEVEL to use. When FIFO_CPUREQ_INT is set to 1, the software can configure data of LEDC_FIFO_TRIG_LEVEL to LEDC.

- DMA mode

The software can enable GLOBAL_INT_EN, WAITDATA_TIMEOUT_INT_EN, FIFO_OVERFLOW_INT_EN, LEDC_TRANS_FINISH_INT_EN, and cooperate with

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LEDC_FIFO_TRIG_LEVEL to use. When DMA receives LEDC DMA_REQ, DMA can transfer data of LEDC_FIFO_TRIG_LEVEL to LEDC.

8.7.4 Programming Guidelines

8.7.4.1 LEDC Normal Configuration Process

Step 1 Configure LEDC_CLK and bus pclk.

Step 2 Configure the written LEDC data.

Step 3 Configure LED_T01_TIMING_CTRL_REG, LEDC_DATA_FINISH_CNT_REG, LED_RESET_TIMING_CTRL_REG, LEDC_WAIT_TIME0_CTRL_REG, LEDC_DMA_CTRL_REG, LEDC_INTERRUPT_CTRL_REG. Configure 0-code, 1-code, reset time, LEDC waiting time, and the number of external connected LEDC and the threshold of DMA transfer data.

Step 4 Configure LEDC_CTRL_REG to enable LEDC_EN, the LEDC will start to output data.

Step 5 When the LEDC interrupt is pulled up, it indicates the configured data has transferred complete, at this time LED_EN will be set to 0, and the read/write point of LEDC FIFO is cleared to 0.

Step 6 Repeat step1, 2, 3, 4 to re-execute a new round of configuration, enable LEDC_EN, the LEDC will start new data transfer.

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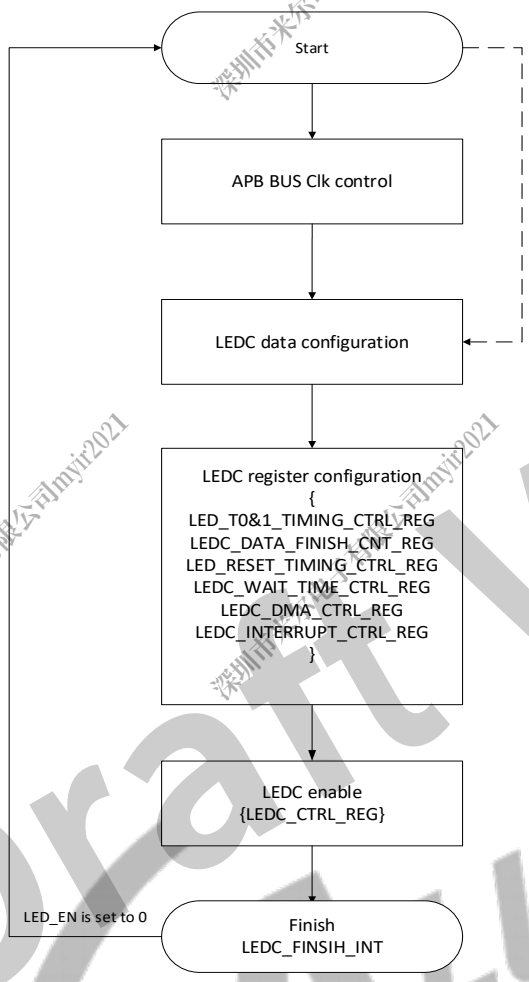
Figure 8-45 LEDC Normal Configuration Process



8.7.4.2 LEDC Abnormal Scene Processing Flow

WAITDATA_TIMEOUT Abnormal Status

Step 1 When WAITDATA_TIMEOUT_INT appears, it indicates the internal FIFO data request of LEDC cannot obtain a response, at this time if the default output level is low, then the external LED may think there was a reset operation and cause LED data to be flushed incorrectly.

Step 2 The LEDC needs to be performed soft_reset operation (LEDC_SOFT_RESET=1); after soft_reset, the LEDC_EN will be pulled-down automatically, all internal status register and control state machine will return to the idle state, the LEDC FIFO read & write point is cleared to 0, the LEDC interrupt is cleared.

Step 3 Setting reset_led_en to 1 indicates LEDC can actively send a reset operation to ensure the external LED lamp in the right state.

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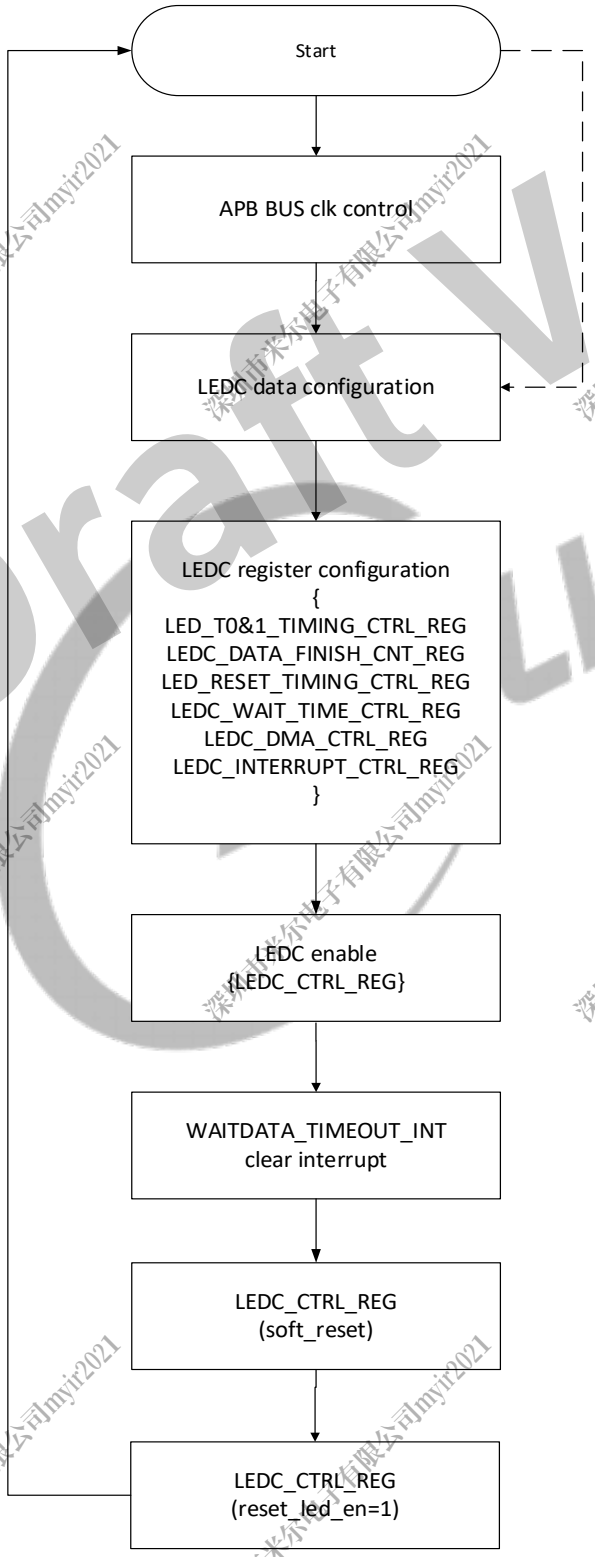
Step 4 The software reads the status of reset_led_en, when the status value is 1, it indicates LEDC does not perform the transmission of LED reset operation; when the status value is 0, the LEDC completes the transmission of LED reset operation.

Step 5 When LEDC reset operation finishes, the LEDC data and register configuration need to be re-operated to start re-transmission data operation.

Figure 8-46 LEDC Timeout Abnormal Processing Flow



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FIFO Overflow Abnormal Status

Step 1 When FIFO_OVERFLOW_INT appears, it indicates the data configured by software exceeds the LEDC FIFO space, at this time the redundant data will be lost.

Step 2 The software needs to read data in LEDC_FIFO_DATA_X to confirm the lost data.

Step 3 The software re-configures the lost data to the LEDC.

Step 4 If the software uses the soft_reset operation, the operation is the same with the timeout abnormal processing flow.

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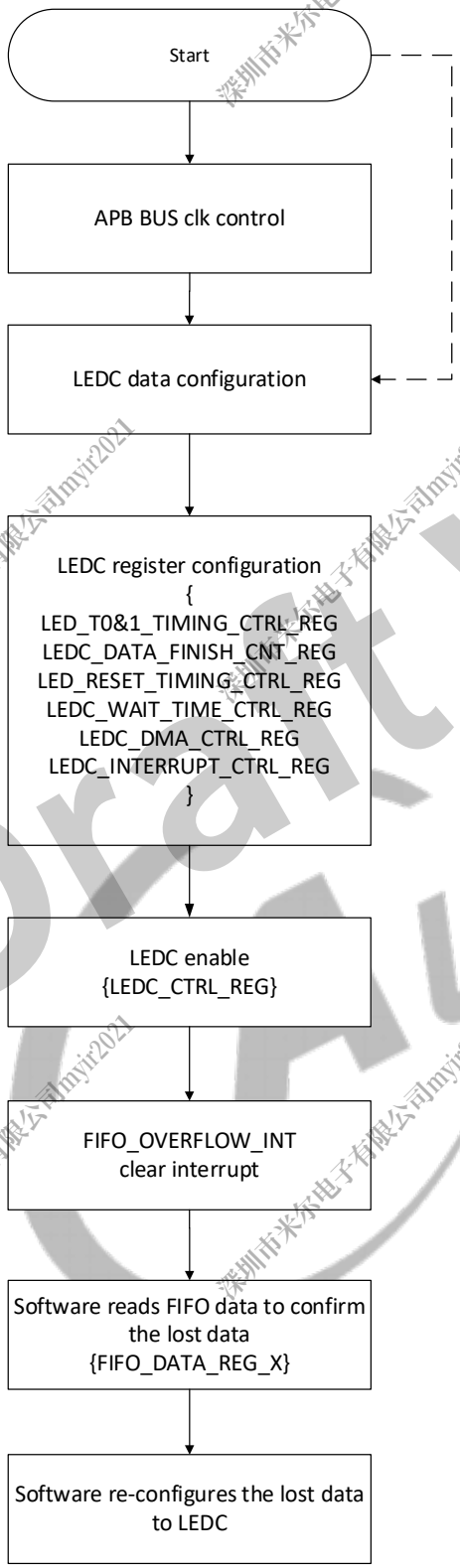
Figure 8-47 FIFO Overflow Abnormal Processing Flow



8.7.5 Register List

Module Name	Base Address
LEDC	0x02008000

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Register Name	Offset	Description
LEDC_CTRL_REG	0x0000	LEDC Control Register
LED_T01_TIMING_CTRL_REG	0x0004	LEDC T0 & T1 Timing Control Register
LEDC_DATA_FINISH_CNT_REG	0x0008	LEDC Data Finish Counter Register
LED_RESET_TIMING_CTRL_REG	0x000C	LEDC Reset Timing Control Register
LEDC_WAIT_TIME0_CTRL_REG	0x0010	LEDC Wait Time0 Control Register
LEDC_DATA_REG	0x0014	LEDC Data Register
LEDC_DMA_CTRL_REG	0x0018	LEDC DMA Control Register
LEDC_INT_CTRL_REG	0x001C	LEDC Interrupt Control Register
LEDC_INT_STS_REG	0x0020	LEDC Interrupt Status Register
LEDC_WAIT_TIME1_CTRL_REG	0x0028	LEDC Wait Time1 Control Register
LEDC_FIFO_DATA_REG	0x0030+0x04*N	LEDC FIFO Data Register

8.7.6 Register Description

8.7.6.1 0x0000 LEDC Control Register (Default Value: 0x0000_003C)

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	TOTAL_DATA_LENGTH Total length of transfer data (range: 0 to 8K, unit: 32-bit, only low 24-bit is valid) The field is recommended to be set to an integer multiple of (LED_NUM+1). If TOTAL_DATA_LENGTH is greater than (LED_NUM+1), but non-integer multiple, the last frame of data will transfer data less than (LED_NUM+1).
15:11	/	/	/

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Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
10	R/WAC	0x0	RESET_LED_EN Write operation: The software writes 1 to the bit, the CPU triggers LEDC to transfer a reset to LED. Only when LEDC is in IDLE status, the reset can be performed. After the reset finished, the control state machine returns to the IDLE status. To return LEDC to the IDLE status, it also needs to be used with SOFT_RESET. When the software sets the bit, the software can read the bit to check if the reset is complete. Read operation: 0: LEDC completes the transmission of the LED reset operation 1: LEDC does not complete the transmission of the LED reset operation
9	/	/	/

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8:6	R/W	0x0	LED_RGB_MODE 000 GRB (bypass) 001 GBR 010 RGB 011 RBG 100 BGR 101 BRG By default, the software configures data to LEDC according to GRB (MSB) mode, the LEDC internal combines data to output to the external LED. Other modes configure as follows.

Software Input Mode	Configuration	LEDC Output Mode
GRB	000	GRB
	001	GBR
	010	RGB
	011	RBG
	100	BGR
	101	BRG
GBR	000	GBR
	001	GRB
	010	BGR
	011	BRG
	100	RGB
	101	RBG
RGB	000	RGB
	001	RBG
	010	GRB
	011	GBR
	100	BRG
	101	BGR
RBG	000	RBG
	001	RGB
	010	BRG
	011	BGR
	100	GRB
	101	GBR
BGR	000	BGR
	001	BRG
	010	GBR
	011	GRB
	100	RBG
	101	RGB

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Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			BRG 000 BRG 001 BGR 010 RBG 011 RGB 100 GBR 101 GRB
5	R/W	0x1	LED_MSB_TOP Adjust sequence of the combined GRB data 0: LSB 1: MSB
4	R/W	0x1	LED_MSB_G MSB control for Green data 0: LSB 1: MSB
3	R/W	0x1	LED_MSB_R MSB control for Red data 0: LSB 1: MSB
2	R/W	0x1	LED_MSB_B MSB control for Blue data 0: LSB 1: MSB

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Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	LEDC_SOFT_RESET LEDC soft reset Write 1 to clear it automatically. The ranges of LEDC soft reset include the following points: all internal status registers, the control state machine returns to in idle status, the LEDC FIFO read & write point is cleared to 0, the LEDC interrupt is cleared; and the affected registers are followed. 1.LEDC_CTRL_REG (LEDC_EN is cleared to 0); 2. PLL_T0&1_TIMING_CTRL_REG remains unchanged; 3. LEDC_DATA_FINISH_CNT_REG (LEDC_DATA_FINISH_CNT is cleared to 0); 4.LED_RESET_TIMING_CTRL_REG remains unchanged; 5. LEDC_WAIT_TIME_CTRL_REG remains unchanged; 6. LEDC_DMA_CTRL_REG remains unchanged; 7. LEDC_INTERRUPT_CTRL_REG remains unchanged; 8.LEDC_INT_STS _REG is cleared to 0; 9. LEDC_CLK_GATING_REG remains unchanged; 10.LEDC_FIFO_DATA_REG remains unchanged;
0	R/W	0x0	LEDC_EN LEDC Enable 0: Disable 1: Enable That the bit is enabled indicates LEDC can be started when LEDC data finished transmission or LEDC_EN is cleared to 0 by hardware in LEDC_SOFT_RESET situation.

8.7.6.2 0x0004 LEDC T0 & T1 Timing Control Register (Default Value: 0x0286_01D3)

Offset: 0x0004			Register Name: LED_T01_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

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Offset: 0x0004			Register Name: LED_T01_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26:21	R/W	0x14	T1H_TIME LED T1H time Unit: cycle (24 MHz), t1h_time =42 ns*(N+1) The default value is 882 ns, the range is 80 ns–2560 ns. N: 1–3F. When is 0, t1h_time = 3F
20:16	R/W	0x6	T1L_TIME LED T1L time Unit: cycle (24 MHz), t1l_time =42 ns*(N+1) The default value is 294 ns, the range is 80 ns–1280 ns. N: 1–1F. When is 0, t1l_time = 1F
15:11	/	/	/
10:6	R/W	0x7	T0H_TIME LED T0h time Unit: cycle (24 MHz), t0h_time =42 ns*(N+1) The default value is 336 ns, the range is 80 ns–1280 ns. N: 1–1F. When is 0, t0h_time = 1F
5:0	R/W	0x13	T0L_TIME LED T0l time Unit: cycle (24 MHz), t0L_time =42 ns*(N+1) The default value is 840 ns, the range is 80 ns–2560 ns. N: 1–3F. When is 0, t0L_time = 3F

8.7.6.3 0x0008 LEDC Data Finish Counter Register (Default Value: 0x1D4C_0000)

Offset: 0x0008			Register Name: LEDC_DATA_FINISH_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x0008			Register Name: LEDC_DATA_FINISH_CNT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R/W	0x1D4C	LED_WAIT_DATA_TIME The value is the time that internal FIFO in LEDC is waiting for data. When the time is exceeded, the LEDC will send the wait_data_timeout_int interrupt. (This is an abnormal situation, software needs to reset LEDC.) The value is about 300 us by default. The adjust range is 80 ns–655 us. led_wait_data_time=42ns*(N+1). N: 1–1FFF. When the field is 0, LEDC_WAIT_DATA_TIME=1FFF
15:13	/	/	/
12:0	R	0x0	LED_DATA_FINISH_CNT The value is the total LED data that have been sent. (Range: 0–8k)

8.7.6.4 0x000C LEDC Reset Timing Control Register (Default Value: 0x1D4C_0000)

Offset: 0x000C			Register Name: LED_RESET_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x1D4C	TR_TIME Reset time control of LED lamp Unit: cycle (24 MHz), tr_time=42 ns*(N+1) The default value is 300 us. The adjust range is 80 ns–327 us. N: 1–1FFF If the value is 0, TR_TIME=1FFF.
15:10	/	/	/
9:0	R/W	0x0	LED_NUM The value is the number of external LED lamp. Maximum up to 1024. The default value 0 indicates that 1 LED lamp is external connected. The range is from 0 to 1023.

8.7.6.5 0x0010 LEDC Wait Time 0 Control Register (Default Value: 0x0000_00FF)

Offset: 0x0010			Register Name: LEDC_WAIT_TIME0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/

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Offset: 0x0010			Register Name: LEDC_WAIT_TIME0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	WAIT_TIM0_EN WAIT_TIME0 enable When it is 1, the controller automatically inserts waiting time between LED package data. 0: Disable 1: Enable
7:0	R/W	0xFF	TOTAL_WAIT_TIME0 Waiting time between 2 LED data. The LEDC output is low level. The adjust range is 80 ns–10 us. wait_time0=42 ns*(N+1) Unit: cycle(24 MHz) N: 1–FF

8.7.6.6 0x0014 LEDC Data Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: LEDC_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	LEDC DATA LED display data (the lower 24-bit is valid)

8.7.6.7 0x0018 LEDC DMA Control Register (Default Value: 0x0000_002F)

Offset: 0x0018			Register Name: LEDC_DMA_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x1	LEDC_DMA_EN LEDC DMA request enable 0: Disable request of DMA transfer data 1: Enable request of DMA transfer data
4:0	R/W	0x0F	LEDC_FIFO_TRIG_LEVEL The remaining space of internal FIFO in LEDC The internal FIFO in LEDC is 24*32. When the remaining space of internal FIFO in LEDC is more than or equal to LEDFIFO_TRIG_LEVEL, the DMA or the CPU request will generate. The default value is 15. The adjusted value is from 1 to 31. The recommended configuration is 7 or 15. When the configuration value is 0, LEDFIFO_TRIG_LEVEL=F.

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8.7.6.8 0x001C LEDC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: LEDC_INTERRUPT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	GLOBAL_INT_EN Global interrupt enable 0: Disable 1: Enable
4	R/W	0x0	FIFO_OVERFLOW_INT_EN FIFO overflow interrupt enable When the data written by the software is more than the internal FIFO level of LEDC, the LEDC is in the data loss state. 0: Disable 1: Enable
3	R/W	0x0	WAITDATA_TIMEOUT_INT_EN The internal FIFO in LEDC cannot get data because of some abnormal situation, after the time of led_wait_data_time, the interrupt will be enabled. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	FIFO_CPUREQ_INT_EN FIFO request CPU data interrupt enable 0: Disable 1: Enable
0	R/W	0x0	LED_TRANS_FINISH_INT_EN Data transmission complete interrupt enable 0: Disable 1: Enable

8.7.6.9 0x0020 LEDC Interrupt Status Register (Default Value: 0x0002_0000)

Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x1	FIFO_EMPTY FIFO empty status flag
16	R	0x0	FIFO_FULL FIFO full status flag

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Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
15:10	R	0x0	FIFO_WLW FIFO internal valid data depth It indicates the space FIFO has been occupied.
9:5	/	/	/
4	R/W1C	0x0	FIFO_OVERFLOW_INT FIFO overflow interrupt The data written by external is more than the maximum storage space of LED FIFO, the LEDC will be in the data loss state. At this time, the software needs to deal with the abnormal situation. The processing mode is as follows. The software can query LED_FIFO_DATA_REG to determine which data has been stored in the internal FIFO of LEDC. The LEDC performs soft_reset operation to refresh all data. 0: FIFO not overflow 1: FIFO overflow
3	R/W1C	0x0	WAITDATA_TIMEOUT_INT When internal FIFO of LEDC cannot get data because of some abnormal situation, after led_wait_data_time, the timeout interrupt is set, the LEDC is in WAIT_DATA state; in the course of wait_data, if the new data arrives, the LEDC will continue to send data, at this time software needs to notice whether the waiting time of LEDC exceeds the operation time of reset. If the waiting time of LEDC exceeds the operation time of reset (this is equivalent to reset operation sent by LEDC), the LED may enter in refresh state, the data has not been sent. 0: LEDC not timeout 1: LEDC timeout
2	/	/	/
1	R/W1C	0x0	FIFO_CPUREQ_INT FIFO request CPU data interrupt When FIFO data is less than the threshold, the interrupt will be reported to the CPU. 0: FIFO does not request that CPU transfers data 1: FIFO requests that CPU transfers data

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Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	LED_TRANS_FINISH_INT Data transfer complete interrupt The value indicates that the data configured as total_data_length is transferred completely. 0: Data is not transferred completely 1: Data is transferred completely

8.7.6.10 0x0028 LEDC Wait Time 1 Control Register (Default Value: 0x01FF_FFFF)

Offset: 0x0028			Register Name: LEDC_WAIT_TIME1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WAIT_TIM1_EN 0: Disable 1: Enable WAIT_TIME1 enable When the bit is 1, the controller automatically inserts the waiting time between the LED frame data.
30:0	R/W	0x01FFFFFF	TOTAL_WAIT_TIME1 Waiting time between 2 frame data. The LEDC output is low level. The adjust range is 80 ns– 85 s. wait_time1=42 ns*(N+1) Unit: cycle (24 MHz) N: 0x80–0x7FFFFFFF If the value is 0, TOTAL_WAIT_TIME1=0x7FFFFFFF

8.7.6.11 0x0030+N*0x04 LEDC FIFO Data Register X (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x04 (N=0–31)			Register Name: LEDC_FIFO_DATA_X
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LEDC_FIFO_DATA_X Internal FIFO data of LEDC The lower 24-bit is valid.

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8.8 Low rate ADC (LRADC)

8.8.1 Overview

The low rate analog-to-digital converter (LRADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection.

The LRADC has the following features:

- 2-ch LRADC input
- 6-bit resolution
- Sampling rate up to 2 KHz
- Supports hold key and general key
- Support normal, continue and single work mode
- Power supply voltage:1.8V, power reference voltage:1.35V

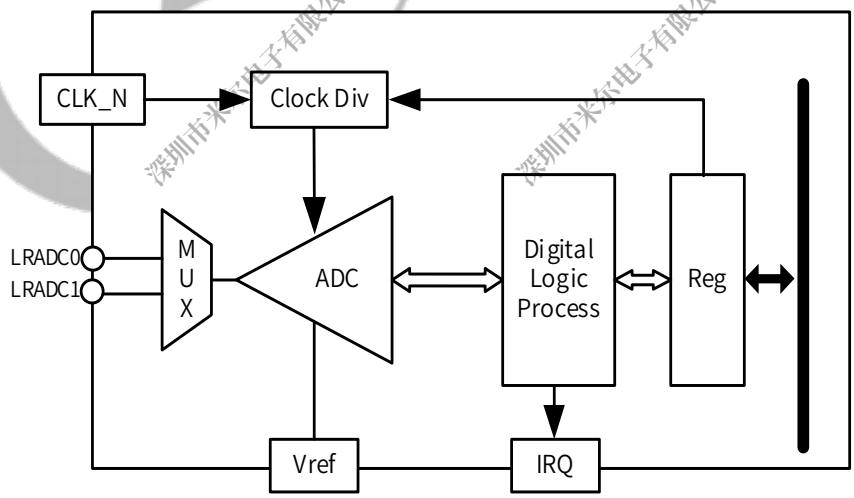
NOTE

The LRADC has a 6-bit resolution, 1-bit offset error, and 1-bit precision error. After the LRADC calibrates 1-bit offset error, the LRADC has 5-bit precision.

8.8.2 Block Diagram

The following figure shows the block diagram of the LRADC.

Figure 8-48 LRADC Block Diagram



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8.8.3 Functional Description

8.8.3.1 External Signals

The following table describes the external signals of the LRADC. The LRADC pin is the analog input signal.

Table 8-31 LRADC External Signals

Signal Name	Description	Type
LRADC0	Low Rate ADC	AI
LRADC1	Low Rate ADC	AI

8.8.3.2 Clock Source

The LRADC has one clock source. The following table describes the clock source for LRADC.

Table 8-32 LRADC Clock Sources

Clock Source	Description
LOSC	32.768 kHz LOSC

8.8.3.3 LRADC Working Mode

- Normal Mode

The LRADC gathers 8 samples, the average value of these 8 samples is updated in the data register, and the data interrupt sign is enabled. It is sampled repeatedly according to this mode until the LRADC is disabled.

- Continuous Mode

The LRADC gathers 8 samples every other 8*(N+1) sample cycle. The average value of every 8 samples is updated in the data register, and the data interrupt sign is enabled. (N is defined in the bit [19:16] of LRADC_CTRL).

- Single Mode

The LRADC gathers 8 samples, and the average value of these 8 samples is updated in the data register, and the data interrupt sign is enabled at the same time, then the LRADC stops sample.

8.8.3.4 Interrupt

Each LRADC channel has five interrupt sources and five interrupt enable controls.

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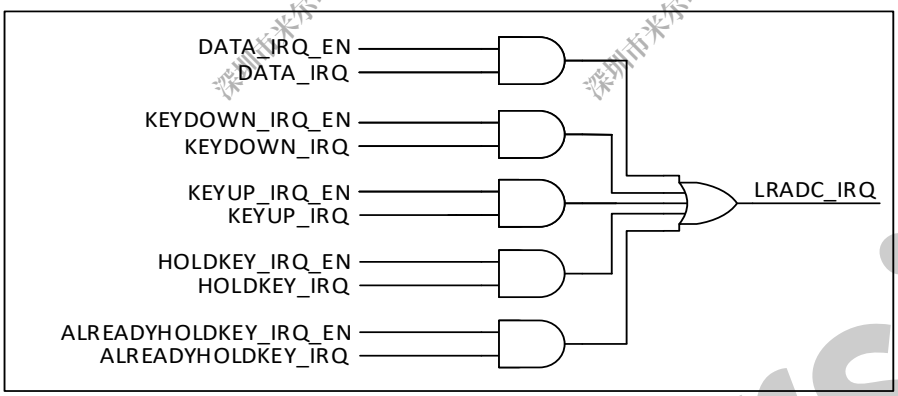
Figure 8-49 LRADC Interrupt



When the input voltage is between LEVEL A (1.35 V) and LEVEL B (control by the bit [5:4] of LRADC_CTRL), the IRQ1 can be generated. When the input voltage is lower than LEVEL B, the IRQ2 can be generated.

If the controller receives IRQ1 and does not receive IRQ2 at the same time, then the controller will generate Hold Key Pending, otherwise Data IRQ Pending.

The Hold KEY usually is used for the self-locking key. When the self-locking key holds a locking status, the controller receives the IRQ2, then the controller will generate Already Hold Pending.

8.8.3.5 Calculation Formula

Calculation formula: LRADC_DATA = Vin/VREF*63, VREF=1.35 V

8.8.4 Programming Guidelines

8.8.4.1 Normal Detecting

Perform the following steps for normal detecting mode:

Step 1 Configure LRADC_BGR_REG[LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG[LRADC_RST] to 1 to deassert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG[LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 0 to set the normal mode.

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Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

8.8.4.2 Single Detecting

Perform the following steps for the single detecting mode:

Step 1 Configure LRADC_BGR_REG[LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG[LRADC_RST] to 1 to deassert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG[LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 1 to set the single mode.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

8.8.4.3 Continuous Detecting

Perform the following steps for continuous detecting mode:

Step 1 Configure LRADC_BGR_REG[LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG[LRADC_RST] to 1 to deassert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG[LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

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Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 2 to set the continuous mode, and configure LRADC_CTRL[CONTINUE_TIME_SELECT] to set a sampling interval.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

8.8.5 Register List

Module Name	Base Address
LRADC	0x02009800

Register Name	Offset	Description
LRADC_CTRL	0x0000	LRADC Control Register
LRADC_INTC	0x0004	LRADC Interrupt Control Register
LRADC_INTS	0x0008	LRADC Interrupt Status Register
LRADC_DATA0	0x000C	LRADC Data Register0
LRADC_DATA1	0x0010	LRADC Data Register1

8.8.6 Register Description

8.8.6.1 0x0000 LRADC Control Register (Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x1	FIRST_CONVERT_DLY ADC First Convert Delay Setting ADC conversion is delayed by n samples.
23:22	R/W	0x0	CHANNEL_SEL Select the channel that be enabled 00: channel 0 only 01: channel 1 only 10: channel 1 and channel 0
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT Continuous Mode Time Select One of 8*(N+1) sample as a valuable sample data.
15:14	/	/	/

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Offset: 0x0000			Register Name: LRADC_CTRL
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x0	KEY_MODE_SELECT Key Mode Select 00: Normal Mode 01: Single Mode 10: Continuous Mode
11:8	R/W	0x1	LEVELA_B_CNT Level A to Level B time threshold select Judge the ADC convert value from level A to level B in n+1 samples.
7	R/W	0x0	LRADC_HOLD_KEY_EN LRADC Hold KEY Enable 0: Disable 1: Enable
6	R/W	0x1	LRADC_CHANNEL_EN LRADC Channel Enable 0: Disable 1: Enable
5:4	R/W	0x2	LEVELB_VOL Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (1.286V) 01: 0x39 (1.221V) 10: 0x36 (1.157V) 11: 0x33 (1.093V)
3:2	R/W	0x2	LRADC_SAMPLE_RATE LRADC Sample Rate 00: 2 kHz 01: 1 kHz 10: 500 Hz 11: 250 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN LRADC Enable 0: Disable 1: Enable

8.8.6.2 0x0004 LRADC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

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Offset: 0x0004			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	ADC1_KEYUP_IRQ_EN ADC1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN ADC1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC1_HOLD_IRQ_EN ADC1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYDOWN_EN ADC1 Key Down Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN ADC1 Data IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN ADC0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN ADC0 Already Hold Key IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN ADC0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN ADC0 Data IRQ Enable 0: Disable 1: Enable

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8.8.6.3 0x0008 LRADC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	ADC1_KEYUP_PENDING ADC1 Key up pending Bit When general Key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
11	R/W1C	0x0	ADC1_ALRDY_HOLD_PENDING ADC1 Already Hold Pending Bit When hold Key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
10	R/W1C	0x0	ADC1_HOLDKEY_PENDING ADC1 Hold Key Pending Bit When Hold Key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
9	R/W1C	0x0	ADC1_KEYDOWN_PENDING ADC1 Key Down IRQ Pending Bit When General Key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

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Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	ADC1_DATA_PENDING ADC1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
7:5	/	/	/
4	R/W1C	0x0	ADC0_KEYUP_PENDING ADC0 Key up Pending Bit When the general key is pulled up, and the corresponding interrupt is enabled, the status bit is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W1C	0x0	ADC0_ALRDY_HOLD_PENDING ADC0 Already Hold Pending Bit When the hold key is pulled down and the general key is pulled down, and the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC0_HOLDKEY_PENDING ADC0 Hold Key Pending Bit When the hold key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

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Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	ADC0_KEYDOWN_PENDING ADC0 Key Down IRQ Pending Bit When the general key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	ADC0_DATA_PENDING ADC0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

8.8.6.4 0x000C LRADC Data Register (Default Value: 0x0000_003F)

Offset: 0x000C			Register Name: LRADC_DATA0
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x3F	LRADC0_DATA LRADC0 Data

8.8.6.5 0x0010 LRADC Data Register (Default Value: 0x0000_003F)

Offset: 0x0010			Register Name: LRADC_DATA1
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x3F	LRADC1_DATA LRADC1 Data

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8.9 USB2.0 DRD

8.9.1 Overview

The USB2.0 dual-role device (USB2.0 DRD) supports both device and host functions which can also be configured as a Host-only or Device-only controller. It complies with the USB2.0 Specification.

For saving CPU bandwidth, the DMA interface of the DRD module can also support the external DMA controller to do the data transfer between the memory and the DRD FIFO. The DRD core also supports USB power saving functions.

The USB2.0 DRD has the following features:

- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports static host operation:
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root port shared between EHCI and OHCI
- Supports static device operation:
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
  - Supports bi-directional endpoint0 (EP0) for Control transfer
  - Up to 10 user-configurable endpoints (EP1 IN/OUT, EP2 IN/OUT, EP3 IN/OUT, EP4 IN/OUT, EP5 IN/OUT) for Bulk transfer, Isochronous transfer and Interrupt transfer
  - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
  - Supports interface to an external Normal DMA controller for every EP (EP1, EP2, EP3, EP4, and EP5)
- Supports an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Includes automatic PING capabilities
- Soft connect/disconnect function
- Hardware handles all data transfer
- Power optimization and power management capabilities
- Device and host controller share an 8K SRAM and a physical PHY

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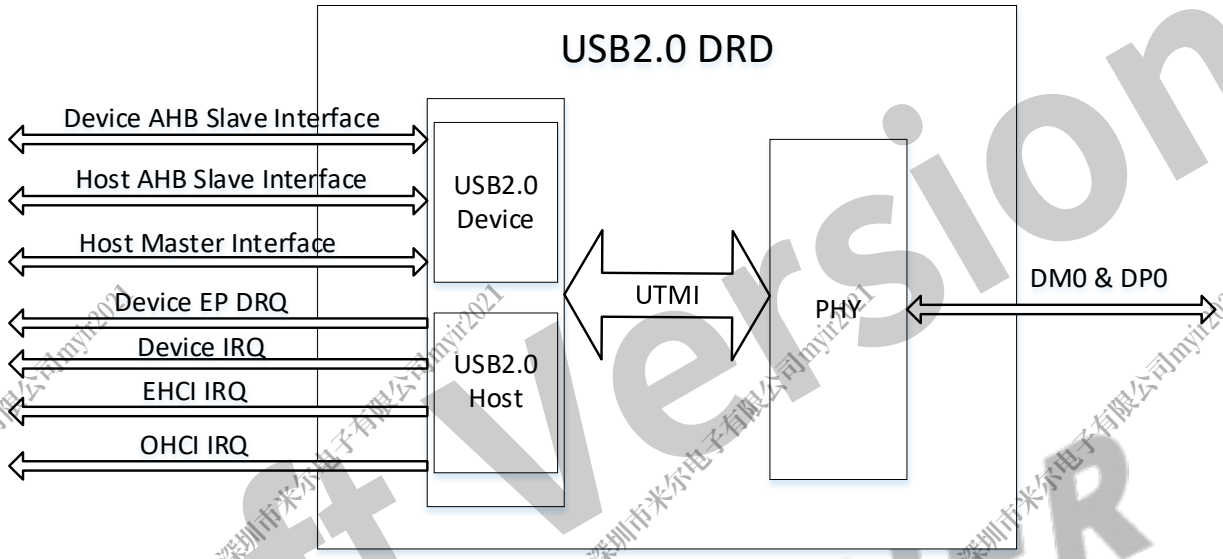
8.9.2 Block Diagram

The following figure shows the block diagram of USB2.0 DRD Controller.

Figure 8-50 USB2.0 DRD Controller Block Diagram



8.9.3 Functional Description

8.9.3.1 External Signals

Table 8-33 USB2.0 DRD External Signals

Signal Name	Description	Type
USB0-DM	USB2.0 Data Signal DM	A I/O
USB0-DP	USB2.0 Data Signal DP	A I/O
USB0-REXT	USB2.0 External Reference Resistor	AO
VCC33-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host	P
VCC33-18-USB	3.3 V/1.8V Analog Power Supply for USB2.0 DRD and USB2.0 Host	P
VDD09-USB	0.9 V USB Digital Power Supply	p

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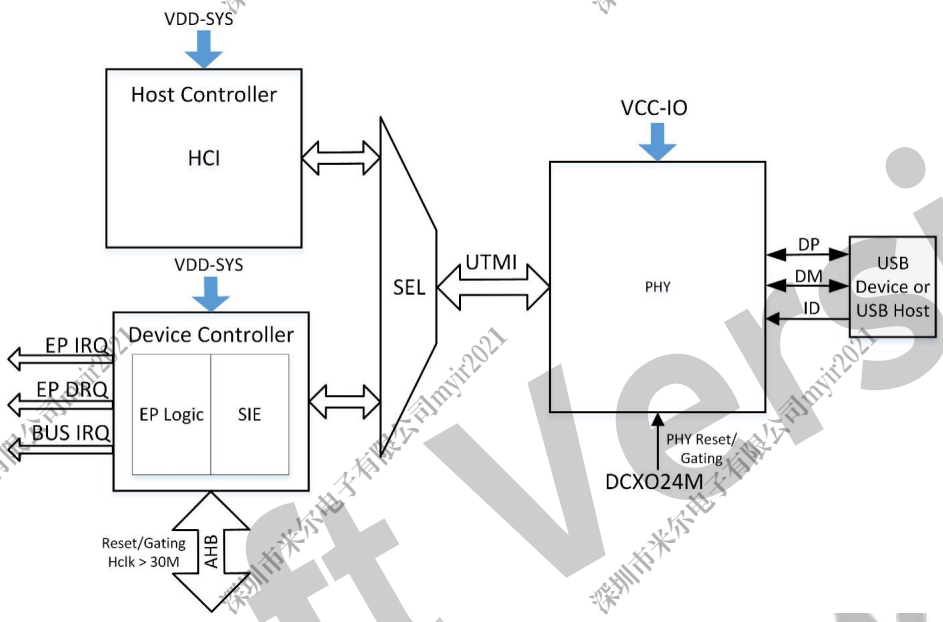
8.9.3.2 Controller and PHY Connection Diagram

Figure 8-51 USB2.0 DRD Controller and PHY Connection Diagram



8.9.4 Register List

There are two groups of registers in USB2.0 DRD.

Module Name	Base Address
USB0 (0x0410 0000---0x041F FFFF)	
USB_DRD_DEVICE	0x04100000
USB_DRD_HOST	0x04101000

8.9.4.1 USB_DRD_DEVICE Register List

Module Name	Base Address
USB_DRD_DEVICE	0x04100000

Register Name	Offset	Description
USB_EPFIFOn	0x0000+N *0x0004 (N=0,1,2,3,4,5)	USB FIFO Entry for Endpoint N
USB_GCS	0x0040	USB Global Control and Status Register
USB_EPINTF	0x0044	USB Endpoint Interrupt Flag Register
USB_EPINTE	0x0048	USB Endpoint Interrupt Enable Register
USB_BUSINTF	0x004C	USB Bus Interrupt Flag Register
USB_BUSINTE	0x0050	USB Bus Interrupt Enable Register

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Register Name	Offset	Description
USB_FNUM	0x0054	USB Frame Number Register
USB_TESTC	0x007C	USB Test Control Register
USB_CSR0	0x0080	USB EP0 Control and Status Register
USB_TXCSR	0x0080	USB EP1-5 Tx Control and Status Register
USB_RXCSR	0x0084	USB EP1-5 Rx Control and Status Register
USB_COUNT0	0x0088	USB EP0 Rx Counter Register
USB_RXCOUNT	0x0088	USB EP1-5 Rx Counter Register
USB_ATTR0	0x008C	USB EP0 Attribute Register
USB_EPATTR	0x008C	USB EP1-5 Attribute Register
USB_TXFIFO	0x0090	USB EP1-5 TxFIFO Setting Register
USB_RXFIFO	0x0094	USB EP1-5 RxFIFO Setting Register
USB_FADDR	0x0098	USB Function Address Register
USB_ISCR	0x0400	USB Interface Status and Control Register
USB_PHY_CTL	0x0410	USB PHY Control Register
USB_PHY_TEST	0x0414	USB PHY Test Register
USB_PHY_TUNE	0x0418	USB PHY Tune Register
USB_PHY_SEL	0x0420	USB PHY Select Register
USB_PHY_STA	0x0424	USB PHY Status Register
USB_DMA_INTE	0x0500	USB DMA Interrupt Enable Register
USB_DMA_INTS	0x0504	USB DMA Interrupt Status Register
USB_DMA_CHAN_CFG	0x0540+N *0x0010(N=0-7)	USB DMA Channel Configuration Register
USB_DMA_SDRAM_ADD	0x0544+N *0x0010(N=0-7)	USB DMA SDRAM Start Address Register
USB_DMA_BC	0x0548+N *0x0010(N=0-7)	USB DMA Byte Counter Register
USB_DMA_RESIDUAL_BC	0x054C+N *0x0010(N=0-7)	USB DMA RESIDUAL Byte Counter Register

8.9.4.2 USB_DRD_HOST Register List

Module Name	Base Address
USB_DRD_HOST	0x04101000

EHCI

Register Name	Offset	Description
E_CAPLENGTH	0x0000	EHCI Identification Register

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Register Name	Offset	Description
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000C	EHCI Companion Port Route Description
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_PERIODICLISTBASE	0x0024	EHCI Periodic Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Current Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status and Control Register

OHCI

Register Name	Offset	Description
O_HcRevision	0x0400	OHCI Revision Register
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register
O_HcHCCA	0x0418	OHCI HCCA Register
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Register
O_HcControlHeadED	0x0420	OHCI Control Head ED Register
O_HcControlCurrentED	0x0424	OHCI Control Current ED Register
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Register
O_HcBulkCurrentED	0x042C	OHCI Bulk Current ED Register
O_HcDoneHead	0x0430	OHCI Done Head Register
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
O_HcRhDescriptorA	0x0448	OHCI Root Hub DescriptorA Register
O_HcRhDesriptorB	0x044C	OHCI Root Hub DescriptorB Register
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register

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HCI

Register Name	Offset	Description
USB_CTRL	0x0800	HCI Interface Register
HCI_CTRL3	0x0808	HCI Control 3 Register
PHY_CTRL	0x0810	PHY Control Register
PHY_TEST	0x0814	PHY Test Register
PHY_TUNE	0x0818	PHY Tune Register
PHY_STA	0x0824	PHY Status Register
USB_SPDCR	0x0828	HCI SIE Port Disable Control Register

8.9.5 USB_DRD_Device Register Description

8.9.5.1 0x0000+N*0x04(N=0-5) USB FIFO Entry for Endpoint N (Default Value:0x0000_0000)

Offset: 0x0000+N*0x04(N=0-5)			Register Name: USB_EPFIFOn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	EPnFIFO FIFO Entry for Endpoint n

8.9.5.2 0x0040 USB Global Control and Status Register (Default Value:0x0000_0020)

Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TX_EDMA 1'b0: DMA_REQ signal for all IN Endpoints will be de-asserted when MAXP bytes have been written to and endpoint. This is late mode. 1'b1: DMA_REQ signal for all IN Endpoints will be de-asserted when MAXP-8 bytes have been written to an endpoint. This is early mode.
30	R/W	0	RX_EDMA 1'b0: DMA_REQ signal for all OUT Endpoints will be de-asserted when MAXP bytes have been read to an endpoint. This is late mode. 1'b1: DMA_REQ signal for all OUT Endpoints will be de-asserted when MAXP-8 bytes have been read to and endpoint. This is early mode.
29	/	/	/

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Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
28:25	R/W	0	BUS_DRQ_SEL USB DMA Request Signal Source Select 4'b0000: Select TX Endpoint 1 DRQ 4'b0001: Select RX Endpoint 1 DRQ 4'b0010: Select TX Endpoint 2 DRQ 4'b0011: Select RX Endpoint 2 DRQ 4'b0100: Select TX Endpoint 3 DRQ 4'b0101: Select RX Endpoint 3 DRQ 4'b0110: Select TX Endpoint 4 DRQ 4'b0111: Select RX Endpoint 4 DRQ 4'b1000: Select TX Endpoint 5 DRQ 4'b1001: Select RX Endpoint 5 DRQ
24	R/W	0	FIFO_BUS_SEL 0: CPU bus for FIFO Access, 1: DMA bus for FIFO operation.
23:20	/	/	/
19:16	R/W	0x0	EPIND Endpoint Index Index is a 4-bit register that determines which endpoint control/status registers are accessed. Before accessing an endpoint's control/status registers at 0x0080-0x00BF, the endpoint number should be written to the Index register to ensure that correct control/status registers in the memory map. **Note: The valid value for Index register is 0-5.**
15	R	0	BDev B-Device 0 => 'A' device; 1 => 'B' device; Only valid while a session is in progress. **Note: If the core is in Force_Host mode (i.e. a session has been started with USB_TMCTL.7=1), this bit will indicate the state of the HOSTDISCON input signal from the PHY.**
14:13	/	/	/

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Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
12:11	R	0x0	VBus These bits encode the current VBus level as follows: <table><tr><th>D4</th><th>D3</th><th>Meaning</th></tr><tr><td>0</td><td>0</td><td>Below SessionEnd</td></tr><tr><td>0</td><td>1</td><td>Above SessionEnd, below AValid</td></tr><tr><td>1</td><td>0</td><td>Above AValid, below VBusValid</td></tr><tr><td>1</td><td>1</td><td>Above VBusValid</td></tr></table>
10	R	0	HostMode Host Mode This bit is set when the USB/DRD is acting as a Host.
9	/	/	/
8	R/W	0	Session When operating as an 'A' device, this bit is set or cleared by the CPU to start or end a session. When operating as an 'B' device, this bit is set/cleared by the USB/DRD when a session starts/ends. It is also set by the CPU to initiate the Session Request Protocol. When the USB/DRD is in Suspend mode, the bit may be cleared by the CPU to perform a software disconnect. **Note: Clearing this bit when the core is not suspending will result in undefined behavior.**
7	R/W	0	IsoUpdateEn Isochronous Update Enable When set by the CPU, the USB/DRD will wait for an SOF token from the Tx packet ready before sending the packet. If an IN token is received before an SOF token, then a zero length data packet will be send. **Note: This bit only affects endpoints performing Isochronous transfer.**
6	R/W	0	SoftConn Soft Connect The USB D+/D- line is enabled when this bit is set by CPU and tri-stated when this bit is cleared by CPU. **Note: Only valid in Peripheral Mode (but not means 'B' Device).**

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Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
5	R/W	1	HSEN High-speed Mode Enable When set by CPU, the USB/DRD will negotiate for High-speed mode when the device is reset by host. If not set, the device will only operate in Full-speed mode.
4	R	0	HSFLAG High-speed Mode Flag When set, this read-only bit indicates High-speed mode successfully negotiated during USB reset. And this bit becomes valid when USB Reset completes (as indicated by USB reset interrupt).
3	R	0	Reset This bit is set when Reset Signaling is present on the bus.
2	R/W	0	Resume Set by the CPU to generate Resume signaling when the function is in Suspend mode. The CPU should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling.
1	R	0	SuspendM Suspend Mode This bit is set on entry into Suspend mode.
0	R/W	0	SuspendMEn Enable SuspendM Set by the CPU to enable the SUSPENDM output of UTMI+ bus.

8.9.5.3 0x0044 USB Endpoint Interrupt Flag Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: USB_EPINTF
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R	0	EP5Rx Rx Endpoint 5 interrupt flag
20	R	0	EP4Rx Rx Endpoint 4 interrupt flag
19	R	0	EP3Rx Rx Endpoint 3 interrupt flag
18	R	0	EP2Rx Rx Endpoint 2 interrupt flag

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Offset: 0x0044			Register Name: USB_EPINTF
Bit	Read/Write	Default/Hex	Description
17	R	0	EP1Rx Rx Endpoint 1 interrupt flag
16:6	/	/	/
5	R	0	EP5Tx Tx Endpoint 5 interrupt flag
4	R	0	EP4Tx Tx Endpoint 4 interrupt flag
3	R	0	EP3Tx Tx Endpoint 3 interrupt flag
2	R	0	EP2Tx Tx Endpoint 2 interrupt flag
1	R	0	EP1Tx Tx Endpoint 1 interrupt flag
0	R	0	EP0 Endpoint 0 interrupt flag

8.9.5.4 0x0048 USB Endpoint Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: USB_EPINTE
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0	EP5Rx Rx Endpoint 5 interrupt enable
20	R/W	0	EP4Rx Rx Endpoint 4 interrupt enable
19	R/W	0	EP3Rx Rx Endpoint 3 interrupt enable
18	R/W	0	EP2Rx Rx Endpoint 2 interrupt enable
17	R/W	0	EP1Rx Rx Endpoint 1 interrupt enable
16:6	/	/	/
5	R/W	0	EP5Tx Tx Endpoint 5 interrupt enable
4	R/W	0	EP4Tx Tx Endpoint 4 interrupt enable
3	R/W	0	EP3Tx Tx Endpoint 3 interrupt enable
2	R/W	0	EP2Tx Tx Endpoint 2 interrupt enable

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Offset: 0x0048			Register Name: USB_EPINTE
Bit	Read/Write	Default/Hex	Description
1	R/W	0	EP1Tx Tx Endpoint 1 interrupt enable
0	R/W	0	EP0 Endpoint 0 interrupt enable

8.9.5.5 0x004C USB Bus Interrupt Flag Register (Default Value:0x0000_0000)

Offset: 0x004C			Register Name: USB_BUSINTF
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	VBusError Set when VBus drops below the VBus Valid threshold during a session. **Note: Only valid when USB/DRD is 'A' device.**
6	R	0	SessionRequest Set when Session Request signaling has been detected. **Note: Only valid when USB/DRD is 'A' device.**
5	R	0	Disconnect Set in Host mode when a device disconnect is detected. Set in Peripheral mode when a session ends. **Note: Valid at all transaction speeds.**
4	R	0	Connect Set in host mode when a device connection is detected. **Note: Only valid in Host mode. Valid at all transaction speeds.**
3	R	0	SOF Set when a new frame starts.
2	R	0	ResetBabble Reset Set in Peripheral mode when Reset signaling is detected on the bus. Babble Set in Host mode when babble is detected. **Note: Only active after first SOF has been sent.**
1	R	0	Resume Set when Resume signaling is detected on the bus while the USB/DRD is in Suspend mode.

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Offset: 0x004C			Register Name: USB_BUSINTF
Bit	Read/Write	Default/Hex	Description
0	R	0	Suspend Set when Suspend signaling is detected on the bus. **Note: Only valid in Peripheral mode.**

8.9.5.6 0x0050 USB Bus Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: USB_BUSINTE
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	VBusError VBusError interrupt enable
6	R/W	0	Session Request Session Request interrupt enable
5	R/W	0	Disconnect Disconnect interrupt enable
4	R/W	0	Connect Connect interrupt enable
3	R/W	0	SOF SOF interrupt enable
2	R/W	0	ResetBabble Reset Reset interrupt enable Babble Babble interrupt enable
1	R/W	0	Resume Resume interrupt enable
0	R/W	0	Suspend Suspend interrupt enable

8.9.5.7 0x0054 USB Frame Number Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: USB_FNUM
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x000	FRNUM Frame Number Hold the last received frame number.

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8.9.5.8 0x007C USB Test Control Register (Default Value:0x0000_0000)

NOTE

Only one of Bits 0-6 should be set at any time.

Offset: 0x007C			Register Name: USB_TESTC
Bit	Read/Write	Default/Hex	Description
31:24	/	0	/
23:16	R	/	FSM USB Operation Finite State Machine for Debug
15:11	/	/	/
10	R/W	0	EXTRXACT Extend Rx Active Signal for safe
9	R/W	0	RESUME_SE0 Resume from SE0 Enable
8	R/W	0	TM1 Test Mode Enable for Simulation.
7	R/W	0	Force_Host The CPU sets this bit to instruct the core to enter Host mode when the Session bit (Bit 0 of USB_DEVCTL) is set, regardless of whether it is connected to any peripheral. The state of the CID input, HostDisconnect and Linestate signals are ignored. The core will then remain in Host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set. While in this mode, the status if the HOSTDISCON signal from the PHY may be read from bit 7 of the USB_DEVCTL (in 0x0060) register. The operating speed is determined from the Force_HS and Force_FS bits as follows:

Force_HS	Force_FS	Operating Speed
0	0	Low Speed
0	1	Full Speed
1	0	High Speed
1	1	Undefined

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Offset: 0x007C			Register Name: USB_TESTC
Bit	Read/Write	Default/Hex	Description
6	W	0	FIFO_Access The CPU sets this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO. It is cleared automatically. **Note: Writing '0' to this bit will be ignored.**
5	R/W	0	Force_FS The CPU sets this bit either in conjunction with bit 7 above or to force the USB/DRD into Full-speed mode when it receive a USB reset.
4	R/W	0	Force_HS The CPU sets this bit either in conjunction with bit 7 above or to force the USB/DRD into High-speed mode when it receive a USB reset.
3	R/W	0	Test_Packet (High-speed mode) The CPU sets this bit to enter Test_Packet test mode. In the mode, the USB/DRD repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the Universal Serial Bus Specification Revision 2.0, Section 7.1.20. **Note: The text packet has a fixed format and must be loaded into the Endpoint 0 FIFO before the test mode is entered.**
2	R/W	0	Test_K (High-speed mode) The CPU sets this bit to enter the Test_K test mode. In this mode, the USB/DRD transmits a continuous K on the bus.
1	R/W	0	Test_J (High-speed mode) The CPU sets this bit to enter the Test_J est mode. In this mode, the USB/DRD transmits a continuous J on the bus.
0	R/W	0	Test_SE0_NAK (High-speed mode) The CPU sets this bit to enter the Test_SE0_NAK test mode. In this mode, the USB/DRD remains in High-speed mode but responds to any valid IN token with a NAK.

8.9.5.9 0x0080 USB EP0 Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: USB_CSR0
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

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Offset: 0x0080			Register Name: USB_CSR0
Bit	Read/Write	Default/Hex	Description
24	W	0	FlushFIFO The CPU writes a '1' to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset, and the TxPktRdy/RxPktRdy bit (below) is cleared. **Note: (i)Writing '0' to this bit is ignored. (ii)Flush FIFO should only be used when TxPktRdy/RxPktRdy is set, at other times, it may cause data to be corrupted.**
23	W	0	ServicedSetupEnd The CPU writes a '1' to this bit to clear the SetupEnd bit. It is cleared automatically.
22	W	0	ServicedRxPktRdy The CPU writes a 1 to this bit to clear the RxPktRdy bit. It is cleared automatically.
21	W	0	SendStall The CPU writes a '1' to this bit to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically. **Note: The FIFO should be flushed before SendStall is set.**
20	R	0	SetupEnd This bit will be set when a control transaction ends before the DataEnd bit has been set. An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing a '1' to the ServicedSetupEnd bit.
19	W	0	DataEnd The CPU sets this bit: When setting TxPktRdy for the last data packet. When clearing RxPktRdy after unloading the last data packet. When setting TxPktRdy for a zero length data packet. It is cleared automatically.
18	R/W	0	SentStall This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.

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Offset: 0x0080			Register Name: USB_CSR0
Bit	Read/Write	Default/Hex	Description
17	R/W	0	TxPktRdy The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
16	R	0	RxPktRdy This bit is set when a data packet has been received. An interrupt is generated (if enabled) when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.
15:0	/	/	/

8.9.5.10 0x0080 USB EP1 to 5 TX Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0	AutoSet If CPU sets this bit, TxPktRdy will be automatically set when data of maximum packet size (value in the USB_TXMAXP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. **Note: Should not be set for high-bandwidth Isochronous/Interrupt endpoints.**
30	R/W	0	ISO The CPU sets this bit to enable the Tx endpoint for Isochronous transfers, and clears it to enable the Tx endpoint for Bulk or Interrupt transfers. **Note: This is only has any effect in Peripheral mode. In Host mode, it always returns zero.**
29	R/W	0	Mode The CPU sets this bit to enable the endpoint direction as Tx, and clears the bit to enable it as Rx. **Note: This bit only has any affect where the same endpoint FIFO is used for Tx and Rx transactions.**
28	R/W	0	DMAReqEnab The CPU sets this bit to enable the DMA request for the Tx endpoint.

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Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
27	R/W	0	FrcDataTog The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
26	R/W	0	DMAReqMode The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. **Note: This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is cleared.**
25:24	/	/	/
23	R/W	0	IncompTx When the endpoint is being used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts. **Note: In anything other than a high-bandwidth transfer, this bit will always return 0. And writing '1' to this bit is ignored.**
22	W	0	ClrDataTog The CPU writes a 1 to this bit to reset the endpoint data toggle to 0. It is cleared automatically. **Note: Writing '0' to this bit is ignored.**
21	R/W	0	SentStall This bit is set when a STALL handshake is transmitted. The FIFO is flushed and the TxPktRdy bit is cleared. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
20	R/W	0	SendStall The CPU writes a 1 to this to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition. **Note: (i)The FIFO should be flushed before SendStall is set. (ii)This bit has no effect where the endpoint is being used for Isochronous transfers.**

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Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
19	W	0	FlushFIFO The CPU writes a 1 to this bit to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. **Note: (i)Writing '0' to this bit is ignored. (ii)Flush FIFO should only be used when TxPktRdy is set, at other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.**
18	R/W	0	UnderRun The USB sets this bit if an IN token is received when the TxPktRdy bit not set. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
17	R/W	0	FIFONotEmpty The USB sets this bit when there is at least 1 packet in the Tx FIFO. **Note: Writing '1' to this bit is ignored.**
16	R/W	0	TxPktRdy The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared prior to loading a second packet to a double buffered FIFO. **Note: Writing '0' to this bit is ignored.**

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Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
15:11	R/W	0x00	PacketCount In the case of Bulk endpoints with the packet splitting option enabled, the Packet Count can be up to 32 and defines the maximum number of USB packets of specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. If the packet splitting option is not enabled, Packet Count is not implemented. For Isochronous/Interrupt endpoints operating in High-speed mode and with the High-bandwidth option enabled, Packet Count may only either 2 or 3 (corresponding to bit 11 or bit 12 set, respectively) and it specifies the maximum number of such transactions that can be take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB/DRD will automatically split any data packet written to the FIFO into up to 2 or 3 USB packet, each containing the specified payload (or less). For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bit 11 and 12 are ignored. **Note: Value for this bits is (Packet Count - 1), but not Packet Count.**

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Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x000	MaximumPayload These bits define the maximum payload (in bytes) transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. **Note: (i) The value written to Maximum Payload (multiplied by Packet Count in the case of high-bandwidth Isochronous/Interrupt transfer) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint, a mismatch could cause unexpected result. (ii)The total amount of data represented by the value written to this register (Maximum payload × Packet Count) must not exceed the FIFO size for Tx endpoint, and should not exceed half the FIFO size if double-buffering is required.**

8.9.5.11 0x0084 USB EP1 to 5 Rx Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0	AutoClear If CPU sets this bit then the RxPktRdy will be automatically cleared when data of maximum packet size (value in the USB_TXMAXP) is unloaded from the Rx FIFO. If a packet of less than the maximum packet size is unloaded, then RxPktRdy will have to be cleared manually. **Note: Should not be set for high-bandwidth Isochronous endpoints.**
30	R/W	0	ISO The CPU sets this bit to enable the Rx endpoint for Isochronous transfers, and clears it to enable the Rx endpoint for Bulk or Interrupt transfers.
29	R/W	0	DMAReqEnab The CPU sets this bit to enable the DMA request for the Rx endpoint.

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Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
28	R/W	0	DisNyet_PIDError DisNyet Bulk/Interrupt Transactions: The CPU sets this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the FIFO becomes full. **Note: This bit only has any affect in High-speed mode, in which mode it should be set for all Interrupt endpoints.** PIDError ISO Transactions: The core sets this bit to indicate a PID error in the received packet.
27	R/W	0	DMAReqMode The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. **Note: This bit must not be cleared in the same cycle as the above RxPktRdy(or DMAReqEnab) bit is cleared.**
26:25	/	/	/
24	R/W	0	IncompRx This bit will be set in a high-bandwidth Isochronous/Interrupt transfer if the packet received is incomplete. It will be cleared when RxPktRdy is cleared. **Note: (i) Writing '1' to this bit is forbidden. (ii) In anything other than a high-bandwidth transfer, this bit will always return 0.**
23	W	0	ClrDataTog The CPU writes a '1' to this bit to reset the endpoint data toggle to 0. It is cleared automatically. **Note: Writing '0' to this bit is ignored.**
22	R/W	0	SentStall This bit is set when a STALL handshake is transmitted. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**

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Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
21	R/W	0	SendStall The CPU writes a '1' to this to issue a STALL handshake. The CPU clears this bit to terminate the stall condition. **Note: (i)The FIFO should be flushed before SendStall is set. (ii)This bit has no effect where the endpoint is being used for Isochronous transfers.**
20	W	0	FlushFIFO The CPU writes a '1' to this bit to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. **Note: (i) Writing '0' to this bit is ignored. (ii) Flush FIFO should only be used when RxPktRdy is set, at other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.**
19	R	0	DataError This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. It is cleared when RxPktRdy is cleared. **Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns zero.**
18	R/W	0	OverRun The USB sets this bit if an OUT token can not be loaded into the Rx FIFO. The CPU should clear this bit. **Note: (i) Writing '1' to this bit is ignored. (ii) This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns zero.**
17	R	0	FIFOFull The USB sets this bit when no more packets can be loaded into the Rx FIFO.

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Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
16	R/W	0	RxPktRdy This bit is set when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set. **Note: Writing '1' to this bit is ignored.**
15:11	R/W	0x00	PacketCount In the case of Bulk endpoints with the packet combining option enabled, the Packet Count can be up to 32 and defines the maximum number of USB packets of specified payload which are to be combined into a single data packet within the FIFO. For Isochronous/Interrupt endpoints operating in High-speed mode and with the High-bandwidth option enabled, Packet Count may only either 2 or 3 (corresponding to bit 11 or bit 12 set, respectively) and it specifies the maximum number of such transactions that can be take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB/DRD will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bit 11 and 12 are ignored. **Note: Value for this bits is (Packet Count - 1), but not Packet Count.**

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Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x000	MaximumPayload These bits define the maximum payload (in bytes) transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. **Note: (i) The value written to Maximum Payload (multiplied by Packet Count in the case of high-bandwidth Isochronous/Interrupt transfer) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint, a mismatch could cause unexpected result. (ii) The total amount of data represented by the value written to this register (Maximum payload × Packet Count) must not exceed the FIFO size for OUT endpoint, and should not exceed half the FIFO size if double-buffering is required.**

8.9.5.12 0x0088 USB EP0 Rx Counter Register (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: USB_COUNT0
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0x00	RxCount0 Endpoint 0 Rx Count These bits indicate the number of received data bytes in the Endpoint 0 FIFO. **Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (of USB_CSR0) is set.**

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8.9.5.13 0x0088 USB EP1 to 5 Rx Counter Register (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: USB_RXCOUNT
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	RqPktCount Sets the number of packets of size MaxP that are to be transferred in a block transfer. **Note: Only used in Host mode when AutoReq (of USB_RXCSR) is set. Has no effect in Peripheral mode or AutoReq is not set.**
15:13	/	/	/
12:0	R	0x0000	RxCount Endpoint Rx Count These bits hold the number of data bytes in the packet currently in line to be read from the Rx FIFO. If the packet was transmitted as multiple bulk packets, the number given will be for the combined packet. **Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (of USB_RXCSR) is set.**

8.9.5.14 0x0090 USB EP1 to 5 TxFIFO Setting Register (Default Value:0x0000_0000)

Offset: 0x0090			Register Name: USB_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0000	AD AD [12:0] Start address of the endpoint FIFO is in units of 8 bytes, and it equals (AD[12:0]*8).
15:5	/	/	/
4	R/W	0	DPB Defines whether double-packet buffering supported. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.

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Offset: 0x0090			Register Name: USB_TXFIFO
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	SZ SZ [3:0] Maximum packet size to be allowed for (*before any* splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission) is $2^{(SZ[3:0]+3)}$ bytes, and the valid values for SZ [3:0] are 0x0–0x09. If DPB=0, the FIFO will also this size; if DPB=1, the FIFO will be twice this size.

8.9.5.15 0x0094 USB EP1 to 5 RxFIFO Setting Register (Default Value:0x0000_0000)

Offset: 0x0094			Register Name: USB_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0000	AD AD [12:0] Start address of the endpoint FIFO is in units of 8 bytes, and it equals (AD[12:0]*8).
15:5	/	/	/
4	R/W	0	DPB Defines whether double-packet buffering supported. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.
3:0	R/W	0x0	SZ SZ [3:0] Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission) is $2^{(SZ[3:0]+3)}$ bytes, and the valid values for SZ [3:0] are 0x0–0x09. If DPB=0, the FIFO will also this size; if DPB=1, the FIFO will be twice this size.

8.9.5.16 0x0098 USB Function Address Register (Default Value:0x0000_0000)

Offset: 0x0098			Register Name: USB_FADDR
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

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Offset: 0x0098			Register Name: USB_FADDR
Bit	Read/Write	Default/Hex	Description
6:0	RW	0x00	FADDR The function address in peripheral mode. This field is reset to zero after a USB bus reset, and should be updated by software after Set_Address Command during USB enumeration.

8.9.5.17 0x0400 USB Interface Status and Control Register (Default Value:0x0000_0000)

Offset: 0x0400			Register Name: USB_ISCR
Bit	Read/Write	Default/Hex	Description
31	/	0	/
30	R	-	VBUSLS USB VBUS Valid Status detected from Line State
29	R	-	VBUSEX USB VBUS Valid Status detected from external VBUS input
28	R	-	IDEX USB ID Status detected from external ID input
27:26	R	-	LS USB Line Status [27]—DM [26]—DP
25	R	-	VBUS USB VBUS Status merged from both internal and external
24	R	-	ID USB ID Status merged from both internal and external
23:18	/	0	/
17	R/W	0	IDPullupEn ID pull up enable 0: disable 1: enable ID pull up
16	R/W	0	DataPullupEn DP/DM pull up enable 0: DP/DM pull up disable 1: DP/DM pull up enable

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Offset: 0x0400			Register Name: USB_ISCR
Bit	Read/Write	Default/Hex	Description
15:14	R/W	0	ForceID Force ID 0x: use external ID Status 10: force ID to LOW 11: force ID to HIGH
13:12	R/W	0	ForceVBUS Force VBUS Valid 0x: use external VBUS Valid Status from VBUS Input or Line State 10: Force VBUS Valid to LOW 11: Force VBUS Valid to HIGH
11:10	R/W	0	VBUSSEL External VBUS Valid Source Select 0x: External VBUS Valid detected from VBUS Input 10: External VBUS Valid detected from DP/DM Input 11: External VBUS Valid detected from either VBUS or DP/DM input
9:8	/	0	/
7	R/W	0	WakeupEn USB Wakeup Enable 0: Disable 1: Enable
6	R/W	0	VBUSCDS VBUS Input Change Detect Status This bit is set by hardware after VBUS input changed when VBUS change detect is enable. Writing '1' will clear this bit.
5	R/W	0	IDCDS ID Input Change Detect Status This bit is set by hardware after ID input changed when ID change detect is enable. Writing '1' will clear this bit.
4	R/W	0	DATACDS DP/DM Input Change Detect Status This bit is set by hardware after DP/DM input changed when DP/DM change detect is enable. Writing '1' will clear this bit.

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Offset: 0x0400			Register Name: USB_ISCR
Bit	Read/Write	Default/Hex	Description
3	R/W	0	WakeupIE USB Wakeup IRQ Enable 1: Enable USB Wakeup IRQ 0: Disable USB Wakeup IRQ If this bit is set to zero, an USB wakeup event (VBUS/ID/DP/DM change) will generate an USB wakeup request to wakeup the system, but not generate an USB wakeup IRQ to CPU.
2	R/W	0	VBUSCDE VBUS Input Change Detect enable 0: Disable; 1: Enable
1	RW	0	IDCDE ID Input Change Detect enable 0: Disable; 1: Enable
0	R/W	0	DATACDE DP/DM Input Change Detect enable 0: Disable; 1: Enable

8.9.5.18 0x0410 USB PHY Control Register (Default Value:0x0000_0008)

Offset: 0x0410			Register Name: USB_PHY_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	VREGBYPASS
7	R/W	0	LOOPBACKENB
6	R/W	0	IDPULLUP
5	R/W	0	VBUSVLDEXT
4	R/W	1	VBUSVLDEXTSEL
3	R/W	1	SIDDQ 1: Write 1 to disable phy. 0: Write 0 to enable phy.
2	R/W	0	COMMONN
1:0	R/W	0	VATESTENB

8.9.5.19 0x0414 USB PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0414			Register Name: USB_PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN

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Offset: 0x0414			Register Name: USB_PHY_TEST
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

8.9.5.20 0x0418 USB PHY Tune Register (Default Value:0x05B3_33D4)

Offset: 0x0418			Register Name: USB_PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.9.5.21 0x0420 USB PHY Select Register (Default Value:0x0000_0001)

Offset: 0x0420			Register Name: USB_PHY_SEL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	Reserved
0	R/W	0x1	OTG_SEL 1: Phy is connected to OTG SIE 0: Phy is connected to HCI SIE

8.9.5.22 0x0424 USB PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0424			Register Name: USB_PHY_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0	TESTDATAOUT

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8.9.5.23 0x0500 USB DMA Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: USB_DMA_INTE
Bit	Read/Write	Default/Hex	Description
31:8	/	/	Reserved
7	R/W	0x0	USB_DMA7_PKG_INT_EN DMA7 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
6	R/W	0x0	USB_DMA6_PKG_INT_EN DMA6 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
5	R/W	0x0	USB_DMA5_PKG_INT_EN DMA5 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
4	R/W	0x0	USB_DMA4_PKG_INT_EN DMA4 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
3	R/W	0x0	USB_DMA3_PKG_INT_EN DMA3 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
2	R/W	0x0	USB_DMA2_PKG_INT_EN DMA2 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
1	R/W	0x0	USB_DMA1_PKG_INT_EN DMA1 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
0	R/W	0x0	USB_DMA0_PKG_INT_EN DMA0 Package End Transfer Interrupt Enable 0: Disable 1: Enable.

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8.9.5.24 0x0504 USB DMA Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0504			Register Name: USB_DMA_INTS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	Reserved
7	R/W	0x0	USB_DMA7_PKG_INT_STA DMA7 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
6	R/W	0x0	USB_DMA6_PKG_INT_STA DMA6 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
5	R/W	0x0	USB_DMA5_PKG_INT_STA DMA5 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
4	R/W	0x0	USB_DMA4_PKG_INT_STA DMA4 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
3	R/W	0x0	USB_DMA3_PKG_INT_STA DMA3 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
2	R/W	0x0	USB_DMA2_PKG_INT_STA DMA2 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
1	R/W	0x0	USB_DMA1_PKG_INT_STA DMA1 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.

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Offset: 0x0504			Register Name: USB_DMA_INTS
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	USB_DMA0_PKG_INT_STA DMA0 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.

8.9.5.25 0x0540+N*0x10(N=0-7) USB DMA Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0540+N*0x10(N=0-7)			Register Name: USB_DMA_CHAN_CFG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA_EN DMA Channel Enable If set to 1, DMA will start the data transfer between the source and the destination. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to this bit will stop the corresponding DMA channel and reset its state machine.
30:27	/	/	/
26:16	R/W	0x0	DMA_BST_LEN DMA Burst Length The value setting on this field should be equated to the USB max packet length of the corresponding endpoint.
15:5	/	/	/
4	R/W	0x0	DMA_DIR DMA Transfer Direction 0: SDRAM to USB FIFO 1: USB FIFO to SDRAM
3:0	R/W	0x0	DMA_FOR_EP DMA Channel for Endpoint The Endpoint number setting on this field selects the DMA channel for the corresponding endpoint.

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8.9.5.26 0x0544+N*0x10(N=0-7) USB DMA SDRAM Start Address Register (Default Value:0x0000_0000)

Offset: 0x0544+N*0x10(N=0-7)			Register Name: USB_DMA_SDRAM_ADD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMA_SDRAM_STR_ADDR DMA SDRAM Start Address The SDRAM start address for the DMA channel transfer between the SDRAM and USB FIFO.

8.9.5.27 0x0548+N*0x10(N=0-7) USB DMA Byte Counter Register (Default Value:0x0000_0000)

Offset: 0x0548+N*0x10(N=0-7)			Register Name: USB_DMA_BC
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	DMA_BC DMA Byte Counter

8.9.5.28 0x054C+N*0x10(N=0-7) USB DMA RESIDUAL Byte Counter Register (Default Value:0x0000_0000)

Offset: 0x054C+N*0x10(N=0-7)			Register Name: USB_DMA_RESIDUAL_BC
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	DMA_RESIDUAL_BC DMA Residual Byte Counter This field contains the residual byte count in current transfer.

8.9.6 EHCI Register Description

8.9.6.1 0x0000 EHCI Identification Register (Default Value:0x10)

Offset:0x0000			Register Name: E_CAPLENGTH
Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

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8.9.6.2 0x0002 EHCI Host Interface Version Number Register (Default Value:0x0100)

Offset: 0x0002			Register Name: E_HCIVERSION
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0100	HCIVERSION This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.9.6.3 0x0004 EHCI Host Control Structural Parameter Register (Default Value:0x0000_1101)

Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R	0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	1	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	1	Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.

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Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
7	R	0	Port Routing Rules This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value: Meaning 0: The first N_PCC ports are routed to the low numbered function companion host contr next N_PCC port are routed to the next low function companion controller, and so on. 1: The port routing is explicitly enumerated b first N_PORTS elements of the HCSP-PORT array. This field will always be '0'.
6:4	/	/	/
3:0	R	1	N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

8.9.6.4 0x0008 EHCI Host Control Capability Parameter Register (Default Value:0x0000_a026)

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R	0xa0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.

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Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
7:4	R	0x2	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	1	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	1	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

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8.9.6.5 0x000C EHCI Companion Port Route Description (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: E_HCSPPORTROUTE
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.9.6.6 0x0010 EHCI USB Command Register (Default Value:0x0008_0b00)

Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x08	Interrupt Threshold Control The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below: Value: Minimum Interrupt Interval 0x00: Reserved 0x01: 1 micro-frame 0x02: 2 micro-frame 0x04: 4 micro-frame 0x08: 8 micro-frame(default, equates to 1 MS) 0x10: 16 micro-frame(2ms) 0x20: 32 micro-frame(4ms) 0x40: 64 micro-frame(8ms) Any other value in this register yields undefined results. The default value in this field is 0x08. Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.
15:12	/	/	/
11	R	1	Asynchronous Schedule Park Mode Enable(OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.
10	/	/	/

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Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
9:8	R	0x3	Asynchronous Schedule Park Mode Count(OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0	Light Host Controller Reset(OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host

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Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
6	R/W	0	Interrupt on Async Advance Doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-Ware must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one. Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.
5	R/W	0	Asynchronous Schedule Enable This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean: Bit Value: Meaning 0: Do not process the Asynchronous Schedu 1: Use the ASYNLISTADDR register to access Asynchronous Schedule. The default value of this field is ‘0b’.
4	R/W	0	Periodic Schedule Enable This bit controls whether the host controller skips processing the Periodic Schedule. Values mean: Bit Value: Meaning 0: Do not process the Periodic Schedule. 1: Use the PERIODICLISTBASE register to ac Periodic Schedule. The default value of this field is ‘0b’.

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Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0	Frame List Size This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean: Bits: Meaning 00b: 1024 elements(4096bytes)Default value 01b: 512 elements(2048byts) 10b: 256 elements(1024bytes)For resource-constr condition 11b: reserved The default value is '00b'.
1	R/W	0	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.

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Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
0	R/W	0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

8.9.6.7 0x0014 EHCI USB Status Register (Default Value:0x0000_1000)

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero, then the status of the Asynchronous Schedule is disabled. If this bit is a one, then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).

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Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
14	R	0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero, then the status of the Periodic Schedule is disabled. If this bit is a one, then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.

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Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
3	R/WC	0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition (e.g. error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

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8.9.6.8 0x0018 EHCI USB Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

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8.9.6.9 0x001C EHCI Frame Index Register (Default Value:0x0000_0000)

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

Offset: 0x001C			Register Name: E_FRINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It Means that each location of the frame list is accessed 8 times (frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

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8.9.6.10 0x0024 EHCI Periodic Frame List Base Address Register (Default Value:0x0000_0000)

NOTE

Writes must be Dword Writes.

Offset: 0x0024			Register Name: E_PERIODICLISTBASE
Bit	Read/Write	Default/Hex	Description
31:12	R/W		Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

8.9.6.11 0x0028 EHCI Current Asynchronous List Address Register (Default Value:0x0000_0000)

NOTE

Writes must be Dword Writes.

Offset: 0x0028			Register Name: E_ASYNCLISTADDR
Bit	Read/Write	Default/Hex	Description
31:5	R/W		Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

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8.9.6.12 0x0050 EHCI Configure Flag Register (Default Value:0x0000_0000)

NOTE

This register is not use in the normal implementation.

Offset: 0x0050			Register Name: E_CONFIGFLAG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: Meaning 0: Port routing control logic default-routs each port to an implementation dependent classic host controller. 1: Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

8.9.6.13 0x0054 EHCI Port Status and Control Register (Default Value:0x0000_2000)

NOTE

This register is only reset by hardware or in response to a host controller reset.

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0	Wake on Disconnect Enable(WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
20	R/W	0	Wake on Connect Enable(WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow: Bits / Test Mode 0000b: The port is NOT operating in a test mode. 0001b: Test J_STATE 0010b: Test K_STATE 0011b: Test SE0_NAK 0100b: Test Packet 0101b: Test FORCE_ENABLE 0110b-1111b: Reserved The default value in this field is '0000b'.
15:14	/	/	/
13	R/W	1	Port Owner This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. Default Value = 1b.
12	/	/	/

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
11:10	R	0	Line Status These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bit[11:10] | USB State | Interpretation 00b | SE0 | Not Low-speed device, perform EHCI reset. 10b | J-state | Not Low-speed device, perform EHCI reset. 01b | K-state | Low-speed device, release ownership of port. 11b | Undefined | Not Low-speed device, perform EHCI reset. This value of this field is undefined if Port Power is zero.
9	/	/	/

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
8	R/W	0	Port Reset 1=Port is in Reset. 0=Port is not in Reset. Default value = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one. This field is zero if Port Power is zero.

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<table>
<tr><th colspan="3">Offset: 0x0054</th><th>Register Name: E_PORTSC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table>
<tr><th>Bits[Port Enables, Suspend]</th><th>Port State</th></tr>
<tr><td>0x</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
<tr><td>11</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
• Software sets the Force Port Resume bit to a zero(from a one).
• Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
</table>

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
6	R/W	0	Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0	Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
4	R	0	Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0	Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0	Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (Disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
1	R/WC	0	Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

8.9.7 OHCI Register Description

8.9.7.1 0x0400 OHCI Revision Register (Default Value:0x10)

Offset: 0x0400				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	/	/	/	/
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

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8.9.7.2 0x0404 OHCI Control Register (Default Value:0x0000_0000)

Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
8	R/W	R	0x0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt is routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.

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Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
7:6	R/W	R/W	0x0	HostControllerFunctionalState for USB 00b USBReset 01b USBResume 10b USBOperational 11b USBSuspend A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	R/W	R	0x0	BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

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Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
4	R/W	R	0x0	ControlListEnable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
3	R/W	R	0x0	IsochronousEnable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.

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Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. CBSR: No. of Control EDs Over Bulk EDs Served 0: 1:1 1: 2:1 2: 3:1 3: 4:1 The default value is 0x0.

8.9.7.3 0x0408 OHCI Command Status Register (Default Value:0x0000_0000)

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.

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Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

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8.9.7.4 0x040C OHCI Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.

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Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be Incremented.

8.9.7.5 0x0410 OHCI Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Resume Detected

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Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Write back Done Head
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Scheduling Overrun

8.9.7.6 0x0414 OHCI Interrupt Disable Register (Default Value:0x0000_0000)

Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Unrecoverable Error

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Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default	Description
	HCD	HC		
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Write back Done Head
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Scheduling Overrun

8.9.7.7 0x0418 OHCI HCCA Register (Default Value:0x0000_0000)

Offset: 0x0418				Register Name: O_HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA [31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA [7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

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8.9.7.8 0x041C OHCI Period Current ED Register (Default Value:0x0000_0000)

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED [31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.7.9 0x0420 OHCI Control Head ED Register (Default Value:0x0000_0000)

Offset: 0x0420				Register Name: O_HcControlHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD [31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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8.9.7.10 0x0424 OHCI Control Current ED Register (Default Value:0x0000_0000)

Offset: 0x0424				Register Name: HcControlCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED [31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.7.11 0x0428 OHCI Bulk Head ED Register (Default Value:0x0000_0000)

Offset: 0x0428				Register Name: O_HcBulkHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED [31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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8.9.7.12 0x042C OHCI Bulk Current ED Register (Default Value:0x0000_0000)

Offset: 0x42C				Register Name: O_HcBulkCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED [31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.7.13 0x0430 OHCI Done Head Register (Default Value:0x0000_0000)

Offset: 0x0430				Register Name: O_HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead [31:4] When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0	R	R	0x0	HcDoneHead [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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8.9.7.14 0x0434 OHCI Frame Interval Register (Default Value:0x0000_2EDF)

Offset: 0x0434				Register Name: O_HcFmInterval
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.9.7.15 0x0438 OHCI Frame Remaining Register (Default Value:0x0000_0000)

Offset: 0x0438				Register Name: O_HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/

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Offset: 0x0438				Register Name: O_HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

8.9.7.16 0x043C OHCI Frame Number Register (Default Value:0x0000_0000)

Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/
15:0	R	R/W	0x0	FrameNumber This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

8.9.7.17 0x0440 OHCI Periodic Start Register (Default Value:0x0000_0000)

Offset: 0x0440				Register Name: O_HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/

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Offset: 0x0440				Register Name: O_HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 0x2A3F (0x3e67). When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.9.7.18 0x0444 OHCI LS Threshold Register (Default Value:0x0000_0628)

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	/
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.9.7.19 0x0448 OHCI Root Hub DescriptorA Register (Default Value:0x0200_1201)

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.

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Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
23:13	/	/	/	/
12	R/W	R	1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0: Over-current status is reported collectively for all downstream ports. 1: No overcurrent protection supported.
11	R/W	R	0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0: Over-current status is reported collectively for all downstream ports. 1: Over-current status is reported on per-port basis.
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.

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Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
9	R/W	R	1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0: All ports are powered at the same time. 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
8	R/W	R	0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0: Ports are power switched. 1: Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

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8.9.7.20 0x044C OHCI Root Hub DescriptorB Register (Default Value:0x0000_0000)

Offset: 0x044C				Register Name: O_HcRhDescriptorB
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. ... Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. ... Bit15 Device attached to Port #15.

8.9.7.21 0x0450 OHCI Root Hub Status Register (Default Value:0x0000_0000)

Offset: 0x0450				Register Name: O_HcRhStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0	(write)ClearRemoteWakeupEnable Write a '1' clears DeviceRemoteWakeupEnable. Write a '0' has no effect.
30:18	/	/	/	/

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Offset: 0x0450				Register Name: O_HcRhStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
17	R/W	R	0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as '0'. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 ConnectStatusChange is not a remote wakeup event. 1 ConnectStatusChange is a remote wakeup event. (write)SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2	/	/	/	/
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'

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Offset: 0x0450				Register Name: O_HcRhStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

8.9.7.22 0x0454 OHCI Root Hub Port Status Register (Default Value:0x0000_0100)

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortEnableStatus 1 change in PortEnableStatus
16	R/W	R/W	0x0	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 no change in PortEnableStatus 1 change in PortEnableStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10	/	/	/	/

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
9	R/W	R/W	-	(read)LowSpeedDeviceAttached This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 full speed device attached 1 low speed device attached (write)ClearPortPower The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
8	R/W	R/W	0x1	(read)PortPowerStatus This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0 port power is off 1 port power is on (write)SetPortPower The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. Note: This bit is always reads '1b' if power switching is not supported.
7:5	/	/	/	/

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
4	R/W	R/W	0x0	(read)PortResetStatus When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 port reset signal is not active 1 port reset signal is active (write)SetPortReset The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.
3	R/W	R/W	0x0	(read)PortOverCurrentIndicator This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal. 0 no overcurrent condition. 1 overcurrent condition detected. (write)ClearSuspendStatus The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R/W	0x0	(read)PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0 port is not suspended 1 port is suspended (write)SetPortSuspend The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
1	R/W	R/W	0x0	(read)PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 port is disabled 1 port is enabled (write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0 No device connected 1 Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read '1' when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).

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8.9.8 HCI Contgroller and PHY Interface Description

8.9.8.1 0x0800 HCI Interface Register (Default Value:0x0000_0000)

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB Standby Clock Sel 0x0: normal mode USB clock as usual 0x1: standby mode USB clock switch to RC 16M clock
30:29	/	/	/
28	R	1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0	OHCI count select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time
24	R/W	0	Simulation mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect
23:21	/	/	/
20	R/W	0	EHCI HS force Set 1 to this field force the EHCI enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19	/	/	/
18	R/W	0	1: within 2us of the Resume-K to SE0 transition 0: random time value of the resume-K to SE0 transition
17:13	/	/	/
12	R/W	0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY

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Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
11	R/W	0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: do not use INCR8,use other enabled INCRX or unspecified length burst INCR
9	R/W	0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: do not use INCR4,use other enabled INCRX or unspecified length burst INCR
8	R/W	0	AHB Master interface INCRX align enable 1: start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of 11:9 is enabled
7:4	/	/	/
3	R/W	0x0	RC Clock Gating 0x0: clock gated 0x1: clock ungated
2	R/W	0x0	RC Generation Enable 0x0: disable 0x1: enable
1	/	/	/
0	R/W	0	ULPI bypass enable。 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

8.9.8.2 0x0808 HCI Control 3 Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
31:17	/	/	Reserved.
16	R/W1C	0	Linestate Change Detect 0: Linestate change not detected. 1: Linestate change detected. Write '1' to clear.
15:10	/	/	Reserved.

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Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
9	R/W	0	Forcesusp 1: Susp_Sel is valid. PHY could be configured into suspend mode when Susp_Sel = 0. 0: Susp_Sel is invalid.
8	R/W	0	Susp_Sel 1: Normal operating mode (PHY) 0: Suspend Mode (PHY) This bit is valid when forcesusp=1.
7:4	/	/	/
3	R/W	0	Remote Wakeup Enable 1: Enable 0: Disable
2	/	/	Reserved.
1	R/W	0	Linestate Change Interrupt Enable 1: Enable 0: Disable
0	R/W	0	Linestate Change Detect Enable 1: Enable 0: Disable

8.9.8.3 0x0810 PHY Control Register (Default Value: 0x0000_0018)

Offset: 0x0810			Register Name: PHY_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	VREGBYPASS
7	R/W	0	LOOPBACKENB
6	R/W	0	IDPULLUP
5	R/W	0	VBUSVLDEXT
4	R/W	1	VBUSVLDEXTSEL
3	R/W	1	SIDDQ 1: Write 1 to disable PHY. 0: Write 0 to enable PHY.
2	R/W	0	COMMONN
1:0	R/W	0	VATESTENB

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8.9.8.4 0x0814 PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0814			Register Name: PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

8.9.8.5 0x0818 PHY Tune Register (Default Value:0x05B3_33D4)

Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.9.8.6 0x0824 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: PHY_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0	TESTDATAOUT

8.9.8.7 0x0828 HCI SIE Port Disable Control Register (Default Value:0x0000_0003)

Offset: 0x0828			Register Name: USB_SPDCR
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0x0828			Register Name: USB_SPDCR
Bit	Read/Write	Default/Hex	Description
16	R/W	0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:5	/	/	/
4	R/W	0	resume_sel When set k-se0 transition 2us, setting this bit to 1, which is cooperated with ss_utmi_backward_enb_i.
3:2	/	/	/
1:0	R/W	0x3	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 Frames

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8.10 USB2.0 HOST

8.10.1 Overview

The USB Host Controller is fully compliant with USB 2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification Revision 1.0 and Open Host Controller Interface (OHCI) Specification Release 1.0a.

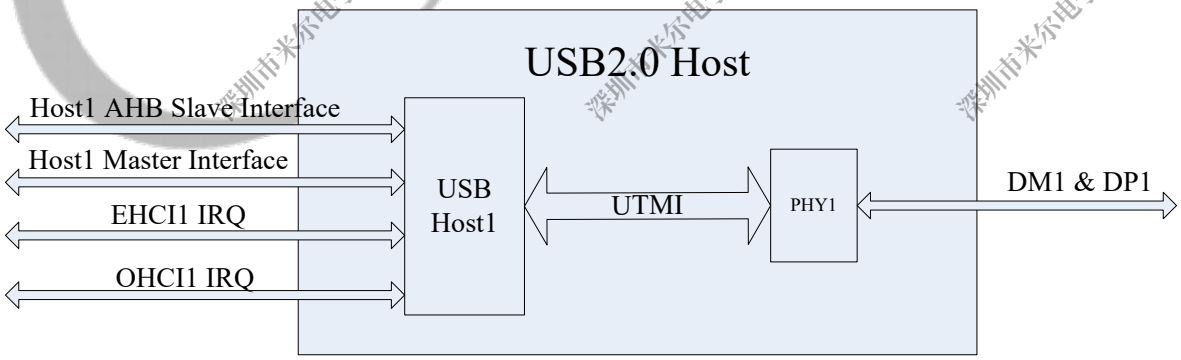
The USB2.0 host controller includes the following features:

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
- Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
- Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
- Supports only 1 USB Root port shared between EHCI and OHCI
- An internal DMA Controller for data transfer with memory
- Supports the UTMI+ Level 3 interface and 8-bit bidirectional data buses
- Industry-standard AMBA High-Performance Bus (AHB), fully compliant with the AMBA Specification, Revision 2.0.
- 32-bit Little Endian AMBA AHB Slave Bus for Register Access
- 32-bit Little Endian AMBA AHB Master Bus for Memory Access

8.10.2 Block Diagram

The following figure shows the block diagram of USB2.0 Host Controller.

Figure 8-52 USB2.0 Host Controller Block Diagram



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8.10.3 Functional Description

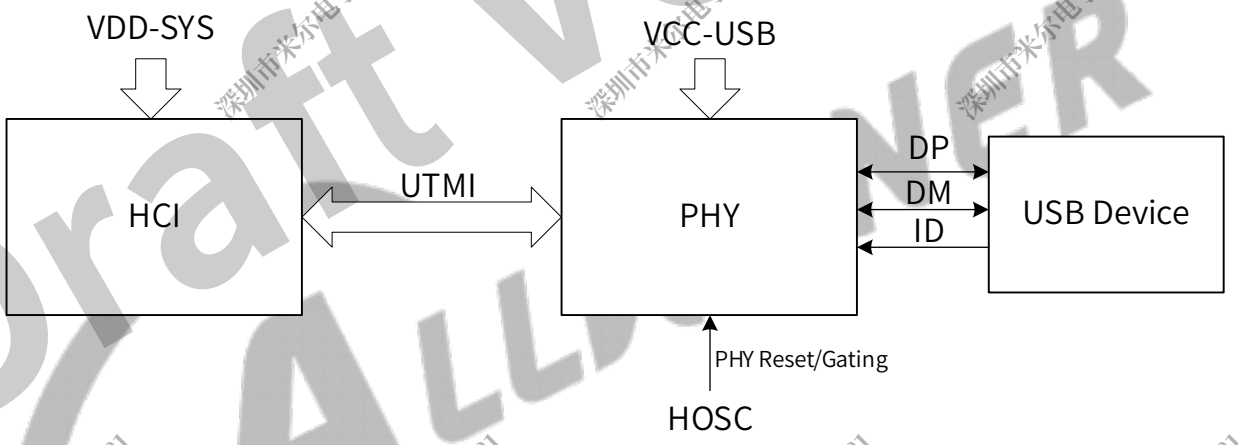
8.10.3.1 External Signals

Table 8-34 USB2.0 Host External Signals

Signal Name	Description	Type
USB1-DM	USB2.0 Data Signal DM	A I/O
USB1-DP	USB2.0 Data Signal DP	A I/O
USB1-REXT	USB2.0 External Reference Resistor AO	AO

8.10.3.2 Controller and PHY Connection Diagram

Figure 8-53 USB2.0 Host Controller and PHY Connection Diagram



8.10.4 Register List

Module Name	Base Address
USB1	0x04200000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x0000	EHCI Capability register Length Register
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000c	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register

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Register Name	Offset	Description
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x0020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x0024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x0418	OHCI HCCA Base
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Base
O_HcControlHeadED	0x0420	OHCI Control Head ED Base
O_HcControlCurrentED	0x0424	OHCI Control Current ED Base
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x042C	OHCI Bulk Current ED Base
O_HcDoneHead	0x0430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x0448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x044C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register
HCI Controller and PHY Interface Register		
USB_CTRL	0x0800	HCI Interface Register
HCI_CTRL3	0x0808	HCI Control 3 Register
PHY_CTRL	0x0810	PHY Control Register
PHY_TEST	0x0814	PHY Test Register
PHY_TUNE	0x0818	PHY Tune Register
PHY_STA	0x0824	PHY Status Register
USB_SPDCR	0x0828	HCI SIE Port Disable Control Register

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8.10.5 EHCI Register Description

8.10.5.1 0x0000 EHCI Identification Register (Default Value:0x10)

Offset:0x0000			Register Name: E_CAPLENGTH
Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

8.10.5.2 0x0002 EHCI Host Interface Version Number Register (Default Value:0x0100)

Offset: 0x0002			Register Name: E_HCIVERSION
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0100	HCIVERSION This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.10.5.3 0x0004 EHCI Host Control Structural Parameter Register (Default Value:0x0000_1101)

Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R	0x0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	0x1	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.

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Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
11:8	R	0x1	Number of Port per Companion Controller (N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0x0	Port Routing Rules This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value: 0 — Meaning: The first N_PCC ports are routed to the lowe numbered function companion host controller, the next N_PCC port are routed t the next lowest function companion controller, and so on. Value: 1 — Meaning: The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. This field will always be '0'.
6:4	/	/	/
3:0	R	0x1	N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

8.10.5.4 0x0008 EHCI Host Control Capability Parameter Register (Default Value:0x0000_A026)

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
15:8	R	0xA0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R	0x2	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	0x1	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	0x1	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.

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Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
0	/	/	/

8.10.5.5 0x000C EHCI Companion Port Route Description (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: E_HCSP-PORTROUTE
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.10.5.6 0x0010 EHCI USB Command Register (Default Value:0x0008_0B00)

Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x08	Interrupt Threshold Control The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below: Value / Minimum Interrupt Interval 0x00 / Reserved 0x01 / 1 micro-frame 0x02 / 2 micro-frame 0x04 / 4 micro-frame 0x08 / 8 micro-frame(default, equates to 1 ms) 0x10 / 16 micro-frame(2ms) 0x20 / 32 micro-frame(4ms) 0x40 / 64 micro-frame(8ms) Any other value in this register yields undefined results. The default value in this field is 0x08 . Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.
15:12	/	/	/
11	R	0x1	Asynchronous Schedule Park Mode Enable (OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.
10	/	/	/

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Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
9:8	R	0x3	Asynchronous Schedule Park Mode Count (OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0x0	Light Host Controller Reset (OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host

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Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	Interrupt on Async Advance Doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one. Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.
5	R/W	0x0	Asynchronous Schedule Enable This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean: Bit Value: Meaning 0: Do not process the Asynchronous Schedule. 1: Use the ASYNLISTADDR register to access the Asynchronous Schedule. The default value of this field is ‘0b’.
4	R/W	0x0	Periodic Schedule Enable This bit controls whether the host controller skips processing the Periodic Schedule. Values mean: Bit Value: Meaning 0: Do not process the Periodic Schedule. 1: Use the PERIODICLISTBASE register to access the Periodic Schedule. The default value of this field is ‘0b’.

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Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x0	Frame List Size This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean: Bits: Meaning 00b: 1024 elements(4096bytes)Default value 01b: 512 elements(2048byts) 10b: 256 elements(1024bytes)For resource constrained condition 11b: reserved The default value is '00b'.
1	R/W	0x0	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.

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Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

8.10.5.7 0x0014 EHCI USB Status Register (Default Value:0x0000_1000)

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).

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Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
14	R	0x0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0x0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.

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Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
3	R/WC	0x0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

8.10.5.8 0x0018 EHCI USB Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/

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Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

8.10.5.9 0x001C EHCI Frame Index Register (Default Value:0x0000_0000)

Offset: 0x001C			Register Name: E_FRINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/

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Offset: 0x001C			Register Name: E_FRINDEX
Bit	Read/Write	Default/Hex	Description
13:0	R/W	0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times (frames or Micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

8.10.5.10 0x0024 EHCI Periodic Frame List Base Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: E_PERIODICLISTBASE
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4 Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

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NOTE

Writes must be Dword Writes.

8.10.5.11 0x0028 EHCI Current Asynchronous List Address Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: E_ASYNCLISTADDR
Bit	Read/Write	Default/Hex	Description
31:5	R/W	0x0	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

8.10.5.12 0x0050 EHCI Configure Flag Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: E_CONFIGFLAG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Configure Flag (CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: Meaning 0: Port routing control logic default-routs each port to an implementation dependent classic host controller. 1: Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

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NOTE

This register is not used in the normal implementation.

8.10.5.13 0x0054 EHCI Port Status and Control Register (Default Value:0x0000_2000)

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	Wake on Disconnect Enable (WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0x0	Wake on Connect Enable (WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0x0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follows: Bits: Test Mode 0000b: The port is NOT operating in a test mode. 0001b: Test J_STATE 0010b: Test K_STATE 0011b: Test SE0_NAK 0100b: Test Packet 0101b: Test FORCE_ENABLE 0110b-1111b: Reserved The default value in this field is '0000b'.
15:14	/	/	/

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
13	R/W	0x1	Port Owner This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. Default Value = 1b.
12	/	/	/
11:10	R	0x0	Line Status These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bit[11:10] / USB State / Interpretation 00b / SE0 / Not Low-speed device, perform EHCI reset. 10b / J-state / Not Low-speed device, perform EHCI reset. 01b / K-state / Low-speed device, release ownership of port. 11b / Undefined / Not Low-speed device, perform EHCI reset. This value of this field is undefined if Port Power is zero.
9	/	/	/

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	Port Reset 1=Port is in Reset. 0=Port is not in Reset. Default value = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: When software writes this bit to a one , it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one. This field is zero if Port Power is zero.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	Suspend Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits[Port Enables, Suspend] / Port State 0x / Disable 10 / Enable 11 / Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: ① Software sets the Force Port Resume bit to a zero(from a one). ② Software sets the Port Reset bit to a one(from a zero). If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0x0	Over-current Change This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	Over-current Active 0 = This port does not have an over-current condition 1 = This port currently has an over-current condition This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
3	R/WC	0x0	Port Enable/Disable Change 1 = Port enabled/disabled status has changed 0 = No change For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	Port Enabled/Disabled 1=Enable 0=Disable Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (Disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0x0	Connect Status Change 1=Change in Current Connect Status 0=No change Indicates a change has occurred in the current connect status of the port. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.

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Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
0	R	0x0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

NOTE

This register is only reset by hardware or in response to a host controller reset.

8.10.6 OHCI Register Description

8.10.6.1 0x0404 OHCI Control Register (Default Value: 0x0000_0000)

Offset: 0x0404				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in *HcInterruptStatus* is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.

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Offset: 0x0404				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
8	R/W	R	0x0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	R/W	0x0	HostControllerFunctionalState for USB 00b USBReset 01b USBResume 10b USBOperational 11b USBSuspend A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.

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Offset: 0x0404				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
5	R/W	R	0x0	BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, the processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcBulkCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcBulkCurrentED* before re-enabling processing of the list.
4	R/W	R	0x0	ControlListEnable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, the processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcControlCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcControlCurrentED* before re-enabling processing of the list.
3	R/W	R	0x0	IsochronousEnable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.

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Offset: 0x0404				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. CBSR — No. of Control EDs Over Bulk EDs Served 0 — 1:1 1 — 2:1 2 — 3:1 3 — 4:1 The default value is 0x0.

8.10.6.2 0x0408 OHCI Command Status Register (Default Value: 0x0000_0000)

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.

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Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.

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Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

8.10.6.3 0x040C OHCI Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.

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Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the SchedulingOverrunCount of *HcCommandStatus* to be incremented.

8.10.6.4 0x0410 OHCI Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Root Hub Status Change

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Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Write back Done Head
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Scheduling Overrun

8.10.6.5 0x0414 OHCI Interrupt Disable Register (Default Value: 0x0000_0000)

Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/

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Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Write back Done Head
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Scheduling Overrun

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8.10.6.6 0x0418 OHCI HCCA Register (Default Value: 0x0000_0000)

Offset: 0x0418				Register Name: O_HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA [31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA [7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

8.10.6.7 0x041C OHCI Period Current ED Register (Default Value: 0x0000_0000)

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED [31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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8.10.6.8 0x0420 OHCI Control Head ED Register (Default Value: 0x0000_0000)

Offset: 0x0420				Register Name: O_HcControlHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD [31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.10.6.9 0x0424 OHCI Control Current ED Register (Default Value: 0x0000_0000)

Offset: 0x0424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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8.10.6.10 0x0428 OHCI Bulk Head ED Register (Default Value: 0x0000_0000)

Offset: 0x0428				Register Name: O_HcBulkHeadED[BHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED [31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.10.6.11 0x042C OHCI Bulk Current ED Register (Default Value: 0x0000_0000)

Offset: 0x042C				Register Name: O_HcBulkCurrentED[BCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED [31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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8.10.6.12 0x0430 OHCI Done Head Register (Default Value: 0x0000_0000)

Offset: 0x0430				Register Name: O_HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead [31:4] When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of *HcInterruptStatus*.
3:0	R	R	0x0	HcDoneHead [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.10.6.13 0x0434 OHCI Frame Interval Register (Default Value: 0x0000_2EDF)

Offset: 0x0434				Register Name: O_HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/

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Offset: 0x0434				Register Name: O_HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.10.6.14 0x0438 OHCI Frame Remaining Register (Default Value: 0x0000_0000)

Offset: 0x0438				Register Name: O_HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of *HcFmInterval* whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

8.10.6.15 0x043C OHCI Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/

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Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
15:0	R	R/W	0x0	FrameNumber This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in *HcInterruptStatus*.

8.10.6.16 0x0440 OHCI Periodic Start Register (Default Value: 0x0000_0000)

Offset: 0x0440				Register Name: O_HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*. A typical value will be 0x2A3F (or 0x3e67). When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.10.6.17 0x0444 OHCI LS Threshold Register (Default Value: 0x0000_0628)

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	/

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Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.10.6.18 0x0448 OHCI Root Hub DescriptorA Register (Default Value: 0x0200_1201)

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	0x1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0: Over-current status is reported collectively for all downstream ports. 1: No overcurrent protection supported.
11	R/W	R	0x0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0: Over-current status is reported collectively for all downstream ports. 1: Over-current status is reported on per-port basis.

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Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	0x1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0 All ports are powered at the same time. 1 Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
8	R/W	R	0x0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 Ports are power switched. 1 Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

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8.10.6.19 0x044C HcRhDescriptorB Register (Default Value: 0x0000_0000)

Offset: 0x044C				Register Name: O_HcRhDescriptorB Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. ... Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. ... Bit15 Device attached to Port #15.

8.10.6.20 0x0450 HcRhStatus Register (Default Value: 0x0000_0000)

Offset: 0x0450				Register Name: O_HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	(write)ClearRemoteWakeupEnable Write a '1' clears DeviceRemoteWakeupEnable. Writing a '0' has no effect.
30:18	/	/	/	/

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Offset: 0x0450				Register Name: O_HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
17	R/W	R	0x0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a '1'. Writing a '0' has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as '0'. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 ConnectStatusChange is not a remote wakeup event. 1 ConnectStatusChange is a remote wakeup event. (write)SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2	/	/	/	/
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'

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Offset: 0x0450				Register Name: O_HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

8.10.6.21 0x0454 HcRhPortStatus Register (Default Value: 0x0000_0100)

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:21	/	/	/	/
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortEnableStatus 1 change in PortEnableStatus
16	R/W	R/W	0x0	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 no change in PortEnableStatus 1 change in PortEnableStatus **Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.**
15:10	/	/	/	/

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
9	R/W	R/W	0x0	(read)LowSpeedDeviceAttached This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 full speed device attached 1 low speed device attached (write)ClearPortPower The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
8	R/W	R/W	0x1	(read)PortPowerStatus This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0 port power is off 1 port power is on (write)SetPortPower The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. **Note: This bit is always reads '1b' if power switching is not supported.**
7:5	/	/	/	/

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
4	R/W	R/W	0x0	(read)PortResetStatus When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 port reset signal is not active 1 port reset signal is active (write)SetPortReset The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.
3	R/W	R/W	0x0	(read)PortOverCurrentIndicator This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal. 0 no overcurrent condition. 1 overcurrent condition detected. (write)ClearSuspendStatus The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R/W	0x0	(read)PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0 port is not suspended 1 port is suspended (write)SetPortSuspend The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

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Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
1	R/W	R/W	0x0	(read)PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 port is disabled 1 port is enabled (write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0 No device connected 1 Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' to this bit has no effect. The CurrentConnectStatus is not affected by any write. **Note: This bit is always read '1' when the attached device is nonremovalble (DviceRemoveable[NumberDownstreamPort]).**

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8.10.7 HCI Contgroller and PHY Interface Description

8.10.7.1 0x0800 HCI Interface Register (Default Value: 0x1000_0000)

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB Standby Clock Sel 0x0: normal mode usb clock as usual 0x1: standby mode usb clock switch to RC 16M clock
30:29	/	/	Reserved
28	R	1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0	OHCI count select 1: Simulation mode. The counters will be much shorter then real time 0: Normal mode. The counters will count full time
24:19	/	/	/
18	R/W	0	1: Within 2 us of the resume-K to SE0 transition 0: Random time value of the resume-K to SE0 transition
17:13	/	/	/
12	R/W	0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: Do not use INCR16, use other enabled INCRX or unspecified length burst INCR
10	R/W	0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: Do not use INCR8, use other enabled INCRX or unspecified length burst INCR
9	R/W	0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: Do not use INCR4, use other enabled INCRX or unspecified length burst INCR

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Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
8	R/W	0	AHB Master interface INCRX align enable 1: Start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of bit[11:9] is enabled
7:4	/	/	/
3	R/W	0x0	RC Clock Gating 0x0: clock gated 0x1: clock ungated
2	R/W	0x0	RC Generation Enable 0x0: disable 0x1: enable
1	/	/	/
0	R/W	0	ULPI bypass enable 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

8.10.7.2 0x0808 HCI Control 3 Register (Default Value: 0x0001_0000)

Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
31:17	/	/	Reserved
16	R/W1C	0	Linestate Change Detect 0: Linestate change not detected 1: Linestate change detected Write '1' to clear.
15:10	/	/	Reserved
9	R/W	0	Forcesusp 1: Susp_Sel is valid. PHY could be configured into suspend mode when Susp_Sel = 0. 0: Susp_Sel is invalid.
8	R/W	0	Susp_Sel 1: Normal operating mode(PHY) 0: Suspend Mode(PHY) This bit is valid when forcesusp=1.
7:4	/	/	/
3	R/W	0	Remote Wakeup Enable 1: Enable 0: Disable
2	/	/	Reserved

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Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
1	R/W	0	Linestate Change Interrupt Enable 1: Enable 0: Disable
0	R/W	0	Linestate Change Detect Enable 1: Enable 0: Disable

8.10.7.3 0x0810 PHY Control Register (Default Value: 0x0000_0018)

Offset: 0x0810			Register Name: PHY_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	VREGBYPASS
7	R/W	0	LOOPBACKENB
6	R/W	0	IDPULLUP
5	R/W	0	VBUSVLDEXT
4	R/W	1	VBUSVLDEXTSEL
3	R/W	1	SIDDQ 1: Write 1 to disable phy. 0: Write 0 to enable phy.
2	R/W	0	COMMONN
1:0	R/W	0	VATESTENB

8.10.7.4 0x0814 PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0814			Register Name: PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

8.10.7.5 0x0818 PHY Tune Register (Default Value:0x05B3_33D4)

Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

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Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.10.7.6 0x0824 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: PHY_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0	TESTDATAOUT

8.10.7.7 0x0828 HCI SIE Port Disable Control Register (Default Value: 0x0000_0000)

Offset: 0x0828			Register Name: USB_SPDCR
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:5	/	/	/
4	R/W	0	resume_sel When set k-se0 transition 2 us, setting this bit to 1, which is cooperated with ss_utmi_backward_enb_i.
3:2	/	/	/
1:0	R/W	0	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 frames

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8.11 PCIe2.1&USB3.1 Top System

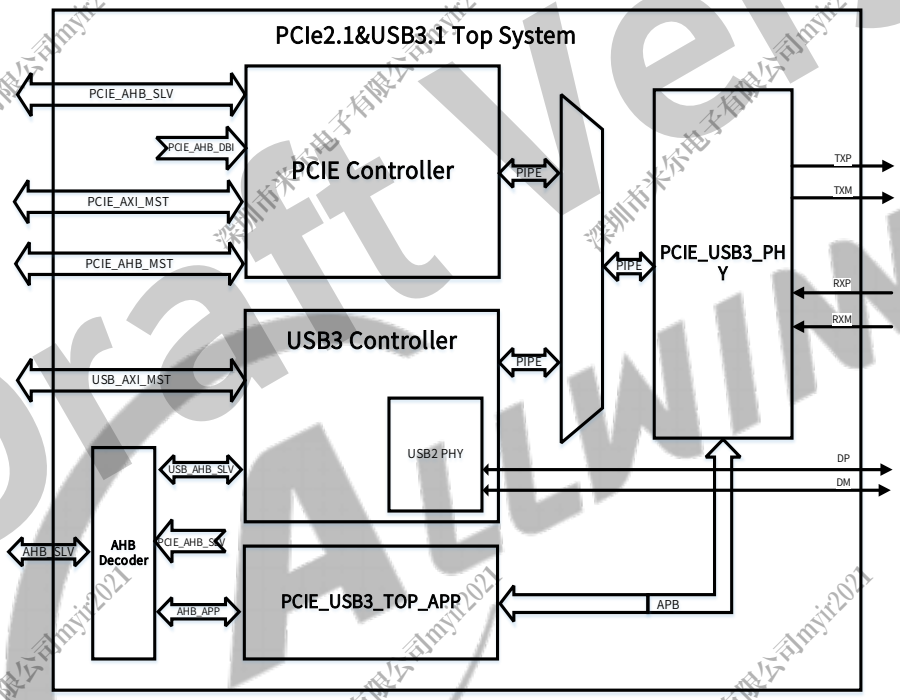
8.11.1 Overview

The PCIe2.1&USB3.1 top system integrates a PCIe2.1 RC controller and a USB3.1 DRD controller with a Combo PHY which supports PCIe GEN1 GEN2 and USB3.1 GEN1 speed and is shared through PIPE interface.

8.11.2 Block Diagram

The following figure shows the block diagram of PCIe2.1&USB3.1 top system.

Figure 8-54 PCIe2.1&USB3.1 Top System Block Diagram



NOTE

This chapter foucuses on the 1 PCIe2.1&USB3.1 combo PHY. For the detailed description of PCIe2.1 and USB3.1 DRD, please refer to section 8.13 PCIe2.1 and section 8.12 USB3.1 DRD.

8.11.3 Register List

Module Name	Base Address
PCIE_USB3_TOP_APP	0x04F00000

Register Name	Offset	Description
PCIEBGR	0x0004	PCIE Bus Gating Reset Register
USB3BGR	0x0008	USB3 Bus Gating Reset Register

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Register Name	Offset	Description
PHYCTL	0x0010	PHY Control Register
PHYSTS0	0x0080	PHY Status Register 0
PHYSTS1	0x0084	PHY Status Register 1
PHYSTS2	0x0088	PHY Status Register 2

8.11.4 Register Description

8.11.4.1 0x0004 PCIE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PCIEBGR
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	PCIE_ACLK_EN PCIE AXI Clock Enable
16	R/W	0x0	PCIE_HCLK_EN PCIE AHB Clock Enable
15:2	/	/	/
1	R/W	0x0	PCIE_PERSTN
0	R/W	0x0	PCIE_POWER_UP_RSTN

8.11.4.2 0x0008 USB3 Bus Gating Reset Register (Default Value:0x0000_0000)

Offset: 0x0008			Register Name: USB3BGR
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	USB3_ACLK_EN USB3 AXI Clock Enable
16	R/W	0x0	USB3_HCLK_EN USB3 AHB Clock Enable
15:1	/	/	/
0	R/W	0x0	USB3_RESETN

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8.11.4.3 0x0010 PHY Control Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: PHYCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY_USE_SEL 0: PHY used by PCIE 1: PHY used by USB3
30	R/W	0x0	PHY_REFCLK_SEL 0: PHY uses internal single end reference clock 1: PHY uses external differential reference clock
29:17	/	/	/
16	R/W	0x0	PHY_BIST_EN
15:10	/	/	/
9	R/W	0x0	PHY_PIPE_RSTN_SW
8	R/W	0x0	PHY_PIPE_RSTN_SEL 0: PHY PIPE resetn is controlled by PCIE or USB3 Controller 1: PHY PIPE resetn is controlled by PHY_PIPE_RSTN_SW
7:5	/	/	/
4	R/W	0x0	PHY_PIPE_CLK_INVERT
3:1	/	/	/
0	R/W	0x0	PHY_RSTN Combo PHY Power On RESET_N

8.11.4.4 0x0080 PHY Status Register 0 (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: PHYSTS0
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PHY_PIPE_PHYSTATUS_ASSERT_PENDING
30	R	0x0	PHY_PIPE_PHYSTATUS
29:2	/	/	/
1	R	0x0	PHY_BIST_PASS
0	R	0x0	PHY_BIST_DONE

8.11.4.5 0x0084 PHY Status Register 1 (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: PHYSTS1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY_PIPE_RX_DBG_EN
30:7	/	/	/
6	R	0x0	PHY_PIPE_RXELECIDLE

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Offset: 0x0084			Register Name: PHYSTS1
Bit	Read/Write	Default/Hex	Description
5	R	0x0	PHY_PIPE_RXVALID
4	R	0x0	PHY_PIPE_RXDATAVALID
3:0	R	0x0	PHY_PIPE_RXDATAK

8.11.4.6 0x0088 PHY Status Register 2 (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: PHYSTS2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PHY_PIPE_RXDATA

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8.12 USB3.1 DRD

8.12.1 Overview

The USB3.1 DRD is a Dual-Role Device (DRD) controller, which supports both device and host functions which can also be configured as a host-only or device-only controller, fully compliant with the USB 3.1 Specification. It can support super-speed (SS, 5-Gbit/s), high-speed (HS, 480-Mbit/s), full-speed (FS, 12-Mbit/s), and low-speed (LS, 1.5-Mbit/s) transfers in Host mode. It can support super-speed (SS, 5-Gbit/s), high-speed (HS, 480-Mbit/s), and full-speed (FS, 12-Mbit/s) in Device mode. Standard USB transceiver can be used through its UTMI+ interface and PIPE interface.

The USB3 DRD controller includes the following features:

- Compliant with USB3.1 GEN1 Specification
- One USB 2.0 UTMI+ PHY (USB2)
- One USB3.1 PIPE PHY (USB3)
- Support Device or Host operation at a time
- USB3.1 DRD Device mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s) and Full-Speed (FS, 12-Mbit/s) for USB2.0 PHY
- USB3.1 DRD HOST mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) for USB2.0 PHY
- AXI interface for DMA operation
- Reading and writing access to Control and Status Registers (CSRs) through AHB Slave interface
- Up to 10 Endpoints, including bi-directional control Endpoint 0 in Device mode:
  - 5 IN Endpoints: User EP1 IN, EP2 IN, EP3 IN, EP4 IN, Control EP0 IN
  - 5 OUT Endpoints: User EP1 OUT, EP2 OUT, EP3 OUT, EP4 OUT, Control EP0 OUT
- Simultaneous IN and OUT transfer in Super-Speed mode
- Dual-port interfaces for TX data buffering, RX data prefetching, descriptor caching, and register caching
- Three RAMs: RX data FIFO RAM, TX data FIFO RAM, and descriptor/register Cache RAM
- Hardware handles all data transfer
- Implements both static and dynamic power reduction techniques at multiple levels

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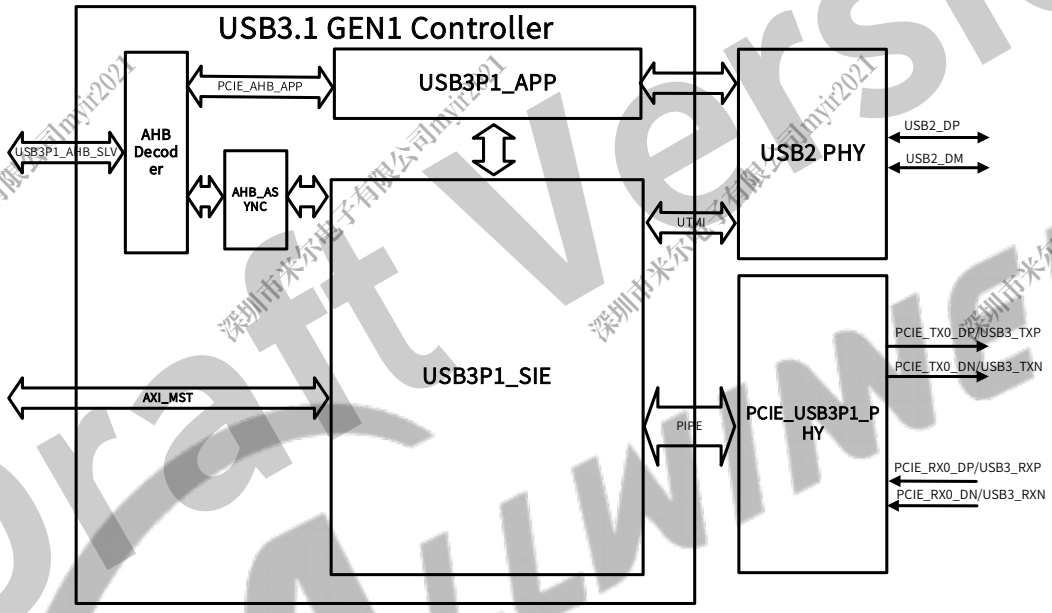
NOTE

USB2.0 PHY and USB3.1 PHY share the same controller. They cannot be used simultaneously.

8.12.2 Block Diagram

The following figure shows the block diagram of USB3.1 DRD Controller

Figure 8-55 USB3.1 DRD Controller Block Diagram



8.12.3 Functional Description

8.12.3.1 External Signals

Table 8-35 USB3.1 DRD External Signals

Signal Name	Description	Type
USB2-DM	USB2.0 Data Signal DM	A I/O
USB2-DP	USB2.0 Data Signal DP	A I/O
USB2-REXT	USB2.0 External Reference Resistor	AO
USB3-RXP	USB3.1 SuperSpeed Differential Signal of RX (Positive)	AI
USB3-RXN	USB3.1 SuperSpeed Differential Signal of RX (Negative)	AI
USB3-TXP	USB3.1 SuperSpeed Differential Signal of TX (Positive)	AO
USB3-TXN	SuperSpeed Differential Signal of TX (Negative)	AO
VCC33-USB-2	3.3 V Power Supply for USB2.0 PHY	P
VCC33-18-USB-2	3.3 V/1.8 V Power Supply for USB2.0 PHY	P

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NOTE

For detailed functional information, please refer to *USB3.1 Specification, USB2.0 Specification,* and *eXtensible Host Controller Interface (XHCI) Specification, Version 1.1.*

8.12.4 Register List

There are four groups of registers in USB3.1 DRD.

Register Class	Offset
USB3 (0x04D0 0000---0x04EF FFFF)	
xHCI Registers	0x00000000 - 0x00007FFF
Global Registers	0x0000C100 - 0x0000C6FF
Device Registers	0x0000C700 - 0x0000CBFF
Application Registers	0x0010 0000 - 0x001007FF

8.12.4.1 xHCI Register List

Register Class	Base Address
xHCI Registers	0x04D0 0000-0x04D0 7FFF

Register Name	Offset	Description
xHCI Capability Registers		
HCCLVER	0x0000	xHC Capability Length and Version Register
HCSPARAMS1	0x0004	xHC Structural Parameter 1 Register
HCSPARAMS2	0x0008	xHC Structural Parameters 2 Register
HCSPARAMS3	0x000C	xHC Structural Parameters 3 Register
HCCPARAMS	0x0010	xHC Capability Parameters Register
DBOFF	0x0014	xHC Doorbell Offset Register
RTSOFF	0x0018	xHC Runtime Register Space Offset Register
HCCPARAMS2	0x001C	xHC Capability Parameters 2 Register
xHCI Operational Registers		
HCUSBCMD	0x0020	xHC USB Command Register
HCUSBSTS	0x0024	xHC USB Status Register
HCPAGESIZE	0x0028	xHC Page Size Register
HCDNCTRL	0x0034	xHC Device Notification Control Register
HCCRCLR	0x0038	xHC Command Ring Control Low Register
HCCRCHR	0x003C	XHC Command Ring Control High Register
HCDCBAAPLR	0x0050	xHC Device Context Base Address Array Pointer Low Register

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Register Name	Offset	Description
HCDCBAAPHR	0x0054	xHC Device Context Base Address Array Pointer High Register
HCCONFIG	0x0058	xHC Configure Register
HCPORT1SC	0x0420	xHC Port1 Status and Control Register (USB2 Protocol)
HCPORT1PMSC	0x0424	xHC Port1 PM Status and Control Register (USB2 Protocol)
HCPORT1LI	0x0428	xHC Port1 Link Info Register (USB2 Protocol)
HCPORT2SC	0x0430	xHC Port2 Status and Control Register (USB3 Protocol)
HCPORT2PMSC	0x0434	XHC Port2 PM Status and Control Register (USB3 Protocol)
HCPORT2LI	0x0438	xHC Port2 Link Info Register (USB3 Protocol)
xHCI Runtime Registers		
HCMFINDEX	0x1000	xHC Microframe Index Register
HCIMAN0	0x1020	xHC Interrupt 0 Management Register
HCIMOD0	0x1024	xHC Interrupt 0 Moderation Register
HCERSTSZ0	0x1028	xHC Interrupt 0 Event Ring Segment Table Size Register
HCERSTBAL0	0x1030	xHC Interrupt 0 Event Ring Segment Table Base Address Low Register
HCERSTBAH0	0x1034	xHC Interrupt 0 Event Ring Segment Table Base Address High Register
HCERDPL0	0x1038	xHC Interrupt 0 Event Ring Dequeue Pointer Low Register
HCERDPH0	0x103C	xHC Interrupt 0 Event Ring Dequeue Pointer High Register
xHCI Doorbell Registers		
HCDBRn (n = 0 to 64)	0x2000+4*n	XHC Doorbell Register n (n=0, 1,笨笨, 64)
xHCI Extended Capabilities Registers		
HCUSBLEGSUP	0x0440	xHC USB Legacy Support Capability Register
HCUSBLEGCTRLSTS	0x0444	xHC USB Legacy Support Control/Status Register
HCSPC1REV	0x0490	xHC Support Protocol Capability 1 Revision Register
HCSPC1STR	0x0494	xHC Support Protocol Capability 1 String Register
HCSPC1PRT	0x0498	xHC Support Protocol Capability 1 Port Register
HCSPC2REV	0x04A0	xHC Support Protocol Capability 2 Revision Register
HCSPC2STR	0x04A4	xHC Support Protocol Capability 2 String Register
HCSPC2PRT	0x04A8	xHC Support Protocol Capability 3 Port Register

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8.12.4.2 Global Register List

Register Class	Base Address
Global Registers	0x04D0 C100 - 0x04D0 C6FF

Register Name	Offset	Description
GSBUSCFG0	0xC100	Global Soc Bus Configuration Register 0
GSBUSCFG1	0xC104	Global Soc Bus Configuration Register 1
GTXTHRCFG	0xC108	Global Tx Threshold Control Register
GRXTHRCFG	0xC10C	Global Rx Threshold Control Register
GCTL	0xC110	Global Core Control Register
GPMSTS	0xC114	Global Power Management Status Register
GSTS	0xC118	Global Status Register
GUCTL1	0xC11C	Global User Control Register 1
GID	0xC120	Global ID Register
GGPIO	0xC124	Global General Purpose Input/Output Register
GUID	0xC128	Global User ID Register
GUCTL	0xC12C	Global User Control Register
GBUSERRADDR_Lo	0xC130	Global Bus Error Address Low Register
GBUSERRADDR_Hi	0xC134	Global Bus Error Address High Register
GPRTBIMAP_Lo	0xC138	Global Super Speed Port to Bus Instance Mapping Low Register
GPRTBIMAP_Hi	0xC13C	Global Super Speed Port to Bus Instance Mapping High Register
GDBGFIFOSPACE	0xC160	Global Debug Queue/FIFO Space Available Register
GBMUCTL	0xC164	Global BMU Control Register
GDBGBMU	0xC16C	Global Debug BMU Register
GDBGLSPMUX	0xC170	Global Debug LSP MUX Register
GDBGLSP	0xC174	Global Debug LSP Register
GDBGEPINFO0	0xC178	Global Debug Endpoint Information Register 0
GDBGEPINFO1	0xC17C	Global Debug Endpoint Information Register 1
GPRTBIMAP_HS_Lo	0xC180	Global High Speed Port to Bus Instance Mapping Low Register
GPRTBIMAP_HS_Hi	0xC184	Global High Speed Port to Bus Instance Mapping High Register
GPRTBIMAP_FS_Lo	0xC188	Global Full Speed Port to Bus Instance Mapping Low Register
GPRTBIMAP_FS_Hi	0xC18C	Global Full Speed Port to Bus Instance Mapping High Register
GHMSOCBWOR	0xC190	Global Host Mode SoC Bandwidth Override Register

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Register Name	Offset	Description
GUSB2PHYCFGn	0xC200	Global USB2 PHY Configuration Register
GUSB3PIPECTLn	0xC2C0	Global USB3 PIPE Control Register
GTXFIFOSIZ	0xC300+0x04*n (n=FIFO_number)	Global Transmit FIFO Size Register n (n=FIFO_number)
GRXFIFOSIZ0	0xC380+0x04*n (n=FIFO_number)	Global Receive FIFO Size Register n (n=FIFO_number)
GEVNTADLRn	0xC400+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Address Lower Register n (0<= n <= EventBuff_number)
GEVNTADHRn	0xC404+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Address Higher Register n (0<= n <= EventBuff_number)
GEVNTSIZn	0xC408+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Size Register n (0<= n <= EventBuff_number)
GEVNTCOUNTn	0xC40C+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Count Register n (0<= n <= EventBuff_number)
GTXFIFOPRIDEV	0xC610	Global Device Tx FIFO DMA Priority Register
GTXFIFOPRIHST	0xC618	Global Host Tx FIFO DMA Priority Register
GRXFIFOPRIHST	0xC61C	Global Host Rx FIFO DMA Priority Register
GDMAHLRATIO	0xC624	Global Host FIFO DMA High-Low Priority Ratio Register

8.12.4.3 Device Register List

Register Class	Base Address
Device Registers	0x04D0 C700 - 0x04D0 CBFF

Register Name	Offset	Description
DCFG	0xC700	Device Configuration Register
DCTL	0xC704	Device Control Register
DEVTEN	0xC708	Device Event Enable Register
DSTS	0xC70C	Device Status Register
DGCMDPAR	0xC710	Device Generic Command Parameter Register
DGCMD	0xC714	Device Generic Command Register
DCTL1	0xC718	Device Control Register 1
DALEPENA	0xC720	Device Active USB Endpoint Enable Register
DLDMENA	0xC724	Device LDM Request Control Register
DEPCMDPAR2_n (n=0 to 9)	0xC800+0x10*n	Device Physical Endpoint-n Command Parameter 2 Register

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Register Name	Offset	Description
DEPCMDPAR1_n (n=0 to 9)	0xC804+0x0010*n	Device Physical Endpoint-n Command Parameter 1 Register
DEPCMDPAR0_n (n=0 to 9)	0xC808+0x0010*n	Device Physical Endpoint-n Command Parameter 0 Register
DEPCMD_n (n=0 to 9)	0xC80c+0x0010*n	Device Physical Endpoint-n Command Register
DEPIMOD	0xCA00	Device Interrupt Moderation Register

8.12.4.4 Application Register List

Register Class	Base Address
Application Registers	0x04E0 0000 - 0x04E007FF

Register Name	Offset	Description
U2_ISCR	0x100000	USB2.0 Interface Status and Control Register
U2_PHYCTL	0x100010	USB2.0 PHY Control Register
U2_PHYTST	0x100014	USB2.0 PHY TEST Register
U2_PHYTUNE	0x100018	USB2.0 PHY Tune Register
U2_PHYSTS	0x100024	USB2.0 PHY Status Register

8.12.5 xHCI Register Description

8.12.5.1 x0000 xHC Capability Length and Version Register (Default Value: 0x0110_0020)

Offset:0x0000			Register Name: HCCLVER
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0110	HCIVERSION HC Interface Version Number This is a 16-bits register containing a BCD encoding of the xHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
15:8	/	/	/
7:0	R	0x20	CAPLENGTH Capability register Length This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

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8.12.5.2 0x0004 xHC Structural Parameters 1 Register (Default Value:0x0200_0140)

Offset: 0x0004			Register Name: HCSPARAMS1
Bit	Read/Write	Default/Hex	Description
31:24	R	0x02	MaxPorts Number of Ports This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Set that are addressable in the Operational Register Space
23:19	/	/	/
18:8	R	0x01	MaxIntrs Number of Interrupters This field specifies the number of Interrupters implemented on this host controller
7:0	R	0x40	MaxSlots Number of Device Slots This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support.

8.12.5.3 0x0008 xHC Structural Parameters 2 Register (Default Value: 0x1400_00F1)

Offset: 0x0008			Register Name: HCSPARAMS2
Bit	Read/Write	Default/Hex	Description
31:27	R	0x2	Max Scratchpad Bufs Lo Max Scratchpad Buffers Low This field indicates the low order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC
26	R	0x1	SPR Scratchpad Restore. If *Max Scratchpad Buffers* is > '0' then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If *Max Scratchpad Buffers* is = '0' then this flag shall be '0'. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events.

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Offset: 0x0008			Register Name: HCSPARAMS2
Bit	Read/Write	Default/Hex	Description
25:21	R	0	Max Scratchpad Bufs Hi Max Scratchpad Buffers High This field indicates the high order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC
20:8	/	/	/
7:4	R	0xF	ERST Max Event Ring Segment Table Max. This field determines the maximum value supported the Event Ring Segment Table Base Size registers, where: The maximum number of Event Ring Segment Table entries = $2^{\text{ERST Max}}$.
3:0	R	0x1	IST Isochronous Scheduling Threshold. The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/ microframes. If bit [3] of IST is cleared to '0', software can add a TRB no later than IST [2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed.

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8.12.5.4 0x000C xHC Structural Parameters 3 Register (Default Value:0x0200_000A)

Offset: 0x000C			Register Name: HCSPARAMS3
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0200	U2DEL U2 Device Exit Latency Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 0000h Zero 0001h Less than 1 µs. 0002h Less than 2 µs. ... 07FFh Less than 2047 µs. 0800-FFFFh Reserved
15:8	/	/	/
7:0	R	0x0A	U1DEL U1 Device Exit Latency Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs. ... 0Ah Less than 10 µs. 0B-FFh Reserved

8.12.5.5 0x0010 xHC Capability Parameters Register (Default Value:0x0110_FFCC)

Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0110	xECP xHCI Extended Capabilities Pointer This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, for Base to the beginning of the first extended capability. Extended Capabilities Offset = xECP<<2 =0x0110<<2 = 0x0440.

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Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
15:12	R	0xF	MaxPSASize Maximum Primary Stream Array Size This field indentifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array Size = $2^{MaxPSASize+1}$. Valid *MaxPSASize* values are 0 to 15, where '0' indicates that Streams are not supported
11	R	0x1	CFC Contiguous Frame ID Capability This flag indicates that the host controller implementation is capable of matching the Frame ID of consecutive Isoch TDs.
10	R	0x1	SEC Stopped EDTLA Capability This flag indicates that the host controller implementation Stream Context support a Stopped EDTLA field.
9	R	0x1	SPC Stopped - Short Packet Capability This flag indicates that the host controller implementation is capable of generating a *Stopped - Short Packet* Completion Code.
8	R	0x1	PAE Parse All Event Data This flag indicates whether the host controller implementation Parses all Event Data TRBs while advancing to the next TD after a Short Packet, or it skips all but the first Event Data TRB. A '1' in this bit indicates that all Event Data TRBs are parsed. A '0' in this bit indicates that only the first Event Data TRB is parsed
7	R	0x1	NSS No Secondary SID Support This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported.

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Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
6	R	0x1	LTC Latency Tolerance Messaging Capability This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. A '0' in this bit indicates that LTM is not supported.
5	R	0x0	LHRC Light HC Reset Capability This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the *Light Host Controller Reset* (LHCRST) flag in the USBCMD register
4	R	0x0	PIND Port Indicators This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	R	0x1	PPC Port Power Control This flag indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the *PP* flag in each port status and control register
2	R	0x1	CSZ Context Size If this bit is set to '1', then the xHC uses 64-byte Context data structures. If this bit is cleared to '0', then the xHC uses 32-byte Context data structures. Note: This flag does *not* apply to Stream Contexts.

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Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
1	R	0x0	BNC BW Negotiation Capability This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: Value Description 0 BW Negotiation not implemented 1 BW Negotiation implemented
0	R	0x0	AC64 64-bit Addressing Capability This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: Value Description 0 32-bit address memory pointers implemented 1 64-bit address memory pointers implemented If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.

8.12.5.6 0x0014 xHC Doorbell Offset Register (Default Value: 0x0000_2000)

Offset: 0x0014			Register Name: HCDBOFF
Bit	Read/Write	Default/Hex	Description
31:2	R	0x800	DBOFF Doorbell Array Offset This field defines the offset in Dwords of the Doorbell Array base address from the Base
1:0	/	/	/

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8.12.5.7 0x0018 xHC Runtime Register Space Offset Register (Default Value: 0x0000_1000)

Offset: 0x0018			Register Name: HCRTSOFF
Bit	Read/Write	Default/Hex	Description
31:5	R	0x80	RTSOFF Runtime Register Space Offset This field defines the 32-byte offset of the xHCI Runtime Registers from the Base.
4:0	/	/	/

8.12.5.8 0x001C xHC Capability Parameters 2 Register (Default Value: 0x0000_003F)

Offset: 0x001C			Register Name: HCCPARAMS2
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	CIC Configuration Information Capability. This bit indicates if the xHC supports extended Configuration Information. When this bit is 1, the *Configuration Value*, *Interface Number*, and *Alternate Setting* fields in the Input Control Context are supported. When this bit is 0, the extended Input Control Context fields are not supported.
4	R	0x1	LEC Large ESIT Payload Capability. This bit indicates whether the xHC supports ESIT Payloads greater than 48K bytes. When this bit is '1', ESIT Payloads greater than 48K bytes are supported. When this bit is '0', ESIT Payloads greater than 48K bytes are not supported.
3	R	0x1	CTC Compliance Transition Capability. This bit indicates whether the xHC USB3 Root Hub ports support the *Compliance Transition Enabled* (CTE) flag. When this bit is '1', USB3 Root Hub port state machine transitions to the Compliance substate shall be explicitly enabled software. When this bit is '0', USB3 Root Hub port state machine transitions to the Compliance substate are automatically enabled.

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Offset: 0x001C			Register Name: HCCPARAMS2
Bit	Read/Write	Default/Hex	Description
2	R	0x1	FSC Force Save Context Capability. This bit indicates whether the xHC supports the *Force Save Context Capability*. When this bit is '1', the *Save State* operation shall save any cached Slot, Endpoint, Stream or other Context information to memory.
1	R	0x1	CMC Configure Endpoint Command Max Exit Latency Too Large Capability. This bit indicates whether a *Configure Endpoint Command* is capable of generating a *Max Exit Latency Too Large Capability Error*. When this bit is '1', a *Max Exit Latency Too Large Capability Error* may be returned by a *Configure Endpoint Command*. When this bit is '0', a *Max Exit Latency Too Large Capability Error* shall not be returned by a *Configure Endpoint Command*. This capability is enabled by the *CME* flag in the USBCMD register.
0	R	0x1	U3C U3 Entry Capability. This bit indicates whether the xHC Root Hub ports support port Suspend Complete notification. When this bit is '1', *PLC* shall be asserted on any transition of *PLS* to the *U3* State.

8.12.5.9 0x0020 xHC USB Command Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	CME CEM Enable When set to '1', a *Max Exit Latency Too Large Capability Error* may be returned by a *Configure Endpoint Command*. When cleared to '0', a *Max Exit Latency Too Large Capability Error* shall not be returned by a *Configure Endpoint Command*. This bit is *Reserved* if *CMC* = '0'.

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Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	SPE Stopped - Short Packet Enable When set to '1', the xHC may generate a *Stopped - Short Packet* Completion Code. This bit is *Reserved* if *CMC* = '0'.
11	R/W	0x0	EU3S Enable U3 MFINDEX Stop When set to '1', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to '0' the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	R/W	0x0	EWE Enable Wrap Event When set to '1', the xHC shall generate a MFINDEX (Micro-Frame Index) Wrap Event every time the MFINDEX register transitions from 0x03FFF to 0. When cleared to '0' no MFINDEX Wrap Events are generated.
9	R/W	0x0	CRS Controller Restore State When set to '1', and HCHalted (HCH) = '1', then the xHC shall perform a Restore State operation and restore its internal state. When set to '1' and Run/Stop (R/S) = '1' or HCHalted (HCH) = '0', or when cleared to '0', no Restore State operation shall be performed. This flag always returns '0' when read. Refer to the Restore State Status (RSS) flag in the HCUSBSTS register for information on Restore State completion. Note that undefined behavior may occur if a Restore State operation is initiated while Save State Status (SSS) = '1'.

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Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	CSS Controller Save State When written by software with '1' and *HCHalted* (HCH) = '1', then the xHC shall save any internal state (that may be restored by a subsequent Restore State operation) and if *FSC* = '1' any cached Slot, Endpoint, Stream, or other Context information (so that software may save it). When written by software with '1' and *HCHalted* (HCH) = '0', or written with '0', no Save State operation shall be performed. This flag always returns '0' when read. Refer to the *Save State Status* (SSS) flag in the USBSTS register for information on Save State completion. Note that undefined behavior may occur if a Save State operation is initiated while *Restore State Status* (RSS) = '1'.
7:4	/	/	/
3	R/W	0x0	HSEE Host System Error Enable When this bit is a '1', and the HSE bit in the HCUSBSTS register is a '1', the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.
2	R/W	0x0	INTE Interrupter Enable This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a '1', then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism.

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Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	HCRST Host Controller Reset This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a '1' to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports; however, a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller in order to return the host controller to an operational state. This bit is cleared to '0' by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a '0' to this bit and shall not write any xHC Operational or Runtime registers while HCRST is '1'. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to '1' when the HCHalted (HCH) bit in the USBSTS register is a '0'. Attempting to reset an actively running host controller may result in undefined behavior.

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Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	RS Run/Stop 0x1: Run 0x0: Stop When set to '1'm the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. The xHC shall halt within 16ms, after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the HCUSBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is '1'). Doing so may yield undefined results. Writing a '0' to this flag when the xHC is in the Running state (i.e. HCH='0') and any Event Rings are in the Event Ring Full state may yield undefined results.

8.12.5.10 0x0024 xHC USB Status Register (Default Value:0x0000_0001)

Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R	0x0	HCE Host Controller Error This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC.

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Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
11	R	0x0	CNR Controller Not Ready Software shall not write any Doorbell or Operational register of the xHC, other than the HCUSBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared ('0') until the next Chip Hardware Reset.
10	R/W1C	0x0	SRE Save/Restore Error If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. *Note: This bit can be cleared by software writing '1'.*
9	R	0x0	RSS Restore State Status When the Controller Restore State (CRS) flag in the HCUSBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to '0'.
8	R	0x0	SSS Save State Status When the Controller Save State (CSS) flag in the HCUSBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to '0'.
7:5	/	/	/

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Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	PCD Port Change Detect The xHC sets this bit to a '1' when any port has a change bit transition from a '0' to a '1'. This bit is allowed to be maintained in the Aux Power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits. This bit provides system software an efficient means of determining if there has been Root Hub port activity. **Note: This bit can be cleared by software writing '1'.**
3	R/W1C	0x0	EINT Event Interrupt The xHC sets this bit to '1' when the Interrupt Pending (IP) bit of any Interrupter transitions from '0' to '1'. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition may occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition shall be lost. **Note: This bit can be cleared by software writing '1'.**
2	R/W1C	0x0	HSE Host System Error The xHC sets this bit to '1' when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the HCUSBCMD register is a '1', the xHC shall also assert out-of-band error signaling to the host. **Note: This bit can be cleared by software writing '1'.**
1	/	/	/

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Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
0	R	0x1	HCH HC Halted This bit is a '0' whenever the Run/Stop (R/S) bit is a '1'. The xHC sets this bit to '1' after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to '0', either by software or by the xHC hardware (e.g. internal error). If this bit is '1', then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC, and any received Transaction Packet shall be dropped.

8.12.5.11 0x0028 xHC Page Size Register (Default Value:0x0000_0001)

Offset: 0x0028			Register Name: HCPAGESIZE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0001	PageSize Page Size This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes.

8.12.5.12 0x0034 xHC Device Notification Control Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: HCDNCTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	NE Notification Enable (N0-N15) When a Notification Enable bit is set, a Device Notification Event shall be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), etc.

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8.12.5.13 0x0038 xHC Command Ring Control Low Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: HCCRCLR
Bit	Read/Write	Default/Hex	Description
31:6	R/W	0x00	CRPL Command Ring Pointer Low This field defines bit [31:6] of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CCR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
5:4	/	/	/
3	R	0x0	CRR Command Ring Running This flag is set to '1' if the Run/Stop (R/S) bit is '1' and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to '0' when the Command Ring is "stopped" after writing a '1' to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to '0'.

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Offset: 0x0038			Register Name: HCCRCLR
Bit	Read/Write	Default/Hex	Description
2	R/W1S	0x0	CA Command Abort Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit always returns '0'.
1	R/W1S	0x0	CS Command Stop Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit shall always return '0'.

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Offset: 0x0038			Register Name: HCCRCLR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	RSC Ring Cycle State This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Writes to this flag are ignored if Command Ring Running (CRR) is '1'. If the HCCRC*R is written while the Command Ring is stopped (CRR = '0'), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the HCCRC*R is not written while the Command Ring is stopped (CRR = '0'), then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns '0'.

8.12.5.14 0x003C xHC Command Ring Control High Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: HCCRCHR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00	CRPH Command Ring Pointer High This field defines bit[63:32] of the initial value of the 64-bit Command Ring Dequeue Pointer.

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8.12.5.15 0x0050 xHC Device Context Base Address Array Pointer Low Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: HCDCBAAPLR
Bit	Read/Write	Default/Hex	Description
31:6	R/W	0x00	DCBAAPL Device Context Base Address Array Pointer Low This field defines bit [31:6] of the 64-bit base address of Device Context Pointer Array. A table of address pointers that reference Device Context structures for the device attached to the host. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
5:0	/	/	/

8.12.5.16 0x0054 xHC Device Context Base Address Array Pointer High Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: HCDCBAAPHR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00	DCBAAPH Device Context Base Address Array Pointer High This field defines bit[63:32] of the 64-bit base address of Device Context Pointer Array.

8.12.5.17 0x0058 xHC Configure Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: HCCONFIG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	CIE Configuration Information Enable When set to '1', the software shall initialize the *Configuration Value*, *Interface Number*, and *Alternate Setting* fields in the Input Control Context when it is associated with a Configure Endpoint Command. When this bit is '0', the extended Input Control Context fields are not supported.

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Offset: 0x0058			Register Name: HCCONFIG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	U3E U3 Entry Enable When set to '1', the xHC shall assert the *PLC* flag ('1') when a Root Hub port transitions to the U3 State.
7:0	R/W	0x00	MaxSlotsEn Max Device Slots Enabled This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running (Run/Stop (R/S) = '1').

8.12.5.18 0x0420 xHC Port1 Status and Control Register (USB2 Protocol) (Default Value:0x0000_02A0)

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WPR Warm Port Reset When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be reserved.
30	R	0x0	DR Device Removable This flag indicates if this port has a removable device attached. 0: Device is removable 1: Device is non-removable
29:28	/	/	/

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	WOE Wake on Over-Current Enable Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events.
26	R/W	0x0	WDE Wake on Disconnect Enable Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events.
25	R/W	0x0	WCE Wake on Connect Enable Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events.
24	R	0x0	CAS Cold Attach Status This bit is set when Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable advance to the Enabled state. Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to '1'. This flag is '0' if PP is '0' or for USB2 protocol ports.
23	R/W1C	0x0	CEC Port Config Error Change This flag indicates that the port failed to configure its link partner. 0: No Change 1: Port Config Error Detected Software shall clear this bit by writing a '1' to it.

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
22	R/W1C	0x0	PLC Port Link State Change This flag is set to ‘1’ due to the following PLS transitions: Note that this flag shall not be set if the PLS transition was due to software setting PP to ‘0’. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it.

Transition	Condition
U3 -> Resume	Wakeup signaling from a device
Resume -> Recovery -> U0	Device Resume complete (USB3 protocol ports only)
Resume -> U0	Device Resume complete (USB2 protocol ports only)
U3 -> Recovery -> U0	Software Resume complete (USB3 protocol ports only)
U3 -> U0	Software Resume complete (USB2 protocol ports only)
U2 -> U0	L1 Resume complete (USB2 protocol ports only)
U0 -> U0	L1 Entry Reject (USB2 protocol ports only)
Any state -> Inactive	Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM.
Any State -> U3	U3 Entry complete. Note: *PLC* is asserted only if *U3E* = ‘1’

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	PRC Port Reset Change This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it.
20	R/W1C	0x0	OCC Over-Current Change This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-Current Active (OCA). Software shall clear this bit by writing a '1' to it.
19	R/W1C	0x0	WRC Warm Port Reset Change This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be Reserved.
18	R/W1C	0x0	PEC Port Enabled/Disabled Change '1' = change in *PED*. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. For a USB2 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point For a USB3 protocol port, this bit shall never be set to '1'.

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	CSC Connect Status Change '1' = Change in *CCS*. '0' = No change. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it.
16	R/W	0x0	LWS Port Link State Write Strobe When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14	R/W	0x0	PIC Port Indicator Control Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: 0: Port indicators are off 1: Amber 2: Green 3: Undefined This field is '0' if PP is '0'.

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
13:10	R	0x0	PSPD Port Speed This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate *Undefined Speed*. 0: Undefined Speed 1-15: Protocol Speed ID (PSI) 1: Full-speed 12 MB/s 2: Low-speed 1.5 Mb/s 3: High-speed 480 Mb/s 4: SuperSpeed 5 Gb/s. **Note: This field is invalid on a USB2 protocol port until after the port is reset.**

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
9	R/W	0x1	PP Port Power This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. 0: This port is in the Powered-off state. 1: This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' =on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port).

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8:5	R/W	0x5	PLS Port Link State Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write value and Description: 0: The link shall transition to a U0 state from any of the U states. 2: USB2 protocol ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 10: USB3 protocol ports only. Shall enable a link transition to the Compliance state, i.e. *CTE* = '1'. 1, 4, 6-9,11-14: Ignored. 15: USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit sub-state, else ignored. **Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field.** **For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall de-assert L1 signaling on the USB. Writing a**

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			value of '1' shall have no effect. The U1 state shall never be reported by a USB2 protocol port. Read value and Meaning: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect Stated 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12-14: Reserved 15: Link is in the Resume State This field is undefined if PP = '0'. **Note: Transitions between different states are not reflected until the transition is complete.**
4	R/W1S	0x0	PR Port Reset '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to this flag to transition a USB2 port from the Polling state to the Enabled state. This flag is '0' if PP is '0'.

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
3	R	0x0	OCA Over-Current Active '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
2	/	/	/

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
1	R/W1CS	0x0	PED Port Enabled/Disabled Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bit. This flag is '0' if PP is '0'.

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Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CCS Current Connect Status '1' = A device is connected to the port. '0' = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to '1'. This flag is '0' if PP is '0'.

8.12.5.19 0x0424 xHC Port1 PM Status and Control Register (USB2 Protocol) (Default Value:0x0000_0000)

Offset: 0x0424			Register Name: HCPORT1PMSC
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	PTC Port Test Control (Test Mode) When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB2 protocol port are: Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes.
27:17	/	/	/

Value	Test Mode
0x0	Test mode not enabled
0x1	Test J_STATE
0x2	Test K_STATE
0x3	Test SE0_NAK
0x4	Test Packet
0x5	Test FORCE_ENABLE
0x6-0xE	Reserved
0xF	Port Test Control Error

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Offset: 0x0424			Register Name: HCPORT1PMSC
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	HLE Hardware LPM Enable If this bit is set to '1', then hardware controlled LPM shall be enabled for this port. **Note: If the USB2 Hardware LMP Capability is not supported (HLC = '0') this field shall be Reserved.**
15:8	R/W	0x0	L1DS L1 Device Slot System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of '0' indicates no device is present. The xHC uses this field to lookup information necessary to generate the LMP Token packet.
7:4	R/W	0x0	BESL Best Effort Service Latency System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1.
3	R/W	0x0	RWE Remote Wake Enable System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.

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Offset: 0x0424			Register Name: HCPORT1PMSC
Bit	Read/Write	Default/Hex	Description
2:0	R	0x0	L1S L1 Status This field is used by software to determine whether an L1-based suspend request (LMP transition) was successful, specifically: Value – Meaning 0x0 – Invalid – This field shall be ignored by software. 0x1 – Success – Port successfully transitioned to L1 (ACK) 0x2 – Not Yet – Device is unable to enter L1 at this time (NYET) 0x3 – Not Supported – Device does not support L1 transitions (STALL) 0x4 – Timeout/Error – Device 0x5-0x7 – Reserved The value of this field is only valid when the port resides in the L0 or L1 state (PLS = '0' or '2').

8.12.5.20 0x0428 xHC Port1 Link Info Register (USB2 Protocol) (Default Value:0x0000_0000)

Offset: 0x0428			Register Name: HCPORT1LI
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.12.5.21 0x0430 xHC Port2 Status and Control Register (USB3 Protocol) (Default Value:0x000002A0)

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WPR Warm Port Reset When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be reserved.

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
30	R	0x0	DR Device Removable This flag indicates if this port has a removable device attached. 0: Device is removable 1: Device is non-removable
29:28	/	/	/
27	R/W	0x0	WOE Wake on Over-Current Enable Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events.
26	R/W	0x0	WDE Wake on Disconnect Enable Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events.
25	R/W	0x0	WCE Wake on Connect Enable Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events.
24	R	0x0	CAS Cold Attach Status This bit is set when Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable advance to the Enabled state. Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to '1'. This flag is '0' if PP is '0' or for USB2 protocol ports.
23	R/W	0x0	CEC Port Config Error Change This flag indicates that the port failed to configure its link partner. 0: No Change 1: Port Config Error Detected Software shall clear this bit by writing a '1' to it.

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
22	R/W	0x0	PLC Port Link State Change This flag is set to '1' due to the following PLS transitions: Note that this flag shall not be set if the PLS transition was due to software setting PP to '0'.

Transition	Condition
U3 -> Resume	Wakeup signaling from a device
Resume -> Recovery -> U0	Device Resume complete (USB3 protocol ports only)
Resume -> U0	Device Resume complete (USB2 protocol ports only)
U3 -> Recovery -> U0	Software Resume complete (USB3 protocol ports only)
U3 -> U0	Software Resume complete (USB2 protocol ports only)
U2 -> U0	L1 Resume complete (USB2 protocol ports only)
U0 -> U0	L1 Entry Reject (USB2 protocol ports only)
Any state -> Inactive	Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM.
Any State -> U3	U3 Entry complete. Note: *PLC* is asserted only if *U3E* = '1'

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	PRC Port Reset Change This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it.
20	R/W1C	0x0	OCC Over-Current Change This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it.
19	R/W1C	0x0	WRC Warm Port Reset Change This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be Reserved.
18	R/W1C	0x0	PEC Port Enabled/Disabled Change Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. For a USB2 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point For a USB3 protocol port, this bit shall never be set to '1'.

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	CSC Connect Status Change This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it.
16	R/W	0x0	LWS Port Link State Write Strobe When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14	R/W	0x0	PIC Port Indicator Control Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: 0: Port indicators are off 1: Amber 2: Green 3: Undefined This field is '0' if PP is '0'.

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
13:10	R	0x0	PSPD Port Speed This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate *Undefined Speed*. 0: Undefined Speed 1-15: Protocol Speed ID (PSI) 1: Full-speed 12 MB/s 2: Low-speed 1.5 Mb/s 3: High-speed 480 Mb/s 4: SuperSpeed 5 Gb/s. **Note: This field is invalid on a USB2 protocol port until after the port is reset.**

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
9	R/W	0x1	PP Port Power This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. 0: This port is in the Powered-off state. 1: This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' =on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port).

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8:5	R/W	0x5	PLS Port Link State Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write value and Description: 0: The link shall transition to a U0 state from any of the U states. 2: USB2 protocol ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 10: USB3 protocol ports only. Shall enable a link transition to the Compliance state, i.e. *CTE* = '1'. 1, 4, 6-9,11-14: Ignored. 15: USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit sub-state, else ignored. **Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field.** **For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall de-assert L1 signaling on the USB. Writing a**

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			value of '1' shall have no effect. The U1 state shall never be reported by a USB2 protocol port. Read value and Meaning: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect Stated 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12-14: Reserved 15: Link is in the Resume State This field is undefined if PP = '0'. **Note: Transitions between different states are not reflected until the transition is complete.**
4	R/W	0x0	PR Port Reset 1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to this flag to transition a USB2 port from the Polling state to the Enabled state. This flag is '0' if PP is '0'.

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
3	R	0x0	OCA Over-Current Active '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
2	/	/	/

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PED Port Enabled/Disabled 1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bit. This flag is '0' if PP is '0'.

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Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CCS Current Connect Status '1' = A device is connected to the port. '0' = A device is not connected This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to '1'. This flag is '0' if PP is '0'.

8.12.5.22 0x0434 xHC Port2 PM Status and Control Register (USB3 Protocol) (Default Value:0x0000_0000)

Offset: 0x0434			Register Name: HCPORT2PMSC
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	FLA Force Link PM Accept When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted. When this bit is cleared to '0', the port shall generate a *Set Link Function* LMP with the Force_LinkPM_Accept bit de-asserted This flag shall be set to '0' by the assertion of PR to '1' or when CCS = transitions from '0' to '1'. Writes to this flag have no effect if PP = '0'. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from '0' to '1'. Refer to Sections 8.4.1, 10.4.2.2 and 10.4.2.9 of the USB3 specification for more details. Improper use of the SS Force_LinkPM_Accept functionality can impact the performance of the link significantly. This bit shall only be used for compliance and testing purposes. Software shall ensure that there are no pending packets at the link level before setting this bit. This flag is '0' if PP is '0'.

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Offset: 0x0434			Register Name: HCPORT2PMSC
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0x00	U2TO U2 Timeout Timeout value for U2 inactivity timer. If equal to 0xFF, the port is disabled from initiating U2 entry. This field shall be set to '0' by the assertion of PR to '1'. The following are permissible values: 0x00: Zero 0x01: 256 us 0x02: 512 us ... 0xFE: 65.024 ms 0xFF: Infinite A U2 Inactivity Timeout LMP shall be sent by the xHC to the device connected on this port when this field is written. Refer to Sections 8.4.3 and 10.4.2.10 of the USB3 specification for more details.
7:0	R/W	0x00	U1TO U1 Timeout Timeout value for U1 inactivity timer. If equal to 0xFF, the port is disabled from initiating U1 entry, this field shall be set to '0' by the assertion of PR to '1'. The following are permissible values: 0x00: Zero 0x01: 1 us 0x02: 1 us ... 0x7F: 127us 0x80-0xFE: Reserved 0xFF: Infinite

8.12.5.23 0x0438 xHC Port2 Link Info Register (USB3 Protocol) (Default Value:0x0000_0000)

Offset: 0x0438			Register Name: HCPORT2LI
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0438			Register Name: HCPORT2LI
Bit	Read/Write	Default/Hex	Description
23:20	R	0x0	RLC Rx Lane Count This field that identifies the number of Receive Lanes negotiated by the port. This is a "zero-based" value, where 0 to 15 represents Lane Counts of 1 to 16, respectively. This value is valid only when *CCS*= '1'. *RLC* shall equal '0' for a simplex Sublink.
19:16	R	0x0	TLC Tx Lane Count This field that identifies the number of Transmit Lanes negotiated by the port. This is a "zero-based" value, where 0 to 15 represents Lane Counts of 1 to 16, respectively. This value is valid only when *CCS*= '1'. *TLC* shall equal '0' for a simplex Sublink.
15:0	R	0x0000	LEC Link Error Count This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from '1' to '0', or when CCS = transitions from '0' to '1'.

8.12.5.24 0x1000 xHC Microframe Index Register (Default Value:0x0000_0000)

Offset: 0x1000			Register Name: HCMFINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R	0x0000	MFI Micro-Frame Index The value in this register increments at the end of each micro-frame (e.g. 125us). Bits [13:3] may be used to determine the current 1ms. Frame index.

8.12.5.25 0x1020 xHC Interrupt 0 Management Register (Default Value:0x0000_0000)

Offset: 0x1020			Register Name: HCIMAN0
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/

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Offset: 0x1020			Register Name: HCIMAN0
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	IE Interrupt Enable This flag specifies whether the interrupter is capable of generating an interrupt. When this bit and the IP bit are set, the interrupter shall generate an interrupt when the interrupter Moderation Counter reaches '0'. If this bit is '0', then the interrupter is prohibited from generation interrupts.
0	R/W1C	0x0	IP Interrupt Pending This flag represents the current state of the interrupter. If IP = '1', an interrupt is pending for this interrupter. A '0' value indicates that no interrupt is pending for interrupter. This bit can be cleared by software writing '1'.

8.12.5.26 0x1024 xHC Interrupt 0 Moderation Register (Default Value:0x0000_0FA0)

Offset: 0x1024			Register Name: HCIMOD0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	IMODC Interrupt Moderation Counter Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate.
15:0	R/W	0x0FA0	IMODI Interrupt Moderation Interval Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The default value is 4000 (1ms).

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8.12.5.27 0x1028 xHC Interrupt 0 Event Ring Segment Table Size Register (Default Value:0x0000_0000)

Offset: 0x1028			Register Name: HCERSTSZ0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	ERSTSZ Event Ring Segment Table Size This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of '0' to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of '0' to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

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8.12.5.28 0x1030 xHC Interrupt 0 Event Ring Segment Table Base Address Low Register (Default 0x1030 Value:0x0000_0000)

Offset: 0x1030			Register Name: HCERSTBAL0
Bit	Read/Write	Default/Hex	Description
31:6	R/W	0x0000	ERSTBAL Event Ring Segment Table Base Address Low This field defines the low order bits [31:6] of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. For Secondary Interrupters: This field may be modified at any time. For the Primary Interrupter: This field shall not be modified if *HCHalted* (HCH) = '0'. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
5:0	/	/	/

8.12.5.29 0x1034 xHC Interrupt 0 Event Ring Segment Table Base Address High Register (Default 0x1034 Value:0x0000_0000)

Offset: 0x1034			Register Name: HCERSTBAH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0000	ERSTBAH Event Ring Segment Table Base Address High This field defines the high order bits [63:32] of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine: EREP Advancement to the Start State. For Secondary Interrupters: This field may be modified at any time. For the Primary Interrupter: This field shall not be modified if *HCHalted* (HCH) = '0'. This field shall not be modified if HCHalted(HCH) = '0'.

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8.12.5.30 0x1038 xHC Interrupt 0 Event Ring Dequeue Poiter Low Register (Default Value:0x0000_0000)

Offset: 0x1038			Register Name: HCERDPL0
Bit	Read/Write	Default/Hex	Description
31:4	R/W	0x0000	ERDPL Event Ring Dequeue Pointer Low This field defines the low order bits [31:4] of the start address of the current Event Ring Dequeue Pointer. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
3	R/W1C	0x0	EHB Event Handler Busy This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	R/W	0x0	DESI Dequeue ERST Segment Index This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

8.12.5.31 0x103C xHC Interrupt 0 Event Ring Dequeue Pointer High Register (Default Value:0x0000_0000)

Offset: 0x103C			Register Name: HCERDPH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0000	ERDPH Event Ring Dequeue Pointer High This field defines the high order bits [63:32] of the start address of the current Event Ring Dequeue Pointer.

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8.12.5.32 0x2000 + 4*n (N = 0-64) xHC Doorbell Register N (n=0, 1, 萃萃, 64) (Default Value:0x0000_0000)

Offset: 0x2000 + 4*n (N = 0-64)			Register Name: HCDBRn (N = 0-64)
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	DBSID Doorbell Stream ID If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams > 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Command Doorbells. This field returns '0' when read.
15:8	/	/	/

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Offset: 0x2000 + 4*n (N = 0-64)			Register Name: HCDBRn (N = 0-64)
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x00	DBT Doorbell Target This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (n = 1-64) 0: Reserved 1: Control EP0 Enqueue Pointer Update 2: EP 1 OUT Enqueue Pointer Update 3: EP 1 IN Enqueue Pointer Update 4: EP 2 OUT Enqueue Pointer Update 5: EP 2 IN Enqueue Pointer Update ... 30: EP 15 OUT Enqueue Pointer Update 31: EP 15 IN Enqueue Pointer Update 32-247: Reserved 248-255: Vendor Defined Host Controller Doorbell (n = 0) 0: Command Doorbell 1-247: Reserved 248-255: Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to '0'.

8.12.5.33 0x0440 xHC USB Legacy Support Capability Register (Default Value:0x0000_0401)

Offset: 0x0440			Register Name: HCUSBLEGSUP
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

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Offset: 0x0440			Register Name: HCUSBLEGSUP
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	OOS HC OS Owned Semaphore System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'.
23:17	/	/	/
16	R/W	0x0	BOS HC BIOS Owned Semaphore The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
15:8	R	0x04	NCP Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability..
7:0	R	0x01	CID Capability ID This field identifies the xHCI Extended capability. Refer to xHCI Spec for a list of the valid xHCI extended capabilities. This extended capability requires one additional 32-bit register for control/status information (HCIUSBLEGCTLSTS), and this register is located at offset xECP+0x04.

8.12.5.34 0x0444 xHC USB Legacy Support Control/Status Register (Default Value:0x0000_0000)

Offset: 0x0444			Register Name: HCUSBLEGCTRLSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	SBAR SMI on BAR This bit is set to '1' whenever the Base Address Register (BAR) is written. This bit can be cleared by software writing '1'.

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Offset: 0x0444			Register Name: HCUSBLEGCTRLSTS
Bit	Read/Write	Default/Hex	Description
30	R/W1C	0x0	SPC SMI on PCI Command This bit is set to '1' whenever the PCI Command Register is written. This bit can be cleared by software writing '1'.
29	R/W1C	0x0	SOOC SMI on OS Ownership Change This bit is set to '1' whenever the HC OS Owned Semaphore bit in HCUSBLEGSUP register transitions from '1' to '0' or '0' to '1'. This bit can be cleared by software writing '1'.
28:21	/	/	/
20	R	0x0	SHSE SMI on Host System Error Shadow bit of Host System Error (HSE) bit in the HCUSBSTS register. To clear this bit to a '0', system software shall write a '1' to the Host System Error (HSE) bit in the HCUSBSTS register.
19:17	/	/	/
16	R	0x0	SEI SMI on Event Interrupt Shadow bit of Event Interrupt (EINT) bit in the HCUSBSTS register. This bit follows the state the Event Interrupt (EINT) bit in the HCUSBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set.
15	R/W	0x0	SBE SMI on BAR Enable When this bit is a '1' AND SMI on BAR is '1', then the host controller will issue an SMI.
14	R/W	0x0	SPCE SMI on PCI Command Enable When this bit is a '1' AND SMI on PCI Command is '1', then the host controller will issue an SMI.
13	R/W	0x0	SOOE SMI on OS Ownership Enable When this bit is a '1' AND the OS Ownership Change bit is '1', the host controller will issue an SMI.
12:5	/	/	/

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Offset: 0x0444			Register Name: HCUSBLEGCTRLSTS
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	SHSEE SMI on Host System Error Enable When this bit is a '1', and the SMI on Host System Error bit in this register is a '1', the host controller will issue an SMI immediately.
3:1	/	/	/
0	R/W	0x0	USE USB SMI Enable When this bit is a '1', and the SMI on Event Interrupt bit in this register is a '1', the host controller will issue an SMI immediately.

8.12.5.35 0x0490 xHC Support Protocol Capability 1 Revision Register (Default Value:0x0200_0402)

Offset: 0x0490			Register Name: HCSPC1REV
Bit	Read/Write	Default/Hex	Description
31:24	R	0x02	MajorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	R	0x00	MinorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	R	0x04	NCP Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability..
7:0	R	0x02	CID Capability ID This field identifies the xHCI Extended capability. Refer to xHCI Spec for a list of the valid xHCI extended capabilities.

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8.12.5.36 0x0494 xHC Support Protocol Capability 1 String Register (Default Value:0x2042_5355)

Offset: 0x0494			Register Name: HCSPC1STR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x20425355	NAME Name String This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined.

8.12.5.37 0x0498 xHC Support Protocol Capability 1 Port Register (Default Value:0x0001_0101)

Offset: 0x0498			Register Name: HCSPC1PRT
Bit	Read/Write	Default/Hex	Description
31:28	R	0x0	PSIC Protocol Speed ID Count This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains.
27:16	R	0x001	PD Protocol Defined This field is reserved for protocol specific definitions.
15:8	R	0x01	CPCNT Compatible Port Count This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are '1' to MaxPorts.
7:0	R	0x01	CPOFF Compatible Port Offset This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

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8.12.5.38 0x04A0 xHC Support Protocol Capability 2 Revision Register (Default Value:0x0300_0002)

Offset: 0x04A0			Register Name: HCSPC2REV
Bit	Read/Write	Default/Hex	Description
31:24	R	0x03	MajorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	R	0x00	MinorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	R	0x00	NCP Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability..
7:0	R	0x02	CID Capability ID This field identifies the xHCI Extended capability. Refer to xHCI Spec for a list of the valid xHCI extended capabilities.

8.12.5.39 0x04A4 xHC Support Protocol Capability 2 String Register (Default Value:0x2042_5355)

Offset: 0x04A4			Register Name: HCSPC2STR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x20425355	NAME Name String This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined.

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8.12.5.40 0x04A8 xHC Support Protocol Capability 2 Port Register (Default Value:0x0000_0102)

Offset: 0x04A8			Register Name: HCSPC2PRT
Bit	Read/Write	Default/Hex	Description
31:28	R	0x0	PSIC Protocol Speed ID Count This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains.
27:16	R	0x000	PD Protocol Defined This field is reserved for protocol specific definitions.
15:8	R	0x01	CPCNT Compatible Port Count This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are '1' to MaxPorts.
7:0	R	0x02	CPOFF Compatible Port Offset This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

8.12.6 Global Register Description

8.12.6.1 0xC100 Global Soc Bus Configuration Register 0 (Default Value:0x0000_0001)

Offset: 0xC100			Register Name: GSBUSCFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0	DatRdReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Data Read. Input to BUS-GM.
27:24	R/W	0	DesRdReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Read. Input to BUS-GM.
23:20	R/W	0	DatWrReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Data Write. Input to BUS-GM.

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Offset: 0xC100			Register Name: GSBUSCFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0	DesWrReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Write. Input to BUS-GM.
15:12	/	/	/
11	R/W	0	DatBigEnd Data Access is Big Endian This bit controls the endian mode for data accesses. 0: Little-endian (default) 1: Big-endian this bit must be set to zero.
10	R/W	0	DescBigend Descriptor Access is Big-Endian This bit controls the endian mode for descriptor accesses. 0: Little-endian (default) 1: Big-endian this bit must be set to zero.
9:8	/	/	/
7	R/W	0	INCR256BrstEna INCR256 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 256-beat burst.Input to BUS-GM.
6	R/W	0	INCR128BrstEna INCR128 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 128-beat burst.Input to BUS-GM.
5	R/W	0	INCR64BrstEna INCR64 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 64-beat burst.Input to BUS-GM.
4	R/W	0	INCR32BrstEna INCR32 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 32-beat burst.Input to BUS-GM.

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Offset: 0xC100			Register Name: GSBUSCFG0
Bit	Read/Write	Default/Hex	Description
3	R/W	0	INCR16BrstEna INCR16 Burst Type Enable For the AHB/AXI configuration, if software set this bit to "1", the AHB/AXI master uses INCR to do the 16-beat burst.Input to BUS-GM.
2	R/W	0	INCR8BrstEna INCR8 Burst Type Enable For the AHB/AXI configuration, if software set this bit to "1", the AHB/AXI master uses INCR to do the 8-beat burst.Input to BUS-GM.
1	R/W	0	INCR4BrstEna INCR4 Burst Type Enable For the AXI configuration, when this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers. Input to BUS-GM.
0	R/W	1	INCRBrstEna Undefined Length INCR Burst Type Enable When enabled, this has higher priority than other burst types. For the AHB/AXI configuration. if this bit is set to “1”, AHB/AXI master tries to do only one INCR burst for each transfer unless it has to break it at a page boundary. If this bit is set to “0”, the AHB/AXI master may still use INCR burst type at the beginning and end bursts of transfers to align the address. The middle bursts are INCR4/8/16, depending when the type is enabled. Input to BUS-GM

8.12.6.2 0xC104 Global Soc Bus Configuration Register 1 (Default Value:0x0000_6F00)

Offset: 0xC104			Register Name: GSBUSCFG1
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0xC104			Register Name: GSBUSCFG1
Bit	Read/Write	Default/Hex	Description
16:13	R/W	0x3	ExtdPipeTransLimit AXI Pipelined Transfers Extended Burst Request Limit The {ExtdPipeTransLimit, PipeTransLimit} fields controls the number of outstanding extended pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 'h0: 1 request 'h1: 2 requests 'h2: 3 requests 'h3: 4 requests and, so on
12	R/W	0	EN1KPAGE 1k Page Boundary Enable By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	R/W	0xf	PipeTransLimit AXI Burst Request Limit The {ExtdPipeTransLimit, PipeTransLimit} fields controls the number of outstanding extended pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 'h0: 1 request 'h1: 2 requests 'h2: 3 requests 'h3: 4 requests and, so on
7:0	/	/	/

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8.12.6.3 0xC108 Global TX Threshold Control Register (Default Value:0x00F0_0000)

Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	UsbTxPktCntSel USB Async ESS Transmit Packet Threshold Enable - Host/Device Modes This field enables/disables the USB transmission multi-packet thresholding for Async endpoints: 0: USB transmission multi-packet thresholding is disabled; the controller starts transmission on the USB as soon as one packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The controller can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is valid in both host and device mode. It is only used for Enhanced SuperSpeed. In device mode, the controller can send ERDY on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO of a Bulk IN endpoint

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Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
25:21	R/W	0x7	USBTxPktCnt USB Async ESS Transmit Packet Threshold Count - Host/Device Modes This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction (burst) for Async endpoints. This field is only valid when the USB Async ESS Transmit Packet Threshold Enable field is set to one. For device mode, this field specifies the number of packets that must be in the TXFIFO before the controller can start transmission of ERDY for the corresponding USB transaction (burst) of Bulk IN endpoint. Valid values for this field is 1 to 16. Note: In host mode, this field must be less than or equal to the USB Maximum TX Burst Size field. In device mode, this field must be less than or equal to the USB endpoint maximum Burst Size amongst all endpoints.
20:16	R/W	0x10	USBMaxTxBurstSize USB Async ESS Maximum TX Burst Size - Host Mode Only When USBTxPktCntSel is 1, this field specifies the Maximum ESS Bulk OUT burst that the controller can execute. When the system bus is slower than the USB, TXFIFO can underrun during a long burst. You can program a smaller value to this field to limit the TX burst size that the controller can execute. It only applies to ESS Bulk OUT endpoints in the host mode. Valid values are from 1 to 16. Note: This field can only be set to 2, 4, 8 or 16.

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Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	UsbTxThrNumPktSel_HS_Prd USB HS High Bandwidth Periodic Transmit Packet Threshold Enable - Host Mode Only This field enables/disables the USB HS High Bandwidth Periodic transmission multi-packet thresholding> 0: USB HS High Bandwidth Periodic transmission multi-packet thresholding is disabled; the controller can start transmission on the USB as soon as one packet has been fetched into the corresponding TXFIFO. 1: USB HS High Bandwidth Periodic transmission multi-packet thresholding is enabled. The controller can start transmission on the USB only after USB HS High Bandwidth Periodic Transmit Packet Threshold Count number of packets for the Periodic High Bandwidth USB transaction is already in the corresponding TXFIFO. This mode is valid in host mode for high speed high bandwidth periodic endpoints
14:13	R/W	0x0	UsbTxThrNumPkt_HS_Prd USB HS High Bandwidth Periodic Transmit Packet Threshold Count - Host Mode Only This field specifies the number of packets that must be available in the TXFIFO before the controller can start transmission for the Periodic High Bandwidth USB transaction. This field is only valid when the USB HS High Bandwidth Periodic Transmit Packet Threshold Enable field is set to one. Valid values are from 1 to 3.
12:11	/	/	/

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Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	UsbTxThrNumPktSel_Prd USB Periodic ESS Transmit Packet Threshold Enable - Host Mode Only This field enables/disables the USB Periodic transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled; the controller starts transmission on the USB as soon as one packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The controller can start transmission on the USB only after USB Periodic ESS Transmit Packet Threshold Count amount of packets for the USB transaction (burst) has been fetched into the corresponding TXFIFO. It is used only for ESS.
9:5	R/W	0x0	UsbTxThrNumPkt_Prd USB Periodic ESS Transmit Packet Threshold Count - Host Mode Only This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction (burst). This field is valid only when the USB Periodic ESS Transmit Packet Threshold Enable field (UsbTxThrNumPktSel_Prd) is set to one. Valid values are from 1 to 16. Note: This field must be less than or equal to the USB Maximum Periodic TX Burst Size field.
4:0	R/W	0x0	UsbMaxTxBurstSize_Prd USB Maximum Periodic ESS TX Burst Size - Host Mode Only When UsbTxThrNumPktSel_Prd is 1, this field specifies the Maximum Periodic OUT burst the controller can execute. When the system bus is slower than the USB, TXFIFO can underrun during a long burst. Note: This field can only be set to 2, 4, 8 or 16.

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8.12.6.4 0xC10C Global RX Threshold Control Register (Default Value:0x00F0_0000)

Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0	USBRxPktCntSel USB Async ESS Receive Packet Threshold Enable - Host/Device Modes This field enables/disables the USB reception multi-packet thresholding: 0: The controller can only start reception on the USB when the RXFIFO has space for at least one packet. 1: The controller can only start reception on the USB when the RXFIFO has space for at least USBRxPktCnt amount of packets. This mode is valid in both host and device mode. It is only used for Enhanced SuperSpeed. In device mode, Setting this bit to 1 also enables the functionality of reporting NUMP in the ACK/ERDY TP based on the RXFIFO space instead of reporting a fixed NUMP derived from DCFG.NUMP for Bulk OUT endpoints. If you are using external buffer control (EBC) feature, disable this mode by setting USBRxPktCntSel to 0.
25:21	R/W	0x7	UsbRxPktCnt USB Async ESS Receive Packet Threshold Count - Host/Device Modes In host mode, this field specifies the space (in terms of the number of packets) that must be available in the RXFIFO before the controller can start the corresponding USB RX transaction (burst). In device mode, this field specifies the space (in terms of the number of packets) that must be available in the RXFIFO before the controller can send ERDY for a flow-controlled Bulk OUT endpoints. This field is valid only when the USB Async ESS Receive Packet Threshold Enable field is set to 1. The valid values for this field are from 1 to 16. Note: This field must be less than or equal to the USB Maximum Receive Burst Size field.

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Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
20:16	R/W	0x10	UsbMaxRxBurstSize USB Async ESS Maximum Receive Burst Size - Host/Device Modes In host mode, this field specifies the Maximum Bulk IN burst the DWC_usb31 controller can perform. When the system bus is slower than the USB, RXFIFO can overrun during a long burst. You can program a smaller value to this field to limit the RX burst size that the controller can perform. It only applies to ESS Bulk endpoints in the host mode. In device mode, this field specifies the NUMP value that is sent in ERDY for a Bulk OUT endpoint. The programmed value should not exceed the RxFIFO size. This field is valid only when USBRxPktCntSel is 1. The valid values for this field are from 1 to 16.
15	R/W	0	UsbRxThrNumPktSel_HS_Prd USB HS High Bandwidth Periodic Receive Packet Threshold Enable - Host Mode Only This field enables/disables the USB reception multi-packet thresholding: 0: USB HS High Bandwidth Periodic Receive multi-packet thresholding is disabled; The controller can start reception on the USB as soon as the RXFIFO has space for one packet. 1: USB HS High Bandwidth Periodic Receive multi-packet thresholding is enabled; the controller can only start reception on the USB when the RXFIFO has space for at least UsbRxThrNumPkt_HS_Prd amount of packets. This mode is valid in host mode for high speed high bandwidth periodic endpoints. In device mode, this field specifies the NUMP value that will be sent in ERDY for an OUT endpoint. This field is valid only when USBRxPktCntSel is one. The valid values for this field are from 1 to 16.

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Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
14:13	R/W	0x0	UsbRxThrNumPkt_HS_Prd USB HS High Bandwidth Periodic Receive Packet Threshold Count - Host Mode Only This field specifies the maximum number of packet space needed in the RXFIFO before the controller can start a HS Periodic High Bandwidth USB transaction. This field is valid only when USBRxPktCntSel_HS_Prd is 1. The valid values for this field are from 1 to 3.
12:11	/	/	/
10	R/W	0x0	UsbRxThrNumPktSel_Prd USB Periodic ESS Receive Packet Threshold Enable - Host Mode Only. This field should be programmed to 0 in Device mode. This field enables/disables the Periodic ESS USB reception multi-packet thresholding: 0: USB Periodic ESS Receive multi-packet thresholding is disabled; the controller can start reception on the USB as soon as the RXFIFO has space for one packet. 1: USB Periodic ESS Receive multi-packet thresholding is enabled; the controller can only start reception on the USB when the RXFIFO has space for at least UsbRxThrNumPkt_Prd amount of packets. This mode is valid only in host mode. It is only used for ESS.

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Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
9:5	R/W	0x0	UsbRxThrNumPkt_Prd USB Periodic ESS Receive Packet Threshold Count - Host Mode Only. This field should be programmed to 0 in Device mode. This field specifies the minimum number of packet space needed in the RXFIFO before the controller can start a ESS periodic high-bandwidth USB transaction. This field is valid only when the USB Periodic ESS Receive Packet Threshold Enable field is set to 1. Valid values are from 1 to 16. Note: This field must be less than or equal to the USB Maximum Periodic RX Burst Size field.
4:0	R/W	0x0	UsbMaxRxBurstSize_Prd USB Maximum Periodic ESS RX Burst Size - Host Mode Only. This field should be programmed to 0 in Device mode. When UsbRxThrNumPktSel_Prd is 1, this field specifies the Maximum ESS Periodic IN burst the controller can execute. When the system bus is slower than the USB, RXFIFO can overrun during a long burst.

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8.12.6.5 0xC110 Global Core Control Register (Default Value:0x30C1_2004)

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
31:19	R/W	0x618	PwrDnScale Power Down Scale The USB3 suspend_clk input replaces pipe3_rx_pclk as a clock source to a small part of the USB3 core that operates when the SS PHY is in its lowest power (P3) state, and therefore does not provide a clock. The Power Down Scale field specifies how many suspend_clk periods fit into a 16 kHz clock period. When performing the division, truncate the remainders instead of rounding up. For example, when using an 8-bit/16-bit/32-bit PHY and 25-MHz Suspend clock, Power Down Scale = 25000 kHz/16 kHz = 13'd1562. Note: Minimum Suspend clock frequency is 32 kHz Maximum Suspend clock frequency is 125 MHz The LTSSM uses Suspend clock for 12-ms and 100-ms timers during suspend mode. According to the USB 3.1 specification, the accuracy on these timers is 0% to +50%. 12 ms + 0-+50% accuracy = 18 ms (Range is 12 ms - 18 ms) 100 ms + 0-+50% accuracy = 150 ms (Range is 100 ms - 150 ms). The suspend clock accuracy requirement is: (12,000/62.5) * (GCTL[31:19]) * actual suspend_clk_period should be between 12,000 and 18,000 (100,0000/62.5) * (GCTL[31:19]) * actual suspend_clk_period should be between 100,000 and 150,000 For example, if your suspend_clk frequency varies from 7.5 MHz to 10.5MHz, then the value needs to programmed is: Power Down Scale = 10500/16 = 657 (rounded up; and fastest frequency used)

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Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	MASTERFILTBYPASS Master Filter Bypass When this bit is set to 1'b1, irrespective of the parameter USB3_EN_BUS_FILTERS chosen, all the filters in the usb3_filter module will be bypassed. The double synchronizers to mac_clk preceding the filters will also be bypassed. For enabling the filters, this bit should be 1'b0.
17	R/W	0x0	BYPSSETADDR Bypass SetAddress in Device Mode When BYPSSETADDR bit is set, the device core uses the value in DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, this feature can be used to avoid sending an actual SET ADDRESS control transfer on the USB to make the device core respond to a new address. Note: This bit must be set for simulation purposes only. In the real hardware, this bit must be set to 1'b0.
16	R/W	0x1	U2RSTECN If the super speed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode.
15:14	R/W	0x0	FRMSCLDWN This field scales down device view of a SOF/USOF/ITP duration. For SS/HS mode: Value of 2'h3 implements interval to be 15.625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be125us For FS mode, the scale-down value is multiplied by 8.

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Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x02	PrtCapDir Port Capability Direction • 2'b01: for Host configurations • 2'b10: for Device configurations • 2'b00, 2'b11: not support **Note: For static Host-only or Device-only applications, use DRD Host or DRD Device mode.**
11	R/W	0x0	CoreSoftReset Core Soft Reset 1'b0 - No soft reset 1'b1 - Soft reset to core Clears the interrupts and all the CSRs except the following registers: - GCTL - GUCTL - GSTS - GGPIO - GUID - GUSB2PHYCFGn registers - GUSB3PIPECTLn registers - DCFG - DCTL - DEVTEN - DSTS When you reset PHYs (using GUBS3PHYCFG or GUSB3PIPECTL registers), you must keep the core in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets.
10	/	/	/
9	R/W	0x0	U1U2TimerScale Disable U1/U2 timer Scaledown If set to '1' along with GCTL[5:4] (ScaleDown) = 2'bX1 disables the scale down of U1/U2 inactive timer values. This is for simulation mode only.

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Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	DebugAttach Debug Attach When this bit is set: • SS Link proceeds directly to the Polling link state (after RUN/STOP in the DCTL register is asserted) without checking remote termination. • Link LFPS polling timeout is infinite • Polling timeout during TS1 is infinite (in case link is waiting for TXEQ to finish).

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Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	RAMClkSel RAM Clock Select 2'b00: bus clock 2'b01: pipe clock 2'b10: In device mode, pipe/2 clock. 2'b11: In device mode, selects mac2_clk as ram_clk when 8-bit UTMI or ULPI is used. (Not supported in 16-bit UTMI mode) In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00. Note: In device mode, if you set RAMClkSel to 2'b11 (mac2_clk), the controller internally switches the ram_clk to bus_clk when the link state changes to Suspend (L2 or L3), and switches the ram_clk back to mac2_clk when the link state changes to resume or U2. In host mode, this register field setting should not be modified. A value of 2 can be chosen only if the pipe data width is 8 or 16 bits. In this case the when the ram_clk is switched to pipe_clk, it uses pipe_clk/2 instead of pipe_clk. If a value of 3 is chosen for RAMClkSel, then when ram_clk is switched to pipe_clk, then pipe_clk is used without any divider. In device mode, when RAMClkSel != 2'b00, the bus_clk_early frequency can be a minimum of 1 MHz. This is tested in simulation and also in hardware with Linux, Microsoft Windows 8, and MCCI Windows7 host drivers. Only control and non periodic transfers are supported when bus_clk is 1 MHz. For periodic applications, the bus_clk_early minimum frequency is higher depending on your application and SoC bus. Even though 1 MHz has been tested with standard host drivers, Synopsys recommends 5 MHz minimum for ASIC designs to provide a margin or at least have a backup option to increase the bus_clk frequency to 5 MHz if needed.

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Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x0	ScaleDown Scale-Down Mode When Scale-Down mode is enabled for simulation, the core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include: - Speed enumeration - HNP/SRP - Host mode suspend and resume 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values. SS Mode 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scaled down SS timing and repeat values including: - Number of TxEq training sequences reduce to 8 - LFPS polling burst time reduce to 100 nS - LFPS warm reset receive reduce to 30 uS. - Refer to the rtl_vip_scaledown_mapping.xls file under <workspace>/sim/SoC_sim directory for the complete list. 2'b10: No TxEq training sequences are sent. Overrides Bit 4. 2'b11: Enables bit 0 and bit 1 scale-down timing values.
3	R/W	0x0	DisScramble Disable Scrambling Transmit request to Link Partner on next transition to Recovery or Polling.

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Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
2	R/W	0x1	U2EXIT_LFPS If this bit is, 0: the link treats 248ns LFPS as a valid U2 exit. 1: the link waits for 8μs of LFPS before it detects a valid U2 exit.
1	R	0x0	GblHibernationEn This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	R/W	0x0	DsblClkGtng Disable Clock Gating When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.

8.12.6.6 0xC114 Global Power Management Status Register (Default Value:0x0000_0000)

Offset: 0xC114			Register Name: GPMSTS
Bit	Read/Write	Default/Hex	Description
31:28	W	0x0	PortSel This field selects the port number
27:17	/	/	/
16:12	R	0	U3Wakeup This field gives the following USB 3.1 port wakeup conditions: Bit [12]: Overcurrent Detected Bit [13]: Resume Detected Bit [14]: Connect Detected Bit [15]: Disconnect Detected Bit [16]: Last Connection State
11:10	/	/	/

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Offset: 0xC114			Register Name: GPMSTS
Bit	Read/Write	Default/Hex	Description
9:0	R	0x0	U2Wakeup This field indicates the following USB 2.0 port wakeup conditions: Bit [0]: Overcurrent Detected Bit [1]: Resume Detected Bit [2]: Connect Detected Bit [3]: Disconnect Detected Bit [4]: Last Connection State Bit [5]: ID Change Detected Bit [6]: SRP Request Detected Bit [7]: ULPI Interrupt Detected Bit [8]: USB Reset Detected Bit [9]: Resume Detected Changed

8.12.6.7 0xC118 Global Status Register (Default Value:0x7E80_0002)

Offset: 0xC118			Register Name: GSTS
Bit	Read/Write	Default/Hex	Description
31:20	R	0x7e8	CBELT Current BELT Value In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:8	/	/	/
7	R	0	Host_IP Host Interrupt Pending This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	R	0	Device_IP Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.

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Offset: 0xC118			Register Name: GSTS
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0	CSRTimeout CSR Timeout When this bit is 1'b1, it indicates that software performed a write or read to a core register that could not be completed within `DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: 65535).
4	R/W1C	0	BusErrAddrVld Bus Error Address Valid Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	/	/	/
1:0	R	0x02	CurMod Current Mode of Operation Indicates the current mode of operation: 2'b00: Device mode 2'b01: Host mode

8.12.6.8 0xC11C Global User Control Register 1 (Default Value: 0x0000_1988)

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DEV_DECOUPLE_L1L2_EVT Enable this bit if you want to use L1 (LPM) events separately and not combine it with L2 events when operating in USB 2.0 speeds. 0: L1 and L2 events (suspend and resume) are not separated. For both L1 and L2 events, common suspend and resume events are generated. 1: L1 and L2 events are separated when operating in USB 2.0 mode. For L1 and L2 events, separate suspend and resume events are generated.

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	DS_RXDET_MAX_TOUT_CTRL This bit is used to control the tRxDetectTimeoutDFP timer for the Enhanced SuperSpeed link. 0: 12ms is used as tRxDetectTimeoutDFP 1: 120ms is used as the tRxDetectTimeoutDFP This bit is used only in host mode. For more details, refer to the *USB 3.1 Specification*.
29	R/W	0x0	FILTER_SE0_FSLS_EOP 0: Single sampling (utmi/ulpi clock) of linestate is checked for SE0 detection. 1: Feature enabled; Two samplings of linestate are checked for SE0 detection This bit is applicable for FS/LS operation. If this feature is enabled, SE0 on the linestate is validated for two consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode (FS): If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the controller ignores single SE0 glitch on the linestate during transmit. Only two or more SE0 is considered as a valid EOP on FS port. Host mode (FS/LS): If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the controller ignores single SE0 glitch on the linestate during transmit. Only two or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if linestate has SE0 glitches during transmission. This bit is quasi-static, that is, it must not be changed during operation.

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	TX_IPGAP_LINECHECK_DIS 0: The linestate transitioning from J to idle for HS mode treated as end of current packet. 1: Feature enabled; For detecting the HS end of packet, a fixed delay is used instead of linestate transition. This bit is applicable for HS operation of U2MAC. If this feature is enabled, then the 2.0 MAC operating in HS ignores the UTMI/ULPI linestate during transmission of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the controller ignores the linestate after TX and waits for a fixed number of clocks (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap (between token to token/data) is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if linestate does not reflect the expected line state (J) during transmission. This bit is quasi-static, that is, it must not be changed during operation.

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	DEV_TRB_OUT_SPR_IND 0: Feature disabled; OUT TRB status does not set the Short Packet received bit 1: Feature enabled; OUT TRB status indicates Short Packet This bit is applicable for device mode only (and ignored in host mode). This feature can be enabled if the device application (software/hardware) wants to know whether a short packet is received for an OUT in the TRB status itself, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the {trbstatus, RSVD, SPR, PCM1, bufsize} dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, that is, it must not be changed during device operatio
26:25	/	/	/

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	DEV_L1_EXIT_BY_HW 0: Disables device L1 hardware exit logic 1: Feature enabled This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wakeup signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This hardware remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests through L1. This bit is quasi-static, it must not be changed during device operation.
23:21	R/W	0x0	IP_GAP_ADD_ON This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC. It should be programmed to a non-zero value only in case where you need to increase the default inter packet delay calculations in the USB 2.0 MAC module ${ldsg}_u2mac.v The inter packet delay is increased by number of utmi/ulpi clock cycles of this field value.

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
20:15	/	/	/
14	R/W	0x0	HW_LPM_CAP_DISABLE Disable hardware LPM capability in the xHCI capability register. When set, it disables hardware LPM capability in xHCI capability register.
13	R/W	0x0	HW_LPM_HLE_DISABLE Disable hardware LPM function in all USB 2.0 ports. When set, it disables hardware LPM function in all USB 2.0 ports.
12	R	0x1	DisUSB2RefClkGtng Disable ref_clk gating for USB 2.0 PHY (DisUSB2RefClkGtng) If ref_clk gating is disabled, then the ref_clk input cannot be turned off to the USB 2.0 PHY and controller. This is independent of the GCTL[DisClkGtng] setting. 1'b0: ref_clk gating enabled for USB 2.0 PHY 1'b1: ref_clk gating disabled for USB 2.0 PHY
11	R	0x1	DisRefClkGtng Disable ref_clk gating (DisRefClkGtng If the ref_clk gating is disabled then input ref_clk cannot be turned off to SSPHY and controller. This is independent of GCTL[DisClkGtng] setting. 1'b0: ref_clk gating Enabled for SSPHY 1'b1: ref_clk gating Disabled for SSPHY
10	R/W	0x0	RESUME_OPMODE_HS_HOST This bit is used only in host mode, and is for 2.0 opmode behaviour in HS Resume. When this bit is set to '1', the utmi/ulpi opmode will be changed to "normal" along with HS terminations after EOR. This is to support certain legacy UTMI/ULPI PHYs. When this bit is set to '0', the utmi/ulpi opmode will be changed to "normal" 2us after HS terminations change after EOR.
9	/	/	/

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
8	R/W	0x1	L1_SUSP_THRLD_EN_FOR_HOST This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: The device accepted BESL/BESLD value is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: The device accepted BESL/BESLD value is less than the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.
7:4	R/W	0x8	L1_SUSP_THRLD_FOR_HOST This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit. Note: Program this register field based on the UTMI/ULPI wakeup time in L1 suspend/sleep. In addition, for PCIe-based implementation, consider the DBESLD register value also.
3	R/W	0x1	HC_ERRATA_ENABLE Host ELD Enable (HELDEn) When this bit is set to 1, it enables the Exit Latency Delta (ELD) support defined in the xHCI 1.1. This bit is used only in the host mode. This bit has to be set to 1 in Host mode.

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Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	HC_PARCHK_DISABLE Host Parameter Check Disable (HParChkDisable) When this bit is set to '0', the xHC checks that the input slot/EP context fields comply to the *xHCI Specification*. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating 'PARAMETER ERROR'. When the bit is set to '1', the xHC does not perform parameter checks and does not generate 'PARAMETER ERROR' completion code.
1	/	/	/
0	R/W	0x0	LOA_FILTER_EN If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables.

8.12.6.9 0xC120 Global ID Register (Default Value: 0x3331_3130)

Offset: 0xC120			Register Name: GID
Bit	Read/Write	Default/Hex	Description
31:0	R	0x33313130	ID

8.12.6.10 0xC124 Global General Purpose Input/Output Register (Default Value:0x0000_0000)

Offset: 0xC124			Register Name: GGPIO
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0	GPO General Purpose Output This field's value is driven out on the gp_o[15:0] core output port.
15:0	R	0	GPI General Purpose Input This field's read value reflects the gp_i[15:0] core input value.

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8.12.6.11 0xC128 Global User ID Register (Default Value:0x1234_5678)

Offset: 0xC128			Register Name: GUID
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x12345678	UserID Application-programmable ID field.

8.12.6.12 0xC12C Global User Control Register (Default Value:0x0A41_6802)

Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x29	REFCLKPER This field indicates the period of ref_clk, in terms of nano seconds. The valid programmable values of this field are as follows: 'h19: 25ns (integer corresponding to the supported ref_clk frequencies of 39.7 MHz) 'h29: 41ns (integer corresponding to the supported ref_clk frequency of 24 MHz) 'h32: 50ns (integer corresponding to the supported ref_clk frequency of 20 MHz) 'h34: 52ns (integer corresponding to the supported ref_clk frequency of 19.2MHz) 'h3A: 58ns (integer corresponding to the supported ref_clk frequency of 17 MHz) 'h3E: 62ns (integer corresponding to the supported ref_clk frequency of 16 MHz) This field needs to be updated during power-on initialization.

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Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
21	R/W	0	NoExtrDl No Extra Delay Between SOF and the First Packet Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host should wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1'b1: Host doesn't wait after a SOF before it sends the first USB packet.
20	R/W	0x0	DMAIgnoreHCE
19	R/W	0x0	IgnoreHCETimeout
18	R/W	0x0	EN_EXTD_TBC_CAP When set, the Extended TBC Capability is reported in HCCPARAMS2 if the DWC_USB31_EXTD_TBC_CAP_EN parameter is enabled.
17	R/W	0	SprsCtrlTransEn Sparse Control Transaction Enable Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1’b1, the host controller schedules transactions for a Control transfer in different microframes/frames.

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Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
16	R/W	0	ResBwHSEPS Reserving 85% Bandwidth for HS Periodic EPs 1'b0: HC reserves 80% of the bandwidth for periodic EPs. 1'b1: HC relaxes the bandwidth to 85% to accommodate two high-speed high-bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two high-bandwidth ISOC devices (HD Webcams) are connected and each device requires 1024-bytes X 3 packets per micro-frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 paylod per micro-frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host mode operation only. This field is ignored for device mode.
15	/	/	/
14	R/W	0	USBHstInAutoRetryEn Host IN Immediate Retry When set, this field enables the Immediate Retry feature. For IN transfers (non-isochronous) that encounter data packets with CRC errors or internal overrun scenarios, the immediate retry feature causes the Host controller to reply to the device with a non-terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP != 0). If the Immediate Retry feature is disabled, the controller will respond with a terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP = 0). 1'b0: Immediate Retry Disabled 1'b1: Immediate Retry Enabled
13	/	/	/

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Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	ExtCapSuptEN External Extended Capability Support Enable When set, this field enables extended capabilities to be implemented outside the controller. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in "Debug Capability" returns 16. A read to the first DWORD of the last internal extended capability (the "xHCI Supported Protocol Capability for USB 3.1" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer field. This indicates there are no more capabilities.

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Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
11	R/W	0	InsrtExtrFSBODl Insert Extra Delay Between FS Bulk OUT Transactions Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. **Note: Setting this bit to one will reduce the Bulk OUT transfer performance for FS devices.**
10:0	R/W	0x2	DTOUT Device Timeout (DTOUT) This field is Host mode parameter which determines how long the host waits for response from Enhanced SuperSpeed Device before considering the transaction to be timeout. Each count indicates duration in terms of 125us. For example a value of 1 indicates timeout at the minimum of 125us and maximum of 250us. The maximum value that can be programmed is 200 which sets 25ms as timeout time (minimum is 25ms and maximum is 25.125ms).

8.12.6.13 0xC130 Global Bus Error Address Low Register (Default Value:0x0000_0000)

Offset: 0xC130			Register Name: GBUSERRADDLR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	BusAddrLo This register contains the lower 32 bits of the first bus address that encountered a bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core.

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8.12.6.14 0xC134 Global Bus Error Address High Register (Default Value:0x0000_0000)

Offset: 0xC134			Register Name: GBUSERRADDHR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	BusAddrHi This register contains the higher 32 bits of the first bus address that encountered a bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core.

8.12.6.15 0xC138 Global Super Speed Port to Bus Instance Mapping Low Register (Default Value:0x0000_0000)

Offset: 0xC138			Register Name: GPRTBIMAPLO
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	BINum1 SS USB Instance Number for Port 1 Application-programmable ID field.

8.12.6.16 0xC13C Global Super Speed Port to Bus Instance Mapping High Register (Default Value:0x0000_0000)

Offset: 0xC13C			Register Name: GPRTBIMAPHI
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.12.6.17 0xC160 Global Debug Queue/FIFO Space Available Register (Default Value: 0x0042_0000)

Offset: 0xC160			Register Name: GDBDFIFOSPACE
Bit	Read/Write	Default/Hex	Description
31:16	R	0x43	Space Available
15:9	/	/	/

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Offset: 0xC160			Register Name: GDBDFIFOSPACE
Bit	Read/Write	Default/Hex	Description
8:0	R/W	0x0	FIFO_Queue_Select • "FIFO/Queue Select[8:5] indicates the FIFO/Queue Type • "FIFO/Queue Select[4:0] indicates the FIFO/Queue Number For example, 9'b0_0010_0001 refers to RxFIFO_1 and 9'b0_0101_1110 refers to TxReqQ_30. 9'b0_0001_1111 to 9'b0_0000_0000: TxFIFO_31 to TxFIFO_0 9'b0_0011_1111 to 9'b0_0010_0000: RxFIFO_31 to RxFIFO_0 9'b0_0101_1111 to 9'b0_0100_0000: TxReqQ_31 to TxReqQ_0 9'b0_0111_1111 to 9'b0_0110_0000: RxReqQ_31 to RxReqQ_0 9'b0_1001_1111 to 9'b0_1000_0000: RxInfoQ_31 to RxInfoQ_0 9'b0_1010_0000: DescFetchQ_0 (for backwards compatibility) 9'b0_1010_0001: EventQ_0 (for backwards compatibility) 9'b0_1010_0010: ProtocolStatusQ_0 9'b0_1101_1111 to 9'b0_1110_0000: DescFetchQ_31 to DescFetchQ_0 9'b0_1111_1111 to 9'b0_1110_0000: WriteBack/EventQ_31 to WriteBack/EventQ_0 9'b1_0000_0111 to 9'b1_0000_0000: AuxEventQ_7 to AuxEventQ_0 (if EN_SEPARATE_DESC_QUEUES=1

8.12.6.18 0xC164 Global BMU Control Register (Default Value:0x9CC2_0026)

Offset: 0xC164			Register Name: GBMUCTL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x9CC2	/
15:6	R	0x0	/

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Offset: 0xC164			Register Name: GBMUCTL
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	separate_psq_en When DWC_USB31_EN_SEPARATE_PSQ_PER_DIR is enabled Separate internal process queue and state machine per direction is enabled when the bit is set to ?1?, BMU will process the plr_msg_type[PSQ_DIR] bit and pushes the messages to separate PSQ based on direction including special handling of control endpoint messages. when the bit is set to ?0?, BMU will ignore the plr_msg_type[PSQ_DIR] bit for all message types and pushes the messages to single PSQ to retain the legacy mode of operation.
4:3	R	0x0	/
2	R/W	0x1	axi_storder_en When DWC_USB31_AXI_STRICT_ORDER_EN parameter is enabled, both descriptor and data RxDMAs should be configured to use non-posted commands. For a given BI, descriptor/event RxDMA won't be issued until the previous issued data RxDMA is completed on the bus
1	R/W	0x1	active_id_en Active Id enabled
0	R/W	0x0	/

8.12.6.19 0xC16C Global Debug BMU Register (Default Value:0x0000_0000)

Offset: 0xC16C			Register Name: GDBGBMU
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	BMU_BCU Debug information
7:4	R	0x0	BMU_DCU Debug information
3:0	R	0x0	BMU_CCU Debug information

8.12.6.20 0xC170 Global Debug LSP MUX Register (Default Value:0x003F_0000)

Offset: 0xC170			Register Name: GDBGLSPMUX
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0xC170			Register Name: GDBGLSPMUX
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x3F	"logic_analyzer_trace" Port MUX Select Currently only bits[21:16] are used. For details on how the mux controls the debug traces, refer to "assign logic_analyzer_trace =" code section in the usb31.v file. A value of 6'h3F drives "0"s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
15	/	/	/
14:0	R/W	0x0	LSP Select In host mode: [14:0] - Selects the LSP debug information presented in the GDBGLSP register. In device mode: [3:0] - Device Endpoint Select (EPSELECT) Selects the Endpoint debug information presented in the GDBGEPINFO registers in device mode [7:4] - Device LSP Select (DEVSELECT) Selects the LSP debug information presented in the GDBGLSP register [14:8] - Host LSP Select Selects the LSP debug information presented in the GDBGLSP register

8.12.6.21 0xC174 Global Debug LSP Register (Default Value:0x0000_0000)

Offset: 0xC174			Register Name: GDBGLSP
Bit	Read/Write	Default/Hex	Description
31：0	R	0	LSP Debug Information This register is for internal use only.

8.12.6.22 0xC178 Global Debug Endpoint Information Register 0 (Default Value:0x0000_0000)

Offset: 0xC178			Register Name: GDBEPINFO0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	Endpoint Debug Information, bits [31:0] This register is for internal use only.

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8.12.6.23 0xC17C Global Debug Endpoint Information Register 1 (Default Value:0x0000_0000)

Offset: 0xC17C			Register Name: GDBGEPINFO1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	Endpoint Debug Information, bits [63:32] This register is for internal use only.

8.12.6.24 0xC180 Global High Speed Port to Bus Instance Mapping Low Register (Default Value:0x0000_0000)

Offset: 0xC180			Register Name: GPRTBIMAPLR_HS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0	BINum1 HS USB Instance Number for Port 1 Application-programmable ID field.

8.12.6.25 0xC184 Global High Speed Port to Bus Instance Mapping High Register (Default Value:0x0000_0000)

Offset: 0xC184			Register Name: GPRTBIMAPHR_HS
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.12.6.26 0xC188 Global Full Speed Port to Bus Instance Mapping Low Register (Default Value:0x0000_0000)

Offset: 0xC188			Register Name: GPRTBIMAPLR_FS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	BINum1 FS USB Instance Number for Port 1 Application-programmable ID field.

8.12.6.27 0xC18C Global Full Speed Port to Bus Instance Mapping High Register (Default Value:0x0000_0000)

Offset: 0xC18C			Register Name: GPRTBIMAPHR_FS
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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8.12.6.28 0xC190 Global Host Mode SoC Bandwidth Override Register (Default Value:0x0000_0000)

Offset: 0xC190			Register Name: GHMSOCBWOR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ovrd_port_soc_bw Overrides the SoC bandwidth port values When this field is set 1, the ovrd_soc_common_rd_wr_bus, ovrd_soc_rd_uF_kB_bandwidth, and ovrd_soc_wr_uF_kB_bandwidth register values are used instead common_soc_rd_wr, soc_rd_uF_kB_bandwidth, and soc_wr_uF_kB_bandwidth input ports
30	R/W	0x0	ovrd_common_soc_rd_wr Override value for the common_soc_rd_wr port 1'b0: Separate SoC Bus for Read and Write 1'b1: Common SoC Bus for Read and Write
29:15	R/W	0x0	ovrd_soc_wr_uF_kB_bandwidth SoC Bus Write Bandwidth in KiloBytes/Micro-Frame Override value for the soc_wr_uF_kB_bandwidth port
14:0	R/W	0x0	ovrd_soc_rd_uF_kB_bandwidth SoC Bus Read Bandwidth in KiloBytes/Micro-Frame Override value for the soc_rd_uF_kB_bandwidth port

8.12.6.29 0xC200 Global USB2 PHY Configuration Register (Default Value:0x0000_2400)

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHYSOFTRST UTMI PHY Soft Reset Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl.Reset register, and the core automatically writes to this register when the core is reset (vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset)
30:26	/	/	/

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	OVRD_FSLS_DISC_TIME Overriding the FS/LS disconnect time to 32us. If this value is 0, the FS/LS disconnect time is set to 2.5us as per the USB specification. If this value is non-0, then the disconnect detection time is set to 32us. Normally this value is set to 0. But if the 2.0 PHYs introduce noise on UTMI linestate and cause SE0 gliches longer than 2.5us, then a false disconnect condition may get triggered. To avoid interoperability issues with these PHYs, this bit can be set to 1
24:22	R/W	0x0	LSTRD LS Turnaround Time (LSTRDTIM) This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 0: 2 bit times 1: 2.5 bit times 2: 3 bit times 3: 3.5 bit times 4: 4 bit times 5: 4.5 bit times 6: 5 bit times 7: 5.5 bit times **Note:** **This field is applicable only in Host mode.** **For normal operation (to work with most LS devices), it is recommended to set the value of this field to 3'h0 (2 bit times).** The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay (~1 LS bit time) from the delay requirement of the device.

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
21:19	R/W	0x2	LSIPD LS Inter-Packet Time (LSIPD) This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: 0: 2 bit times 1: 2.5 bit times 2: 3 bit times 3: 3.5 bit times 4: 4 bit times 5: 4.5 bit times 6: 5 bit times 7: 5.5 bit times **Note:** **This field is applicable only in Host mode. For normal operation (to work with most LS devices), it is recommended to set this field to 3'h2 (3 bit times).** The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay (~1 LS bit time) from the delay requirement of the device.
18	R/W	0x0	ULPIExtVbusIndicator ULPI External VBUS Indicator Indicates the ULPI PHY VBUS over-current indicator. • 1'b0: PHY uses an internal VBUS valid comparator. • 1'b1: PHY uses an external VBUS valid comparator.

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	ULPIExtVbusDrv ULPI External VBUS Drive Selects supply source to drive 5V on VBUS, in the ULPI PHY. • 1'b0: PHY drives VBUS with internal charge pump (default). • 1'b1: PHY drives VBUS with an external supply.
16	/	/	/
15	R/W	0x0	ULPIAutoRes ULPI Auto Resume Sets the AutoResume bit in Interface Control register on the ULPI PHY. • 1'b0: PHY does not use the AutoResume feature. • 1'b1: PHY uses the AutoResume feature.
14	/	/	/
13:10	R/W	0x09	USBTrdTim USB 2.0 Turnaround Time Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). These following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: • 4'h5: When the MAC interface is 16-bit UTMI+. • 4'h9: When the MAC interface is 8-bit UTMI+. If SoC bus does not require 60 MHz and USB turnaround time is not critical, this field can be set to a larger value.

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	XCVRDLY Transceiver Delay: Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 1 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: If you enable the hibernation feature when the device controller comes out of power-off, you must re-initialize this bit with the appropriate value because the controller does not save and restore this bit value during hibernation. This bit is valid only in device mode.
8	R/W	0x0	EnblSlpM Enable utmi_sleep_n and utmi_l1_suspend_n The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is transferred to the external PHY. **Note: In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.**

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	PHYSel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select The application uses this bit to select a high-speed PHY or a full-speed transceiver. • 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY This bit is always 0, with Write Only access. • 1'b1: USB 1.1 full-speed serial transceiver This bit is always 1, with Write Only access. If both interface types are selected in global (parameters values are not zero), the application uses this bit to select the active interface is active, with Read-Write bit access. Note: USB 1.1 full-serial transceiver is not supported. This bit always reads as 1'b0.
6	R/W	0x0	SusPHY Suspend USB2.0 HS/FS/LS PHY When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. For DRD/OTG configurations, it is recommended that this bit is set to '0' during coreConsultant configuration. If it is set to '1', then the application should clear this bit after power-on reset. Application needs to set it to '1' after the core initialization is completed. For all other configurations, this bit can be set to '1' during core configuration. Note: In host mode, on reset, this bit is set to '1'. Software can override this bit after reset.
5	R/W	0x0	FSIntf Full-Speed Serial Interface Select The application uses this bit to select a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. • 1'b0: 6-pin unidirectional full-speed serial interface This bit is set to 0 with Read Only access. • 1'b1: 3-pin bidirectional full-speed serial interface This bit is set to 0 with Read Only access. Note: USB 1.1 full-speed serial interface is not supported. This bit always reads as 1'b0.

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	ULPI_UTMI_Sel ULPI or UTMI+ Select The application uses this bit to select a UTMI+ or ULPI Interface. • 1'b0: UTMI+ Interface • 1'b1: ULPI Interface
3	R/W	0x0	PHYIf PHY Interface If UTMI+ is selected, the application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. • 1'b0: 8 bits • 1'b1: 16 bits If ULPI is selected , this bit is reserved to '0'. Note: All the enabled 2.0 ports should have the same clock frequency as Port0 clock frequency (utmi_clk[0]). The UTMI 8-bit and 16-bit modes cannot be used together for different ports at the same time (that is, all the ports should be in 8-bit mode, or all of them should be in 16-bit mode, at a time). If any of the USB 2.0 ports is selected as ULPI port for operation, then all the USB 2.0 ports should be operating at 60 MHz.

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Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	TOutCal HS/FS Timeout Calibration The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor. This factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: • One 30-MHz PHY clock = 16 bit times • One 60-MHz PHY clock = 8 bit times Full-speed operation: • One 30-MHz PHY clock = 0.4 bit times • One 60-MHz PHY clock = 0.2 bit times • One 48-MHz PHY clock = 0.25 bit times

8.12.6.30 0xC2C0 Global USB3 PIPE Control Register (Default Value:0x010C_0002)

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHYSoftRst PHY soft-reset; to issue PHY reset, software should set this bit and reset this bit after meeting PHY reset timing.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.1 cable. This bit enables placing the SS port link into a compliance state. By default, this bit should be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: Disconnect any plugged in devices. Perform USBCMD.HCRST or power-on-chip reset. Set PORTSC.PP=0. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence (toggle the set GUSB3PIPECTL. HstPrtCmpl): Set GUSB3PIPECTL.HstPrtCmpl=0. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	U2P3ok Enable P3 entry during U2/SSInactive (U2P3ok). This is not recommended with Synopsys PHY which has P3 exit time of ~1ms and P2 exit time of ~100uS. This is recommended only if your PHYs P3 exit time is close to P2 exit time. Putting the ESS PHY in P3 during U2 would affect ESS Asynchronous endpoint performance and also this could prevent U2 entry if there are ESS periodic endpoints and their BInterval is in the sub milli-second range. rammer's Guide for more details. 0: During link state U2/ESS.Inactive, put PHY in P2 (Default) 1: During link state U2/ESS.Inactive, put PHY in P3 (Not recommended for Synopsys PHY). Note: For a port, if GUSB3PIPECTL[7]=1 and GUSB3PIPECTL[29]=1, set GUSB3PIPECTL[11] to 1
28	R/W	0x0	DisRxDetP3 Disabled receiver detection in P3 0: If PHY is in P3 and Core needs to perform receiver detection, Core will perform receiver detection in P3 1: If PHY is in P3 and Core needs to perform receiver detection, Core will change PHY power state to P2 and then perform receiver detection. After receiver detection, Core will change PHY power state to P3.
27	R/W	0x0	Ux_exit_in_Px Ux Exit in Px 0: The core does U1/U2/U3 exit in PHY power state P0 (default behavior) 1: The core does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively This bit is added for SS PHY workaround where SS PHY injects a glitch on pipe3_RxElecIdle while receiving Ux exit LFPS, and pipe3_PowerDown change is in progress. Note: This bit is used by third-party SS PHY, else it should be set to '0'.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	ping_enhancement_en Ping Enhancement Enable When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for Downstream port only. Note: This bit is used by third-party SS PHY, else it should be set to '0'.
25	R/W	0x0	u1u2exitfail_to_recov U1U2exitfail to Recovery When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.
24	R/W	0x1	request_p1p2p3 Always Request P1/P2/P3 for U1/U2/U3 When set, the core always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the core does not request P1/P2/P3 power state change. Note: For third-party SS PHY, check with your PHY vendor, else this bit should be set to '1'.
23	R/W	0x0	StartRxdetU3RxDet Start Receiver Detection in U3/Rx.Detect If USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the core starts receiver detection on the rising edge of this bit. This can only be used for Downstream ports. This bit must be set to “0” for Upstream ports. This feature must not be enabled for normal operation.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
22	R/W	0x0	DisRxDetU3RxDet Disable Receiver Detection in U3/Rx.Det When set, the core does not handle receiver detection in either U3 or Rx.Detect states. USB3_GUSB3PIPECTL_INIT[23] should be used to start receiver detection manually. This bit can only be used for Downstream port. This bit must be set to “0” for Upstream ports. This feature must not be enabled for normal operation.
21:19	R/W	0x0	Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality.
18	R/W	0x0	DELAYP1TRANS Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively • 1’b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 • 1’b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit should be set to '1' for self PHY. It is also used by third-party SS PHY.
17	R/W	0x1	Suspend USB3.1 SS PHY When set, and if Suspend conditions are valid, the USB 3.1 PHY enters Suspend mode. For DRD/OTG configurations, it is recommended that this bit is set to ‘0’ during coreConsultant configuration. If it is set to ’1’, then the application should clear this bit after power-on reset. Application needs to set it to ’1’ after the core initialization is completed. For all other configurations, this bit can be set to ’1’ during core configuration.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
16:15	R	0x0	DatWidth PIPE Data Width • 2'b00: 32 bits • 2'b01: 16 bits • 2'b10: 8 bits One clock after reset, these bits receive the value seen on the "pipe3_DataBusWidth".The simulation testbench uses the coreConsultant parameter to configure the VIP. These bits in the coreConsultant parameter should match your PHY data width and the "pipe_DataBusWidth" port.
14	R/W	0x0	AbortRxDetInU2 Abort Rx Detect in U2 When set, and the link state is U2, then the core will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for Downstream port only. **Note: This bit is used by third-party SS PHY. It should be set to '0' for self PHY.**
13	R/W	0x0	SkipRxDet Skip Rx Detect When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	R/W	0x0	LFPSP0Algn LFPS P0 Align When this bit is set, LFPS during U1/U2/U3 exit is extended until data is ready at the PIPE to ensure the 20-ns gap between LFPS and SS/SSP.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	P3P2TranOK P3 P2 Transitions OK When set, the core transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 specification. According to PIPE3 Specification, any direct transition between P3 and P2 is illegal. This bit is used only for some non-Synopsys PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It should be set to '0' for self PHY.
10	R/W	0x0	P3ExSigP2 P3 Exit Signal in P2 (P3ExSigP2) When this bit is set, the controller always changes the PHY power state to P2, before attempting a U3 exit handshake.
9	R/W	0x0	LFPSFilt LFPS Filter When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.
8	R/W	0x0	RX_DETECT to Polling.LFPS Control 1'b0 (Default): Enables a 400µs delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1'b1: Disables the 400µs delay to start Polling LFPS after RX_DETECT.
7	/	/	/
6	R/W	0x0	TxSwing Tx Swing Refer to the PIPE specification.
5:3	R/W	0x0	TxMargin Tx Margin[2:0]
2:1	R/W	0x1	TxDeemphasis Tx Deemphasis The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.

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Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	ElasticBufferMode Elastic Buffer Mode

8.12.6.31 0xC300+0x04*n Global Transmit FIFO Size Register n (Default Value: 0x0000_0043)

Offset: 0xC300+0x04*n (n=FIFO_number)			Register Name: GTXFIFOSIZ0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	TxFStAddr_n Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn.
15	/	/	/
14:0	R/W	0x43	TxFDep_n TxFIFOn Depth This value is in terms of depth*Tx RAM Data width. • Minimum value: 32 • Maximum value: 32,767

8.12.6.32 0xC380+0x04*n Global Receive FIFO Size Register n (Default Value: 0x0000_0413)

Offset: 0xC380+0x04*n (n=FIFO_number)			Register Name: GRXFIFOSIZ0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	RxFStAddr_n RxFIFOn RAM Start Address This field contains the memory start address for RxFIFOn.
15	/	/	/
14:0	R/W	0x413	RxFDep_n RxFIFOn Depth This value is in terms of depth*Tx RAM Data width. • Minimum value: 32 • Maximum value: 16,384

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8.12.6.33 0xC400+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Address Lower Register n (Default Value:0x0000_0000)

Offset: 0xC400+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTADLRn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EvntAdrLo Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

8.12.6.34 0xC404+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Address Higher Register n (Default Value:0x0000_0000)

Offset: 0xC404+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTADHRn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EvntAdrHi Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

8.12.6.35 0xC408+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Size Register n (Default Value:0x0000_0000)

Offset: 0xC408+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTSIZn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EvntIntMask Event Interrupt Mask When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
30:16	/	/	/
15:0	R/W	0x0	EVNTSiz Event Buffer Size in bytes Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization.

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8.12.6.36 0xC40C+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Count Register n (Default Value:0x0000_0000)

Offset: 0xC40C+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTCOUNTn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EVNT_HANDLER_BUSY Event Handler Busy Device software event handler busy indication. The controller sets this bit when the interrupt line is asserted due to pending events. Software clears this bit (with 1'b1) when it has finished processing the events (along with updating the EVNTCOUNT in this register). The controller does not raise the interrupt line for a new event unless this bit is cleared. Note: When Interrupt moderation is disabled (that is, DEVICE_IMODI = 0), this bit is ignored.
30:16	/	/	/
15:0	R/W	0x0	EVNTCount Event Count When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. The interrupt line remains high when count is not 0.

8.12.6.37 0xC610 Global Device TX FIFO DMA Priority Register (Default Value:0x0000_0000)

Offset: 0xC610			Register Name: GTXFIFOPRIDEV
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

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Offset: 0xC610			Register Name: GTXFIFOPRIDEV
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	gtxfifopridev Device TXFIFO priority This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. High-priority TXFIFOs are granted access using round-robin arbitration 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the controller is configured to operate in the device mode (includes DRD). The register size corresponds to the number of Device IN endpoints. Note Since the device mode uses only one RXFIFO, there is no Device RXFIFO DMA Priority Register.

8.12.6.38 0xC618 Global Host TX FIFO DMA Priority Register (Default Value:0x0000_0000)

Offset: 0xC618			Register Name: GTXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/

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Offset: 0xC618			Register Name: GTXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x0	gtxfifoprihst Host TXFIFO priority This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). 2. The TX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

8.12.6.39 0xC61C Global Host RX FIFO DMA Priority Register (Default Value:0x0000_0000)

Offset: 0xC61C			Register Name: GRXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

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Offset: 0xC61C			Register Name: GRXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x0	grxfifoprihst Host RXFIFO priority This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). 2. The RX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

8.12.6.40 0xC624 Global Host FIFO DMA High-Low Priority Ratio Register (Default Value:0x0A0A_0101)

Offset: 0xC624			Register Name: GDMAHLRATIO
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

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Offset: 0xC624			Register Name: GDMAHLRATIO
Bit	Read/Write	Default/Hex	Description
28:24	R/W	0xa	hstrxfifo_mac RX MAC ESS Priority Count Specifies the Global Host FIFO MAC access Ratio Register's (GDMAHLRATIO) RX SS:HSFSLS Ratio power-on initialization value (bit[28:24]). This register specifies MAC write access count relation between ESS FIFOs vs HS+FSLS FIFOs. Specifically, FIFO access arbiter prioritizes the HS+FSLS FIFOs for one clock after the specified number of write access to the SS FIFOs.
23:21	/	/	/
20:16	R/W	0xa	hsttxfifo_mac TX MAC ESS Priority Count Specifies the Global Host FIFO MAC access Ratio Register's (GDMAHLRATIO) TX SS:HSFSLS Ratio power-on initialization value (bit[20:16]). This register specifies MAC read access count relation between ESS FIFOs vs HS+FSLS FIFOs. Specifically, FIFO read access arbiter prioritizes the HS+FSLS FIFOs for one clock after the specified number of read access to the SS FIFOs.
15:13	/	/	/

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Offset: 0xC624			Register Name: GDMAHLRATIO
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x1	hstrxfifo_dma RX DMA ESS Priority Count Specifies the Global Host FIFO DMA access Ratio Register's (GDMAHLRATIO) RX SS:HSFSLS Ratio power-on initialization value (bit[12:8]). This register specifies the relative priority of the SS FIFOs vs. the HS+FSLS FIFOs. Specifically, the DMA arbiter prioritizes the HS/FSLS round-robin arbiter group for one packet after the specified number of packet grants to the ESS round-robin arbiter group. When a standard driver is used, such as the xHCI driver from Microsoft, this register must be initialized to meet system requirements before synthesizing the controller. If you are developing your own xHCI host driver, then this register can be configured by your driver. It is recommended to keep this value as 1 so that HS/FSLS gets same priority as ESS. The HS/FSLS bandwidth requirement is negligible compared to ESS, so keeping this value as 1 ensures USB 2.0 operation is not affected by high bandwidth ESS.
7:5	/	/	/

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Offset: 0xC624			Register Name: GDMAHLRATIO
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x1	hsttxfifo_dma TX DMA ESS Priority Count Specifies the Global Host FIFO DMA access Ratio Register's (GDMAHLRATIO) TX SS:HSFSLS Ratio power-on initialization value (bit[4:0]). This register specifies the access weight of the SS FIFOs vs. the HS+FSLS FIFOs. Specifically, the DMA arbiter prioritizes the HS/FSLS round-robin arbiter group for one packet after the specified number of packet grants to the ESS round-robin arbiter group. When a standard driver is used, such as the xHCI driver from Microsoft, this register must be initialized to meet system requirements before synthesizing the controller. If you are developing your own xHCI host driver, then this register can be configured by your driver. It is recommended to keep this value as 1 so that HS/FSLS gets same priority as ESS. The HS/FSLS bandwidth requirement is negligible compared to ESS, so keeping this value as 1 ensures USB 2.0 operation is not affected by high bandwidth ESS.

8.12.7 Device Register Description

8.12.7.1 0xC700 Device Configuration Register (Default Value:0x0008_0805)

Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	ISPP Ignore Stream Packet Pending This bit only effect stream-capable bulk endpoints. When this bit is set to ‘0’ and the controller receives a Data Packet with the Packet Pending (PP) bit set to ‘0’ for OUT endpoints, or it receives an ACK with the NumP field set to ‘0’ and PP set to ‘0’ for IN endpoints, the core attempts to search for another stream (CStream) to initiate to the host. However, there are two situations where this behavior is not optimal: When the host is setting PP=’0’ even though it has not finished the stream, or When the endpoint on the device is configured with one transfer resource and therefore does not have any other streams to initiate to the host. When this bit is set to '1', the core ignores the Packet Pending bit for the purposes of stream selection and does not search for another stream when it receives DP(PP=’0’) or ACK(NumP=’0’, PP=’0’). This can enhance the performance when the device system bus bandwidth is low or the host responds to the core's ERDY transmission very quickly.
22	R/W	0x0	LPMCAP LPM Capable The application uses this bit to control the USB Device LPM capabilities. If the core operates as a non-LPM-capable device, it cannot respond to LPM transactions. 0: LPM capability is not enabled. 1: LPM capability is enabled.

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Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
21:17	R/W	0x4	NUMP Number of Receive Buffer This bit indicates the number of receive buffers to be reported in the ACK TP. The usb3 controller uses this field if GRXTHRCFG.USBRxPktCntSel is set to '0'. The application can program this value based on RxFIFO size, buffer sizes programmed in descriptors, and system latency. For an OUT endpoint, this field controls the number of receive buffers reported in the NumP field of the ACK TP transmitted by the controller.
16:12	R/W	0x0	INTRNUM Interrupt Number Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts are generated.
11:10	/	0x2	/
9:3	R/W	0x0	DEVADDR Device Address The application must perform the following: Program this field after every SetAddress control command. Reset this field to zero after USB reset.

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Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x5	DEVSPD Device Speed Indicates the speed at which the application requires the controller to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the controller is connected. 3'b101: Enhanced SuperSpeed (USB 3.1 PHY clock is 156.25 MHz or 312.5 MHz operating at 10Gbps) 3'b100: SuperSpeed (USB 3.1 PHY clock is 125 MHz or 250 MHz operating at 5Gbps) 3'b000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 3'b001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) Values: 0x5 (EnhancedSuperSpeed): Enhanced SuperSpeed (USB 3.1 PHY clock is 156.25 MHz or 312.5 MHz operating at 10Gbps) 0x4 (SuperSpeed): SuperSpeed (USB 3.1 PHY clock is 125 MHz or 250 MHz operating at 5Gbps) 0x0 (HighSpeed): High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 0x1 (FullSpeed): Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)

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8.12.7.2 0xC704 Device Control Register (Default Value:0x0000_0000)

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RS Run/Stop Software writes 1 to this bit to start the device controller operation. To stop device controller operation, software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the STS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: After power-on reset and CSR initialization, software must write 1 to this bit to start the device controller. The controller will not signal connect to the host until this bit is set. Software uses this bit to control the device controller to perform a soft disconnect. When software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until software writes 1 to this bit. If software is attempting a connect after the soft disconnect, it should set DCTL[8:5] to 5 before reasserting the Run/Stop bit. When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller.

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Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	CSFTRST Core Soft Reset Resets the all clock domains as follows: This bit clears the interrupts and all the CSRs except GSTS, USB31_IP_NAME, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the core. This is a self-clearing bit; the core clears this bit after all necessary logic is reset in the core and all the PHY clocks are active/running after PHY reset, which may take several milliseconds depending on the PHY's clock latency. Software can have a poll rate of 1 ms or more to check if this bit has been cleared or not. Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation.
29	/	/	/

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Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
28:24	R/W	0x0	HIRDTH HIRD Threshold The core asserts output signals UTMI_L1_SUSPEND_n and UTMI_SLEEP_n on the basis of this signal: The core asserts UTMI_L1_SUSPEND_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: HIRD value is greater than or equal to the value in DCTL.HIRDTH[3:0] DCTL.HIRDTH[4] is set to '1' The core asserts UTMI_SLEEP_n on L1 when one of the following is true: If the HIRD value is less than HIRDTH[3:0] or HIRDTH[4] is set to '0'.
23:20	R/W	0xf	LPM_NYET_thres Bits [23:20]: LPM NYET Response Threshold (LPM_NYET_thres) Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The controller always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The controller responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). No data is pending in the TxFIFO and the RxFIFO is empty. The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0]

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Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	KeepConnect When '1', this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device core disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ('0'), or if the core should not disconnect when RunStop is set to 0 ('1'). This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2.
18	R/W	0x0	L1HibernationEn When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core will not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	W	0x0	CRS Controller Restore State This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'.
16	W	0x0	CSS Controller Save State This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'.

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Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
15:13	/	/	/
12	R/W	0x0	INITU2EN Initiate U2 Enable 0x0: May not initiate U2 0x1: May initiate U2 On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received. If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
11	R/W	0x0	ACCEPTU2EN Accept U2 Enable 0x0: Reject U2 except when Force_LinkPM_Accept bit is set 0x1: Core accepts transition to U2 state if nothing is pending on the application side. On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving a SetConfiguration command.
10	R/W	0x0	INITU1EN Initiate U1 Enable 0x0: May not initiate U1 0x1: May initiate U1 On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.
9	R/W	0x0	ACCEPTU1EN Accept U1 Enable 0x0: Reject U1 except when Force_LinkPM_Accept bit is set 0x1: Core accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving a SetConfiguration command.

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Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
8:5	R/W	0x0	ULSTCHGREQ USB/Link State Change Request Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Refer to the USB3 specification. Alternatively, you can force the local link directly into Compliance mode, by resetting the SS link with the RUN/STOP bit set to zero. If you then write “10” to the USB/Link State Change field and “1” to RUN/STOP, the Link will go to Compliance. Once you are in Compliance, you may alternately write “zero” and “10” to this field to advance the compliance pattern. In SS mode: Value Requested Link State Transition/Action 0 No Action 4 SS.Disabled 5 Rx.Detect 6 SS.Inactive 8 Recovery 10 Compliance Others Reserved In HS/FS/LS mode: Value Requested USB state transition 8 Remote wakeup request Others Reserved The Remote wakeup request should be issued 2μs after the device goes into suspend state (DSTS[21:18] is 3). Note: After coming out of hibernation, software should write 8 (Recovery) into this field to confirm exit from the suspended state

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Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
4:1	R/W	0x0	TSTCTL Test Control • 4'b000: Test mode disabled • 4'b001: Test_J mode • 4'b010: Test_K mode • 4'b011: Test_SE0_NAK mode • 4'b100: Test_Packet mode • 4'b101: Test_Force_Enable • Others: Reserved
0	/	/	/

8.12.7.3 0xC708 Device Event Enable Register (Default Value:0x0000_0000)

Offset: 0xC708			Register Name: DEVTEN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	LDMEVTEN LDM Response Event Enable. Enables interrupt when response to LDM request is received.
14	R/W	0x0	L1WKUPEVTEN L1 Resume Detected Event Enable.
13	/	/	/
12	R/W	0x0	VndrDevTstRcvEn Vendor Device Test LMP Received Event Enable
11:10	/	/	/
9	R/W	0x0	ErrticErrEn Erratic Error Event Enable
8	R/W	0x0	L1SUSPEN L1 Suspend Event Enable
7	R/W	0x0	SofEn Start of (micro-)Frame Enable For debug purpose only; normally software must disable this event.
6	R/W	0x0	U3L2L1SuspEn U3/L2-L1 Suspend Event Enable.
5	R/W	0x0	HibernationReqEvtEn This bit enables/disables the generation of the Hibernation Request Event.

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Offset: 0xC708			Register Name: DEVTEN
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	WkUpEvtEn Resume/Remote Wakeup Detected Event Enable
3	R/W	0x0	ULStChgEn USB/Link State Change Event Enable
2	R/W	0x0	ConnectDoneEn Connect Done Enable
1	R/W	0x0	USBRstEn USB Reset Enable
0	R/W	0x0	DisconnEvtEn Disconnect Detected Event Enable

8.12.7.4 0xC70C Device Status Register (Default Value:0x0002_0004)

Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R	0x0	DCNRD Device Controller Not Ready The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when USB3_EN_PWROPT is set to 2 and GCTL[1].GblHibernationEn =1.
28	R/W1C	0x0	SRE Save/Restore Error This bit is currently not supported.
27:26	/	/	/
25	R	0x0	RSS Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the restore process, it will complete the command by setting DSTS.RSS to '0'.

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Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
24	R	0x0	SSS Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	R	0x0	CoreIdle Core Idle The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. **Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the core and does not hold a static value.**
22	R	0x0	DevCtrlHlt Device Controller Halted This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to '0', the core is idle and the lower layer finishes the disconnect process. When Halted =1, the core does not generate Device events.
21:18	R	0x0	USBLnkSt USB/Link State In SS mode: (LTSSM State) 0x0: U0 0x1: U1 0x2: U2 0x3: U3 0x4: SS_DIS 0x5: RX_DET 0x6: SS_INACT 0x7: POLL 0x8: RECOV 0x9: HRESET 0xA: CMPLY 0xB: LPBK

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Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
			0xF: Resume/Reset In HS/FS/LS mode: 0x0: On state 0x2: Sleep state 0x3: Suspend state 0x4: Disconnected state (Default state) 0x5: Early Suspend state (valid only when Hibernation is disabled, GCTL [1]. GblHibernationEn =0) 0xE: Reset (valid only when Hibernation is disabled, GCTL [1]. GblHibernationEn =1) 0xF: Resume (valid only when Hibernation is disabled, GCTL [1]. GblHibernationEn=1) The Resume/Reset link state indicates that the core received a resume or USB reset request from the host while the link was in hibernation. Software must write '8' (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request. The Early Suspend link state is an early indication of device suspend in HS/FS. The link state changes to Early Suspend after detecting bus idle for 3ms. In HS operation, this is an indication that the USB bus (that is, LineState) has been in idle (SE0) for 3ms. However, it does not confirm whether the next process is Suspend or Reset. The device checks the bus again after pull up enable delay and if the line state indicates Suspend (full speed J), then the device waits for additional time (~3ms) to indicate the actual Suspend state. In FS operation, this is an indication that the USB bus (that is, LineState) has been in idle (J) for 3ms. The device waits for additional time (~3ms of Idle) to indicate the actual Suspend state. When Hibernation is enabled, GCTL [1]. GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL [31].Run/Stop set to '1' and DSTS[29].DCNRD = 0.
17	R	0x1	RXFIFOEMP RxFIFO Empty

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Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
16:3	R	0x0000	SOFFN Frame/Micro-Frame Number of the Received SOF When the controller is operating at SuperSpeed/SuperSpeedPlus, [16:3] indicates the microframe/ITP number When the core is operating at high-speed, [16:6] indicates the frame number [5:3] indicates the microframe number When the core is operating at full- or low-speed, [16:14] is not used. Software can ignore these 3 bits [13:3] indicates the frame number
2:0	R	0x4	ConnectSpd Connected Speed Indicates the speed at which the core has come up after speed detection through a chirp sequence. 0x0: High-Speed (PHY clock is running at 30 or 60 MHz) 0x1: Full-Speed (PHY clock is running at 30 or 60 MHz) 0x4: Super-Speed (PHY clock is running at 125 or 250 MHz) Low-speed is not supported for device using a UTMI+ PHY

8.12.7.5 0xC710 Device Generic Command Parameter Register (Default Value:0x0000_0000)

Offset: 0xC710			Register Name: DGCMDPAR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PAR Parameter [31:0] This register indicates the device command parameter. This must be programmed before or along with the device command.

8.12.7.6 0xC714 Device Generic Command Register (Default Value:0x0000_0000)

Offset: 0xC714			Register Name: DGCMD
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0xC714			Register Name: DGCMD
Bit	Read/Write	Default/Hex	Description
15:12	R	0x0	CMDSTS Command Status 1: CmdErr: Indicates that the device controller encountered an error while processing the command. 0: Indicates command success.
11	/	/	/
10	R/W	0x0	CMDACT Command Active The software sets this bit to '1' to enable the device controller to excute the generic command. The device controller clears this bit to '0' after executing the command.
9	/	/	/
8	R/W	0x0	CMDIOC Command Interrupt on Complete When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum.
7:0	R/W	0x00	CMDTYP Command Type Specifies the type of command the software driver is requesting the core to perfrom. 02h: Set Periodic Parameters 04h: Set Scratchpad Buffer Array Address Lo 05h: Set Scratchpad Buffer Array Address Hi 07h: Transmit Device Notification 09h: Selected FIFO Flush 0Ah: All FIFO Flush 0Ch: Set Endpoint NRDY 11h: Restart After Disconnect All other values are reserved.

8.12.7.7 0xC718 Device Control Register 1 (Default Value:0x0000_0000)

Offset: 0xC718			Register Name: DCTL1
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

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Offset: 0xC718			Register Name: DCTL1
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	EN_ENDXFER_ON_RJCT_STRM Enable bit for new reject stream flow. On receiving a reject stream(FFFF) on USB side, Controller updates the application SW with STREAMEVT_NOTFOUND with streamid as FFFF, On decoding this event application SW needs to apply an ENDXFER command which flushes all FIFO's . Until an ENDXFER is issued, Any stream packet received(on USB) will not lead to search of available streams in cache and release of ERDY.Controller writes STREAM_NOT_FOUND events until ENDXFER completion. 0: Feature disabled. No Reject status is updated to application SW. 1: Feature enabled, Reject staus is updated on receiving a reject stream(on USB).Decoding this event application SW needs to apply an ENDXFER.
1	R/W	0x0	DIS_CLRSPR_SXFER Disable bit to clear intrenal SPR bit during start transfer. If an End Transfer Command is issued during a transfer, there is a possibility that the internal SPR (short packet received/retry received) gets set, but not cleared. The SPR clearing is now done when the new Start Transfer command is issued. Using this register bit, you can disable the clearing of the SPR bit during a Start Transfer command. 0: The SPR bit is cleared when a Start Transfer command is issued (default value). 1: The SPR bit is not cleared when a Start Transfer command is issued.
0	/	/	/

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8.12.7.8 0xC720 Device Active USB Endpoint Enable Register (Default Value:0x0000_0000)

Offset: 0xC720			Register Name: DALEPENA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	USBACTEP USB Active Endpoints This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0–15 and OUT endpoints 0–15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN ... The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Application software clears these bits for all endpoints (other than EP0- OUT and EP0-IN) after detecting a USB reset. After receiving SetConfiguration and SetInterface request, the application must program endpoint registers accordingly and set these bits.

8.12.7.9 0xC724 Device LDM Request Control Register (Default Value:0x0000_0000)

Offset: 0xC724			Register Name:DLDMENA
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	LDMADJ LDM request interval duration This field indicates Link Delay adjustment in terms of nano-seconds After receiving Link Delay through LDM events the application must set these bits with average value. After receiving ClearFeature(LDM_ENABLE) the application must program and reset these bits.

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Offset: 0xC724			Register Name:DLDMENA
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0x0	LDMDUR LDM request interval duration This field indicates gap between two LDM request in terms of microframes After receiving SetFeature(LDM_ENABLE) the application must set these bits. After receiving ClearFeature(LDM_ENABLE) the application must program and reset these bits.
7:4	R/W	0x0	NOLOWPWRDUR No Low Power Duration After starting a transfer on an ESS ISOC endpoint, the application must program these bits. Each count represents the duration in terms of 8 ms. For example, a value of 3 represents 24 ms.
3:1	R/W	0x0	LDMRQS LDM number of requests This field indicates how many LDM requests Controller sends. A value of zero indicates request to send forever After receiving SetFeature(LDM_ENABLE) the application must set these bits. After receiving ClearFeature(LDM_ENABLE) the application must program and reset these bits
0	R/W	0x0	LDMENA LDM enabled This field indicates PTM protocol LDM request is enabled After receiving SetFeature(LDM_ENABLE) the application must set this bit. After receiving ClearFeature(LDM_ENABLE) the application must program and reset this bit. After receiving 4 consecutive timeout response to LDM, Hardware resets this bit.

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8.12.7.10 0xC800 + 0x10*n (n=0-9) Device Physical Endpoint-n Command Parameter 2 Register (Default Value:0x0000_0000)

Offset: 0xC800 + 0x10*n (n=0-9)			Register Name: DEPCMDPAR2_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	PAR2 Parameter 2 This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

8.12.7.11 0xC804 + 0x10*n (n=0-9) Device Physical Endpoint-n Command Parameter 1 Register (Default Value:0x0000_0000)

Offset: 0xC804 + 0x10*n (n=0-9)			Register Name: DEPCMDPAR1_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	PAR1 Parameter 1 This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command.

8.12.7.12 0xC808 + 0x10*n (n=0-9) Device Physical Endpoint-n Command Parameter 0 Register (Default Value:0x0000_0000)

Offset: 0xC808 + 0x10*n (n=0-9)			Register Name: DEPCMDPAR0_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	PAR0 Parameter 0 This register indicates the physical endpoint command Parameter 0. This must be programmed before or along with the command. For commands needing only one 32-bit parameter, it must be programmed before issuing the command.

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8.12.7.13 0xC80C + 0x10*n (n=0-9) Device Physical Endpoint-n Command Register (Default Value:0x0000_0000)

Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	CMDPAR (W) Command Parameters, when this register is written: For Start Transfer command: [31:16]: Stream ID. The USB Stream ID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: [31:16]: Start Micro-Frame Number, indicates the (micro-)frame number to which the first TRB applies For Update Transfer, End Transfer, and Start New Configuration commands: [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. EVTPAR (R) Event Parameters, when this register is read: For XferNotReady, XferComplete, and Stream events on Bulk Endpoints: [31:16]: StreamID. Applies only to bulk endpoints that support streams. This indicates the Stream ID of the transfer for which the event is generated For XferInProgress: [31:16]: Isochronous Microframe Number (IsocMicroFrameNum): Indicates the microframe number of the beginning of the interval that generated the XferInProgress event (debug purposes only) For XferNotReady events on Isochronous Endpoints: [31:16]: Isochronous Microframe Number (IsocMicroFrameNum). Indicates the microframe number during which the endpoint was not ready EPCmdCmplt events For all EPCmdCmplt events [27:24]: Command Type. The command type that completed (Valid only in a DEPEVT event. Undefined when read from the DEPCMD.EventParam field).

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Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
			For EPCmdCmplt events in response to Get Data Sequence command: [20:16]: Current Data Sequence Number (CurDatSeqNum). The endpoint's current data sequence number is returned in this field. For EPCmdCmplt event in response to Start Transfer command: [22:16]: Transfer Resource Index (XferRscIdx). The internal hardware transfer resource index assigned to this transfer. This index must be used in all Update Transfer and End Transfer commands.

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15:12	R/W	0x0	CMDSTS Command Completion Status Additional information about the completion of this command is available in this field. Within an XferNotReady event: • [15]: Indicates the reason why the XferNotReady event is generated: - 1'b0: XferNotActive: Host initiated a transfer, but the requested transfer is not present in the hardware - 1'b1: XferActive: Host initiated a transfer, the transfer is present, but no valid TRBs are available • [14]: Not Used • [13:12]: For control endpoints, indicates what stage was requested when the transfer was not ready: - 2'b00: SETUP Request - 2'b01: Control Data Request - 2'b10: Control Status Request Within an XferComplete or XferInProgress event: • [15]: LST bit of the completed TRB (XferComplete only) • [15]: MissedIsoc: Indicates the interval did not complete successfully (XferInProgress only) • [14]: IOC bit of the TRB that completed • [13]: Indicates the TRB completed with a short packet reception or the last packet of an isochronous interval • [12]: Indicates a Bus Error occurred If the host aborted the data stage or an isochronous time passed condition occurred, the EventStatus bits may all be '0', with the reason for the transfer completion reflected in the TRB Status field. Within a Stream Event: • [15:12]: - 4'h2: StreamNotFound: This stream event is issued when the stream-capable endpoint performed a search in its transfer resource cache, but could not find an active and ready stream. - 4'h1: StreamFound: This stream event is issued when the stream-capable endpoint found an active and ready stream in its transfer resource cache, and initiated traffic for that stream to the host. The ID of the selected Stream is in the EventParam field. In response to a Start Transfer command: • [15:12]:

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Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
			- 4'h2: Indicates expiry of the bus time reflected in the Start Transfer command. - 4'h1: Indicates there is no transfer resource available on the endpoint. In response to a Set Transfer Resource (DEPXFERCFG) command: • [15:12]: - 4'h1: Indicates an error has occurred because software is requesting more transfer resources to be assigned than have been configured in the hardware.
11	R/W	0x0	ForceRM ForceRM: Only valid for End Transfer command ClearPendIN: Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued. Only valid for Clear Stall command Only applicable for SS and ESS mode of operation
10	R/W	0x0	CMDACT Command Active Software sets this bit to '1' to enable the device endpoint controller to execute the generic command. The device controller clears this bit to '0' when the CMDSTS field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	/	/	/
8	R/W	0x0	CMDIOC Command Interrupt on Complete When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command.
7:4	/	/	/

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Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	CMDTYP Command Type Specifies the type of command the software driver is requesting the core to perform. 0x0: Reserved 0x1: Set Endpoint Configuration, 64-bit Parameter 0x2: Set Endpoint Transfer Resource Configuration, 32-bit Parameter 0x3: Get Endpoint State, No Parameter Needed 0x4: Set Stall, No Parameter Needed 0x5: Clear Stall, No Parameter Needed 0x6: Start Transfer, 64-bit parameter 0x7: Update Transfer, No Parameter Needed 0x8: End Transfer, No Parameter Needed 0x9: Start New Configuration, No Parameter Needed

8.12.7.14 0xCA00 Device Interrupt Moderation Register (Default Value:0x0000_0000)

Offset: 0xCA00			Register Name: DEPIMOD
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	DEVICE_IMODC Interrupt Moderation Down Counter Loaded with the DEVICE_IMODI value, whenever the hardware interrupt(n) line is de-asserted from the asserted state, counts down to 0, and stops. The interrupt(n) is signaled whenever this counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events (that is, event count is non-zero). This counter may be directly written by software at any time to alter the interrupt rate.
15:0	R/W	0x0	DEVICE_IMODI Moderation Interval (DEVICE_IMODI) This field holds the minimum inter-interrupt interval between events. The interval is specified in terms of 250ns increments. A value of 0 disables the interrupt throttling logic and interrupts are generated immediately if event count becomes non-zero. In scaledown simulation mode, 4 ram clocks are used to time 250ns

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8.12.8 Application Register Description

8.12.8.1 0x100000 USB2.0 Interface Status and Control Register (Default Value: 0x0000_0000)

Offset: 0x100000			Register Name:USB2_ISCR
Bit	Read/Write	Default/Hex	Description
31:27	R	0	BC_ID_Value_Status These fields indicate the Mult ID value.
26:25	R	0	USB Line Status [26]-DM [27]-DP
24	R	0	USB VBUS Status These filed indicate the VBUS status.
23:18	R/W	0	Forcerid 1xxxxx: Force the ID value of bit[22:18] output to SIE 0xxxxx: Select phy output the ID value to SIE
17:16	/	/	/
15:14	R/W	0	Force ID 0x: use external ID Status 10: force ID to LOW 11: force ID to HIGH
13:12	R/W	0	Force VBUS Valid (For SIE) 0x: use external VBUS Valid Status from VBUS Input or Line State 10: force VBUS Valid to LOW 11: force VBUS Valid to HIGH
11:10	R/W	0	External VBUS Valid Source Select 0x: External VBUS Valid detected from VBUS Input 10: External VBUS Valid detected from DP/DM Input 11: External VBUS Valid detected from either VBUS or DP/DM input
9	R/W	0	USB Wakeup Enable 0: Disable 1: Enable
8	R/W	0	USB Wakeup HOSC Enable 0: Disable 1: Enable
7	R/W1C	0	USB ID Mult Value Change Interrupt Status 0 :No Change 1: Has Change

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Offset: 0x100000			Register Name:USB2_ISCR
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0	VBUS Input Change Detect Interrupt Status 0 :No Change 1: Has Change
5	R/W1C	0	ID Input Change Detect Interrupt Status 0 :No Change 1: Has Change
4	R/W1C	0	DP/DM Input Change Detect Interrupt Status 0 :No Change 1: Has Change
3	R/W	0	USB ID Mult Value Detect Enable 0 :Disable 1: Enable
2	R/W	0	VBUS Input Change Detect Interrupt Enable 0: Disable 1: Enable
1	R/W	0	ID Input Change Detect Interrupt Enable 0: Disable 1: Enable
0	R/W	0	DP/DM Input Change Detect Interrupt Enable 0: Disable 1: Enable

8.12.8.2 0x100010 USB2.0 PHY Control Register (Default Value: 0x0000_0018)

Offset: 0x100010			Register Name: USB2_PHYCTL
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
10	R/W	0x0	OTGDISABLE
9	R/W	0x0	DRVVBUS
8	R/W	0x0	VREGBYPASS
7	R/W	0x0	LOOPBACKENB
6	R/W	0x0	IDPULLUP
5	R/W	0x0	VBUSVLDEXT
4	R/W	0x1	VBUSVLDEXTSEL
3	R/W	0x1	SIDDQ
2	R/W	0x0	COMMONONN
1:0	R/W	0x0	VATESTENB

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8.12.8.3 0x100014 USB2.0 PHY TEST Register (Default Value: 0x0000_0000)

Offset: 0x100014			Register Name: USB2_PHYTST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR[3:0]
7:0	R/W	0x0	TESTDATAIN[7:0]

8.12.8.4 0x100018 USB2.0 PHY Tune Register (Default Value: 0x05B3_33D4)

Offset: 0x100018			Register Name: USB2_PHYTUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.12.8.5 0x100024 USB2.0 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x100024			Register Name: USB2_PHYSTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	TESTDATAOUT[3:0]

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8.13 PCIe2.1

8.13.1 Overview

The PCI Express Controller (PCIe) is a general purpose I/O interconnect, which provides low pin count, high reliability, and high-speed data transfer at rates of up to 5.0 Gbit/s per lane per direction.

The PCIe controller includes the following features:

- Compliance to PCI Express Base Specification, Revision 2.1
- Supports Gen1(2.5 Gbit/s), Gen2 (5.0 Gbit/s) speed
- Supports 62.5MHz/125 MHz operation on PIPE interface for Gen1/Gen2, respectively
- Constant 32-bit PIPE width for Gen1/Gen2 modes
- Supports Root Complex (RC) mode
- Supports 1 lane link width
- Eight Traffic Classes (TC)
- Maximum payload size of 1K bytes
- 8 inbound and 8 outbound address translation regions
- 4 write/read channels for embedded DMA
- Maximum number of non-posted outstanding transactions: 32
- Supports Active State Power Management (ASPM)
- Support Advanced Error Reporting (AER)
- Support MSI interrupt

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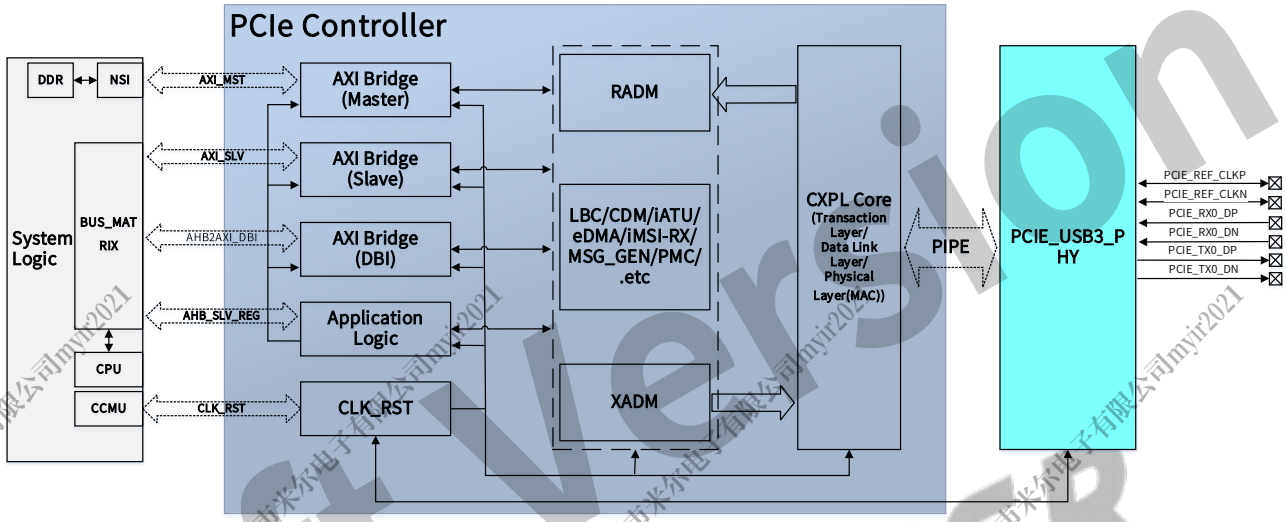
8.13.2 Block Diagram

The following figure shows the functional block diagram of the PCIe.

Figure 8-56 PCIe Block Diagram



The PCIe controller contains the following modules:

Table 8-36 PCIe Module

Module	Description
Common Express Port Logic (CXPL)	This module implements the basic functionality for the PCI Express physical, link, and transaction layers. The CXPL implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The CXPL connects to the external PHY through the PIPE.
Transmit Application-Dependent Module (XADM)	This module implements the application-specific functionality of the PCI Express transaction layer for packet transmission. Its functions include: ● TLP Arbitration ● TLP Formation ● Flow Control (FC) Credit checking The transmit path uses a cut-through architecture. It does not implement transmit buffering/queues (other than the retry buffer). The controller maintains an internal Target Completion Lookup Table to store certain TLP header information from the Rx request. Your application can use this information for transmitting completions.

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Module	Description
Receive Application-Dependent Module (RADM)	This module implements application-specific functionality of the PCI Express transaction layer for packet reception. Its functions include: ● Sorting/filtering of received TLPs. The filtering rules and routing are configurable. ● Buffering and queuing of the received TLPs. ● Routing of received TLP to the controller's receive interfaces. The RADM maintains a Receive Completion Lookup Table (LUT) for completion tracking and completion-timeout monitoring of Tx non-posted requests. It indicates a timeout when an expected Rx completion does not arrive within the timeout period.
Configuration-Dependent Module (CDM)	This module implements: ● Standard PCI Express configuration space ● Controller-specific register space (Port Logic Registers)
Power Management Controller (PMC)	This module implements the power management features of the PCIe controller.
Local Bus Controller (LBC) and Data Bus Interface (DBI)	The LBC module provides a mechanism for a link partner (in EP mode only) or a local CPU (through the DBI) to access: ● Internal registers (in the CDM) ● External application registers connected externally to the ELBI
Message Generation Module (MSG_GEN)	This module transmits messages generated by the controller.
Integrated MSI Receiver (iMSI-RX)	The AXI bridge provides an integrated MSI reception module to detect and terminate inbound MSI requests(received on the RX wire).
Embedded DMA (eDMA)	The RC system CPU, or the EP application CPU, can offload the transferring of large blocks of data to the embedded DMA controller1, leaving the CPU free to perform other tasks. You can configure the DMA to have one to eight read channels and one to eight write channels.
Internal Address Translation Unit (iATU)	The PCIe controller uses the iATU to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

8.13.3 Functional Description

8.13.3.1 External Signals

The following table describes the external signals of the PCIe.

Table 8-37 PCIe External Signals

Signal Name	Description	Type
PCIE-REF-CLKP	PCIe2.1 Differential Signal REFCLK (Positive)	A I/O
PCIE-REF-CLKN	PCIe2.1 Differential Signal REFCLK (Negative)	A I/O

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Signal Name	Description	Type
PCIE-REXT	PCIe2.1 External Reference Resistor	AO
PCIE-RX0-DP	PCIe2.1 Differential Signal of RX (Positive)	A I
PCIE-RX0-DN	PCIe2.1 Differential Signal of RX (Negative)	A I
PCIE-TX0-DP	PCIe2.1 Differential Signal of TX (Positive)	A O
PCIE-TX0-DN	PCIe2.1 Differential Signal of TX (Negative)	A O
PCIE0-PERSTN	PCIe2.1 Warm Reset	O
PCIE0-WAKEN	PCIe2.1 Wake Up	I
PCIE0-CLKREQN	PCIe2.1 Clock Request from PCIe Peripheral	I
VCC18-PCIE	1.8 V Power Supply for PCIe2.1	P
VDD09-PCIE	0.9 V Power Supply for PCIe2.1	P

8.13.3.2 Clock Sources

The following table describes the clock sources of the PCIe.

Table 8-38 PCIe Clock Sources

Clock Sources	Description	Module
USB3_PCIE_REF_CLK	24 MHz, USB3.1 DRD&Pcie2.1 PHY reference clock.	CCU
AUX_CLK	24 MHz, working clock in low power mode of the PCIe.	
MBUS_CLK	600 MHz, PCIe AXI master/slave bus clock.	
AHB_CLK	200 MHz, PCIe bus clock.	
PIPE_CLK	62.5 MHz/ 125MHz, normal working clock for the PCIe controller operating in Gen1/Gen2 mode.	

8.13.3.3 PCIe Reference Clock

PCIe reference clock is a 100 MHz differential clock supplied for the PCIe PHY. It has two clock sources.

- From Internal SoC

Configure PHY to use internal clock and enable the clock output via software. The REFCLKP/REFCLKN signal of PCIe controller serves as output signal and provides 100M differential clock for external EP.

- From External Clock Generator

Configure PHY to use external clock and disable the clock output via software. The REFCLKP/REFCLKN signal of PCIe controller serves as input signal and the external clock generator provides 100M differential clock for the PCIe PHY.

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8.13.3.4 PCIe Memory Mapping

The address space of PCIe controller can be partitioned into three spaces.

- Core Configuration Space (CCS): The configuration register space of the PCIe controller itself. It is also the standartd configuration register space defined by the PCIe specification.
- User Defined Space (UDS): The custom register space for the PCIe controller itself.
- Slave Command Space (SCS): Address space for configuraion transaction and memory transaction. The read and write operations in this space will be transformed into configuration read and write transactions or memory read and write transactions in the PCIe domain by the PCIe controller. The PCIe command space segmentation is 0x20000000-0x2FFFFFFF.

8.13.3.5 ATU Operation

ATU is an address translation unit in PCIe controller and is used for transaction transformation and address translation. There are two types of ATU: Outbound ATU and Inbound ATU.

Outbound ATU

Outbound ATU is used to transform the read/write operation in the CPU domain of the original address space into the read/write transaction in the PCIe domain of the target address space. If the Outbound ATU is used, the original address in the CPU domain will be translated into another different address in the PCIe domain. If the Outbound ATU is not used, the PCIe controller will not perform address translation. The read/write operation initiated in the CPU domain will be transformed into the read/write transaction at the same address in the PCIe domain.

The following shows an example:

- When Outbound ATU is used, set address Region N in the CPU domain to be translated into Region K in PCIe domain. The read/write operation initiated at address Region N (CPU domain) will be transformed into the read/write transaction at address Region K (PCIe domain).
- When Outbound ATU is not used, read/write operation initiated at address Region N (CPU domain) will be transformed into the read/write transaction at address Region N (PCIe domain).

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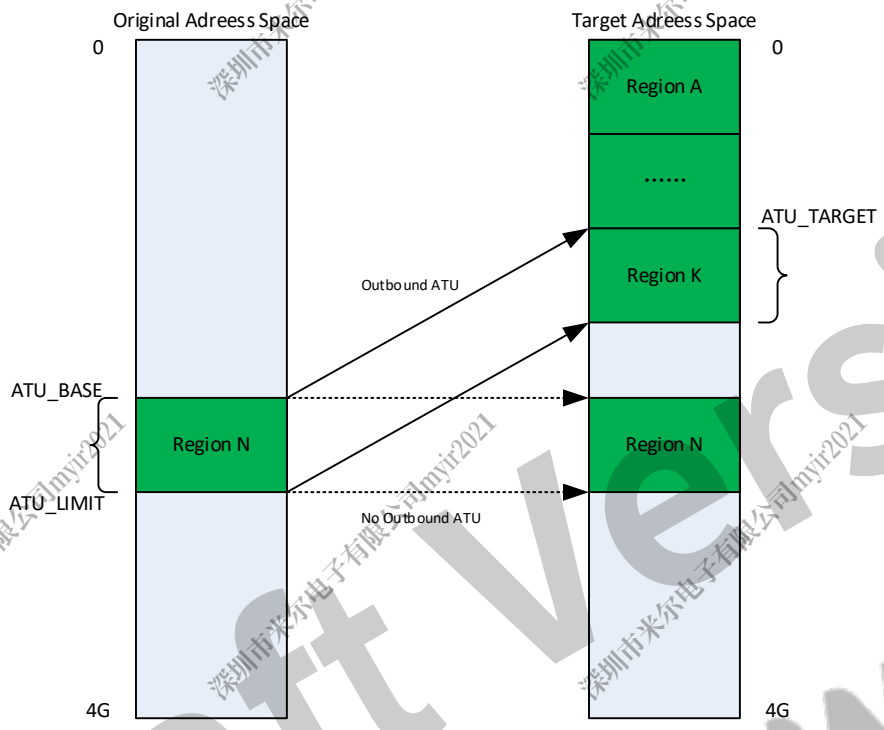
Figure 8-57 Outbound ATU



Inbound ATU

Inbound ATU is used to transform the read/write transaction in the PCIe domain of the original address space into the read/write operation in the CPU domain of the target address space. If Inbound ATU is used, the original address in the PCIe domain will be translated into another different address in the CPU domain. If the Inbound ATU is not used, the PCIe controller will not perform address translation. The read/write transaction initiated in the PCIe domain will be transformed into the read/write operation at the same address in the CPU domain.

The following shows an example:

- When Inbound ATU is used, set address Region N in the PCIe domain to be translated into Region K in the CPU domain. The read/write transaction initiated at address Region N (PCIe domain) will be transformed into the read/write operation at address Region K (CPU domain).
- When Inbound ATU is not used, read/write transaction initiated at address Region N (PCIe domain) will be transformed into the read/write operation at address Region N (CPU domain).

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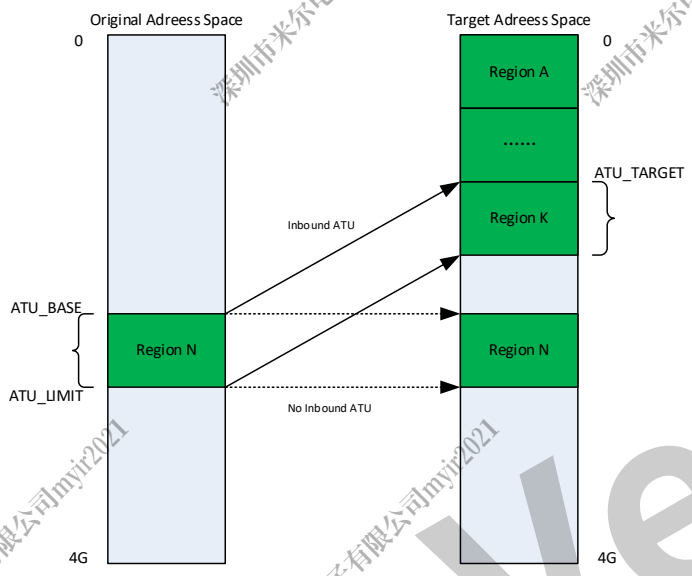
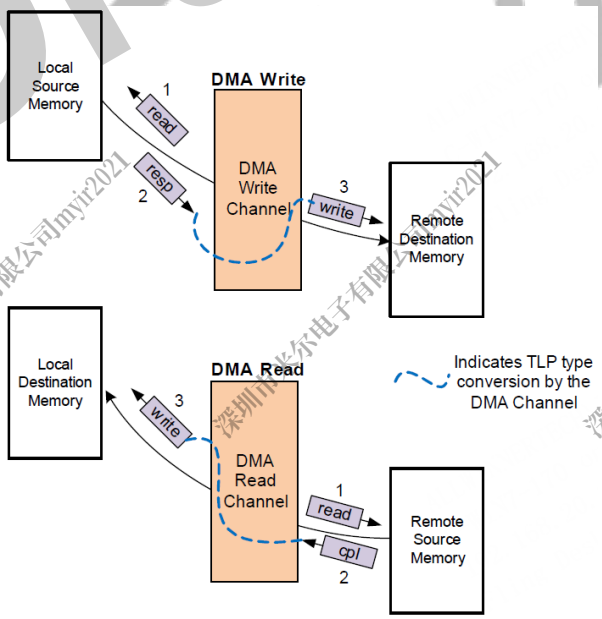
Figure 8-58 Inbound ATU



8.13.3.6 DMA Operation

There is a private DMA with read channels and write channels in the PCIe controller. The following figure deiscribes the DMA write and read process.

Figure 8-59 DMA Operation



- DMA Write Channel

  the DMA write channel is used for data transfer from local bus address space to the address space in the PCIe domain. First, DMA controller reads data from the local bus address space and writes them to the address space in the CPU domain. Then, the PCIe controller transforms the write operation initiated by DMA into a write transaction in the PCIe domain and writes data to the destination address space in the PCIe domain.

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- DMA Read Channel

  The DMA read channel is used for data transfer from the address space in the PCIe domain to the local bus address space such as DRAM address space. If a read operation is initiated by DMA in the original address space of the CPU domain, the PCIe controller will transform the read operation into a read transaction in the PCIe domain and write data to the local bus address space.

8.13.3.7 MSI Operation

Message Signaled Interrupt (MSI) is a kind of mechanism that Endpoints send interrupt requests to the CPU connected with the Root Complex, which uses memory write transaction. The transaction message for transmitting interrupt information is MSI message.

Assume an Endpoint needs to send a MSI interrupt request to CPU. First, the Endpoint needs to initiate a memory write transaction in MSI address of PCIe domain, which will be transformed into a MSI interrupt signal to CPU by the PCIe controller after the transaction is detected. Software obtains the Endpoint sending interrupt request and its interrrupt vector according to the MSI message.

8.13.4 Register List

Module Name	Base Address
PCIE	0x04800000

Register Class	Offset
User Defined Registers	0x00400000 - 0x0047FFFF

Register Name	Offset	Description
MSTR_AWMISC_INFO_0	0x0100	PCIE AXI Master Write Misc Information Register0
MSTR_AWMISC_INFO_1	0x0104	PCIE AXI Master Write Misc Information Register1
MSTR_AWMISC_INFO_HDR_34DW_0	0x0108	PCIE AXI Master Write Misc Information Header Register0
MSTR_AWMISC_INFO_HDR_34DW_1	0x010C	PCIE AXI Master Write Misc Information Header Register1
MSTR_AWMISC_INFO_OTHER	0x0110	PCIE AXI Master Write Misc Information Other Register
MSTR_ARMISC_INFO_0	0x0120	PCIE AXI Master Read Misc Information Register0
MSTR_ARMISC_INFO_1	0x0124	PCIE AXI Master Read Misc Information Register1
MSTR_ARMISC_INFO_OTHER	0x0130	PCIE AXI Master Read Misc Information Other Register
MSTR_BMISC_INFO	0x0150	PCIE AXI Master Write Response Misc Information Register

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Register Name	Offset	Description
MSTR_RMISC_INFO	0x0160	PCIE AXI Master Read Misc Information Register
PCIE_SLV_AWMISC_CTRL	0x0200	PCIE Write Transaction Control Register
SLV_AWMISC_INFO_ATU_BYP	0x0204	PCIE AXI SLAVE Write Misc Information ATU Register
SLV_AWMISC_INFO_HDR_34DW_0	0x0208	PCIE AXI SLAVE Write Misc Information Header Register0
SLV_AWMISC_INFO_HDR_34DW_1	0x020C	PCIE AXI SLAVE Write Misc Information Header Register1
SLV_AWMISC_INFO_OTHER_0	0x0210	PCIE AXI SLAVE Write Misc Information Other Register0
SLV_AWMISC_INFO_OTHER_1	0x0214	PCIE AXI SLAVE Write Misc Information Other Register1
SLV_ARMISC_CTRL	0x0220	PCIE AXI SLAVE Read Control Register
SLV_ARMISC_INFO_ATU_BYP	0x0224	PCIE AXI SLAVE Read Misc Information ATU Register
SLV_ARMISC_INFO_OTHER	0x0230	PCIE AXI SLAVE Read Misc Information Other Register
SLV_BMISC_INFO	0x0250	PCIE AXI Slave Write Response Misc Information Register
SLV_RMISC_INFO	0x0260	PCIE AXI Slave Read Response Misc Information Register
APP_CLK_REQ_N	0x0400	PCIE APP Clock Request Register
APP_INIT_RST	0x0500	PCIE APP Initial Reset Register
VEN_MSG_REQ	0x0700	PCIE VEN MSG Request Register
VEN_MSG_CFG_0	0x0704	PCIE VEN MSG Config Register0
VEN_MSG_CFG_1	0x0708	PCIE VEN MSG Config Register1
VEN_MSG_DATA_0	0x070C	PCIE VEN MSG Data Register0
VEN_MSG_DATA_1	0x0710	PCIE VEN MSG Data Register1
SII_ELEC	0x0A00	PCIE SII Electromechanical Register
FRS_READY	0x0B04	PCIE FRS READY Register
PCIE_LTSSM_ENABLE	0x0C00	PCIE LTSSM Enable Register
SII_INT_MASK_0	0x0E00	PCIE SII Interrupt Mask Register0
SII_INT_MASK_1	0x0E04	PCIE SII Interrupt Mask Register1
SII_INT_0	0x0E08	PCIE SII Interrupt Register0
SII_INT_1	0x0E0C	PCIE SII Interrupt Register1
SII_APP_PM_UNLOCK	0x1000	PCIE SII APP PM UNLOCK Register
SII_APP_PM_0	0x1100	PCIE SII Power Manage Register0

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8.13.5 Register Description

8.13.5.1 0x0100 PCIE AXI Master Write Misc Information Register0 (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: MSTR_AWMISC_INFO_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_0 AXI Master Write Misc Information. AXI master write transaction associated miscellaneous information from the TLP received by the native PCIe controller. This is a signal that the application can optionally use. It is not part of the standard AXI interface. • Bus number, device number, function number, and register numbers are overlaid to the address bus when type is configuration transactions. • Message contents are also overlaid to the address bus for MSG TLPs. Bits [7:0] indicate the message code when the type is message. The bit fields are mapped as follows: • [7:0]: Reserved except for MSG TLP. Bits [7:0] indicate the message code when the type is message. • [8:6]: BAR number of TLP • [9]: TLP is an I/O • [10]: TLP is in ROM range • [13:11]: TLP's Function number. Function numbering starts at '0'. This field is not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. • [14]: TLP's NS bit • [15]: TLP's RO bit • [18:16]: TLP's TC bits • [23:19]: TLP's TYPE • 31:24]: TLP's requester ID_0

8.13.5.2 0x0104 PCIE AXI Master Write Misc Information Register1 (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: MSTR_AWMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0104			Register Name: MSTR_AWMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0	MSTR_AWMISC_INFO_1 AXI Master Write Misc Information. AXI master write transaction associated miscellaneous information from the TLP received by the native PCIe controller. This is a signal that the application can optionally use. It is not part of the standard AXI interface. • Bus number, device number, function number, and register numbers are overlaid to the address bus when type is configuration transactions. • Message contents are also overlaid to the address bus for MSG TLPs. Bits [7:0] indicate the message code when the type is message. The bit fields are mapped as follows: [8:0]: TLP's requester ID_1 [15:9]: TLP's TAG

8.13.5.3 0x0108 PCIE AXI Master Write Misc Information Header Register0 (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: MSTR_AWMISC_INFO_HDR_34DW_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_HDR_34DW_0 mstr_awmisc_info_hdr_34dw_status[31:0]

8.13.5.4 0x010C PCIE AXI Master Write Misc Information Header Register1 (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: MSTR_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_HDR_34DW_1 mstr_awmisc_info_hdr_34dw_status[63:32]

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8.13.5.5 0x0110 PCIE AXI Master Write Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: MSTR_AWMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	MSTR_AWMISC_INFO_LAST_DCMP_TLP mstr_awmisc_info_last_dcmp_tlp_status
26	R	0x0	MSTR_AWMISC_INFO_EP mstr_awmisc_info_ep_status
25	R	0x0	MSTR_AWMISC_INFO_NW mstr_awmisc_info_nw_status
24	R	0x0	MSTR_AWMISC_INFO_IDO mstr_awmisc_info_ido_status
23:22	R	0x0	MSTR_AWMISC_INFO_ATS mstr_awmisc_info_ats_status[1:0]
21:16	R	0x0	MSTR_AWMISC_INFO_DMA mstr_awmisc_info_dma_status[5:0]
15:11	/	/	/
10:0	R	0x0	MSTR_AWMISC_INFO_TPH mstr_awmisc_info_tph_status[10:0]

8.13.5.6 0x0120 PCIE AXI Master Read Misc Information Register0 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: MSTR_ARMISC_INFO_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_ARMISC_INFO_0 mstr_armisc_info_status[31:0]

8.13.5.7 0x0124 PCIE AXI Master Read Misc Information Register1 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: MSTR_ARMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	MSTR_ARMISC_INFO_1 mstr_armisc_info_status[47:32]

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8.13.5.8 0x0130 PCIE AXI Master Read Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: MSTR_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	MSTR_ARMISC_INFO_ZEROREAD mstr_armisc_info_zeroread_status
27	R	0x0	MSTR_ARMISC_INFO_LAST_DCMP_TLP mstr_armisc_info_last_dcmp_tlp_status
26	/	/	/
25	R	0x0	MSTR_ARMISC_INFO_NW mstr_armisc_info_nw_status
24	R	0x0	MSTR_ARMISC_INFO_IDO mstr_armisc_info_ido_status
23:22	/	/	/
21:16	R	0x0	MSTR_ARMISC_INFO_DMA mstr_armisc_info_dma_status[5:0]
15:11	/	/	/
10:0	R	0x0	MSTR_ARMISC_INFO_TPH mstr_armisc_info_tph_status[10:0]

8.13.5.9 0x0150 PCIE AXI Master Write Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: MSTR_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSTR_BMISC_INFO_CPL_STAT AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. ▪ 00: SC (Successful Completion) ▪ 01: CA (Completer Abort) ▪ 10: UR (Unsupported Request) ▪ 11: SC (Successful Completion) Your application must drive the same value on mstr_bmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_bmisc_info_cpl_stat to UR:

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Offset: 0x0150			Register Name: MSTR_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
			▪ If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. ▪ If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.

8.13.5.10 0x0160 PCIE AXI Master Read Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: MSTR_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x0	MSTR_RMISC_INFO_CPL_STAT AXI Master Read Response selection bus. This bus controls the response sent on the PCIe wire in the case of successful read requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. ▪ 00: SC (Successful Completion) ▪ 01: CA (Completer Abort) ▪ 10: UR (Unsupported Request) ▪ 11: SC (Successful Completion) Your application must drive the same value on mstr_rmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_rmisc_info_cpl_stat to UR: ▪ If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. ▪ If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.
15:13	/	/	/

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Offset: 0x0160			Register Name: MSTR_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
12:0	R/W	0x0	MSTR_RMISC_INFO AXI Master Read Response Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of standard AXI interface. All reserved bits must be connected to logic '0'. ▪ [1:0]: Reserved ▪ [2]: Reserved. ▪ [6:3]: Reserved ▪ [7]: TLP's EP bit ▪ [12:8]: Reserved.

8.13.5.11 0x0200 PCIE SLAVE Write Msic Control Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PCIE_SLV_AWMISC_CTRL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	AXI transaction is a DBI access. This is for SHARED DBI mode only.
20:13	R/W	0x00	MSG TLP’ s MSG Code
12:10	R/W	0x0	TC TLP’ s TC bits
9	R/W	0x0	RO TLP’ s RO bit
8	R/W	0x0	NS TLP’ s NS bit
7	/	/	/
6	R/W	0x0	EP TLP’ s EP bit
5	R/W	0x0	SERIALIZE_NP_REQ Serialize NP Requests
4:0	R/W	0x0	TYPE TLP’ s TYPE

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8.13.5.12 0x0204 PCIE AXI SLAVE Write Misc Information ATU Register (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: SLV_AWMISC_INFO_ATU_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_AWMISC_INFO_ATU_BYPASS AXI Slave Write Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit

8.13.5.13 0x0208 PCIE AXI SLAVE Write Misc Information Header Register0 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: SLV_AWMISC_INFO_HDR_34DW_0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SLV_AWMISC_INFO_HDR_34DW_0 slv_awmisc_info_hdr_34dw[31:0] ,AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. **Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.**

8.13.5.14 0x020C PCIE AXI SLAVE Write Misc Information Header Register1 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: SLV_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SLV_AWMISC_INFO_HDR_34DW_1 slv_awmisc_info_atu_bypass[63:32] ,AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. **Note: The data is in big endian format.**

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8.13.5.15 0x0210 PCIE AXI SLAVE Write Misc Information Other Register0 (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: SLV_AWMISC_INFO_OTHER_0
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	SLV_AWMISC_INFO_NW AXI Slave Write Transaction's Request ATS No Write (NW) Bit. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
24	R/W	0x0	SLV_AWMISC_INFO_IDO AXI Slave Write Transaction's IDO bit. Enables ID-base ordering on outbound requests. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
23:11	/	/	/
10:0	R/W	0x0	SLV_AWMISC_INFO_TPH AXI Slave Write Request TLP Processing Hints. The bits are mapped as follows: ▪ [0]: TH (TLP Processing Hint present) ▪ [2:1] PH (TLP Processing Hint) ▪ [10:3] ST (Steering Tag)

8.13.5.16 0x0214 PCIE AXI SLAVE Write Misc Information Other Register1 (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: SLV_AWMISC_INFO_OTHER_1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLV_AWMISC_INFO_P_TAG AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your application normally sets this to '0' except when generating ATS invalidate requests.

8.13.5.17 0x0220 PCIE AXI SLAVE Read Control Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: SLV_ARMISC_CTRL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

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Offset: 0x0220			Register Name: SLV_ARMISC_CTRL
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	AXI transaction is a DBI access. This is for SHARED DBI mode only.
20:13	R/W	0x00	MSG TLP’s MSG Code
12:10	R/W	0x0	TC TLP’s TC bits
9	R/W	0x0	RO TLP’s RO bit
8	R/W	0x0	NS TLP’s NS bit
7	/	/	/
6	R/W	0x0	EP TLP’s EP bit
5	/	/	/
4:0	R/W	0x0	TYPE TLP’s TYPE

8.13.5.18 0x0224 PCIE AXI SLAVE Read Misc Information ATU Register (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: SLV_ARMISC_INFO_ATU_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_ARMISC_INFO_ATU_BYPASS AXI Slave Read Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit

8.13.5.19 0x0230 PCIE AXI SLAVE Read Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: SLV_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	SLV_ARMISC_INFO_NW AXI Slave Read Transaction's Request AT No Write (NW) Bit. This is a signal that the application can optionally use. It is not part of the standard AXI interface.

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Offset: 0x0230			Register Name: SLV_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	SLV_ARMISC_INFO_IDO AXI Slave Read Transaction's IDO bit. Enables ID-base ordering on outbound requests. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
23:11	/	/	/
10:0	R/W	0x0	SLV_ARMISC_INFO_TPH AXI Slave Read Request TLP Processing Hints. The bits are mapped as follows: ▪ [0]: TH (TLP Processing Hint present) ▪ [2:1] PH (TLP Processing Hint) ▪ [10:3] ST (Steering Tag)

8.13.5.20 0x0250 PCIE AXI Slave Write Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: SLV_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	SLV_BMISC_INFO_STATUS slv_bmisc_info_status

8.13.5.21 0x0260 PCIE AXI Slave Read Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: SLV_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R	0x0	SLV_RMISC_INFO_IDO_STATUS slv_rmisc_info_ido_status
23:11	/	/	/
10:0	R	0x0	MSTR_RMISC_INFO mstr_rmisc_info

8.13.5.22 0x0400 PCIE APP Clock Request Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: APP_CLK_REQ_N
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0400			Register Name: APP_CLK_REQ_N
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	APP_CLK_REQ_N Indicates that the application logic is ready to have reference clock removed. In designs which support reference clock removal through either L1 PM Sub-states or L1 CPM, the application should set this signal to 1'b when it is ready to have reference clock removed. If the application does not want to remove reference clock it should set this signal to 1'b0.

8.13.5.23 0x0500 PCIE APP Initial Reset Register (Default Value: 0x0000_0000)

Offset: 0x0500			Register Name: APP_INIT_RST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	APP_INIT_RST app_init_rst_ahb Request from your application to send a hot reset to the upstream port. The hot reset request is sent when a single cycle pulse is applied to this pin. In an upstream port, you should set this input to '0'. Note: This signal is not used by the controller to set the SBR field in the BRIDGE_CTRL_INT_PIN_INT_LINE_REG register. During the transition from DL_Active to DL_inactive, assertion of app_init_rst signal indicates a Surprise Down Error, but setting of SBR field in the BRIDGE_CTRL_INT_PIN_INT_LINE_REG register through DBI does not trigger a Surprise Down Error.

8.13.5.24 0x0700 PCIE VEN MSG Request Register (Default Value: 0x0000_0000)

Offset: 0x0700			Register Name: VEN_MSG_REQ
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	VEN_MSG_REQ ven_msG_req_ahb, Request from your application to send a vendor-defined Message. Once asserted, ven_msg_req must remain asserted until the controller asserts ven_msg_grant.

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8.13.5.25 0x0704 PCIE VEN MSG Config Register0 (Default Value: 0x0000_0000)

Offset: 0x0704			Register Name: VEN_MSG_CFG_0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	VEN_MSG_CODE The Message Code for the vendor-defined Message TLP.
23:16	/	/	/
15:13	R/W	0x0	VEN_MSG_ATTR The Attributes field for the vendor-defined Message TLP. ▪ Width is three bits when CX_IDO_ENABLE =1 ▪ Width is two bits when CX_IDO_ENABLE =0
12:8	R/W	0x0	VEN_MSG_TYPE The Type field for the vendor-defined Message TLP.
7:6	R/W	0x0	VEN_MSG_FMT The Format field for the vendor-defined Message TLP. Should be set to 0x1.
5:3	R/W	0x0	VEN_MSG_TC The Traffic Class field for the vendor-defined Message TLP.
2	R/W	0x0	VEN_MSG_TD The TLP Digest (TD) bit for the vendor-defined Message TLP, valid when ven_msg_req is asserted.
1	R/W	0x0	VEN_MSG_EP The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
0	/	/	/

8.13.5.26 0x0708 PCIE VEN MSG Config Register1 (Default Value: 0x0000_0000)

Offset: 0x0708			Register Name: VEN_MSG_CFG_1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	VEN_MSG_TAG Tag for the vendor-defined Message TLP.
15:13	/	/	/
12:10	R/W	0x0	VEN_MSG_FUNC_NUM Function Number for the vendor-defined Message TLP. Function numbering starts at '0'.

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Offset: 0x0708			Register Name: VEN_MSG_CFG_1
Bit	Read/Write	Default/Hex	Description
9:0	R/W	0x0	VEN_MSG_LEN The Length field for the vendor-defined Message TLP (indicates length of data payload in dwords). Should be set to 0x0.

8.13.5.27 0x070C PCIE VEN MSG Data Register0 (Default Value: 0x0000_0000)

Offset: 0x070c			Register Name: VEN_MSG_DATA_0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VEN_MSG_DATA_0 fourth dwords of the Vendor Defined Message header where: ▪ Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15

8.13.5.28 0x0710 PCIE VEN MSG Data Register1 (Default Value: 0x0000_0000)

Offset: 0x0710			Register Name: VEN_MSG_DATA_1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VEN_MSG_DATA_1 third dwords of the Vendor Defined Message header where: ▪ Bytes 8-11 (third header dword) =ven_msg_data[63:32]

8.13.5.29 0x0A00 PCIE SII Electromechanical Register (Default Value: 0x0000_0000)

Offset: 0x0A00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	SYS_EML_INTERLOCK_ENGAGED sys_eml_interlock_engaged [0] , System Electromechanical Interlock Engaged. Indicates whether the system electromechanical interlock is engaged and controls the state of the Electromechanical Interlock Status bit in the Slot Status register.

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Offset: 0x0A00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	SYS_CMD_CPLED_INT sys_cmd_cpled_int[0] , Command completed Interrupt. Indicates that the Hot-Plug controller completed a command. There is a separate sys_cmd_cpled_int input bit for each function in your controller configuration
5	R/W	0x0	SYS_PRE_DET_CHGED sys_pre_det_chged[0] Presence Detect Changed. Indicates that the state of card present detector has changed. There is a separate sys_pre_det_chged input bit for each function in your controller configuration.
4	R/W	0x0	SYS_MRL_SENSOR_CHGED sys_mrl_sensor_chged[0] , MRL Sensor Changed. Indicates that the state of MRL sensor has changed. There is a separate sys_mrl_sensor_chged input bit for each function in your controller configuration.
3	R/W	0x0	SYS_PWR_FAULT_DET sys_pwr_fault_det[0] , Power Fault Detected. Indicates the power controller detected a power fault at this slot. There is a separate sys_pwr_fault_det input bit for each function in your controller configuration.
2	R/W	0x0	SYS_MRL_SENSOR_STATE sys_mrl_sensor_state[0] , MRL Sensor State. Indicates the state of the manually-operated retention latch (MRL) sensor: ▪ 0: MRL is closed ▪ 1: MRL is open There is a separate sys_mrl_sensor_state input bit for each function in your controller configuration.
1	R/W	0x0	SYS_PRE_DET_STATE sys_pre_det_state[0] , Presence Detect State. Indicates whether or not a card is present in the slot: ▪ 0: Slot is empty ▪ 1: Card is present in the slot There is a separate sys_pre_det_state input bit for each function in your controller configuration.

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Offset: 0x0A00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SYS_ATTEN_BUTTON_PRESSED sys_atten_button_pressed[0] , Attention Button Pressed. Indicates that the system attention button was pressed, sets the Attention Button Pressed bit in the Slot Status Register. There is a separate sys_atten_button_pressed input bit for each function in your controller configuration.

8.13.5.30 0x0B04 PCIE FRS READY Register (Default Value: 0x0000_0000)

Offset: 0x0B04			Register Name: FRS_READY
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	APP_PF0_FRS_READY app_pf_frs_ready[0] Defers FRS messaging when set to '0'.
3:0	/	/	/

8.13.5.31 0x0C00 PCIE LTSSM Enable Register (Default Value: 0x0000_0040)

Offset: 0x0C00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	APP_DBI_RO_WR_DISABLE app_dbi_ro_wr_disable DBI Read-only Write Disable ▪ 0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. ▪ 1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only.
30:1	/	/	/
0	R/W	0x0	APP_LTSSM_ENABLE Link Training Enable 0: Disable link training 1: Enable link training Driven low by your application after cold, warm or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable

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Offset: 0x0C00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
			to allow the LTSSM to continue link establishment. Can also be used to delay hot resetting of the controller until you have read out any register status. Cold Reset: ▪ Optionally hold LTSSM and delay link training, so that you can reprogram some registers through DBI. ▪ Set app_ltssm_enable =0 before your application de-asserts Power-On Reset (power_up_rst_n). Best way is to set app_ltssm_enable =0 at power-up or at assertion of core_rst_n. ▪ Wait for de-assertion of core_rst_n, sticky_rst_n, and non_sticky_rst_n. ▪ Write any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Link training starts. Hot Reset (Link Down Reset) : ▪ Optionally delay reset of the controller, so that you can read some registers through DBI. ▪ Set app_ltssm_enable =0 immediately (combinatorially) upon falling edge of smlh_req_rst_not. ▪ Keep app_ltssm_enable =0 until bridge finishes "flushing mode". ▪ Read any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Reset of controller begins (sticky_rst is not asserted). ▪ Optionally hold LTSSM and delay link training, so that you can reprogram some registers through DBI. ▪ Set app_ltssm_enable =0 immediately (combinatorially) upon falling edge of core_rst_n. ▪ Write any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Link training starts. ▪ **Note: For Hot Reset, you can do both or either of the above (delay reset and/or delay link training). If you do both, you must do in order presented.** ▪ **Note: You must only de-assert this signal using one of the recommended timings described in**

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Offset: 0x0C00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
			the "Reset Requirements" section in the Architecture chapter of the Databook To do otherwise (that is, de-assert it outside of the Detect LTSSM state) causes the controller to be reset and the LTSSM moves immediately back to the Detect state. This transition is outside of the PCIe Specification and it might cause a PIPE protocol violation.

8.13.5.32 0x0E00 PCIE SII Interrupt Mask Register0 (Default Value: 0x0000_0000)

Offset: 0x0E00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	RADM_MSG_LTR_EN_MASK 0: Mask 1: Not Mask
28	R/W	0x0	DEASSERT_INTD_GRT_EN_MASK 0: Mask 1: Not Mask
27	R/W	0x0	DEASSERT_INTC_GRT_EN_MASK 0: Mask 1: Not Mask
26	R/W	0x0	DEASSERT_INTB_GRT_EN_MASK 0: Mask 1: Not Mask
25	R/W	0x0	DEASSERT_INTA_GRT_EN_MASK 0: Mask 1: Not Mask
24	R/W	0x0	ASSERT_INTD_GRT_EN_MASK 0: Mask 1: Not Mask
23	R/W	0x0	ASSERT_INTC_GRT_EN_MASK 0: Mask 1: Not Mask
22	R/W	0x0	ASSERT_INTB_GRT_EN_MASK 0: Mask 1: Not Mask
21	R/W	0x0	ASSERT_INTA_GRT_EN_MASK 0: Mask 1: Not Mask

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Offset: 0x0E00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	CFG_LINK_EQ_REQ_INT_EN_MASK 0: Mask 1: Not Mask
19	R/W	0x0	CFG_BW_MGT_MSI_EN_MASK 0: Mask 1: Not Mask
18	R/W	0x0	CFG_BW_MGT_INT_EN_MASK 0: Mask 1: Not Mask
17	R/W	0x0	CFG_LINK_AUTO_BW_MSI_EN_MASK 0: Mask 1: Not Mask
16	R/W	0x0	CFG_LINK_AUTO_BW_INT_EN_MASK 0: Mask 1: Not Mask
15	R/W	0x0	PF0_HP_MSI_EN_MASK 0: Mask 1: Not Mask
14	R/W	0x0	PF0_HP_INT_EN_MASK 0: Mask 1: Not Mask
13	R/W	0x0	PF0_HP_PME_EN_MASK 0: Mask 1: Not Mask
12	R/W	0x0	RADM_INTD_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
11	R/W	0x0	RADM_INTC_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
10	R/W	0x0	RADM_INTB_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
9	R/W	0x0	RADM_INTA_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
8	R/W	0x0	RADM_INTD_ASSERTED_EN_MASK 0: Mask 1: Not Mask

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Offset: 0x0E00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	RADM_INTC_ASSERTED_EN_MASK 0: Mask 1: Not Mask
6	R/W	0x0	RADM_INTB_ASSERTED_EN_MASK 0: Mask 1: Not Mask
5	R/W	0x0	RADM_INTA_ASSERTED_EN_MASK 0: Mask 1: Not Mask
4	R/W	0x0	PF0_CFG_PME_MSI_EN_MASK 0: Mask 1: Not Mask
3	R/W	0x0	PF0_CFG_PME_INT_EN_MASK 0: Mask 1: Not Mask
2	R/W	0x0	PF0_CFG_AER_RC_ERR_MSI_MASK 0: Mask 1: Not Mask
1	R/W	0x0	PF0_CFG_AER_RC_ERR_INT_EN_MASK 0: Mask 1: Not Mask
0	R/W	0x0	PF0_CFG_VPD_INT_EN_MASK 0: Mask 1: Not Mask

8.13.5.33 0x0E04 PCIE SII Interrupt Mask Register1 (Default Value: 0x0000_0000)

Offset: 0x0E04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCIE_WAKE_N_CLR_EN_MASK 0: Mask 1: Not Mask
30	R/W	0x0	WAKE_CLR_EN_MASK 0: Mask 1: Not Mask
29	R/W	0x0	RADM_PM_TO_ACK_CLR_EN_MASK 0: Mask 1: Not Mask

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Offset: 0x0E04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	RADM_PM_PME_CLR_EN_MASK 0: Mask 1: Not Mask
27	R/W	0x0	RADM_FATAL_ERR_CLR_EN_MASK 0: Mask 1: Not Mask
26	R/W	0x0	RADM_NONFATAL_ERR_CLR_EN_MASK 0: Mask 1: Not Mask
25	R/W	0x0	RADM_CORRECTABLE_ERR_CLR_EN_MASK 0: Mask 1: Not Mask
24	R/W	0x0	CFG_SYS_ERR_RC_CLR_EN_MASK 0: Mask 1: Not Mask
23:22	/	/	/
21	R/W	0x0	PF0_FRS_GRANT_EN_MASK 0: Mask 1: Not Mask
20	R/W	0x0	RADM_VENDOR_MSG_EN_MASK 0: Mask 1: Not Mask
19	/	/	/
18	R/W	0x0	PF0_FRSQ_MSI_EN_MASK 0: Mask 1: Not Mask
17	R/W	0x0	PF0_CFG_UP_DRS_TO_FRS_EN_MASK 0: Mask 1: Not Mask
16	R/W	0x0	PF0_CFG_DRS_MSI_EN_MASK 0: Mask 1: Not Mask
15:12	/	/	/
11	R/W	0x0	PCIE_PERI_AR_INT_EN_MASK 0: Mask 1: Not Mask
10	R/W	0x0	PCIE_PERI_AW_INT_EN_MASK 0: Mask 1: Not Mask

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Offset: 0x0E04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	RADM_QOVERFLOW_1_EN_MASK 0: Mask 1: Not Mask
8	R/W	0x0	RADM_QOVERFLOW_0_EN_MASK 0: Mask 1: Not Mask
7:5	/	/	/
4	R/W	0x0	RTLH_RFC_UPD_0_EN_MASK 0: Mask 1: Not Mask
3	R/W	0x0	LINK_REQ_RST_NOT_EN_MASK 0: Mask 1: Not Mask
2	/	/	/
1	R/W	0x0	RDLH_LINK_UP_INT_MASK RDLH Link Up Interrupt Mask 0: Mask 1: Not Mask
0	R/W	0x0	SMLH_LINK_UP_INT_MASK SMLH Link Up Interrupt Mask 0: Mask 1: Not Mask

8.13.5.34 0x0E08 PCIE SII Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W1C	0x0	RADM_MSG_LTR One-clock-cycle pulse that indicates that the controller received an LTR message. The controller makes the message header available the radm_msg_payload output. It is also available the app_ltr_latency output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
28	R/W1C	0x0	DEASSERT_INTD_GRT The signal deassert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTD Message to the upstream device.

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
27	R/W1C	0x0	DEASSERT_INTC_GRT The signal deassert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTC Message to the upstream device.
26	R/W1C	0x0	DEASSERT_INTB_GRT The signal deassert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTB Message to the upstream device.
25	R/W1C	0x0	DEASSERT_INTA_GRT The signal deassert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTA Message to the upstream device.
24	R/W1C	0x0	ASSERT_INTD_GRT The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device.
23	R/W1C	0x0	ASSERT_INTC_GRT The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device.
22	R/W1C	0x0	ASSERT_INTB_GRT The signal assert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTB Message to the upstream device.
21	R/W1C	0x0	ASSERT_INTA_GRT The signal assert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTA Message to the upstream device.
20	R/W1C	0x0	CFG_LINK_EQ_REQ_INT Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set.

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
19	R/W1C	0x0	CFG_BW_MGT_MSI The controller sets this pin when following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated ▪ The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. reuse-pragma beginAttr Description This pin is set as a notification when the Link Bandwidth Management Status register (Link Status register bit 14) is updated and the Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set and in addition the msi or msix aare enabled . This bit is not applicable to, and is reserved, for endpoint devices and upstream ports of Switches. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
18	R/W1C	0x0	CFG_BW_MGT_INT The controller asserts cfg_bw_mgt_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0, and ▪ The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1, and ▪ The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. The cfg_bw_mgt_msi output is a pulse signal (only asserted for one clock cycle); but cfg_bw_mgt_int is a level signal. For upstream port: Reserved.

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	CFG_LINK_AUTO_BW_MSI The controller sets this pin when following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. ▪ The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
16	R/W1C	0x0	CFG_LINK_AUTO_BW_INT The controller asserts cfg_link_auto_bw_int when all of the following conditions are true: ▪ The INTx assertion disable bit in the Command register is 0, and ▪ The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and ▪ The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. The cfg_link_auto_bw_msi output is a pulse signal (only asserted for one clock cycle); but cfg_link_auto_bw_int is a level signal. For upstream port: Reserved.

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
15	R/W1C	0x0	PF0_HP_MSI The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: ▪ MSI or MSI-X is enabled. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).
14	R/W1C	0x0	PF0_HP_INT The controller asserts hp_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.hp_int[0]

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	PF0_HP_PME The controller asserts hp_pme when all of the following conditions are true: ▪ The PME Enable bit in the Power Management Control and Status register is set to 1. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.
12	R/W1C	0x0	RADM_INTD_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTD Message from the downstream device.
11	R/W1C	0x0	RADM_INTC_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTC Message from the downstream device.
10	R/W1C	0x0	RADM_INTB_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTB Message from the downstream device.
9	R/W1C	0x0	RADM_INTA_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTA Message from the downstream device.
8	R/W1C	0x0	RADM_INTD_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTD Message from the downstream device.

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	RADM_INTC_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTC Message from the downstream device.
6	R/W1C	0x0	RADM_INTB_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTB Message from the downstream device.
5	R/W1C	0x0	RADM_INTA_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTA Message from the downstream device.
4	R/W1C	0x0	PF0_CFG_PME_MSI The controller asserts cfg_pme_msi (as a one-cycle pulse) when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
3	R/W1C	0x0	PF0_CFG_PME_INT The controller asserts cfg_pme_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	PF0_CFG_AER_RC_ERR_MSI The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ A reported error condition causes a bit to be set in the Root Error Status register. ▪ The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
1	R/W1C	0x0	PF0_CFG_AER_RC_ERR_INT Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. **Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.**

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Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	PF0_CFG_VPD_INT This pin is set as a one cycle pulse to notify your application to read the VPD registers. The sequence of events for a VPD read cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '0' indicating a read request. Your application fetches four bytes of data from the VPD Address location and transfers this to the VPD Data register. ▪ Your application sets the VPD Flag bit to '1' indicating the request is complete. The sequence of events for a VPD write cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '1' indicating a write request. Your application reads the VPD Data register and transfers this to the location specified by the VPD Address register. ▪ Your application sets the VPD Flag bit to '0' indicating the request is complete.

8.13.5.35 0x0E0C PCIE SII Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PCIE_WAKE_N remote wake (USP)

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Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
30	R/W1C	0x0	WAKE local wake. Wake up from power management unit. The controller generates wake to request the system to restore power and clock when a wakeup event has been detected such as apps_pm_xmt_pme, apps_pm_vf_xmt_pme, or outband_pwrup_cmd. The wake signal is an active high signal and its rising edge should be detected to drive the WAKE# the connector. Assertion of wake could be for a single clock cycle or multiple clock cycles. Not used in RC mode.
29	R/W1C	0x0	RADM_PM_TO_ACK One-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message. Upstream port: Reserved.
28	R/W1C	0x0	RADM_PM_PME One-clock-cycle pulse that indicates that the controller received a PM_PME message.
27	R/W1C	0x0	RADM_FATAL_ERR One-clock-cycle pulse that indicates that the controller received an ERR_FATAL message.
26	R/W1C	0x0	RADM_NONFATAL_ERR One-clock-cycle pulse that indicates that the controller received an ERR_NONFATAL message.
25	R/W1C	0x0	RADM_CORRECTABLE_ERR One-clock-cycle pulse that indicates that the controller received an ERR_COR message. The controller makes the message header available the radm_msg_payload output.
24	R/W1C	0x0	PF0_CFG_SYS_ERR_RC System error detected. A one-clock-cycle pulse that indicates if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL. Also asserted when an internal error is detected. There is one bit of cfg_sys_err_rc assigned to each configured function.
23:22	/	/	/

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Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	PF0_FRS_GRANT Indicator of when an FRS message for this function has been scheduled for transmission.
20	R/W1C	0x0	RADM_VENDOR_MSG One-cycle pulse that indicates the controller received a vendor-defined message. The controller makes the message header available the radm_msg_payload output. When FX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then both bits are asserted.
19	/	/	/
18	R/W1C	0x0	PF0_FRSQ_MSI FRSQ Interrupt Pulse. The RC asserts this output when it receives an FRQ message or when the FRS queue overflows.
17	R/W1C	0x0	PF0_CFG_UP_DRS_TO_FRS DRS to FRS Pulse. The PCIe controller asserts the cfg_up_drs_to_frsoutput and sends an FRS message with the reason code set to 'DRS Message Received' when: ▪ It receives a DRS message, and ▪ PCIE_CAP_DRS_SIGNALING_CONTROL in INK_CONTROL_LINK_STATUS_REG is 2'b10
16	R/W1C	0x0	PF0_CFG_DRS_MSI DRS Message Received Interrupt Pulse. The PCIe controller asserts the cfg_drs_msi output when all of the following are true: ▪ It receives a DRS message ▪ PCIE_CAP_DRS_SIGNALING_CONTROL in INK_CON_TROL_LINK_STATUS_REG is 2'b01 ▪ MSI or MSI-X is enabled
15:12	/	/	/
11	R/W1C	0x0	PCIE_PERI_AR_INT PCIe read peripherals space(0-1G) int
10	R/W1C	0x0	PCIE_PERI_AW_INT PCIe write peripherals space(0-1G) int

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Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	RADM_QOVERFLOW_1 Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism.
8	R/W1C	0x0	RADM_QOVERFLOW_0 Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism.
7:5	/	/	/
4	R/W1C	0x0	RTLH_RFC_UPD Indicates that the controller received a flow control update DLLP. Used for applications that implement flow Control outside the controller.
3	R/W1C	0x0	LINK_REQ_RST_NOT Reset request because the link has gone down or the controller received a hot-reset request. A low level indicates that the controller is requesting external logic to reset the controller because the PHY link is down. When the AXI bridge module is enabled the link reset request is delayed until all pending AXI transfers have completed. When the AXI Bridge module is not enabled the link reset request is sent immediately.
2	/	/	/
1	R/W1C	0x0	RDLH_LINK_UP Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. ▪ 1: Link is up ▪ 0: Link is down
0	R/W1C	0x0	SMLH_LINK_UP PHY Link up/down indicator: ▪ 1: Link is up ▪ 0: Link is down

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8.13.5.36 0x1000 PCIE SII APP PM UNLOCK Register (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: SII_APP_PM_UNLOCK
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	APP_UNLOCK_MSG app_unlock_msg_ahb Request from your application to generate an Unlock message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
0	R/W	0x0	APP_PM_XMT_TURNOFF apps_pm_xmt_turnoff_ahb Request from your application to generate a PM_Turn_Off message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.

8.13.5.37 0x1100 PCIE SII Power Manage Register0 (Default Value: 0x0000_0000)

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	APP_L1SUB_DISABLE The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register.
11	R/W	0x0	APP_L1_PWR_OFF_EN Application permits to gate power to parts of the controller in L1 state
10	R/W	0x0	ACK_EN_VMAIN Acknowledge from power switch responsible for autonomous power-gating in L1.2. This signal is syncronized using aux_clk and can be driven/supplied asynchronously to the controller in certain low-power modes.
9	R/W	0x0	TEST_BYPASS_LP Test mode override of isolation enable

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Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	APP_CLK_PM_EN Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register.
7	R/W	0x0	CLKREQ_IN_N Status of the CLKREQ# bidirectional CMOS board-level signal. Used by the controller to determine when to enter and exit L1 Substates when using the CLKREQ#-based mechanism.
6	R/W	0x0	APP_XFER_PENDING Indicates that your application has transfers pending and prevents the controller from entering L1. This is a level signal used to inform the controller about the state of external queues and pipeline stages that contain transactions to be transmitted by the controller. The controller uses this information to determine when to enter/exit L1. When this signal is asserted, it indicates that there are transactions outside the controller that the controller needs to transmit. When de-asserted, it indicates that there are no transactions outside the controller. The controller responds to an assertion on this signal as follows: ▪ Upstream Ports: Prevents generation of requests to enter L1. Triggers exit if already in L1. ▪ Downstream Ports: Triggers exit if already in L1. You can instruct the controller to exit L1 by asserting either or both of app_xfer_pending and app_req_exit_l1. The controller only samples app_req_exit_l1 when the controller is already in the L1 state.
5	R/W	0x0	APP_REQ_EXIT_L1 Application request to Exit L1. Request from your application to exit L1. It is only effective when L1 is enabled.

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Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	APP_READY_ENTR_L23 Application Ready to Enter L23. Indication from your application that it is ready to enter the L23 state. The app_ready_entr_l23 signal is provided for applications that must control L23 entry (in case certain tasks must be performed before going into L23). The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. Hardwire to 1 for applications that do not require this feature. **Note: The controller ignores this input in RC mode.**
3	R/W	0x0	APP_REQ_ENTR_L1_AHB Application request to Enter L1 ASPM state. The app_req_entr_l1 signal is for use by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. Note: The controller ignores this input in RC mode.
2	R/W	0x0	SYS_AUX_PWR_DET Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present.
1:0	/	/	/

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8.14 Two Wire Interface (TWI)

8.14.1 Overview

The Two Wire Interface (TWI) provides an interface between a CPU and any TWI-bus-compatible device that connects via the TWI bus. The TWI is designed to be compatible with the standard I2C bus protocol. The communication of the TWI is carried out by a byte-wise mode based on interrupt polled handshaking. Each device on the TWI bus is recognized by a unique address and can operate as either transmitter or receiver, a device connected to the TWI bus can be considered as master or slave when performing data transfers. Note that a master device is a device that initiates a data transfer on the bus and generates the clock signals to permit the transfer. During this transfer, any device addressed by this master is considered a slave.

The TWI has the following features:

- Up to 9 TWI controllers
  - 6 TWI controllers in CPUX domain: TWI0, TWI1, TWI2, TWI3, TWI4, and TWI5
  - 3 TWI controllers in CPUS domain: S_TWI0, S_TWI1, and S_TWI2
- Compliant with I2C bus standard
- 7-bit and 10-bit device addressing modes
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports general call and start byte
- Master mode supports the following:
  - Bus arbitration in the case of multiple master devices
  - Clock synchronization and bit and byte waiting
  - Packet transmission and DMA
- Slave mode supports Interrupt on address detection

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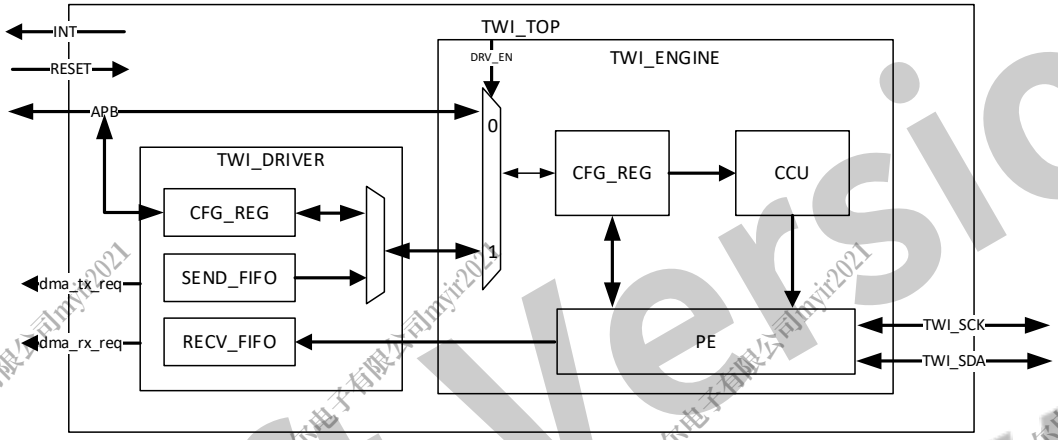
8.14.2 Block Diagram

the following figure shows the block diagram of TWI.

Figure 8-60 TWI Block Diagram



TWI contains the following sub-blocks:

Table 8-39 TWI Sub-blocks

Sub-block	Description
RESET	Module reset signal
INT	Module output interrupt signal
CFG_REG	Module configuration register in TWI
PE	Packet encoding/decoding
CCU	Module clock controller unit
SEND_FIFO	The register address bytes and the written data bytes are buffered in SEND_FIFO
RECV_FIFO	The read data bytes are buffered in RECV_FIFO

The controller includes TWI engine and TWI driver. Each time the TWI engine sends a START signal, a STOP signal, or a BYTE data, or a corresponding ACK, the TWI engine will generate an interrupt, and wait for the CPU to process and clear the interrupt before the next START, STOP, or BYTE, ACK transmission can be performed. Therefore, when a device communication is completed, many interrupts will be generated, and the CPU needs to wait for the previous interrupt before it can configure the next one. The TWI driver defines each communication with the device as a packet transmission. The CPU can directly configure the slave address, register address and data transmission for one or more package transmissions without waiting for interruption, then start the TWI driver, and the TWI driver can control the TWI engine to complete a pre-configured communication, and report an interrupt to the CPU after completion.

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8.14.3 Functional Description

8.14.3.1 External Signals

The following table describes the external signals of the TWI. The TWIn-SCK and TWIn-SDA are bidirectional I/O, when the TWI is configured as a master device, the TWIn-SCK is an output pin; when the TWI is configurable as a slave device, the TWIn-SCK is an input pin. When using TWI, the corresponding PADs are selected as TWI function via section 8.6 GPIO.

Table 8-40 TWI External Signals

Signal Name	Description	Type
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O
TWI4-SCK	TWI4 Serial Clock Signal	I/O
TWI4-SDA	TWI4 Serial Data Signal	I/O
TWI5-SCK	TWI5 Serial Clock Signal	I/O
TWI5-SDA	TWI5 Serial Data Signal	I/O
S-TWI0-SCK	S-TWI0 Serial Clock Signal	I/O
S-TWI0-SDA	S-TWI0 Serial Data Signal	I/O
S-TWI1-SCK	S-TWI1 Serial Clock Signal	I/O
S-TWI1-SDA	S-TWI1 Serial Data Signal	I/O
S-TWI2-SCK	S-TWI1 Serial Clock Signal	I/O
S-TWI2-SDA	S-TWI1 Serial Data Signal	I/O

8.14.3.2 Clock Sources

Each TWI controller has an input clock source. The following table describes the clock sources for TWI. After selecting a proper clock, users must open the gating of TWI and release the corresponding reset bit.

For more details on the clock setting, configuration, and gating information, see section 2.7 Clock Controller Unit (CCU) and section 2.13 Power Reset Clock Management (PRCM).

Table 8-41 TWI Clock Sources

Clock Sources	Descsription	Module
APB1 Bus	TWI clock source. Refer to CCU for details on APB1.	CCU
APBS1 Bus	S_TWI clock source. Refer to PRCM for details on APBS1.	PRCM

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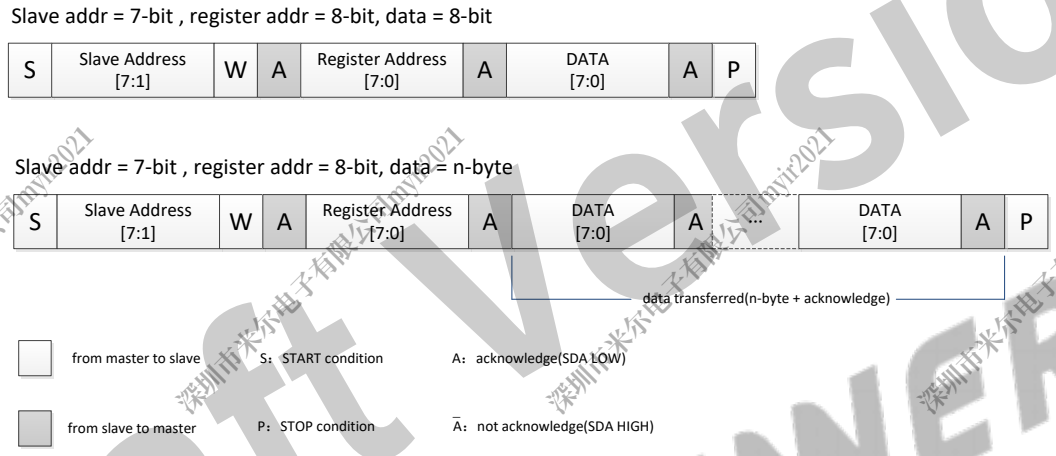
8.14.3.3 Write/Read Timing in Standard and Extended Addressing Mode

This section is the 7-bit/10-bit addressing mode of the entire TWI protocol to read and write device registers. It can be achieved by directly using the TWI engine or using the TWI driver to control the TWI engine.

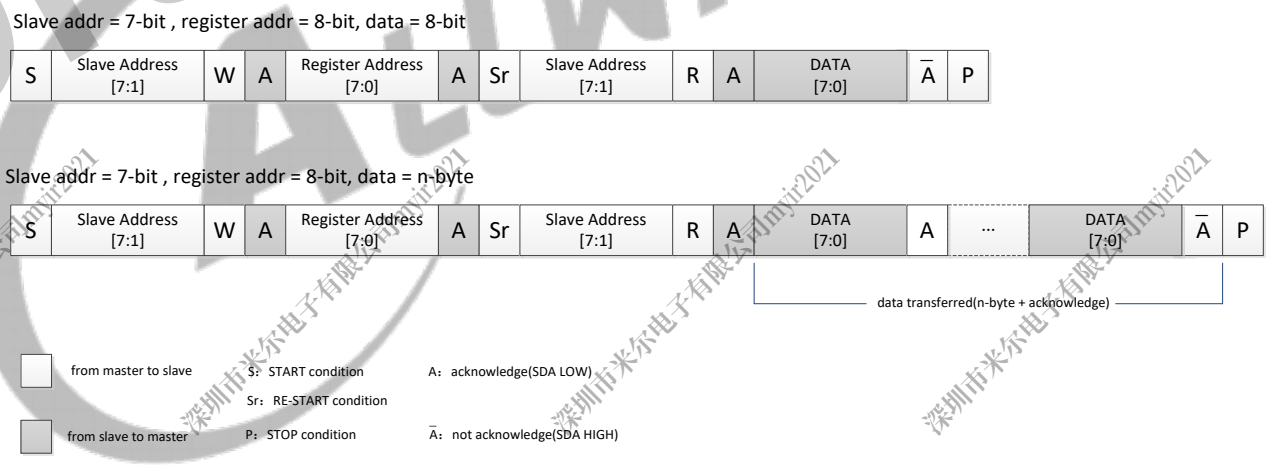
The following figure describes the write timing in 7-bit standard addressing mode.

Figure 8-61 Write Timing in 7-bit Standard Addressing Mode



The following figure describes the read timing in 7-bit standard address mode.

Figure 8-62 Read Timing in 7-bit Standard Addressing Mode



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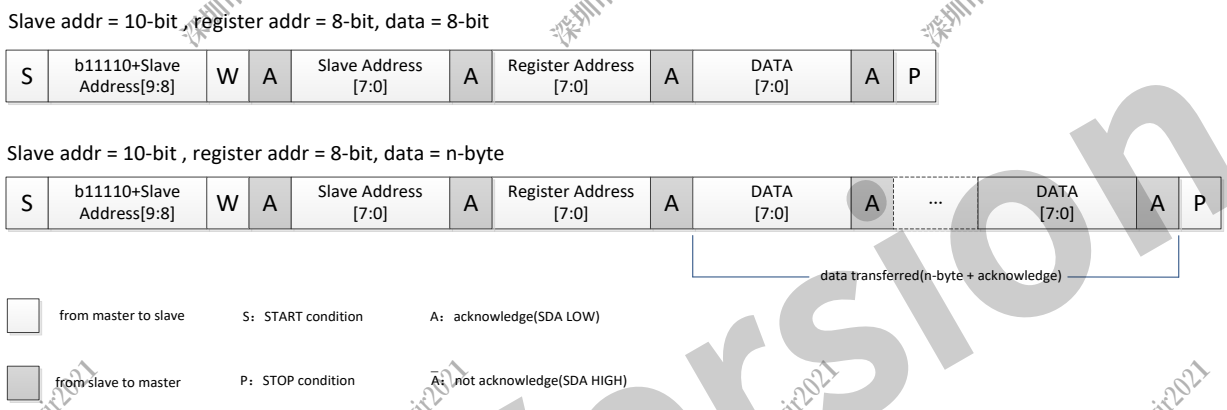
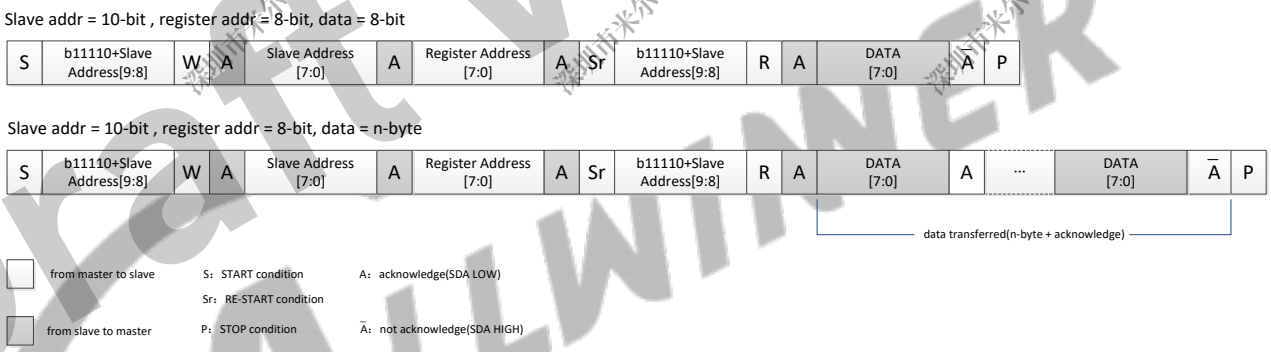
The following figure describes the write timing in 10-bit extended address mode.

Figure 8-63 Write Timing in 10-bit Extended Addressing Mode



The following figure describes the read timing in 10-bit extended address mode.

Figure 8-64 Read Timing in 10-bit Extended Addressing Mode



8.14.3.4 Write/Read Packet Transmission of TWI Driver

The TWI driver is only supported for master mode. When the TWI works in master mode, the TWI driver drives the TWI engine for one or more packet transmission instead of the CPU host. Packet transmission is defined in the following figures. The register address bytes and the written data bytes are buffered in SEND_FIFO, the read data bytes are buffered in RECV_FIFO.

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Figure 8-65 TWI Driver Write Packet Transmission

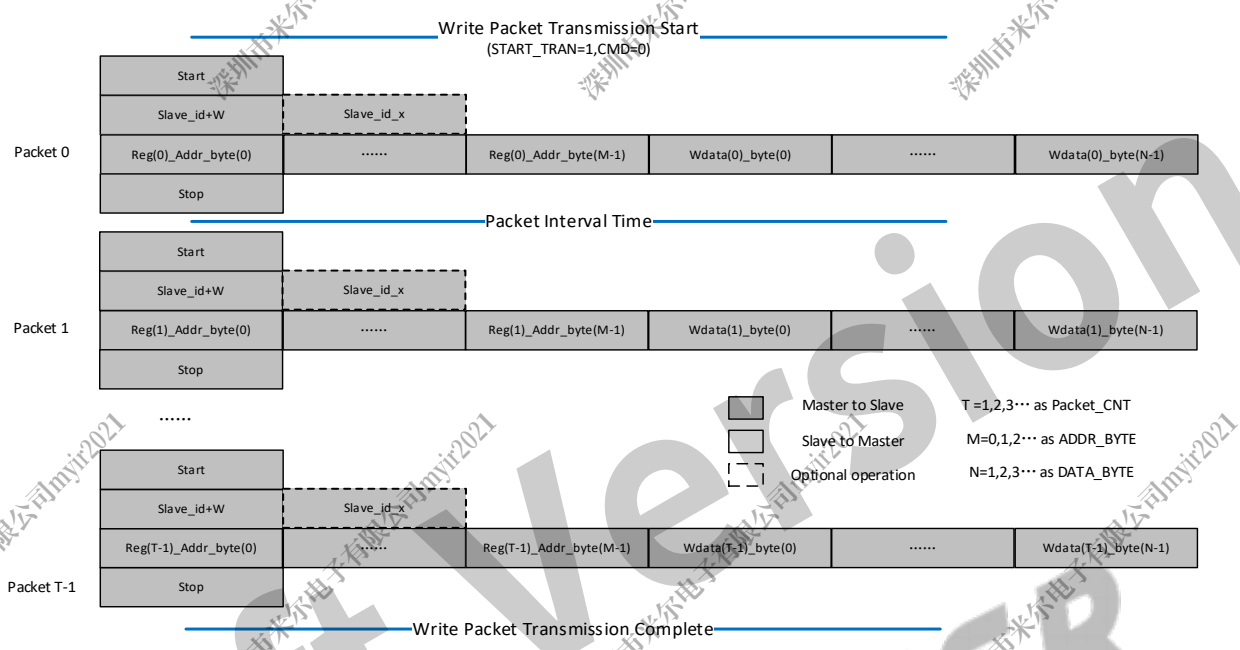

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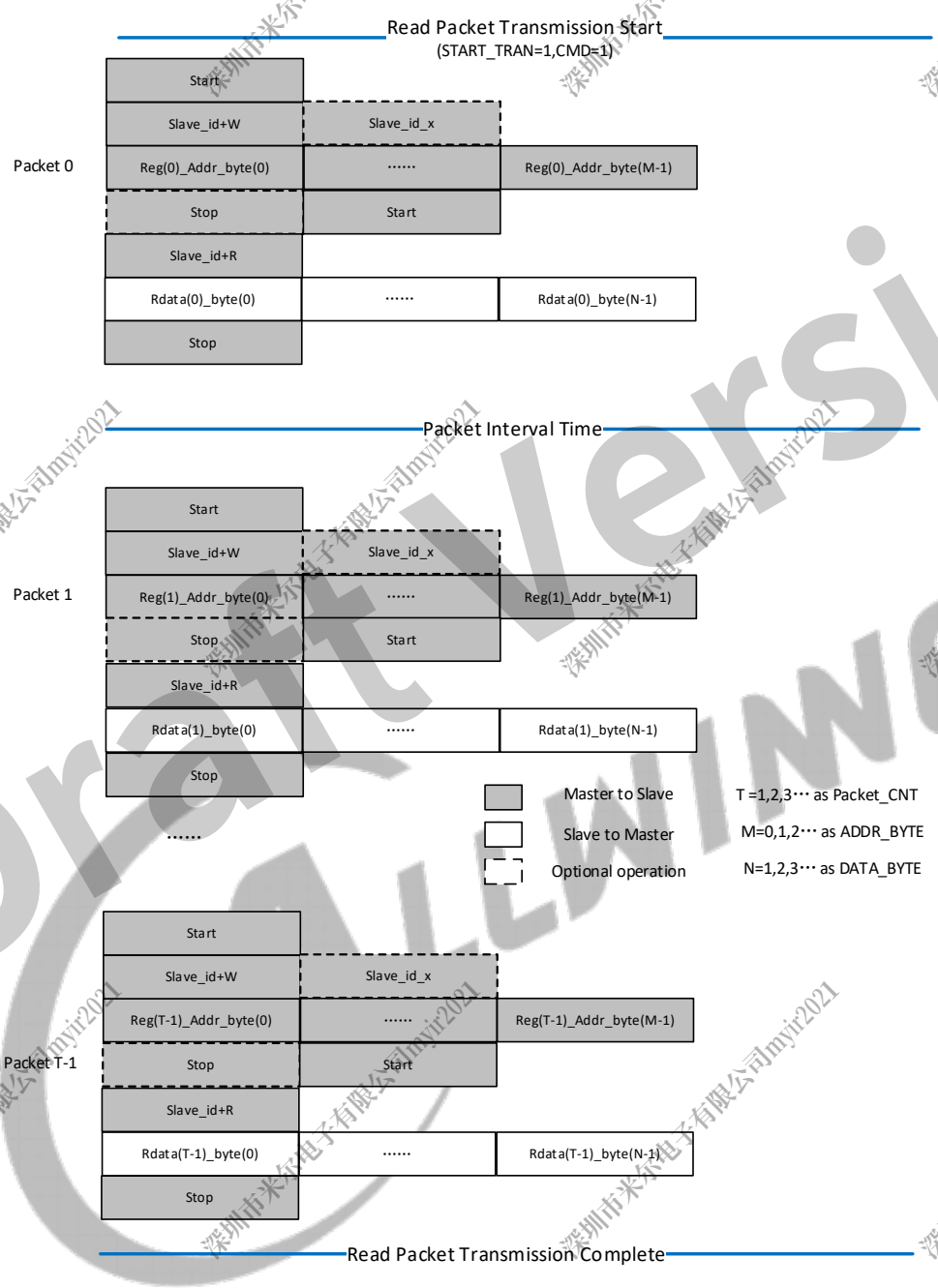
Figure 8-66 TWI Driver Read Packet Transmission



8.14.3.5 Master and Slave Mode of TWI Engine

In Master mode, the CPU host controls the TWI engine by writing command and data to its registers. The TWI engine transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP command is detected. The CPU host can poll the status register if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting TWI_CNTR[M_STA] to high. The TWI engine will assert the INT line and TWI_CNTR[INT_FLAG] to indicate a completion for the START command and each consequent

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byte transfer. At each interrupt, the CPU host needs to check the current state by the TWI_STAT register. A transfer must conclude with the STOP command by setting TWI_CNTR[M_STP] to high.

In Slave mode, the TWI engine also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed, and the TWI engine interrupts the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write the TWI_DATA register, and set the TWI_CNTR register. After each byte transfer, a slave device always stops the operation of the remote master by holding the next low pulse on the SCL line until the CPU host responds to the status of the previous byte transfer or START command.

8.14.3.6 Generation of Repeated Start

After the data transfer, if the master still requires the bus, it can signal another Start followed by another slave address without signaling a Stop.

8.14.3.7 Programming State Diagram

Figure 8-67 shows the TWI programming state diagram. For the value between two states, see the TWI_STAT register in section 8.14.6.5.

M_SEND_S: master sends START signal;

M_SEND_ADDR: master sends slave address;

M_SEND_XADD: master sends slave extended address;

M_SEND_SR: master repeated start;

M_SEND_DATA: master sends data;

M_SEND_P: master sends STOP signal;

M_RECV_DATA: master receives data;

ARB_LOST: Arbitration lost;

C_IDLE: Idle.

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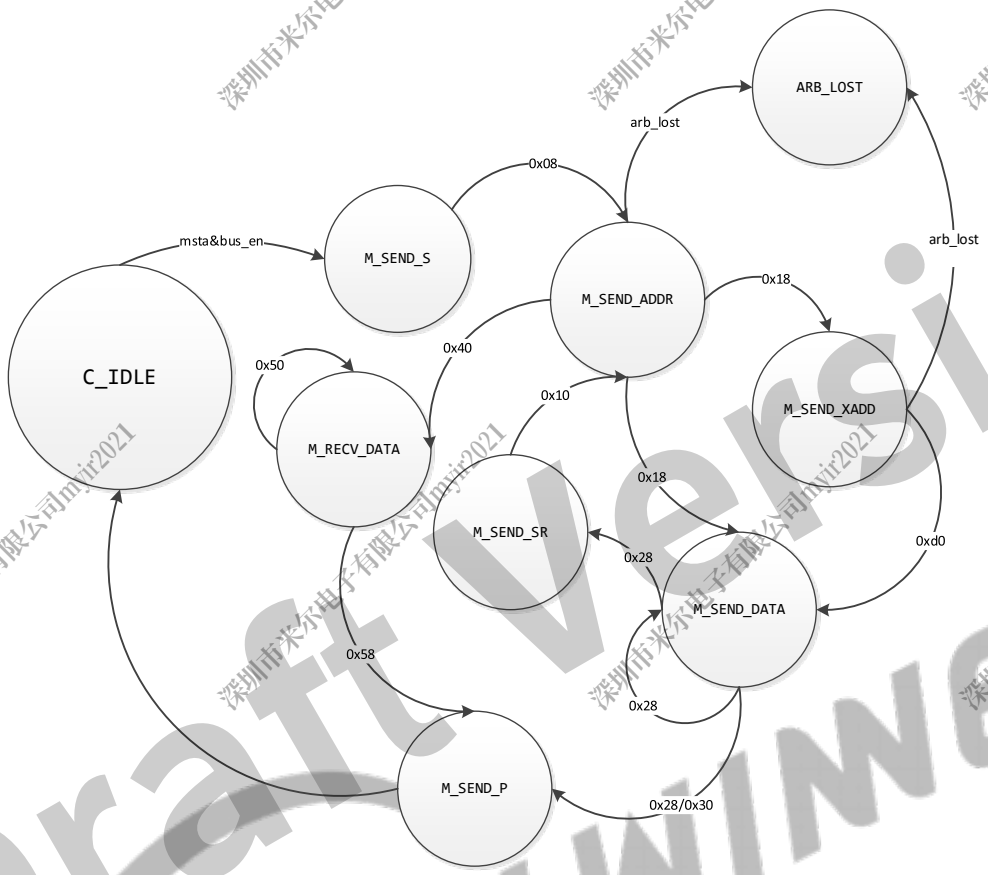
Figure 8-67 TWI Programming State Diagram



8.14.4 Programming Guidelines

The TWI controller operates in an 8-bit data format. The data on the TWI_SDA line is always 8 bits long. At first, the TWI controller sends a start condition. When in the addressing formats of 7-bit, the TWI sends out an 8-bit message which includes 7 MSB slave address and 1 LSB read/write flag. The least significant of the salve address indicates the direction of transmission. When the TWI works in 10-bit slave address mode, the operation will be divided into two steps, for details on the operation, refer to register description in Section 8.14.6.1 and 8.14.6.2.

The following takes the TWI module in the CPUX domain as an example.

8.14.4.1 Initialization for TWI Engine

To initialize the TWI engine, perform the following steps:

Step 1 Configure corresponding GPIO multiplex function as TWI mode.

Step 2 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 0 to close TWIn clock.

Step 3 For TWIn, set TWI_BGR_REG[TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.

Step 4 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 1 to open TWIn clock.

Step 5 Configure TWI_CCR[CLK_M] and TWI_CCR[CLK_N] to get the needed rate (The clock source of TWI is from APB1).

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Step 6 Configure TWI_CNTR[BUS_EN] and TWI_CNTR[A_ACK], when using interrupt mode, set TWI_CNTR[INT_EN] to 1, and register the system interrupt through GIC module. In slave mode, configure TWI_ADDR and TWI_XADDR registers to finish TWI initialization configuration.

8.14.4.2 Writing Data Operation for TWI Engine

To write data to the device, perform the following steps:

Step 1 Clear TWI_EFR register, and configure TWI_CNTR[M_STA] to 1 to transmit the START signal.

Step 2 After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step 3 The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).

Step 4 Interrupt is triggered after data address transmission completes, write data to be transmitted to TWI_DATA (For consecutive write data operation, every byte transmission completion triggers interrupt, during interrupt write the next byte data to TWI_DATA).

Step 5 After transmission completes, write TWI_CNTR[M_STP] to 1 to transmit the STOP signal and end this write-operation.

8.14.4.3 Reading Data Operation for TWI Engine

To read data from the device, perform the following steps:

Step 1 Clear TWI_EFR register, and set TWI_CNTR[A_ACK] to 1, and configure TWI_CNTR[M_STA] to 1 to transmit the START signal.

Step 2 After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first-byte ID, secondly write the second-byte ID in the next interrupt).

Step 3 The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).

Step 4 The Interrupt is triggered after data address transmission completes, write TWI_CNTR[M_STA] to 1 to transmit new START signal, and after interrupt triggers, write device ID to TWI_DATA to start read-operation.

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Step 5 After device address transmission completes, each receive completion will trigger an interrupt, in turn, read TWI_DATA to get data, when receiving the previous interrupt of the last byte data, clear [A_ACK] to stop acknowledge signal of the last byte.

Step 6 Write TWI_CNTR[M_STP] to 1 to transmit the STOP signal and end this read-operation.

8.14.4.4 Initialization for TWI Driver

To initialize the TWI driver, perform the following steps:

Step 1 Configure corresponding GPIO multiplex function as TWI mode.

Step 2 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 0 to close TWIn clock.

Step 3 For TWIn, set TWI_BGR_REG[TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.

Step 4 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 1 to open TWIn clock.

Step 5 Set TWI_DRV_CTRL[TWI_DRV_EN] to 1 to enable the TWI driver.

Step 6 Configure TWI_DRV_BUS_CTRL[CLK_M] and TWI_DRV_BUS_CTRL[CLK_N] to get the needed rate (The clock source of TWI is from APB1).

Step 7 Set TWI_DRV_CTRL[RESTART_MODE] to 0 and [READ_TRAN_MODE] to 1, set TWI_DRV_INT_CTRL[TRAN_COM_INT_EN] to 1.

Step 8 When using DMA for data transmission, set TWI_DRV_DMA_CFG[DMA_RX_EN] and TWI_DRV_DMA_CFG[DMA_TX_EN] to 1, and configure TWI_DRV_DMA_CFG[RX_TRIG] and TWI_DRV_DMA_CFG[TX_TRIG] to set the thresholds of RXFIFO and TXFIFO.

8.14.4.5 Writing Packet Transmission for TWI Driver

To write package to the device, perform the following steps:

Step 1 Configure TWI_DRV_SLV[SLV_ID] to set the device ID, and configure TWI_DRV_SLV[CMD] to 0 to set the write operation.

Step 2 Configure TWI_DRV_FMT[ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT[DATA_BYTE] according to the written data count in a packet.

Step 3 Configure TWI_DRV_CFG[PACKET_CNT] to set the written packet number.

Step 4 Configure DMA channel, including TWI TXFIFO, device register address, and the written data.

Step 5 Set [START_TRAN] to 1 to start TWI Driver transmission.

Step 6 When TWI driver transmission completes, the interrupt is triggered, it indicates that the write packet transmission ends.

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8.14.4.6 Reading Packet Transmission for TWI Driver

Step 1 To read package from the device, perform the following steps:

Step 2 Configure TWI_DRV_SLV[SLV_ID] to set the device ID, and configure TWI_DRV_SLV[CMD] to 1 to set the read operation.

Step 3 Configure TWI_DRV_FMT[ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT[DATA_BYTE] according to the read data count in a packet.

Step 4 Configure TWI_DRV_CFG[PACKET_CNT] to set the read packet number.

Step 5 Configure DMA channel, including TWI TXFIFO, TWI RXFIFO, device register address and the read data.

Step 6 Set [START_TRAN] to 1 to start TWI Driver transmission.

Step 7 When TWI driver transmission completes, the interrupt is triggered, it indicates that the read packet transmission ends.

8.14.5 Register List

Module Name	Base Address	Comments
TWI0	0x0250 2000	
TWI1	0x0250 2400	TWI1 register is the same with TWI0.
TWI2	0x0250 2800	TWI2 register is the same with TWI0.
TWI3	0x0250 2C00	TWI3 register is the same with TWI0.
TWI4	0x0250 3000	TWI4 register is the same with TWI0.
TWI5	0x0250 3400	TWI5 register is the same with TWI0.
S_TWI0	0x0708 1400	R-TWI0 register is the same with TWI0.
S_TWI1	0x0708 1800	R-TWI1 register is the same with TWI0.
S_TWI2	0x0708 1C00	R-TWI2 register is the same with TWI0.

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address Register
TWI_XADDR	0x0004	TWI Extended Slave Address Register
TWI_DATA	0x0008	TWI Data Byte Register
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset Register
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register

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Register Name	Offset	Description
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register
TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

8.14.6 Register Description

8.14.6.1 0x0000 TWI Slave Address Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address For 7-bit addressing, the bit[7:1] indicates: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 For 10-bit addressing, the bit[7:1] indicates: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

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NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with b'11110, the TWI recognizes b'11110 as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (For example, SLAX9 and SLAX8 for the extended address of the device), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

8.14.6.2 0x0004 TWI Extend Address Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

8.14.6.3 0x0008 TWI Data Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

8.14.6.4 0x000C TWI Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

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Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus SDA/SCL is ignored and the TWI controller will not respond to any address on the bus. 1: The TWI will respond to call to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Note: In master operation mode, this bit should be set to '1'.
5	R/WAC	0x0	M_STA Master Mode Start When the M_STA is set to '1', the TWI controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.

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Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	M_STP Master Mode Stop If the M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode), then transmit the START condition. The M_STP bit is cleared automatically. Writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag The INT_FLAG is automatically set to '1' when any of the 28 (out of the possible 29) states is entered (see 'STAT Register' below). The state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when INT_FLAG is set to '1'. If the TWI is operating in slave mode, the data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.

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Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the GCE bit in the ADDR register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1	/	/	/
0	R/W	0x0	CLK_COUNT_MODE 0: scl clock high period count on oscl 1: scl clock high period count on iscl

8.14.6.5 0x0010 TWI Status Register (Default Value: 0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

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7:0	R	0xF8	STA Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in the address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in the address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in the address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received

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Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
			0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: The Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

8.14.6.6 0x0014 TWI Clock Register (Default Value: 0x0000_0080)

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit [7] takes effect 1: 30%
7	R/W	0x1	CLK_DUTY Setting duty cycle of clock as master 0: 50% 1: 40%
6:3	R/W	0x0	CLK_M The TWI SCL output frequency, in master mode, is F1/10: F1 = F0/(CLK_M + 1) Fscl = F1/10 = Fin/(2^CLK_N * (CLK_M + 1)*10) Specially, Fscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.

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Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin/2^CLK_N The TWI SCL output frequency, in master mode, is F1/10: F1 = F0/(CLK_M + 1) Fscl = F1/10 = Fin/(2^CLK_N * (CLK_M + 1)*10) Specially, Fscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce. For Example: Fin = 24 MHz (APB clock input) For 400 kHz full speed 2-wire, CLK_N = 1, CLK_M = 2 F0 = 24 MHz/2^1 = 12 MHz, F1 = F0/(10*(2+1)) = 0.4 MHz For 100 kHz standard speed 2-wire, CLK_N = 1, CLK_M = 11 F0 = 24 MHz/2^1 = 12 MHz, F1 = F0/(10*(11+1)) = 0.1 MHz

8.14.6.7 0x0018 TWI Soft Reset Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation.

8.14.6.8 0x001C TWI Enhance Feature Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/

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Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00: No data byte can be written after the read command 01: Only 1-byte data can be written after the read command 10: 2-bytes data can be written after the read command 11: 3-bytes data can be written after the read command

8.14.6.9 0x0020 TWI Line Control Register (Default Value: 0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When the line control mode is enabled (bit[2] is set), this bit decides the output level of TWI_SCL. 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode

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Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When the line control mode is enabled (bit[0] is set), this bit decides the output level of TWI_SDA. 0: Output low level 1: Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

8.14.6.10 0x0200 TWI_DRV Control Register (Default Value: 0x00F8_1000)

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	START_TRAN Start transmission 0: Transmission idle 1: Start transmission Automatically cleared to '0' when finished. If the slave is not responding for the expected status over the time defined by TIMEOUT, the current transmission will stop. All setting formats and data will be loaded from registers and FIFO when the transmission starts.
30	/	/	/
29	R/W	0x0	RESTART_MODE Restart mode 0: RESTART 1: STOP+START Define the TWI_DRV action after sending the register address.
28	R/W	0x0	READ_TRAN_MODE Read transition mode 0: Send slave_id+W 1: Not send slave_id+W Setting this bit to 1 if reading from a slave in which the register width is equal to 0.

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Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
27:24	R	0x0	TRAN_RESULT Transition result 000: OK 001: FAIL Other: Reserved
23:16	R	0xf8	TWI_STA TWI status 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending the 9th SCL clock Other: Reserved
15:8	R/W	0x10	TIMEOUT_N Timeout number When sending the 9th clock, assert fail signal when the slave device does not respond after N*F_{SCL} cycles. And the software must do a reset to the TWI_DRV module and send a stop condition to slave.
7:2	/	/	/
1	R/W	0x0	SOFT_RESET Software reset 0: Normal 1: Reset

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Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TWI_DRV_EN TWI driver enable 0: Module disable 1: Module enable (only use in TWI Master Mode)

8.14.6.11 0x0204 TWI_DRV Transmission Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0204			Register Name: TWI_DRV_CFG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL F_{SCL} cycles.
15:0	R/W	0x1	PACKET_CNT The FIFO data is transmitted as PACKET_CNT packets in current format.

8.14.6.12 0x0208 TWI_DRV Slave ID Register (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID For 7-bit addressing, the bit[7:1] indicates: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 For 10-bit addressing, the bit[7:1] indicates: 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD R/W operation to slave device 0: Write 1: Read
7:0	R/W	0x0	SLV_ID_X SLAX[7:0] The low 8 bits for slave device ID with 10-bit addressing.

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8.14.6.13 0x020C TWI_DRV Packet Format Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE How many bytes be sent as slave device reg address 0-255
15:0	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1-65535

8.14.6.14 0x0210 TWI_DRV Bus Control Register (Default Value: 0x0000_80C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit [15] takes effect 1: 30%
16	W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl
15	R/W	0x1	CLK_DUTY Setting duty cycle of clock as Master 0: 50% 1: 40%
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10 Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/

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Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output enable
0	R/W	0x0	SDA_MOE SDA manual output enable

8.14.6.15 0x0214 TWI_DRV Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
19	R/W	0x0	RX_REQ_INT_EN If set, an interrupt is sent when RX_REQ_PD sets.
18	R/W	0x0	TX_REQ_INT_EN If set, an interrupt is sent when TX_REQ_PD sets.
17	R/W	0x0	TRAN_ERR_INT_EN If set, an interrupt is sent when TRAN_ERR_PD sets.
16	R/W	0x0	TRAN_COM_INT_EN If set, an interrupt is sent when TRAN_COM_PD sets.
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG.
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO.
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failure pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completion pending

8.14.6.16 0x0218 TWI_DRV DMA Configure Register (Default Value: 0x0010_0010)

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

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Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	DMA_RX_EN DMA RX Enable
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG RX trigger When DMA_RX_EN is set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG, or the read transmission is completed, the data of RECV_FIFO does not reach RX_TRIG but as long as the RECV_FIFO is not empty.
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN DMA TX Enable
7:6	/	/	/
5:0	R/W	0x10	TX_TRIG TX trigger When DMA_TX_EN is set, send DMA TX Req when the space of SEND_FIFO (FIFO Level – data volume) reaches TX_TRIG.

8.14.6.17 0x021C TWI_DRV FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV_FIFO pointer, and this bit is cleared automatically.
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV_FIFO
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer, and this bit is cleared automatically.
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

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8.14.6.18 0x0300 TWI_DRV Send Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TWI_DRV_SEND_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Address of a 32x8 SEND_FIFO, which stores reg address and data sending to the slave device.

8.14.6.19 0x0304 TWI_DRV Receive Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RECV_DATA_FIFO Address of a 32x8 RECV_FIFO, which stores data received from the slave device.

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8.15 PWM

8.15.1 Overview

The Pulse Width Modulation (PWM) module can output the configurable PWM waveforms and measure the external input waveforms.

The PWM has the following features:

- Up to 30 PWM channels and 4 PWM controllers:
  - PWM [15:0] for PWMCTRL0 controller
  - PWM [19:16] for PWMCTRL1 controller
  - S-PWM [1:0] for S_PWMCTRL controller
  - S-PWM [9:2] for DSP_PWMCTRL controller
- Maximum 16 independent PWM channels for PWM controller
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz (when the clock source is DCXO24M)
    - 0 to 100 MHz (when the clock source is APB1 clock)
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Maximum 8 complementary pairs output
  - The pairing methods for each controller are as follows. The components are internal PWM channels:
    - Maximum 8 pairs for PWMCTRL0:

      PWM0 + PWM1, PWM2 + PWM3, PWM4 + PWM5, PWM6 + PWM7, PWM8 + PWM9, PWM10 + PWM11, PWM12 + PWM13, PWM14 + PWM15
    - Maximum 2 pairs for PWMCTRL1:

      PWM0+PWM1, PWM2+PWM3
    - Maximum 1 pair for S_PWMCTRL:

      PWM0+PWM1
    - Maximum 4 pairs for DSP_PWMCTRL:

      PWM0+PWM1, PWM2+PWM3, PWM4+PWM5, PWM6+PWM7
  - Supports dead-zone generator, and the dead-zone time is configurable
- Maximum 4 group of PWM channel output for controlling stepping motors

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- Supports any plural channels to form a group, and output the same duty-cycle pulse
- In group mode, the relative phase of the output waveform for each channel is configurable

- Maximum 16 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

The basic features for four PWM controllers are as follows:

PWM controller	Domain	Channels	Pairs
PWMCTRL0	CPUX	16	8 PWM pairs PWM01 (PWM0+PWM1) PWM23 (PWM2+PWM3) PWM45 (PWM4+PWM5) PWM67 (PWM6+PWM7) PWM89 (PWM8+PWM9) PWMab (PWM10+PWM11) PWMcd (PWM12+PWM13) PWMef (PWM14+PWM15)
PWMCTRL1	CPUX	4	2 PWM pairs PWM01 (PWM0+PWM1) PWM23 (PWM2+PWM3)
S_PWMCTRL	CPUS	2	1 PWM pair PWM01 (PWM0+PWM1)
DSP_PWMCTRL	CPUS	8	4 PWM pair PWM01 (PWM0+PWM1) PWM23 (PWM2+PWM3) PWM45 (PWM4+PWM5) PWM67 (PWM6+PWM7)

NOTE

For the corresponding relationship between the channels of each PWM controller and the external signals, please refer to section 8.15.3.1 External Signals.

8.15.2 Block Diagram

The PWM includes multi PWM channels. Each channel can generate different PWM waveform by the independent counter and duty-ratio configuration register. Each PWM pair shares one group of clock and dead-zone generator to generate PWM waveform.

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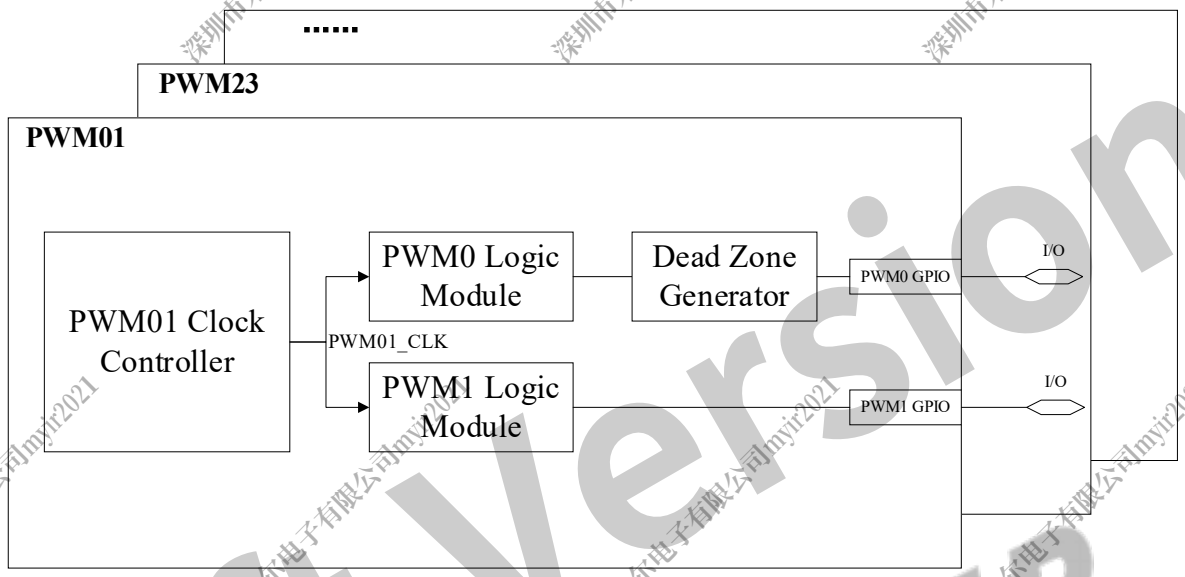
Figure 8-68 PWM Block Diagram



Each PWM pair consists of 1 clock module, 2 timer logic module, and 1 programmable dead-zone generator.

8.15.3 Functional Description

8.15.3.1 External Signals

The following table describes the external signals of the PWM.

Table 8-42 PWM External Signals

Signal	Description	Type
PWMCTRL0		
PWM0	PWM channel0 in PWMCTRL0	I/O
PWM1	PWM channel1 in PWMCTRL0	I/O
PWM2	PWM channel2 in PWMCTRL0	I/O
PWM3	PWM channel3 in PWMCTRL0	I/O
PWM4	PWM channel4 in PWMCTRL0	I/O
PWM5	PWM channel5 in PWMCTRL0	I/O
PWM6	PWM channel6 in PWMCTRL0	I/O
PWM7	PWM channel7 in PWMCTRL0	I/O
PWM8	PWM channel8 in PWMCTRL0	I/O
PWM9	PWM channel9 in PWMCTRL0	I/O
PWM10	PWM channel10 in PWMCTRL0	I/O
PWM11	PWM channel11 in PWMCTRL0	I/O
PWM12	PWM channel12 in PWMCTRL0	I/O
PWM13	PWM channel13 in PWMCTRL0	I/O

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Signal	Description	Type
PWM14	PWM channel14 in PWMCTRL0	I/O
PWM15	PWM channel15 in PWMCTRL0	I/O
PWMCTRL1		
PWM16	PWM channel0 in PWMCTRL1	I/O
PWM17	PWM channel1 in PWMCTRL1	I/O
PWM18	PWM channel2 in PWMCTRL1	I/O
PWM19	PWM channel3 in PWMCTRL1	I/O
S_PWMCTRL		
S-PWM0	PWM channel0 in S_PWMCTRL	I/O
S-PWM1	PWM channel1 in S_PWMCTRL	I/O
DSP_PWMCTRL		
S-PWM2	PWM channel0 in DSP_PWMCTRL	I/O
S-PWM3	PWM channel1 in DSP_PWMCTRL	I/O
S-PWM4	PWM channel2 in DSP_PWMCTRL	I/O
S-PWM5	PWM channel3 in DSP_PWMCTRL	I/O
S-PWM6	PWM channel4 in DSP_PWMCTRL	I/O
S-PWM7	PWM channel5 in DSP_PWMCTRL	I/O
S-PWM8	PWM channel6 in DSP_PWMCTRL	I/O

8.15.3.2 Clock Sources

The following table describes the clock sources of the PWM controllers.

Table 8-43 PWM clock sources

PWM	Clock Sources	Description	Module
PWMCTRL0 PWMCTRL1	HOSC	24 MHz, external clock.	CCU
	APB1_CLK	24 MHz, PWM bus clock.	
S_PWMCTRL DSP_PWMCTRL	CLK24M	By default, CLK24M is 24 MHz.	PRCM
	CLK32K	By default, CLK32K is 32 kHz.	
	CLK_RC	By default, CLK_RC is 16 MHz.	

8.15.3.3 Typical Application

- Suitable for display device, such as LCD
- Suitable for electric motor control

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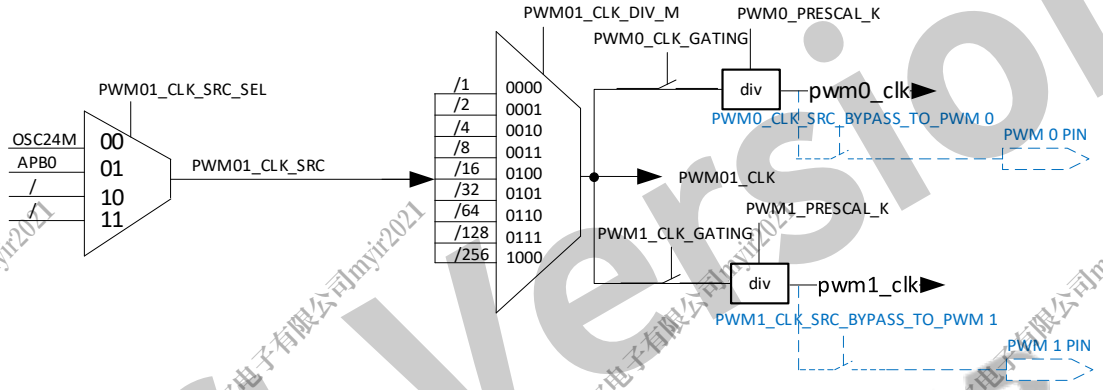
8.15.3.4 Clock Controller

Using PWM01 as an example. The other PWM pairs are the same as PWM01.

Figure 8-69 PWM01 Clock Controller Diagram



The clock controller of each PWM pair includes clock source select (PWM01_CLK_SRC), 1-256 scaler (PWM01_CLK_DIV_M). Each PWM channel has the secondary frequency division (PWM_PRESCAL_K), clock source bypass (PWMx_CLK_BYPASS) and clock switch (PWMx_CLK_GATING).

The clock sources have HOSC and APB0. The HOSC comes from the external high-frequency oscillator; the APB0 is APB0 bus clock.

The bypass function of the clock source is that the clock source directly accesses PWM output, the PWM output waveform is the waveform of the clock controller output. The BYPASS gridlines in the above figure indicate the bypass function of the clock source, see Figure 8-70 for the details about implement. At last, the output clock of the clock controller is sent to the PWM logic module.

8.15.3.5 PWM Output

Taking PWM01 as an example, Figure 8-70 indicates the PWM01 output logic diagram. The logic diagrams of other PWM pairs are the same as PWM01.

The timer logic module of PWM consists of one 16-bit up-counter (PCNTR) and three 16-bit parameters (PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE, PWM_COUNTER_START). The PWM_ENTIRE_CYCLE is used to control the PWM cycle, the PWM_ACT_CYCLE is used to control the duty-cycle, the PWM_COUNTER_START is used to control the output phase (multi-channel synchronization work requirements).

The PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE support the cache load, after PWM output is enabled, the register values of the PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE can be changed anytime, the changed value caches into the cache register. When the PCNTR counter outputs a period of PWM waveform, the value of the cache register can be updated for the PCNTR control.

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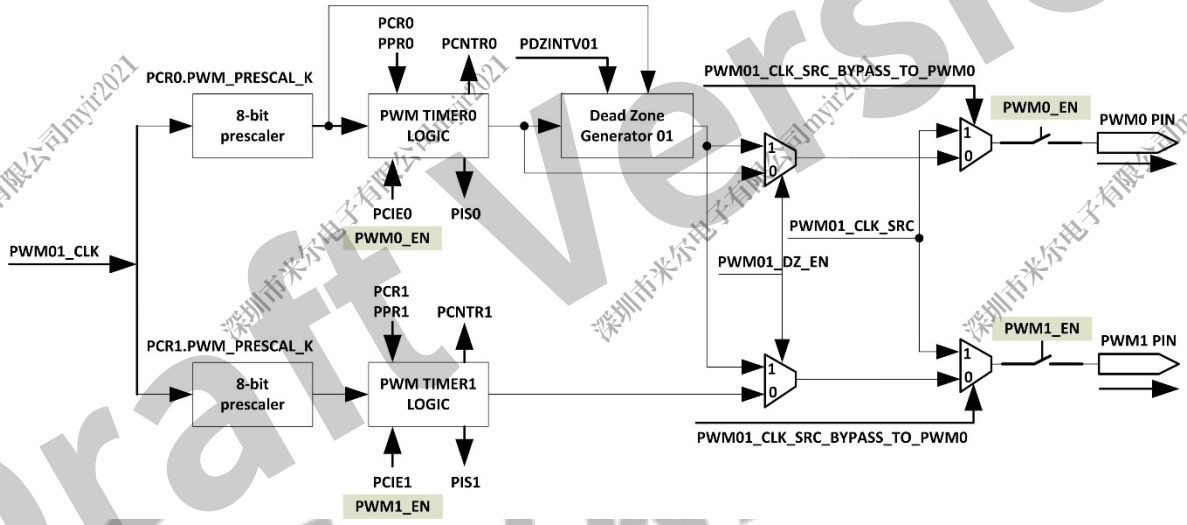
The purpose of the cache load is to avoid the unstable PWM output waveform with glitches when updating the values of the PWM_ENTIRE_CYCLE and PWM_ACT_CYCLE.

The PWM supports cycle and pulse waveform output.

Cycle mode: The PWM outputs the setting PWM waveform continually, that is, the output waveform is a continuous PWM square wave.

Pulse mode: After setting the PWM_PUL_NUM parameter, the PWM outputs (PWM_PULNUM+1) periods of PWM waveform, that is, the waveform with several pulses are output.

Figure 8-70 PWM01 Output Logic Module Diagram



8.15.3.6 Pulse Mode and Cycle Mode

The PWM output supports pulse mode and cycle mode. PWM in pulse mode outputs PCR[PWM_PUL_NUM] +1 cycles waveform, but PWM in cycle mode outputs continuous waveform. The following figure shows the PWM output waveform in pulse mode and cycle mode.

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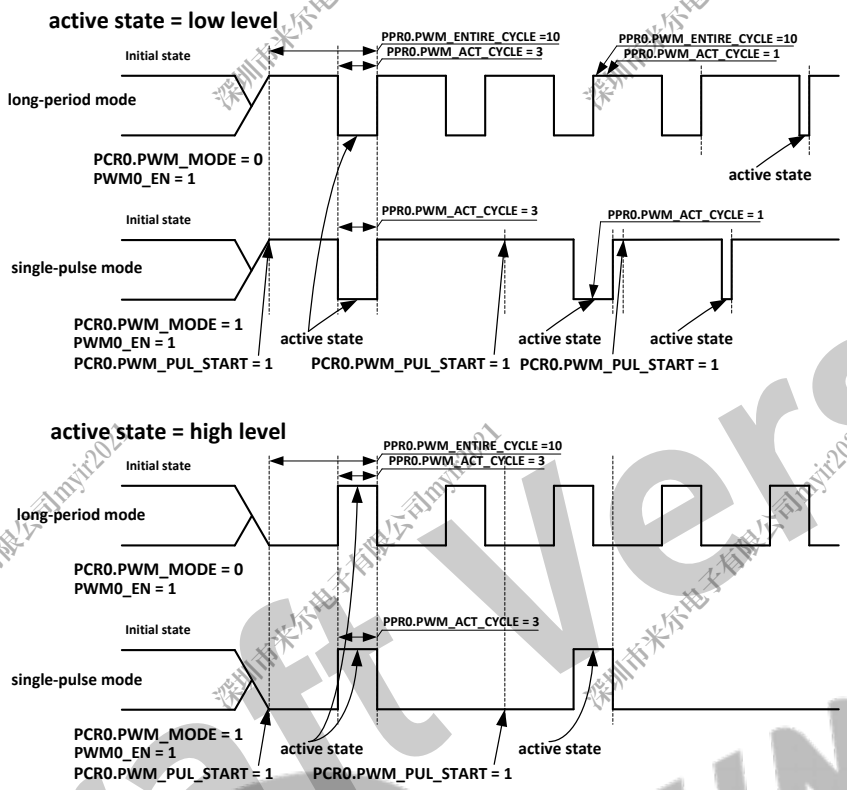
Figure 8-71 PWM0 Output Waveform in Pulse Mode and Cycle Mode



Each channel of the PWM module supports the PWM output of pulse mode and cycle mode, the active state of the PWM output waveform can be programmed to control.

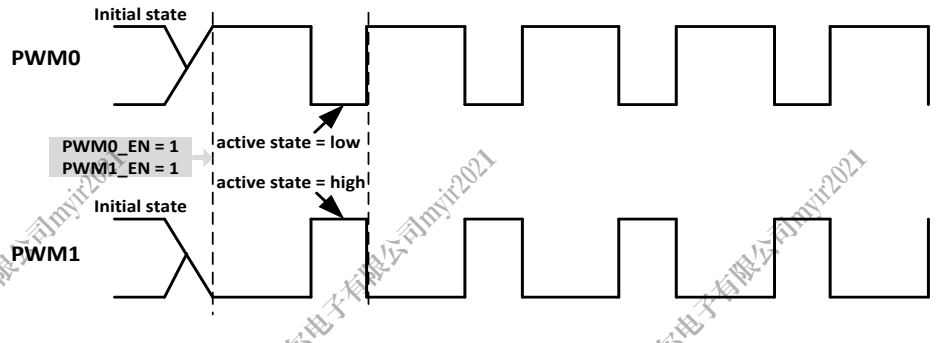
When PCR[PWM_MODE] is 0, the PWM0 outputs in cycle mode. When PCR[PWM_MODE] is 1, the PWM0 outputs in pulse mode.

Specifically, in pulse mode, after the PWM0 channel enabled, PCR[PWM_PUL_START] needs to be set to 1 when the PWM0 needs to output pulse waveform, after completed the output, PCR[PWM_PUL_START] can be cleared to 0 by hardware. The next setting 1 can be operated after PCR[PWM_PUL_START] is cleared.

8.15.3.7 Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time. the following figure shows the complementary pair output of PWM01.

Figure 8-72 PWM01 Complementary Pair Output



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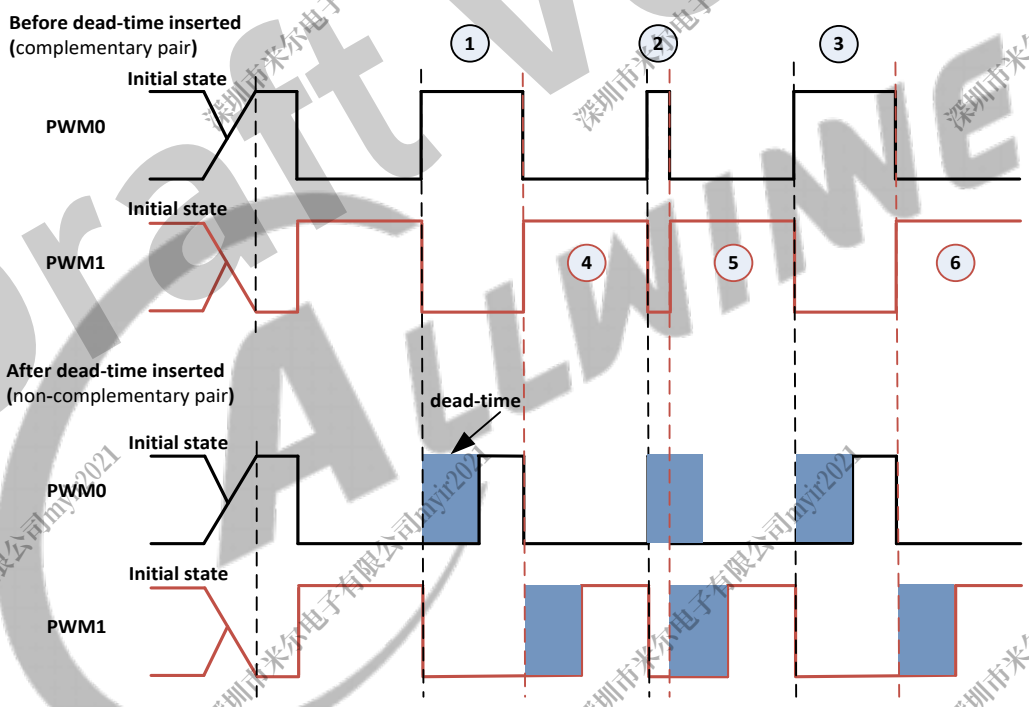
The complementary pair output needs to satisfy the following conditions:

- PWM0 and PWM1 have the same clock divider, frequency, duty-cycle, and phase
- PWM0 and PWM1 have an opposite active state
- Enable the clock gating of PWM0 and PWM1 at the same time
- Enable the waveform output of PWM0 and PWM1 at the same time

8.15.3.8 Dead-time Generator

Every PWM pair has a programmable dead-time generator. When the dead-time function of the PWM pair enabled, the PWM01 output waveform is decided by PWM timer logic and DeadZone Generator. the following figure shows the output waveform.

Figure 8-73 Dead-time Output Waveform



The PWM waveform before the insertion of dead-time indicates a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.

The PWM waveform after the insertion of dead-time indicates a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01. The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.

For the complementary pair of Dead Zone Generator 01, the principle of inserting dead-time is that to insert dead-time as soon as the rising edge came. If the high level time for mark② in the above figure is less than dead-time, then dead-time will override the high level. The setting of dead-time needs to consider the period and the duty-cycle of the output waveform. The dead-time formula is defined as follows:

Dead-time = $(PWM01_CLK / PWM0_PRESCALE_K)^{-1} * PDZINTV01$

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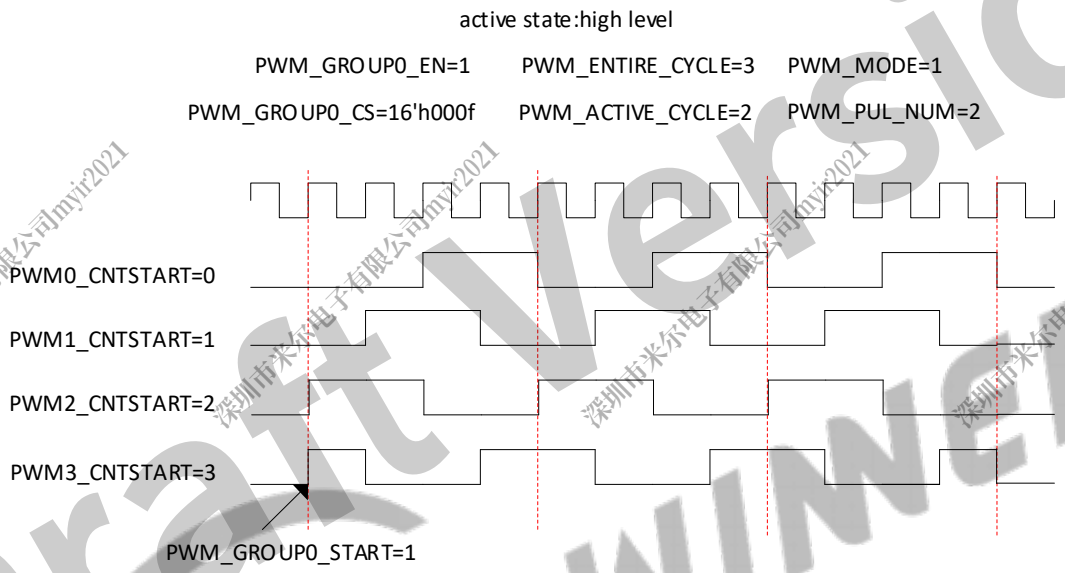
8.15.3.9 PWM Group Mode

Taking PWM Group0 as an example. The same group of PWM channel is selected to work by PGR0.CS; the same PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE are set by the same clock configuration; the different PWM_COUNTER_START can output PWM group signals with the same duty-cycle and the different phase.

Figure 8-74 Group 0-3 PWM Signal Output



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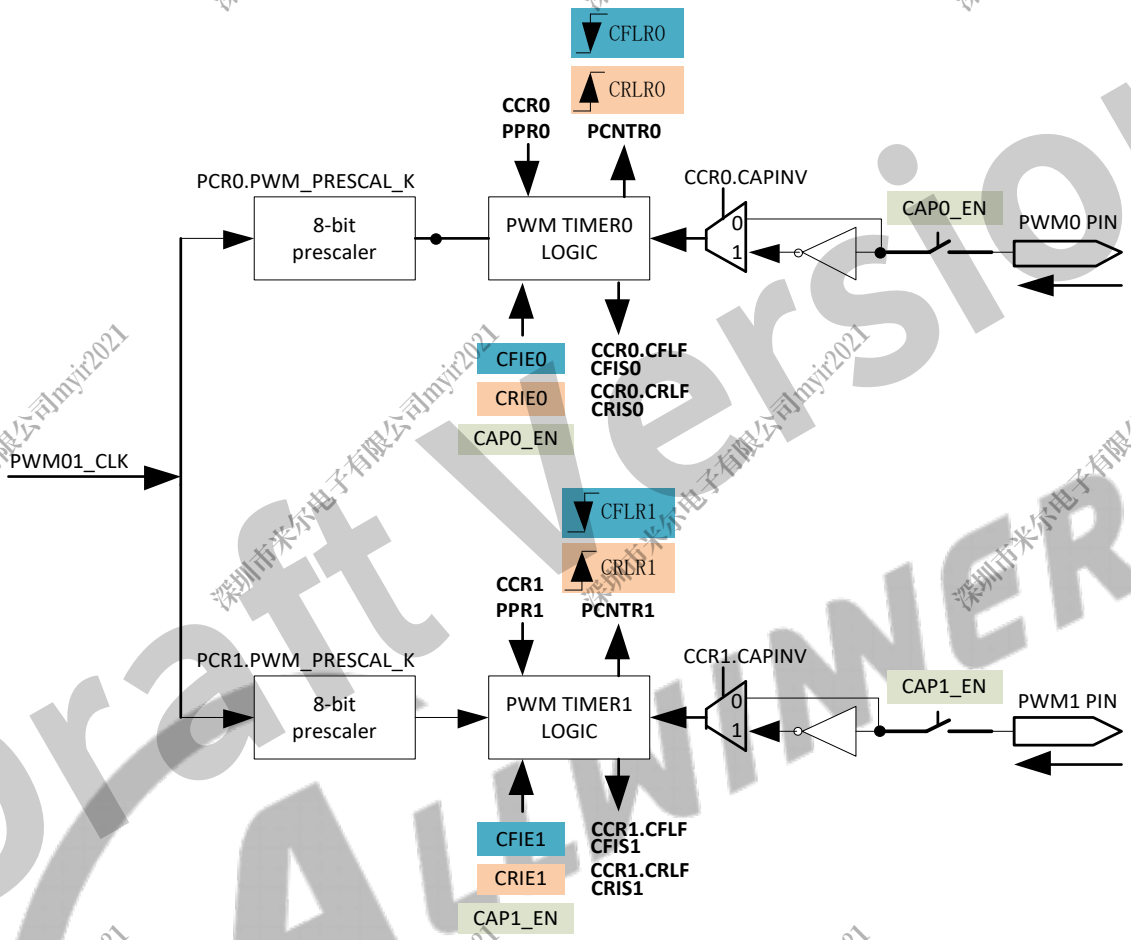
8.15.3.10 Capture Input

Figure 8-75 PWM01 Capture Logic Module Diagram



Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture the rising edge and the falling edge of the external clock. Using the PWM0 channel as an example, the PWM0 channel has one CFLR0 and one CRLR0 for capturing up-counter value on the falling edge and rising edge, respectively. You can calculate the period of the external clock by CFLR0 and CRLR0.

Thigh-level = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

Tlow-level = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

Tperiod = Thigh-level + Tlow-level

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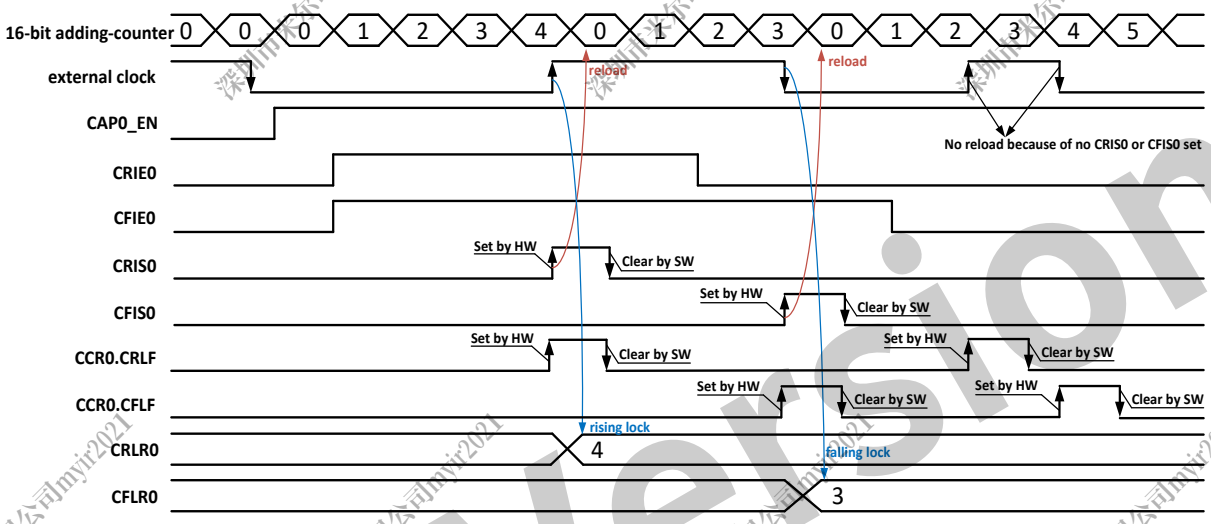
Figure 8-76 PWM0 Channel Capture Timing



When the capture input function of the PWM0 channel is enabled, the PCNTR of the PWM0 channel starts to work.

When the timer logic module of PWM0 captures a rising edge, the current value of the up-counter is locked to CRLR0 and CCR0[CRLF] is set to 1. If CRIE0 is 1, then CRIS0 is set to 1, the PWM0 channel sends interrupt requests, and the up-counter is loaded to 0 and continues to count. If CRIE0 is 0, the timer logic module of PWM0 captures a rising edge, CRIS0 cannot be set to 1, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of PCNTR is locked to CFLR0 and CCR0[CFLF] is set to 1. If CFIE0 is 1, then CFIS0 is set to 1, the PWM0 channel sends interrupt requests, and the up-counter is loaded to 0 and continues to count. If CFIE0 is 0, the timer logic module of PWM0 captures a falling edge, CFIS0 cannot be set to 1, the up-counter is not loaded to 0.

8.15.4 Programming Guidelines

The following working mode takes PWM01 as an example, other PWM pairs and PWM01 are consistent.

8.15.4.1 Configuring Clock

Step 1 PWM gating: When using PWM, write 1 to PCGR[PWMx_CLK_GATING].

Step 2 PWM clock source select: Set PCCR01[PWM01_CLK_SRC] to select HOSC or APB0 clock.

Step 3 PWM clock divider: Set PCCR01[PWM01_CLK_DIV_M] to select different frequency division coefficient (1/2/4/8/16/32/64/128/256).

Step 4 PWM clock bypass: Set PCGR[PWM_CLK_SRC_BYPASS_TO_PWM] to 1, output the PWM clock after the secondary frequency division to the corresponding PWM output pin.

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Step 5 PWM internal clock configuration: Set PCR[PWM_PRESCAL_K] to select any frequency division coefficient from 1 to 256.

NOTE

For the channel of complementary output and group mode, firstly, set the same clock configurations (clock source selects APB0, clock division configures the same division factor); secondly, open clock gating at the same time; thirdly, configure PWM parameters; finally, enable PWM output at the same time to ensure each channel sync.

We suggest that the two channels of the same PWM pair cannot subject to two groups because of they have the same first level clock division and gating. If must allocate based on this way, the first level of clock division of the channel used by all groups needs to set to the same coefficient and open gating at the same time. And the total module needs to be reset when the group mode regroups.

8.15.4.2 Configuring PWM

Step 1 PWM mode: Set PCR[PWM_MODE] to select cycle mode or pulse mode, if pulse mode, PCR[PWM_PUL_NUM] needs to be configured.

Step 2 PWM active level: Set PCR[PWM_ACT_STA] to select a low level or high level.

Step 3 PWM duty-cycle: Configure PPR[PWM_ENTIRE_CYCLE] and PPR[PWM_ACT_CYCLE] after clock gating is opened.

Step 4 PWM starting/stoping phase: Configure PCNTR[PWM_COUNTER_START] after the clock gating is enabled and before the PWM is enabled. You can verify whether the configuration was successful by reading back PCNTR[PWM_COUNTER_STATUS].

Step 5 Enable PWM: Configure PER to select the corresponding PWM enable bit; when selecting pulse mode, PCR[PWM_PUL_START] needs to be enabled.

8.15.4.3 Configuring Deadzone

Step 1 Set initial value: set [PDZINTV01].

Step 2 Enable Deadzone: set [PWM01_DZ_CN].

8.15.4.4 Configuring Capture Input

Step 1 Enable capture: Configure CER to enable the corresponding channel.

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Step 2 Capture mode: Configure CCR[CRLF] and CCR[CFLF] to select rising edge capture or falling edge capture, configure CCR[CAPINV] to select whether the input signal does reverse processing.

8.15.5 Register List

Module Name	Base Address
PWMCTRL0	0x0200 0C00
PMWCTRL1	0x0205 1000
S_PWMCTRL	0x0702 0C00
DSP_PWMCTRL	0x0710 3000

Register Name	Offset	Description	PWM CTRL 0	PMWCTRL1	S_PWM CTRL	DSP_PWMCTRL
PIER	0x0000	PWM IRQ Enable Register	√	√	√	√
PISR	0x0004	PWM IRQ Status Register	√	√	√	√
CIER	0x0010	Capture IRQ Enable Register	√	√	√	√
CISR	0x0014	Capture IRQ Status Register	√	√	√	√
PCCR01	0x0020	PWM01 Clock Configuration Register	√	√	√	√
PCCR23	0x0024	PWM23 Clock Configuration Register	√	√	-	√
PCCR45	0x0028	PWM45 Clock Configuration Register	√	-	-	√
PCCR67	0x002C	PWM67 Clock Configuration Register	√	-	-	√
PCCR89	0x0030	PWM89 Clock Configuration Register	√	-	-	-
PCCRab	0x0034	PWMab Clock Configuration Register	√	-	-	-
PCCRcd	0x0038	PWMcd Clock Configuration Register	√	-	-	-
PCCRef	0x003C	PWMef Clock Configuration Register	√	-	-	-
PCGR	0x0040	PWM Clock Gating Register	√	√	√	√
PDZCR01	0x0060	PWM01 Dead Zone Control Register	√	√	√	√
PDZCR23	0x0064	PWM23 Dead Zone Control Register	√	√	-	√
PDZCR45	0x0068	PWM45 Dead Zone Control Register	√	-	-	√
PDZCR67	0x006C	PWM67 Dead Zone Control Register	√	-	-	√
PDZCR89	0x0070	PWM89 Dead Zone Control Register	√	-	-	-
PDZCRab	0x0074	PWMab Dead Zone Control Register	√	-	-	-
PDZCRcd	0x0078	PWMcd Dead Zone Control Register	√	-	-	-

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Register Name	Offset	Description	PWM CTRL 0	PMWCTRL1	S_PWM CTRL	DSP_PWMCTRL
PDZCRef	0x007C	PWMef Dead Zone Control Register	√	-	-	-
PER	0x0080	PWM Enable Register	√	√	√	√
PGR0	0x0090	PWM Group0 Register	√	√	√	√
PGR1	0x0094	PWM Group1 Register	√	√	√	√
PGR2	0x0098	PWM Group2 Register	√	√	√	√
PGR3	0x009C	PWM Group3 Register	√	√	√	√
CER	0x00c0	Capture Enable Register	√	√	√	√
PCR	0x0100+N*0x0020	PWM Control Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
PPR	0x0104+N*0x0020	PWM Period Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
PCNTR	0x0108+N*0x0020	PWM Counter Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
PPCNTR	0x010C+N*0x0020	PWM Pulse Counter Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
CCR	0x0110+N*0x0020	Capture Control Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
CRLR	0x0114+N*0x0020	Capture Rise Lock Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
CFLR	0x0118+N*0x0020	Capture Fall Lock Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

8.15.6 Register Description

8.15.6.1 0x0000 PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	PGIE3 PWM group 3 Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PGIE2 PWM group 2 Interrupt Enable 0: Disable 1: Enable

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Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	PGIE1 PWM group 1 Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	PGIE0 PWM group 0 Interrupt Enable 0: Disable 1: Enable
15	R/W	0x0	PCIE15. PWM channel 15 Interrupt Enable. 0: PWM channel 15 Interrupt Disable; 1: PWM channel 15 Interrupt Enable.
14	R/W	0x0	PCIE14. PWM channel 14 Interrupt Enable. 0: PWM channel 14 Interrupt Disable; 1: PWM channel 14 Interrupt Enable.
13	R/W	0x0	PCIE13. PWM channel 13 Interrupt Enable. 0: PWM channel 13 Interrupt Disable; 1: PWM channel 13 Interrupt Enable.
12	R/W	0x0	PCIE12. PWM channel 12 Interrupt Enable. 0: PWM channel 12 Interrupt Disable; 1: PWM channel 12 Interrupt Enable.
11	R/W	0x0	PCIE11. PWM channel 11 Interrupt Enable. 0: PWM channel 11 Interrupt Disable; 1: PWM channel 11 Interrupt Enable.
10	R/W	0x0	PCIE10. PWM channel 10 Interrupt Enable. 0: PWM channel 10 Interrupt Disable; 1: PWM channel 10 Interrupt Enable.
9	R/W	0x0	PCIE9. PWM channel 9 Interrupt Enable. 0: PWM channel 9 Interrupt Disable; 1: PWM channel 9 Interrupt Enable.
8	R/W	0x0	PCIE8. PWM channel 8 Interrupt Enable. 0: PWM channel 8 Interrupt Disable; 1: PWM channel 8 Interrupt Enable.

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Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	PCIE7. PWM channel 7 Interrupt Enable. 0: PWM channel 7 Interrupt Disable; 1: PWM channel 7 Interrupt Enable.
6	R/W	0x0	PCIE6. PWM channel 6 Interrupt Enable. 0: PWM channel 6 Interrupt Disable; 1: PWM channel 6 Interrupt Enable.
5	R/W	0x0	PCIE5. PWM channel 5 Interrupt Enable. 0: PWM channel 5 Interrupt Disable; 1: PWM channel 5 Interrupt Enable.
4	R/W	0x0	PCIE4. PWM channel 4 Interrupt Enable. 0: PWM channel 4 Interrupt Disable; 1: PWM channel 4 Interrupt Enable.
3	R/W	0x0	PCIE3. PWM channel 3 Interrupt Enable. 0: PWM channel 3 Interrupt Disable; 1: PWM channel 3 Interrupt Enable.
2	R/W	0x0	PCIE2. PWM channel 2 Interrupt Enable. 0: PWM channel 2 Interrupt Disable; 1: PWM channel 2 Interrupt Enable.
1	R/W	0x0	PCIE1. PWM channel 1 Interrupt Enable. 0: PWM channel 1 Interrupt Disable; 1: PWM channel 1 Interrupt Enable.
0	R/W	0x0	PCIE0. PWM channel 0 Interrupt Enable. 0: PWM channel 0 Interrupt Disable; 1: PWM channel 0 Interrupt Enable.

8.15.6.2 0x0004 PWM IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W1C	0x0	PGIS3 PWM group 3 Interrupt Status

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Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	PGIS2 PWM group 2 Interrupt Status
17	R/W1C	0x0	PGIS1 PWM group 1 Interrupt Status
16	R/W1C	0x0	PGIS0 PWM group 0 Interrupt Status
15	R/W1C	0x0	PIS15. PWM channel 15 Interrupt Status. When PWM channel 15 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 15 interrupt is not pending. 1: PWM channel 15 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 15 interrupt status.
14	R/W1C	0x0	PIS14. PWM channel 14 Interrupt Status. When PWM channel 14 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 14 interrupt is not pending. 1: PWM channel 14 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 14 interrupt status.
13	R/W1C	0x0	PIS13. PWM channel 13 Interrupt Status. When PWM channel 13 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 13 interrupt is not pending. 1: PWM channel 13 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 13 interrupt status.

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Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	PIS12. PWM channel 12 Interrupt Status. When PWM channel 12 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 12 interrupt is not pending. 1: PWM channel 12 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 12 interrupt status.
11	R/W1C	0x0	PIS11. PWM channel 11 Interrupt Status. When PWM channel 11 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 11 interrupt is not pending. 1: PWM channel 11 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 11 interrupt status.
10	R/W1C	0x0	PIS10. PWM channel 10 Interrupt Status. When PWM channel 10 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 10 interrupt is not pending. 1: PWM channel 10 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 10 interrupt status.

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Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	PIS9. PWM channel 9 Interrupt Status. When PWM channel 9 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 9 interrupt is not pending. 1: PWM channel 9 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 9 interrupt status.
8	R/W1C	0x0	PIS8. PWM channel 8 Interrupt Status. When PWM channel 8 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 8 interrupt is not pending. 1: PWM channel 8 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 8 interrupt status.
7	R/W1C	0x0	PIS7. PWM channel 7 Interrupt Status. When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. 1: PWM channel 7 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6. PWM channel 6 Interrupt Status. When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. 1: PWM channel 6 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 6 interrupt status.

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Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	PIS5. PWM channel 5 Interrupt Status. When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. 1: PWM channel 5 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4. PWM channel 4 Interrupt Status. When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. 1: PWM channel 4 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3. PWM channel 3 Interrupt Status. When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. 1: PWM channel 3 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2. PWM channel 2 Interrupt Status. When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. 1: PWM channel 2 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 2 interrupt status.

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Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	PIS1. PWM channel 1 Interrupt Status. When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. 1: PWM channel 1 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0. PWM channel 0 Interrupt Status. When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. 1: PWM channel 0 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 0 interrupt status.

8.15.6.3 0x0010 Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CFIE15 If this enable bit is set 1, when capture channel 15 captures falling edge, it generates a capture channel 15 pending. 0: Capture channel 15 fall lock Interrupt disable; 1: Capture channel 15 fall lock Interrupt enable.
30	R/W	0x0	CRIE15 If this enable bit is set 1, when capture channel 15 captures rising edge, it generates a capture channel 15 pending. 0: Capture channel 15 rise lock Interrupt disable; 1: Capture channel 15 rise lock Interrupt enable.

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Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	CFIE14 If this enable bit is set 1, when capture channel 14 captures falling edge, it generates a capture channel 14 pending. 0: Capture channel 14 fall lock Interrupt disable; 1: Capture channel 14 fall lock Interrupt enable.
28	R/W	0x0	CRIE14 If this enable bit is set 1, when capture channel 14 captures rising edge, it generates a capture channel 14 pending. 0: Capture channel 14 rise lock Interrupt disable; 1: Capture channel 14 rise lock Interrupt enable.
27	R/W	0x0	CFIE13 If this enable bit is set 1, when capture channel 13 captures falling edge, it generates a capture channel 13 pending. 0: Capture channel 13 fall lock Interrupt disable; 1: Capture channel 13 fall lock Interrupt enable.
26	R/W	0x0	CRIE13 If this enable bit is set 1, when capture channel 13 captures rising edge, it generates a capture channel 13 pending. 0: Capture channel 13 rise lock Interrupt disable; 1: Capture channel 13 rise lock Interrupt enable.
25	R/W	0x0	CFIE12 If this enable bit is set 1, when capture channel 12 captures falling edge, it generates a capture channel 12 pending. 0: Capture channel 12 fall lock Interrupt disable; 1: Capture channel 12 fall lock Interrupt enable.

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Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	CRIE12 If this enable bit is set 1, when capture channel 12 captures rising edge, it generates a capture channel 12 pending. 0: Capture channel 12 rise lock Interrupt disable; 1: Capture channel 12 rise lock Interrupt enable.
23	R/W	0x0	CFIE11 If this enable bit is set 1, when capture channel 11 captures falling edge, it generates a capture channel 11 pending. 0: Capture channel 11 fall lock Interrupt disable; 1: Capture channel 11 fall lock Interrupt enable.
22	R/W	0x0	CRIE11 If this enable bit is set 1, when capture channel 11 captures rising edge, it generates a capture channel 11 pending. 0: Capture channel 11 rise lock Interrupt disable; 1: Capture channel 11 rise lock Interrupt enable.
21	R/W	0x0	CFIE10 If this enable bit is set 1, when capture channel 10 captures falling edge, it generates a capture channel 10 pending. 0: Capture channel 10 fall lock Interrupt disable; 1: Capture channel 10 fall lock Interrupt enable.
20	R/W	0x0	CRIE10 If this enable bit is set 1, when capture channel 10 captures rising edge, it generates a capture channel 10 pending. 0: Capture channel 10 rise lock Interrupt disable; 1: Capture channel 10 rise lock Interrupt enable.

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Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	CFIE9 If this enable bit is set 1, when capture channel 9 captures falling edge, it generates a capture channel 9 pending. 0: Capture channel 9 fall lock Interrupt disable; 1: Capture channel 9 fall lock Interrupt enable.
18	R/W	0x0	CRIE9 If this enable bit is set 1, when capture channel 9 captures rising edge, it generates a capture channel 9 pending. 0: Capture channel 9 rise lock Interrupt disable; 1: Capture channel 9 rise lock Interrupt enable.
17	R/W	0x0	CFIE8 If this enable bit is set 1, when capture channel 8 captures falling edge, it generates a capture channel 8 pending. 0: Capture channel 8 fall lock Interrupt disable; 1: Capture channel 8 fall lock Interrupt enable.
16	R/W	0x0	CRIE8 If this enable bit is set 1, when capture channel 8 captures rising edge, it generates a capture channel 8 pending. 0: Capture channel 8 rise lock Interrupt disable; 1: Capture channel 8 rise lock Interrupt enable.
15	R/W	0x0	CFIE7 If this enable bit is set 1, when capture channel 7 captures falling edge, it generates a capture channel 7 pending. 0: Capture channel 7 fall lock Interrupt disable; 1: Capture channel 7 fall lock Interrupt enable.
14	R/W	0x0	CRIE7 If this enable bit is set 1, when capture channel 7 captures rising edge, it generates a capture channel 7 pending. 0: Capture channel 7 rise lock Interrupt disable; 1: Capture channel 7 rise lock Interrupt enable.

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Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	CFIE6 If this enable bit is set 1, when capture channel 6 captures falling edge, it generates a capture channel 6 pending. 0: Capture channel 6 fall lock Interrupt disable; 1: Capture channel 6 fall lock Interrupt enable.
12	R/W	0x0	CRIE6 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
11	R/W	0x0	CFIE5 If this enable bit is set 1, when capture channel 5 captures falling edge, it generates a capture channel 5 pending. 0: Capture channel 5 fall lock Interrupt disable; 1: Capture channel 5 fall lock Interrupt enable.
10	R/W	0x0	CRIE5 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
9	R/W	0x0	CFIE4 If this enable bit is set 1, when capture channel 4 captures falling edge, it generates a capture channel 4 pending. 0: Capture channel 4 fall lock Interrupt disable; 1: Capture channel 4 fall lock Interrupt enable.
8	R/W	0x0	CRIE4 If this enable bit is set 1, when capture channel 4 captures rising edge, it generates a capture channel 4 pending. 0: Capture channel 4 rise lock Interrupt disable; 1: Capture channel 4 rise lock Interrupt enable.

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Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	CFIE3 If this enable bit is set 1, when capture channel 3 captures falling edge, it generates a capture channel 3 pending. 0: Capture channel 3 fall lock Interrupt disable; 1: Capture channel 3 fall lock Interrupt enable.
6	R/W	0x0	CRIE3 If this enable bit is set 1, when capture channel 3 captures rising edge, it generates a capture channel 3 pending. 0: Capture channel 3 rise lock Interrupt disable; 1: Capture channel 3 rise lock Interrupt enable.
5	R/W	0x0	CFIE2 If this enable bit is set 1, when capture channel 2 captures falling edge, it generates a capture channel 2 pending. 0: Capture channel 2 fall lock Interrupt disable; 1: Capture channel 2 fall lock Interrupt enable.
4	R/W	0x0	CRIE2 If this enable bit is set 1, when capture channel 2 captures rising edge, it generates a capture channel 2 pending. 0: Capture channel 2 rise lock Interrupt disable; 1: Capture channel 2 rise lock Interrupt enable.
3	R/W	0x0	CFIE1 If this enable bit is set 1, when capture channel 1 captures falling edge, it generates a capture channel 1 pending. 0: Capture channel 1 fall lock Interrupt disable; 1: Capture channel 1 fall lock Interrupt enable.
2	R/W	0x0	CRIE1 If this enable bit is set 1, when capture channel 1 captures rising edge, it generates a capture channel 1 pending. 0: Capture channel 1 rise lock Interrupt disable; 1: Capture channel 1 rise lock Interrupt enable.

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Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CFIE0 If this enable bit is set 1, when capture channel 0 captures falling edge, it generates a capture channel 0 pending. 0: Capture channel 0 fall lock Interrupt disable; 1: Capture channel 0 fall lock Interrupt enable.
0	R/W	0x0	CRIE0 If this enable bit is set 1, when capture channel 0 captures rising edge, it generates a capture channel 0 pending 0: Capture channel 0 rise lock Interrupt disable; 1: Capture channel 0 rise lock Interrupt enable.

8.15.6.4 0x0014 Capture IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CFIS15 Capture channel 15 falling lock interrupt status. When capture channel 15 captures falling edge, if capture channel 15 fall lock interrupt (CFIE15) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 15 interrupt is not pending. 1: Capture channel 15 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 15 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
30	R/W1C	0x0	CRIS15 Capture channel 15 rising lock interrupt status. When capture channel 15 captures rising edge, if capture channel 15 rise lock interrupt (CRIE15) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 15 interrupt is not pending. 1: Capture channel 15 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 15 interrupt status.
29	R/W1C	0x0	CFIS14 Capture channel 14 falling lock interrupt status When capture channel 14 captures falling edge, if capture channel 14 fall lock interrupt (CFIE14) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 14 interrupt is not pending. 1: Capture channel 14 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 14 interrupt status.
28	R/W1C	0x0	CRIS14 Capture channel 14 rising lock interrupt status When capture channel 14 captures rising edge, if capture channel 14 rise lock interrupt (CRIE14) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 14 interrupt is not pending. 1: Capture channel 14 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 14 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
27	R/W1C	0x0	CFIS13 Capture channel 13 falling lock interrupt status When capture channel 13 captures falling edge, if capture channel 13 fall lock interrupt (CFIE13) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 13 interrupt is not pending. 1: Capture channel 13 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 13 interrupt status.
26	R/W1C	0x0	CRIS13 Capture channel 13 rising lock interrupt status When capture channel 13 captures rising edge, if capture channel 13 rise lock interrupt (CRIE13) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 13 interrupt is not pending. 1: Capture channel 13 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 13 interrupt status.
25	R/W1C	0x0	CFIS12 Capture channel 12 falling lock interrupt status When capture channel 12 captures falling edge, if capture channel 12 fall lock interrupt (CFIE12) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 12 interrupt is not pending. 1: Capture channel 12 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 12 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	CRIS12 Capture channel 12 rising lock interrupt status When capture channel 12 captures rising edge, if capture channel 12 rise lock interrupt (CRIE12) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 12 interrupt is not pending. 1: Capture channel 12 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 12 interrupt status.
23	R/W1C	0x0	CFIS11 Capture channel 11 falling lock interrupt status When capture channel 11 captures falling edge, if capture channel 11 fall lock interrupt (CFIE11) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 11 interrupt is not pending. 1: Capture channel 11 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 11 interrupt status.
22	R/W1C	0x0	CRIS11 Capture channel 11 rising lock interrupt status. When capture channel 11 captures rising edge, if capture channel 11 rise lock interrupt (CRIE11) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 11 interrupt is not pending. 1: Capture channel 11 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 11 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	CFIS10 Capture channel 10 falling lock interrupt status When capture channel 10 captures falling edge, if capture channel 10 fall lock interrupt (CFIE10) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 10 interrupt is not pending. 1: Capture channel 10 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 10 interrupt status.
20	R/W1C	0x0	CRIS10 Capture channel 10 rising lock interrupt status When capture channel 10 captures rising edge, if capture channel 10 rise lock interrupt (CRIE10) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 10 interrupt is not pending. 1: Capture channel 10 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 10 interrupt status.
19	R/W1C	0x0	CFIS9 Capture channel 9 falling lock interrupt status When capture channel 9 captures falling edge, if capture channel 9 fall lock interrupt (CFIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 9 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	CRIS9 Capture channel 9 rising lock interrupt status When capture channel 9 captures rising edge, if capture channel 9 rise lock interrupt (CRIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 9 interrupt status.
17	R/W1C	0x0	CFIS8 Capture channel 8 falling lock interrupt status When capture channel 8 captures falling edge, if capture channel 8 fall lock interrupt (CFIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 8 interrupt status.
16	R/W1C	0x0	CRIS8 Capture channel 8 rising lock interrupt status When capture channel 8 captures rising edge, if capture channel 8 rise lock interrupt (CRIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 8 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
15	R/W1C	0x0	CFIS7 Capture channel 7 falling lock interrupt status When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (CFIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capture channel 7 rising lock interrupt status When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (CRIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6 Capture channel 6 falling lock interrupt status When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (CFIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	CRIS6 Capture channel 6 rising lock interrupt status When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (CRIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capture channel 5 falling lock interrupt status When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (CFIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
10	R/W1C	0x0	CRIS5 Capture channel 5 rising lock interrupt status When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (CRIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	CFIS4 Capture channel 4 falling lock interrupt status When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (CFIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
8	R/W1C	0x0	CRIS4 Capture channel 4 rising lock interrupt status When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (CRIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (CFIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 3 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (CRIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (CFIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (CRIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 2 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (CFIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (CRIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (CFIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 0 interrupt status.

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Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (CRIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 0 interrupt status.

8.15.6.5 0x0020 PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PCCR01
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM01_CLK_SRC Select PWM01 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM01_CLK_DIV_M PWM01 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

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8.15.6.6 0x0024 PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PCCR23
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM23_CLK_SRC_SEL Select PWM23 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM23_CLK_DIV_M PWM23 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.15.6.7 0x0028 PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PCCR45
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM45_CLK_SRC_SEL Select PWM45 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/

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Offset: 0x0028			Register Name: PCCR45
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0000	PWM45_CLK_DIV_M PWM45 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.15.6.8 0x002C PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PCCR67
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM67_CLK_SRC_SEL Select PWM67 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM67_CLK_DIV_M PWM67 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

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8.15.6.9 0x0030 PWM89 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PCCR89
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM89_CLK_SRC_SEL Select PWM89 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM89_CLK_DIV_M PWM89 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.15.6.10 0x0034 PWMab Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PCCRab
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWMab_CLK_SRC_SEL Select PWMab clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/

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Offset: 0x0034			Register Name: PCCRab
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0000	PWMab_CLK_DIV_M PWMab clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.15.6.11 0x0038 PWMcd Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PCCRcd
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWMcd_CLK_SRC_SEL Select PWMcd clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWMcd_CLK_DIV_M PWMcd clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

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8.15.6.12 0x003C PWMef Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PCCRef
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWMef_CLK_SRC_SEL Select PWMef clock source 00: DCXO24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWMef_CLK_DIV_M PWMef clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.15.6.13 0x0040 PWM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PWM15_CLK_BYPASS Bypass clock source (after pre-scale) to PWM15 output 0: not bypass 1: bypass
30	R/W	0x0	PWM14_CLK_BYPASS Bypass clock source (after pre-scale) to PWM14 output 0: not bypass 1: bypass
29	R/W	0x0	PWM13_CLK_BYPASS Bypass clock source(after pre-scale) to PWM13 output 0: not bypass 1: bypass

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Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	PWM12_CLK_BYPASS Bypass clock source (after pre-scale) to PWM12 output 0: not bypass 1: bypass
27	R/W	0x0	PWM11_CLK_BYPASS Bypass clock source(after pre-scale) to PWM11 output 0: not bypass 1: bypass
26	R/W	0x0	PWM10_CLK_BYPASS Bypass clock source(after pre-scale) to PWM10 output 0: not bypass 1: bypass
25	R/W	0x0	PWM9_CLK_BYPASS Bypass clock source(after pre-scale) to PWM9 output 0: not bypass 1: bypass
24	R/W	0x0	PWM8_CLK_BYPASS Bypass clock source(after pre-scale) to PWM8 output 0: not bypass 1: bypass
23	R/W	0x0	PWM7_CLK_BYPASS Bypass clock source(after pre-scale) to PWM7 output 0: not bypass 1: bypass
22	R/W	0x0	PWM6_CLK_BYPASS Bypass clock source(after pre-scale) to PWM6 output 0: not bypass 1: bypass
21	R/W	0x0	PWM5_CLK_BYPASS Bypass clock source(after pre-scale) to PWM5 output 0: not bypass 1: bypass

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Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	PWM4_CLK_BYPASS Bypass clock source(after pre-scale) to PWM4 output 0: not bypass 1: bypass
19	R/W	0x0	PWM3_CLK_BYPASS Bypass clock source(after pre-scale) to PWM3 output 0: not bypass 1: bypass
18	R/W	0x0	PWM2_CLK_BYPASS Bypass clock source(after pre-scale) to PWM2 output 0: not bypass 1: bypass
17	R/W	0x0	PWM1_CLK_BYPASS Bypass clock source(after pre-scale) to PWM1 output 0: not bypass 1: bypass
16	R/W	0x0	PWM0_CLK_BYPASS Bypass clock source (after pre-scale) to PWM0 output 0: not bypass 1: bypass
15	R/W	0x0	PWM15_CLK_GATING Gating clock for PWM15 0: Mask 1: Pass
14	R/W	0x0	PWM14_CLK_GATING Gating clock for PWM14 0: Mask 1: Pass
13	R/W	0x0	PWM13_CLK_GATING Gating clock for PWM13 0: Mask 1: Pass
12	R/W	0x0	PWM12_CLK_GATING Gating clock for PWM12 0: Mask 1: Pass

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Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	PWM11_CLK_GATING Gating clock for PWM11 0: Mask 1: Pass
10	R/W	0x0	PWM10_CLK_GATING Gating clock for PWM10 0: Mask 1: Pass
9	R/W	0x0	PWM9_CLK_GATING Gating clock for PWM9 0: Mask 1: Pass
8	R/W	0x0	PWM8_CLK_GATING Gating clock for PWM8 0: Mask 1: Pass
7	R/W	0x0	PWM7_CLK_GATING Gating clock for PWM7 0: Mask 1: Pass
6	R/W	0x0	PWM6_CLK_GATING Gating clock for PWM6 0: Mask 1: Pass
5	R/W	0x0	PWM5_CLK_GATING Gating clock for PWM5 0: Mask 1: Pass
4	R/W	0x0	PWM4_CLK_GATING Gating clock for PWM4 0: Mask 1: Pass
3	R/W	0x0	PWM3_CLK_GATING Gating clock for PWM3 0: Mask 1: Pass
2	R/W	0x0	PWM2_CLK_GATING Gating clock for PWM2 0: Mask 1: Pass

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Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PWM1_CLK_GATING Gating clock for PWM1 0: Mask 1: Pass
0	R/W	0x0	PWM0_CLK_GATING Gating clock for PWM0 0: Mask 1: Pass

8.15.6.14 0x0060 PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: PDZCR01
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01 PWM01 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.15.6.15 0x0064 PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: PDZCR23
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN PWM23 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

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8.15.6.16 0x0068 PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: PDZCR45
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM45_DZ_INTV PWM45 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN PWM45 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.15.6.17 0x006C PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: PDZCR67
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM67_DZ_INTV PWM67 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN PWM67 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.15.6.18 0x0070 PWM89 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PDZCR89
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM89_DZ_INTV PWM89 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM89_DZ_EN PWM89 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

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8.15.6.19 0x0074 PWMab Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: PDZCRab
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWMab_DZ_INTV PWMab Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWMab_DZ_EN PWMab Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.15.6.20 0x0078 PWMcd Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: PDZCRcd
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWMcd_DZ_INTV PWMcd Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWMcd_DZ_EN PWMcd Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.15.6.21 0x007C PWMef Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PDZCRef
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWMef_DZ_INTV PWMef Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWMef_DZ_EN PWMef Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

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8.15.6.22 0x0080 PWM Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	PWM15_EN PWM Channel 15 Enable 0: PWM disable 1: PWM enable
14	R/W	0x0	PWM14_EN PWM Channel14 Enable 0: PWM disable 1: PWM enable
13	R/W	0x0	PWM13_EN PWM Channel 13 Enable 0: PWM disable 1: PWM enable
12	R/W	0x0	PWM12_EN PWM Channel 12 Enable 0: PWM disable 1: PWM enable
11	R/W	0x0	PWM11_EN PWM Channel 11 Enable 0: PWM disable 1: PWM enable
10	R/W	0x0	PWM10_EN PWM Channel 10 Enable 0: PWM disable 1: PWM enable
9	R/W	0x0	PWM9_EN PWM Channel 9 Enable 0: PWM disable 1: PWM enable
8	R/W	0x0	PWM8_EN PWM Channel 8 Enable 0: PWM disable 1: PWM enable
7	R/W	0x0	PWM7_EN PWM Channel 7 Enable 0: PWM disable 1: PWM enable

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Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	PWM6_EN PWM Channel 6 Enable 0: PWM disable 1: PWM enable
5	R/W	0x0	PWM5_EN PWM Channel 5 Enable 0: PWM disable 1: PWM enable
4	R/W	0x0	PWM4_EN PWM Channel 4 Enable 0: PWM disable 1: PWM enable
3	R/W	0x0	PWM3_EN PWM Channel 3 Enable 0: PWM disable 1: PWM enable
2	R/W	0x0	PWM2_EN PWM Channel 2 Enable 0: PWM disable 1: PWM enable
1	R/W	0x0	PWM1_EN PWM Channel 1 Enable 0: PWM disable 1: PWM enable
0	R/W	0x0	PWM0_EN PWM Channel 0 Enable 0: PWM disable 1: PWM enable

8.15.6.23 0x0090 PWM Group0 Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: PGR0
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG0_START PWM channels selected in PWMG0_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG0_EN PWM Group0 Enable

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Offset: 0x0090			Register Name: PGR0
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	PWMG0_CS If bit[i] is set, PWM i is selected as one channel of PWM Group0

8.15.6.24 0x0094 PWM Group1 Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: PGR1
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG1_START PWM channels selected in PWMG1_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG1_EN PWM Group1 Enable
15:0	R/W	0x0	PWMG1_CS If bit[i] is set, PWM i is selected as one channel of PWM Group1.

8.15.6.25 0x0098 PWM Group2 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: PGR2
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG2_START PWM channels selected in PWMG2_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG2_EN PWM Group2 Enable
15:0	R/W	0x0	PWMG2_CS If bit[i] is set, PWM i is selected as one channel of PWM Group2.

8.15.6.26 0x009C PWM Group3 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PGR3
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

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Offset: 0x009C			Register Name: PGR3
Bit	Read/Write	Default/Hex	Description
17	R/WAC	0x0	PWMG3_START PWM channels selected in PWMG3_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG3_EN PWM Group2 Enable
15:0	R/W	0x0	PWMG3_CS If bit[i] is set, PWM i is selected as one channel of PWM Group3.

8.15.6.27 0x00C0 Capture Enable Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	CAP15_EN When enable capture function, the 16-bit up-counter starts working and capture channel 15 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
14	R/W	0x0	CAP14_EN When enable capture function, the 16-bit up-counter starts working and capture channel 14 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
13	R/W	0x0	CAP13_EN When enable capture function, the 16-bit up-counter starts working and capture channel 13 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

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Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	CAP12_EN When enable capture function, the 16-bit up-counter starts working and capture channel 12 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
11	R/W	0x0	CAP11_EN When enable capture function, the 16-bit up-counter starts working and capture channel 11 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
10	R/W	0x0	CAP10_EN When enable capture function, the 16-bit up-counter starts working and capture channel 10 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
9	R/W	0x0	CAP9_EN When enable capture function, the 16-bit up-counter starts working and capture channel 9 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
8	R/W	0x0	CAP8_EN When enable capture function, the 16-bit up-counter starts working and capture channel 8 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

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Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	CAP7_EN When enable capture function, the 16-bit up-counter starts working and capture channel 7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
6	R/W	0x0	CAP6_EN When enable capture function, the 16-bit up-counter starts working and capture channel 6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
5	R/W	0x0	CAP5_EN When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
4	R/W	0x0	CAP4_EN When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
3	R/W	0x0	CAP3_EN When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

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Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CAP2_EN When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
1	R/W	0x0	CAP1_EN When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
0	R/W	0x0	CAP0_EN When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

8.15.6.28 0x0100+N*0x0020 PWM Control Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0020			Register Name: PCR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_PUL_NUM In pulse mode, PWM output pulse for PWM_CYCLE_NUM+1 times and then stop.
15:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM period register ready 0: PWM period register is ready to write 1: PWM period register is busy.

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Offset: 0x0100+N*0x0020			Register Name: PCR
Bit	Read/Write	Default/Hex	Description
10	R/WAC	0x0	PWM_PUL_START PWM pulse output start 0: no effect 1: output pulse for PWM_CYCLE_NUM+1 After finishing configuration for outputting pulse, set this bit once and then PWM would output waveform. After the waveform is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM output mode select 0: cycle mode 1: pulse mode
8	R/W	0x0	PWM_ACT_STA PWM active state 0: Low Level 1: High Level
7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1) K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256

8.15.6.29 0x0104+N*0x0020 PWM Period Register (Default Value: 0x0000_0000)

Offset: 0x0104+N*0x0020			Register Name: PPR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock 0 = 1 cycle 1 = 2 cycles ..... N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK .

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Offset: 0x0104+N*0x0020			Register Name: PPR
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	PWM_ACT_CYCLE Number of the active cycles in the PWM clock 0 = 0 cycle 1 = 1 cycles ..... N = N cycles

8.15.6.30 0x0108+N*0x0020 PWM Counter Register (Default Value: 0x0000_0000)

Offset: 0x0108+N*0x0020			Register Name: PCNTR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_COUNTER_START PWM counter value is set for phase control.
15:0	R	0x0	PWM_COUNTER_STATUS On PWM output or capture input, reading this register could get the current value of the PWM 16 bit up-counter.

8.15.6.31 0x010C+N*0x0020 PWM Pulse Counter Register (Default Value: 0x0000_0000)

Offset: 0x010C+N*0x0020			Register Name: PPCNTR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	PWM_PUL_COUNTER_STATUS On PWM output , reading this register could get the current value of the PWM pulse counter.

8.15.6.32 0x0110+N*0x0020 Capture Control Register (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x0020			Register Name: CCR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	CRLF When capture channel captures rising edge, the 16-bit up-counter's current value is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.

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Offset: 0x0110+N*0x0020			Register Name: CCR
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	CFLF When capture channel captures falling edge, the 16-bit up-counter's current value is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
2	R/W	0x0	CRTE Rising edge capture trigger enable
1	R/W	0x0	CFTE Falling edge capture trigger enable
0	R/W	0x0	CAPINV Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: not inverse 1: inverse

8.15.6.33 0x0114+N*0x0020 Capture Rise Lock Register (Default Value: 0x0000_0000)

Offset: 0x0114+N*0x0020			Register Name: CRLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CRLR When capture channel captures rising edge, the 16-bit up-counter's current value is latched to this register.

8.15.6.34 0x0118+N*0x0020 Capture Fall Lock Register (Default Value: 0x0000_0000)

Offset: 0x0118+N*0x0020			Register Name: CFLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CFLR When capture channel captures falling edge, the 16-bit up-counter's current value is latched to this register.

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8.16 SPI

8.16.1 Overview

The Serial Peripheral Interface (SPI) is a full-duplex, synchronous, four-wire serial communication interface between a CPU and SPI-compliant external devices. The SPI controller contains a 64 x 8 bits receiver buffer (RXFIFO) and a 64 x 8 bits transmit buffer (TXFIFO). It can work in master mode and slave mode.

The SPI has the following features:

- Three SPI interfaces:
  - SPI0 and SPI2 in CPUX Domain
  - S_SPI0 in CPUS Domain
- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmmable serial data frame length of 1 bit to 32 bits
- Maximum clock frequency: 100MHz
- TX/RX DMA slave interface
- 8-bit wide and 64-entry FIFO for both transmitting and receiving data
- 8-bit wide and 4-entry buffer for transmitting
- 8-bit wide and 128-entry buffer for receiving data
- Supports mode0, mode1, mode2, and mode3
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

NOTE

This chapter only describes SPI0, SPI2, and S_SPI0. For detailed information of SPI1 (supports SPI mode and DBI mode), please refer to section 8.17 SPI_DBI.

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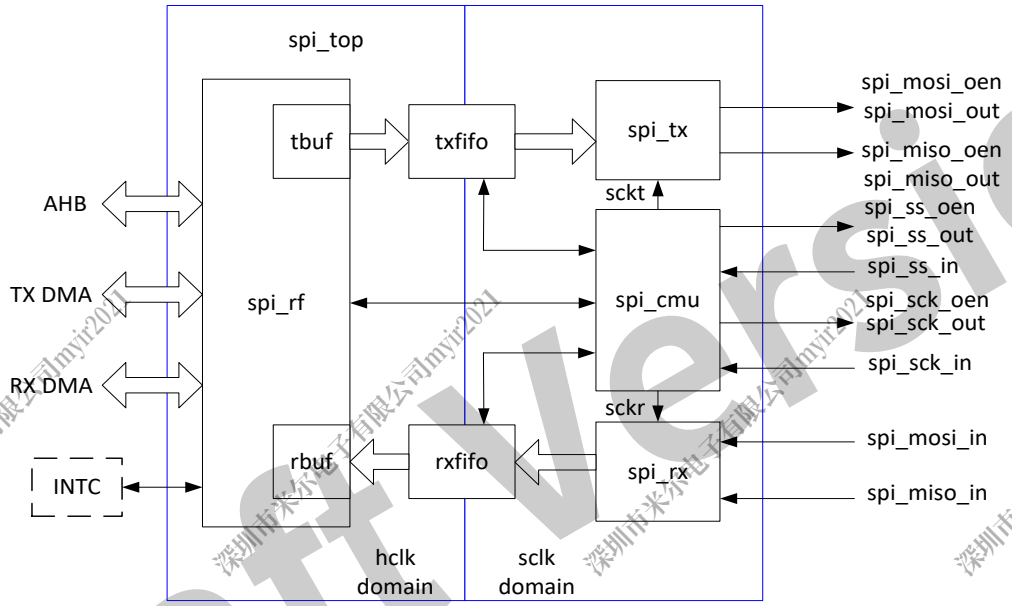
8.16.2 Block Diagram

The following figure shows a block diagram of the SPI.

Figure 8-77 SPI Block Diagram



SPI contains the following sub-blocks:

Table 8-44 SPI Sub-blocks

Sub-block	Description
spi_rf	Responsible for implementing the internal register, interrupt, and DMA Request.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	Responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.
spi_tx	Responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	Responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.

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8.16.3 Functional Description

8.16.3.1 External Signals

The following table describes the external signals of SPI. The MOSI and MISO are bidirectional I/O, when SPI is as a master device, the CLK and CS are the output pin; when SPI is as a slave device, the CLK and CS are the input pin. When using SPI, the corresponding PADs are selected as SPI function via section 8.6 GPIO.

Table 8-45 SPI External Signals

Signal Name	Description	Type
SPI0-CS[1:0]	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal Provides serial interface timing.	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI0-HOLD	SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI2-CS0	SPI2 Chip Select Signal, Low Active	I/O
SPI2-CLK	SPI2 Clock Signal Provides serial interface timing.	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
S-SPI0-CS0	S-SPI Chip Select Signal, Low Active	I/O
S-SPI0-CLK	S-SPI Clock Signal Provides serial interface timing.	I/O
S-SPI0-MOSI	S-SPI Master Data Out, Slave Data In	I/O
S-SPI0-MISO	S-SPI Master Data In, Slave Data Out	I/O

8.16.3.2 Clock Sources

Every SPI controller gets 5 different clock sources, users can select one of them to make SPI clock source. The following table describes the clock sources for SPI. For more details on the clock setting, configuration, and gating information, see section 2.7 Clock Controller Unit (CCU) and section 2.13 Power Reset Clock Management (PRCM).

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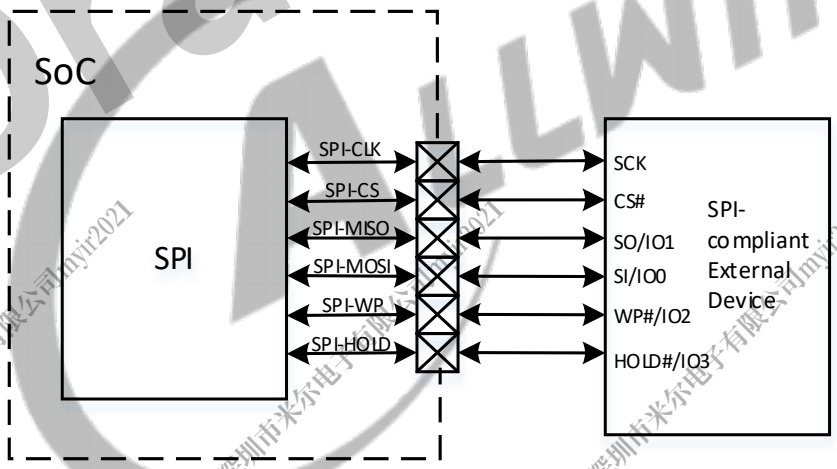
Table 8-46 SPI Clock Sources

SPI	Clock Sources	Description	Clock Module
SPI0, SPI2	HOSC	24 MHz Crystal	CCU
	PERI0_200M	Peripheral Clock, default value is 200 MHz.	
	PERI0_300M	Peripheral Clock, default value is 300 MHz.	
	PERI1_200M	Peripheral Clock, default value is 200 MHz.	
	PERI1_300M	Peripheral Clock, default value is 300 MHz.	
S_SPI0	DCXO24M	24 MHz Crystal	PRCM
	PERIPLL_DIV	Peripheral Clock, default value is 200 MHz.	
	PERI0_300M	Peripheral Clock, default value is 300 MHz.	
	PERI1_300M	Peripheral Clock, default value is 300 MHz.	
	AUDIO1PLL4X	Audio system clock, the defult value is 768 MHz.	

8.16.3.3 Typical Application

The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 8-78 SPI Application Block Diagram



8.16.3.4 SPI Transmit Format

The SPI supports 4 different formats for data transfer. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR (Offset: 0x0008). The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

The CPOL (SPI_TCR [1]) defines the polarity of the clock signal (SPI_SCLK). The SPI_SCLK is a high level when CPOL is '1' and it is a low level when CPOL is '0'. The CPHA (SPI_TCR [0]) decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used to setup data when CPHA is '1', and sample data when CPHA is '0'. The following table lists the four modes.

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Table 8-47 SPI Transmit Format

Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
Mode0	0	0	Sample on the rising edge	Setup on the falling edge
Mode1	0	1	Setup on the rising edge	Sample on the falling edge
Mode2	1	0	Sample on the falling edge	Setup on the rising edge
Mode3	1	1	Setup on the falling edge	Sample on the rising edge

The following figures describe four waveform for SPI_SCLK.

Figure 8-79 SPI Phase 0 Timing Diagram

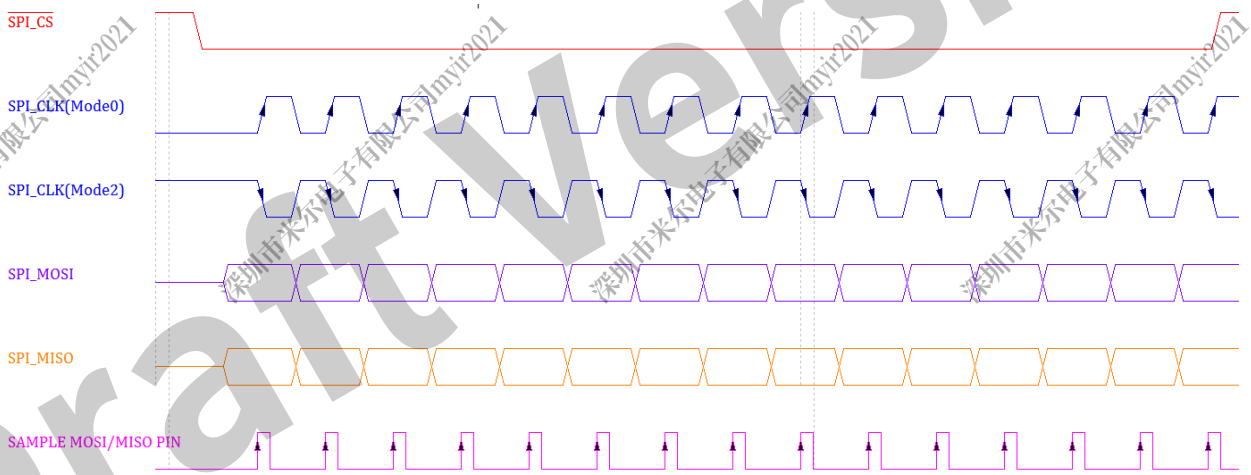
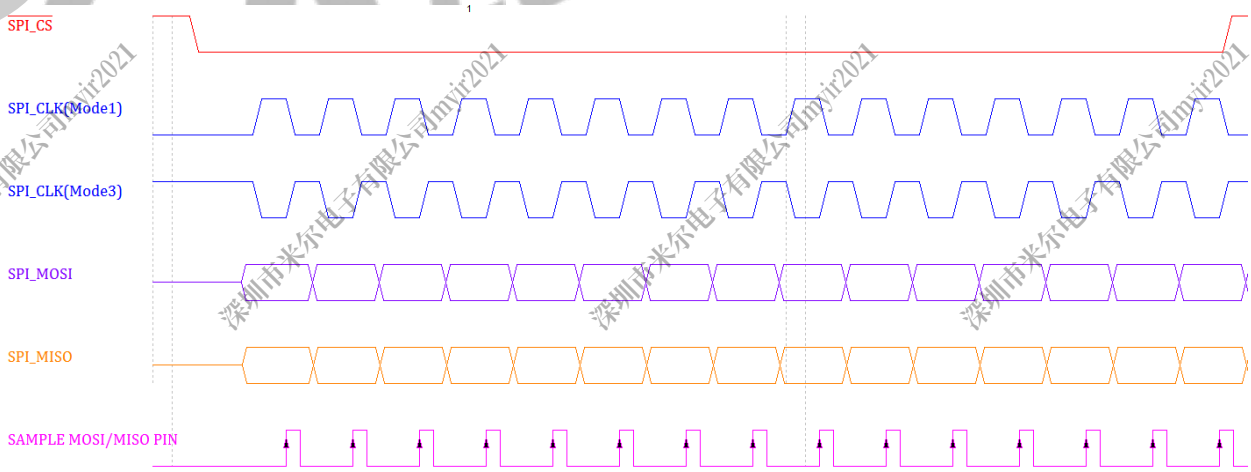


Figure 8-80 SPI Phase 1 Timing Diagram



8.16.3.5 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATCR [1:0]) is equal to 0x2. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes the 3-wire mode.

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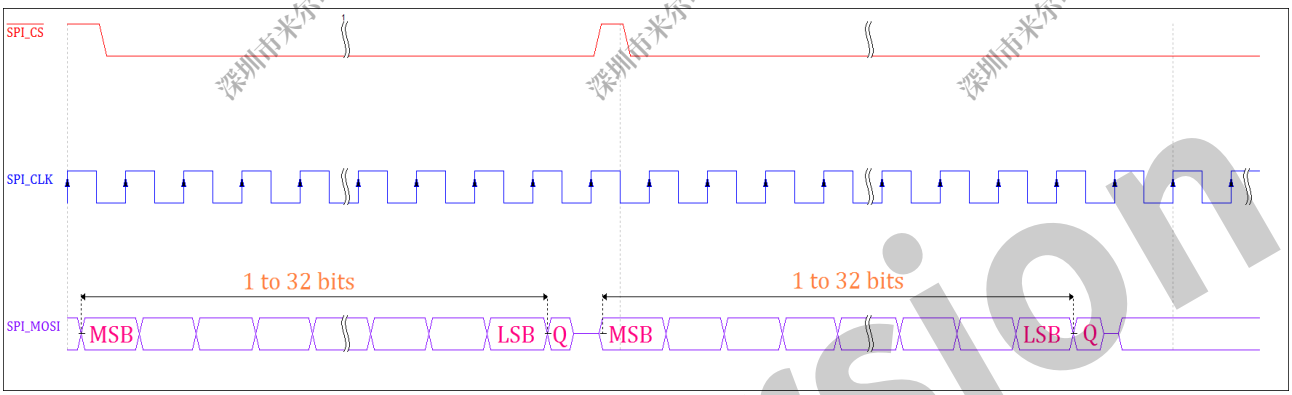
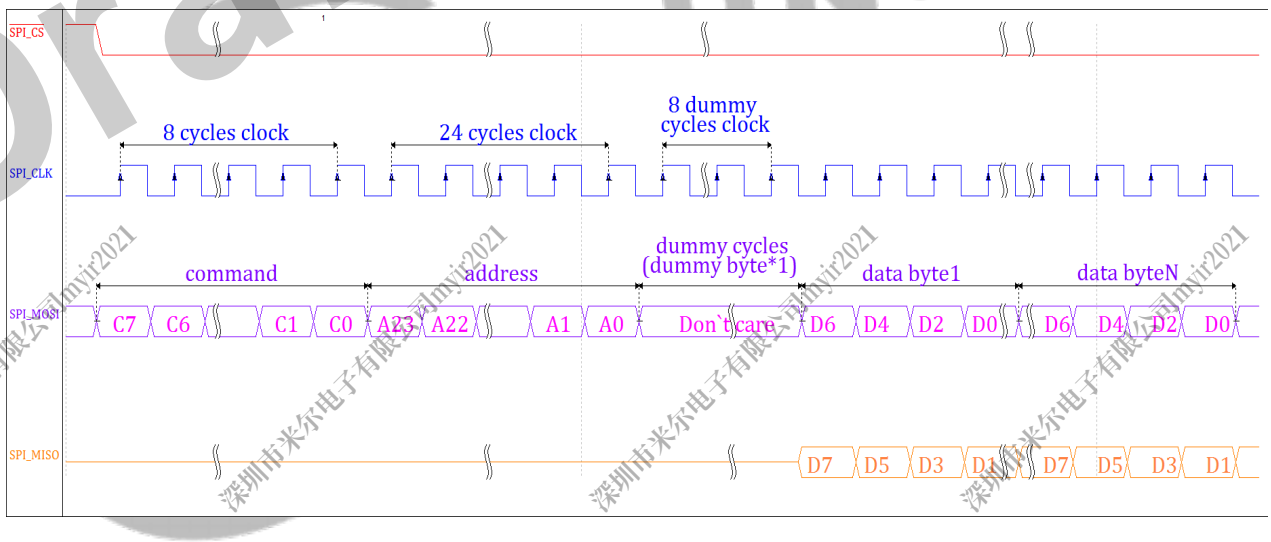
Figure 8-81 SPI 3-Wire Mode



8.16.3.6 SPI Dual-Input/Dual-Output and Dual I/O Mode

The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC (Offset: 0x0038) [28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI.

Figure 8-82 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

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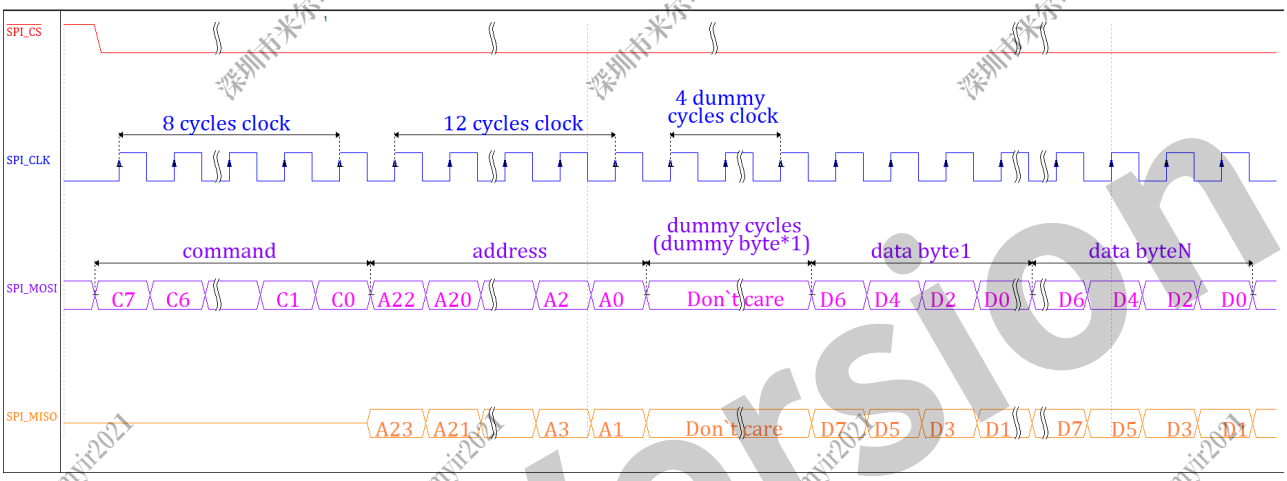
Figure 8-83 SPI Dual I/O Mode

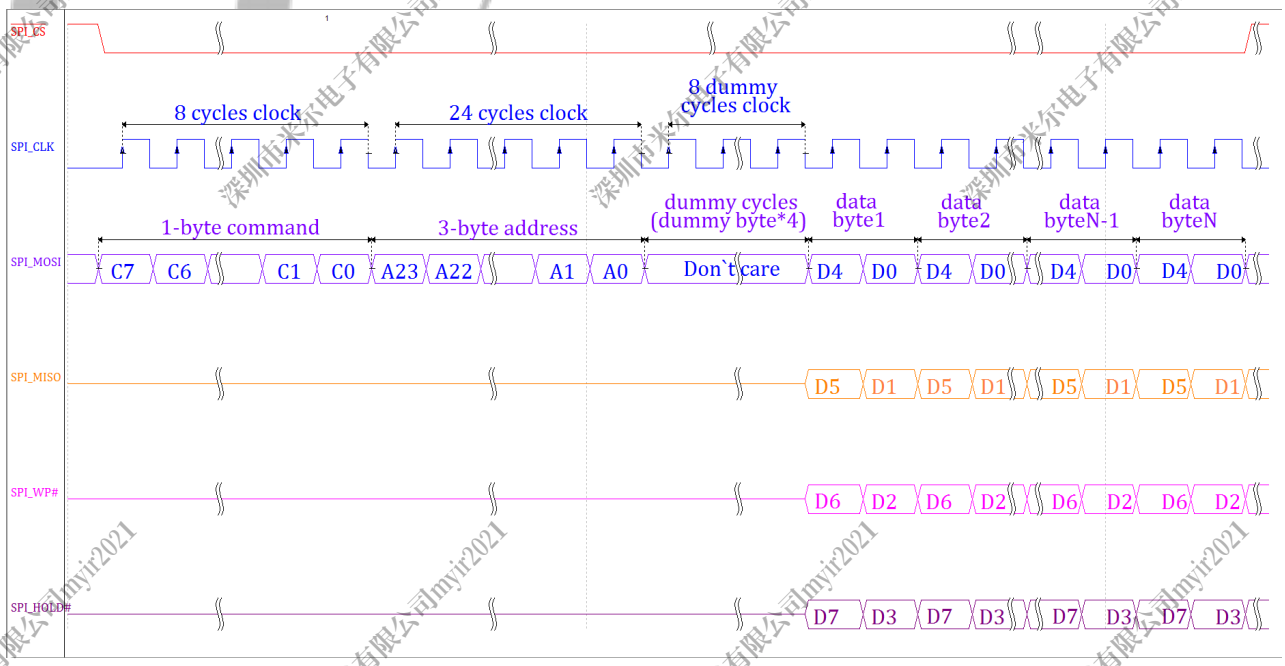


In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

8.16.3.7 SPI Quad-Input/Quad-Output Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC (Offset: 0x0038) [29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#) and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Figure 8-84 SPI Quad-Input/Quad-Output Mode



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In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

8.16.3.8 Transmission/Reception Bursts in Master Mode

In SPI master mode, the transmission and reception bursts (byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmission bursts are written in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. The transmission bursts in single mode before automatically sending dummy bursts are written in STC (bit [23:0]) of the SPI Master Burst Control Counter Register. For dummy data, the SPI controller can automatically send before receiving by writing DBC (bit [27:24]) in the SPI Master Burst Control Counter Register. If users do not use the SPI controller to send dummy data automatically, then the dummy bursts are used as the transmission counters to write together in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. In master mode, the total burst numbers are written in MBC (bit [23:0]) of the SPI Master Burst Counter Register. When all transmission and reception bursts are transferred, the SPI controller will send a completed interrupt, at the same time, the SPI controller will clear DBC, MWTC, and MBC.

8.16.3.9 SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz–100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in the master mode. The SPI clock is selected from different clock sources, the SPI must configure different work mode. There are three work modes: normal sample mode, delay half-cycle sample mode, delay one-cycle sample mode. Delay half-cycle sample mode is the default mode of the SPI controller. When the SPI runs at 40 MHz or below 40 MHz, the SPI can work at normal sample mode or delay half-cycle sample mode. When the SPI runs over 80 MHz, setting the SDC bit in the SPI Transfer Control Register to '1' makes the internal read sample point with a half-cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. The following tables show the different configurations of the SPI sample mode.

Table 8-48 SPI Old Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24 MHz
delay half cycle sample	0	0	<=40 MHz
delay one cycle sample	0	1	>=80 MHz

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CAUTION

The remaining spectrum is not recommended. Because when the output delay of SPI flash (refer to the datasheet of the manufactures for the specific delay time) is the same with the half-cycle time of SPI working clock, the variable edge of the output data for the device bumps into the clock sampling edge of the controller, so setting 1 cycle of sampling delay would cause stability problem.

Table 8-49 SPI New Sample Mode

SPI Sample Mode	SDM (bit13)	SDC (bit11)	SDC1 (bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

8.16.3.10 SPI Error Conditions

If any error conditions occur, the hardware will set the corresponding status bits in the SPI Interrupt Status Register (Offset: 0x0014) and stop the transfer. For the SPI controller, the following error scenarios can happen.

- TX_FIFO Underrun

The TX_FIFO underrun happens when the CPU/DMA reads data from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- TX_FIFO Overflow

The TX_FIFO overflow happens when the CPU/DMA writes data into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Underrun

The RX_FIFO underrun happens when the CPU/DMA reads data from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt

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if interrupts are enabled. The software has to clear the error bit and the RF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Overflow

The RX_FIFO overflow happens when the CPU/DMA writes data into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

8.16.4 Programming Guidelines

8.16.4.1 Writing/Reading Data Process

The SPI transfers serial data between the processor and the external device. The CPU mode and DMA mode are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX channel and RX channel. The TX channel has the path from TX FIFO to the external device. The RX channel has the path from the external device to RX FIFO.

Write Data: The CPU or DMA must write data on the SPI_TXD (Offset: 0x0200), the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, the CPU or DMA must access the SPI_RXD (Offset: 0x0300) and the data are automatically sent to the SPI_RXD (Offset: 0x0300).

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor after each transmission is complete.

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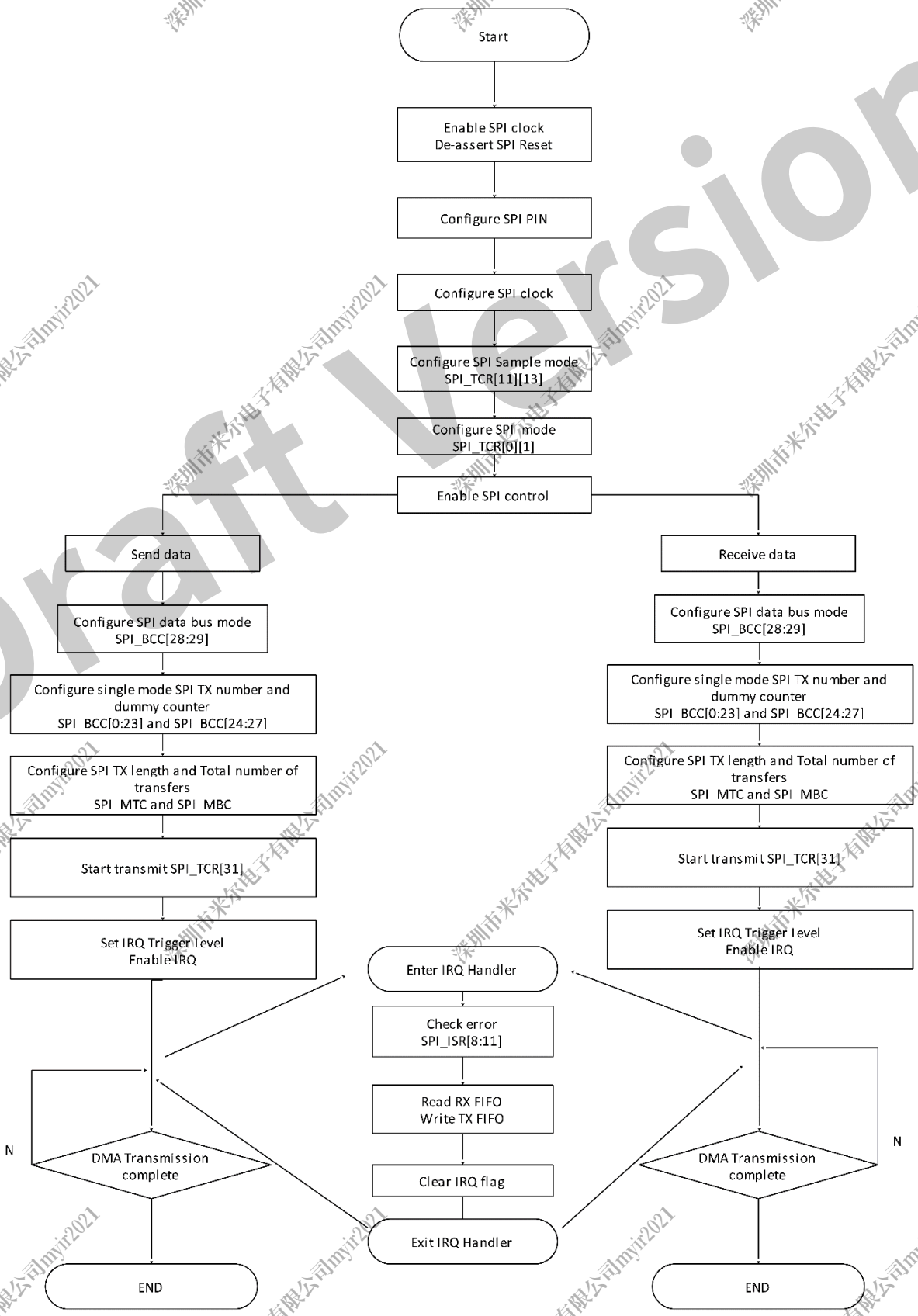
CPU Mode

Figure 8-85 SPI Write/Read Data in CPU Mode



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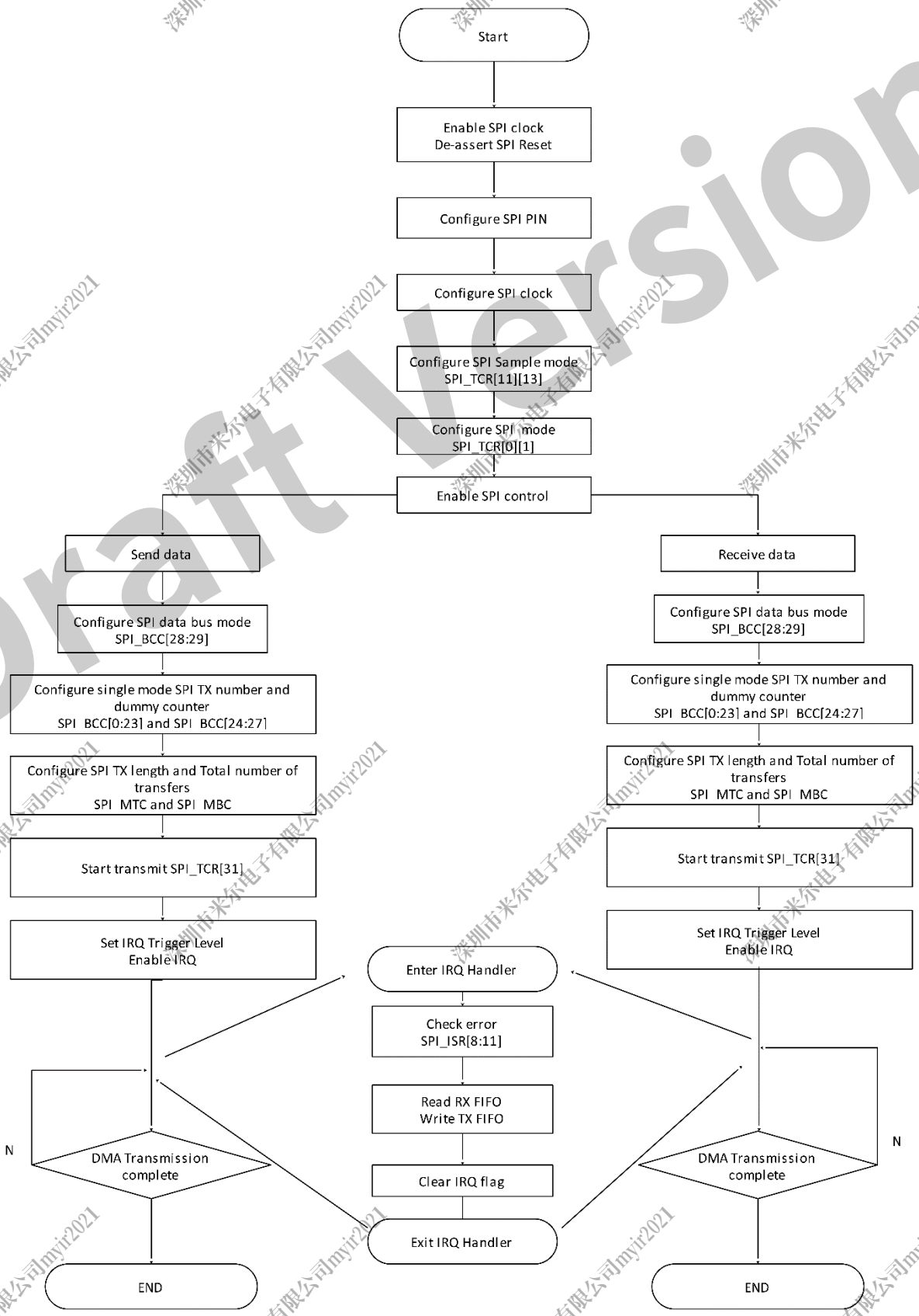
DMA Mode

Figure 8-86SPI Write/Read Data in DMA Mode



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8.16.5 Register List

Module Name	Base Address
SPI0	0x0402 5000
SPI2	0x0402 7000
S_SPI0	0x0709 2000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter register
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register
SPI_BSR	0x0400	SPI BUF Status register

8.16.6 Register Description

8.16.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect.
30:8	/	/	/

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Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: stop transmit data when RXFIFO full 0: normal operation, ignore RXFIFO status **Note: This bit cannot be written when XCH=1.**
6:3	/	/	/
2	R/W	0x0	MODE_SEL Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing **Note: This bit cannot be written when XCH=1.**
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode **Note: This bit cannot be written when XCH=1.**
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable **Note: After transforming from bit_mode to byte_mode, it must Enable the SPI Module again.**

8.16.6.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write “1” to SRST will also clear this bit. Write ‘0’ to this bit has no effect. **Note: This bit cannot be written when XCH=1.**
30:16	/	/	/

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Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point **Note: This bit cannot be written when XCH=1.**
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual I/O mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1 - Normal Sample Mode 0 - Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first **Note：Can't be written when XCH=1.**

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Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point **Note: This bit can't be written when XCH=1.**
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode Note: Can't be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one **Note: This bit can't be written when XCH=1.**
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. **Note: This bit can't be written when XCH=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: This bit can't be written when XCH=1.**

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Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: This bit can't be written when XCH=1.**
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: This bit can't be written when XCH=1.**
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts **Note: This bit can't be written when XCH=1.**
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: This bit can't be written when XCH=1.**
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: This bit can't be written when XCH=1.**
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) **Note: This bit can't be written when XCH=1.**

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8.16.6.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

8.16.6.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, when set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed

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Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	TF_UDF TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty

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Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing "1" to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL <= RX_TRIG_LEVEL 1: RX_WL > RX_TRIG_LEVEL This bit is set any time if RX_WL > RX_TRIG_LEVEL. Writing "1" to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.16.6.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write '1' to this bit will reset the control portion of the TX FIFO and auto clear to '0' when completing reset operation, write to '0' has no effect.

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Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable In normal mode, TX FIFO can only be read by SPI controller, write '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable

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Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level CAUTION: Whether in CPU mode or in DMA mode, trigger level should be set properly that actual data amount reaches trigger level.

8.16.6.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO ... 64 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO + RX BUFFER 0: 0 byte in RX FIFO & RX BUFFER 1: 1 byte in RX FIFO & RX BUFFER ... 64: 64 bytes in RX FIFO & RX BUFFER ... 192:192bytes in RX FIFO & RX BUFFER other: Reserved

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8.16.6.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch waits clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. **Note: This bit can't be written when XCH=1.**
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted Note: 1. Can't be written when XCH=1;

8.16.6.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

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8.16.6.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst ... N: N bursts Note: (i) Can't be written when XCH=1; (ii) Total transfer data, include the TXD, RXD and dummy burst.

8.16.6.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

8.16.6.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

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Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable **Note:** • **Can't be written when XCH=1;** • **Quad mode includes Quad-Input and Quad-Output.**
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode **Note:** • **Can't be written when XCH=1;** • **It is only valid when Quad_Mode_EN=0.**
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don't care by the device. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

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8.16.6.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bit's frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Write "1" to this bit will start to transfer serial bits' frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed **Note: It is only valid when Work Mode Select==0x10/0x11.**
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable **Note: It is only valid when Work Mode Select==0x10/0x11.**

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Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
15:14	/	/	/
13:8	R/W	0x00	TX_FRM_LEN Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**

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Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
1:0	R/W	0x0	*WMS* *Work Mode Select* 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

8.16.6.13 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. Note: In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

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8.16.6.14 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. Note: In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

8.16.6.15 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: DMA_active is low 01: DMA_active is high 10: DMA_active is controlled by dma_request(DRQ) 11:DMA_active is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ACK 1: active fall must after detect ACK is high
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to dma_active high

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8.16.6.16 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note: This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

8.16.6.17 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

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8.16.6.18 0x0400 SPI BUF Status Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
15:8	/	/	/
7:0	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer

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8.17 SPI_DBI

8.17.1 Overview

The T527 provides a 3/4 line SPI display bus interface (SPI_DBI) for video data transmission. It supports DBI mode or SPI mode. The DBI mode is compatible with multiple video data formats at the same time. The SPI mode is used for low-cost display schemes.

The SPI mode has the following features:

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
- Maximum clock frequency: 100MHz
- TX/RX DMA slave interface
- 8-bit wide by 64-entry FIFO for both transmitting and receiving data
- Supports mode0, mode1, mode2, and mode3
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

The DBI mode has the following features:

- DBI Type C 3 Line/4 Line Interface Mode
- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

NOTE

This chapter only describes SPI1 (SPI mode and DBI mode). For detailed information of SPI0, SPI2, and S_SPI0, please refer to section 8.16 SPI.

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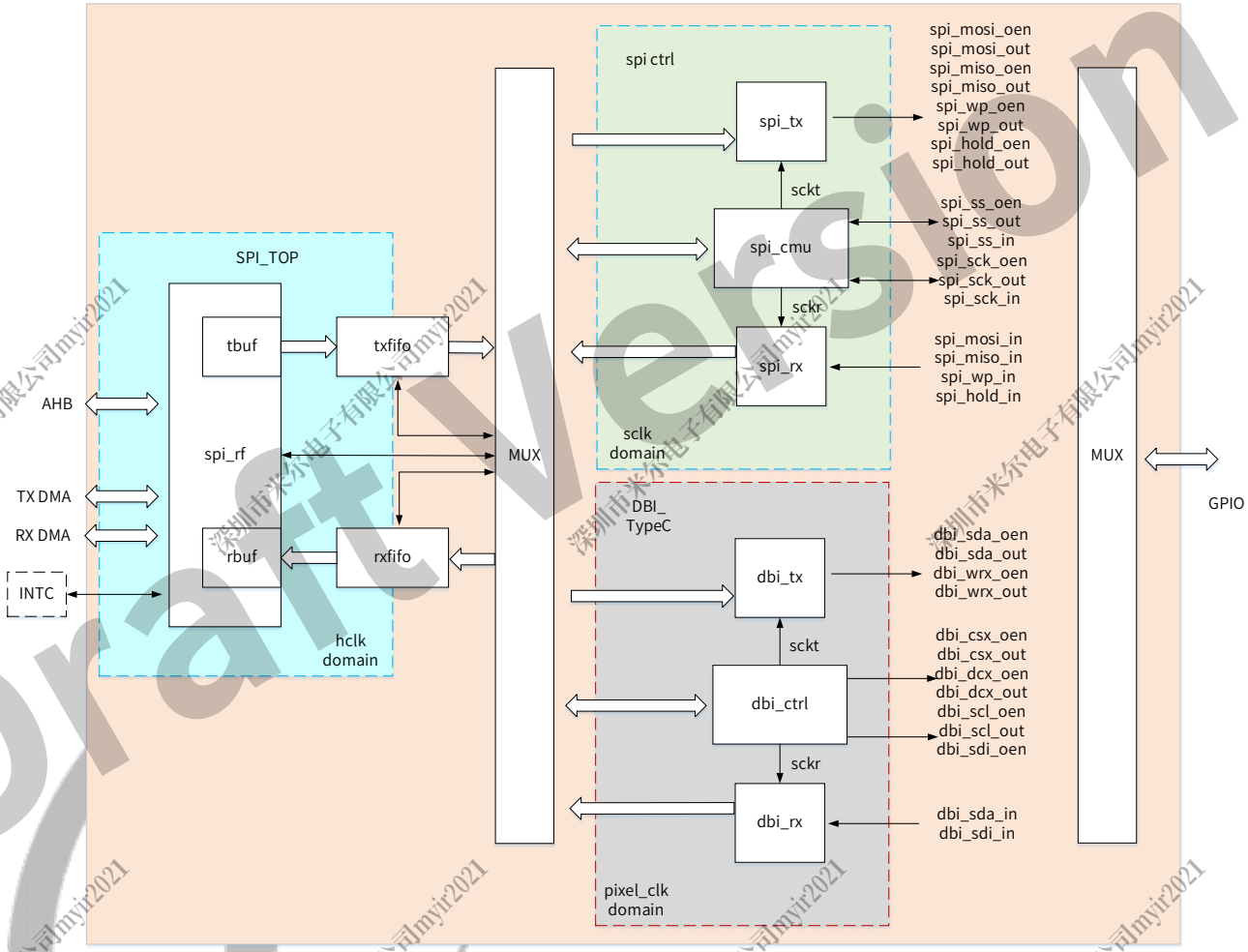
8.17.2 Block Diagram

The following figure shows a block diagram of the SPI_DBI.

Figure 8-87 SPI_DBI Block Diagram



SPI_DBI contains the following sub-blocks:

Table 8-50 SPI_DBI Sub-blocks

Sub-block	Description
spi_rf	Responsible for implementing the internal register, interrupt, and DMA Request.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	Responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.

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Sub-block	Description
spi_tx	Responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	Responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.
dbi_ctrl	Responsible for implementing DBI bus clock, chip select, data command select, RGB format reshape.
dbi_tx	Responsible for implementing DBI data transfer, the interface of the internal TXFIFO, and status register.
dbi_rx	Responsible for implementing DBI data receive, the interface of the internal RXFIFO, and status register.

8.17.3 Functional Description

8.17.3.1 External Signals

The following table describes the external signals of SPI_DBI. When using SPI_DBI, the corresponding PADs are selected as SPI_DBI function via section 8.6 GPIO.

Table 8-51 GPIO multiplexing of SPI1 and DBI

DBI	SPI1
DBI-CSX	SPI1-CS0
DBI-SCLK	SPI1-CLK
DBI-SDO	SPI1-MOSI
DBI-SDI/ DBI-TE/ DBI-DCX	SPI1-MISO
DBI-DCX/DBI-WRX	SPI1-HOLD
DBI-TE	SPI1-WP

Table 8-52 SPI_DBI External Signals

Signal Name	Description	Type
SPI Mode		
SPI1-CS0	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal Provides serial interface timing.	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O

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Signal Name	Description	Type
SPI1-HOLD	SPI1 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
DBI Mode		
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

8.17.3.2 Clock Sources

The SPI_DBI controller gets 5 different clock sources, users can select one of them to make SPI_DBI clock source. The following table describes the clock sources for SPI_DBI. For more details on the clock setting, configuration, and gating information, see section 2.7 Clock Controller Unit (CCU).

Table 8-53 SPI_DBI Clock Sources

Clock Sources	Description	Clock Module
HOSC	24 MHz Crystal	CCU
PERI0_200M	Peripheral Clock, default value is 200 MHz.	
PERI0_300M	Peripheral Clock, default value is 300 MHz.	
PERI1_200M	Peripheral Clock, default value is 200 MHz.	
PERI1_300M	Peripheral Clock, default value is 300 MHz.	

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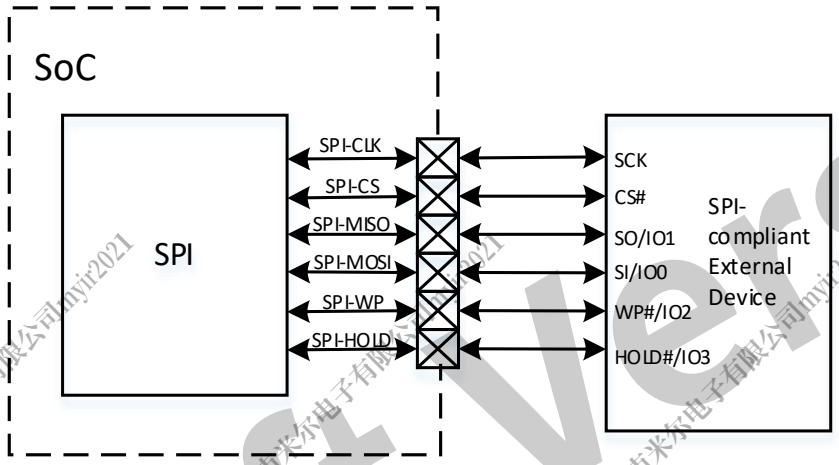
8.17.3.3 Typical Application

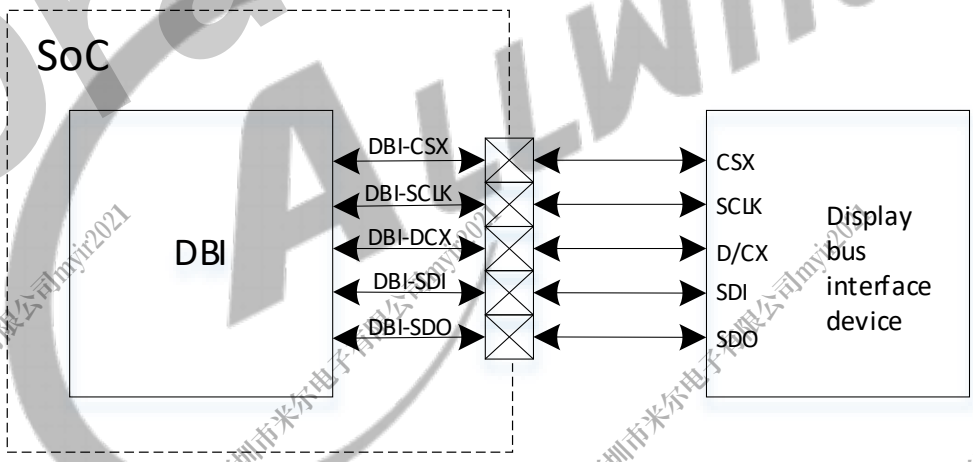
The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 8-88 SPI Application Block Diagram



The following figure shows the application block diagram when the DBI master device is connected to a display bus interface device.

Figure 8-89 DBI Application Block Diagram



8.17.3.4 SPI Transmission Format

The SPI supports 4 different formats for data transmission. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

The CPOL (SPI_TCR[1]) defines the polarity of the clock signal (SPI_SCLK). The SPI_SCLK is a high level when CPOL is '1' and it is a low level when CPOL is '0'. The CPHA (SPI_TCR[0]) decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used to setup data when CPHA is '1', and sample data when CPHA is '0'. The following table lists the four modes.

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Table 8-54 SPI Transmit Format

SPI Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
mode0	0	0	Sample on the rising edge	Setup on the falling edge
mode1	0	1	Setup on the rising edge	Sample on the falling edge
mode2	1	0	Sample on the falling edge	Setup on the rising edge
mode3	1	1	Setup on the falling edge	Sample on the rising edge

The following figures describe four waveforms for SPI_SCLK.

Figure 8-90 SPI Phase 0 Timing Diagram

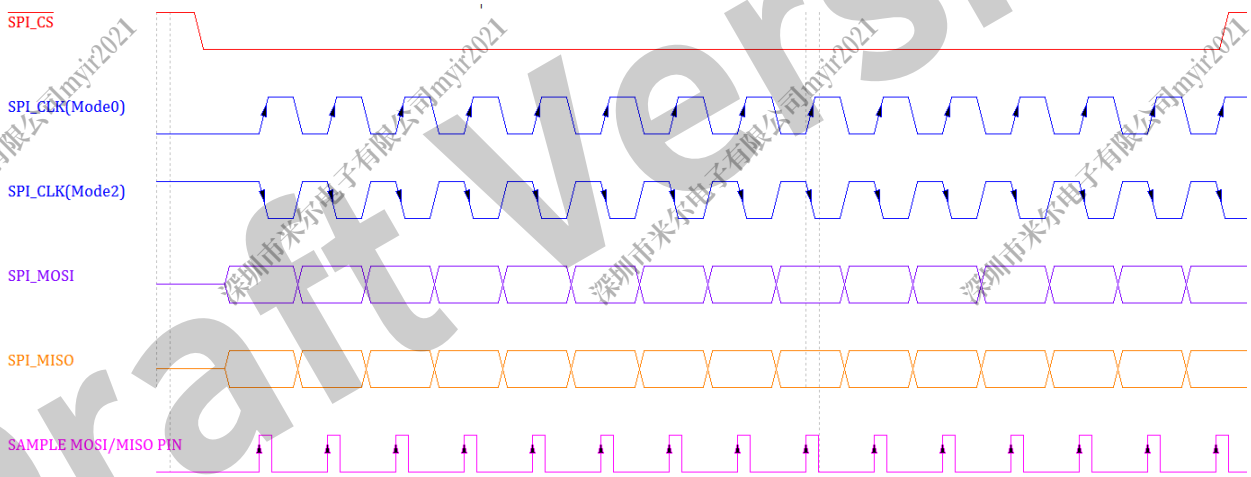
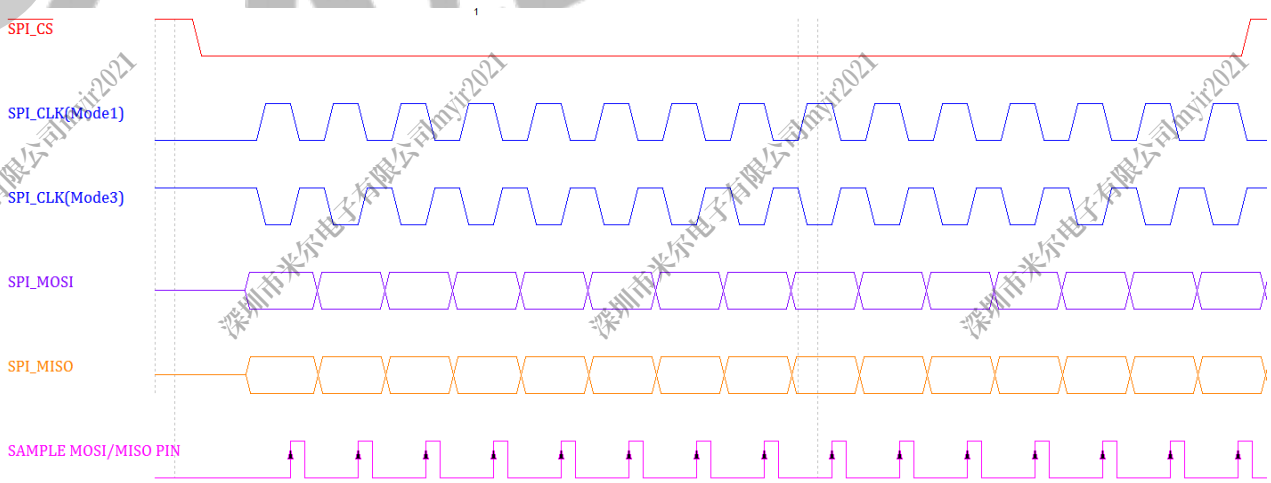


Figure 8-91 SPI Phase 1 Timing Diagram



8.17.3.5 SPI Master and Slave Mode

The SPI controller can be configured to a master or slave device. The master mode is selected by setting the MODE bit (SPI_GCR[1]); the slave mode is selected by clearing the MODE bit.

In master mode, the SPI_CLK is generated and transmitted to the external device, and the data from the TX FIFO is transmitted on the MOSI pin, the data from the slave is received on the MISO pin and sent to RX FIFO. The Chip Select (SPI_SS) is an active low signal, and it must be set low

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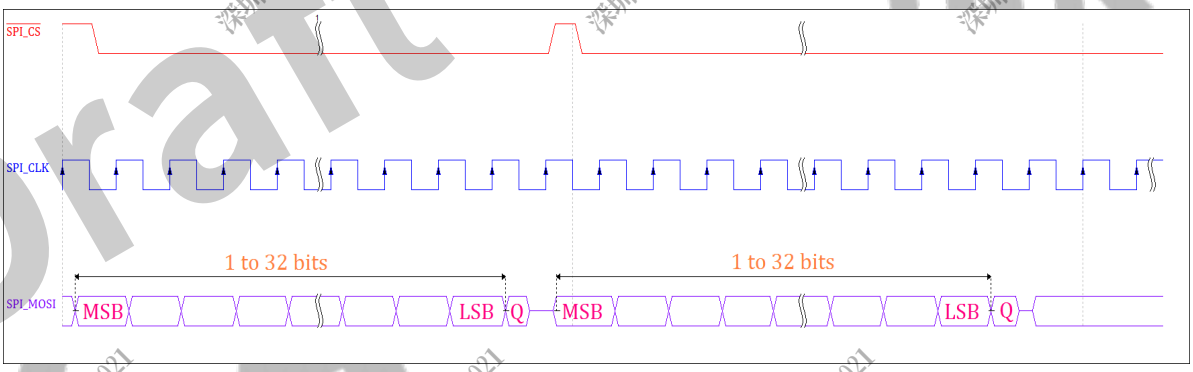
before the data are transmitted or received. The SPI_SS can be selected the auto control mode or the software manual control mode. When using auto control, the SS_OWNER (SPI_TCR[6]) must be cleared (default value is 0); when using manual control, the SS_OWNER must be set. And the level of SPI_SS is controlled by SS_LEVEL (SPI_TCR[7]).

In slave mode, after the software selects the MODE bit (SPI_GCR [1]) to '0', it waits for master initiate a transaction. When the master asserts SPI_SS, and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on the MISO pin, and the data from the MOSI pin is received in RX FIFO.

8.17.3.6 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATC [1:0]) is equal to 0x2. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes the 3-wire mode.

Figure 8-92 SPI 3-Wire Mode



8.17.3.7 SPI Dual-Input/Dual-Output and Dual I/O Mode

The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC [28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode SPI

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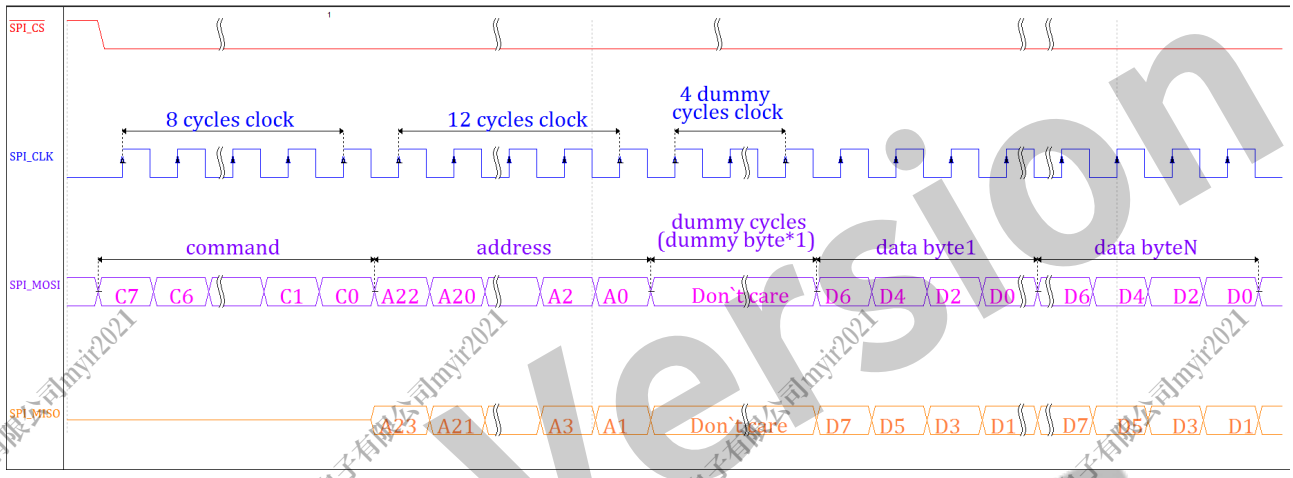
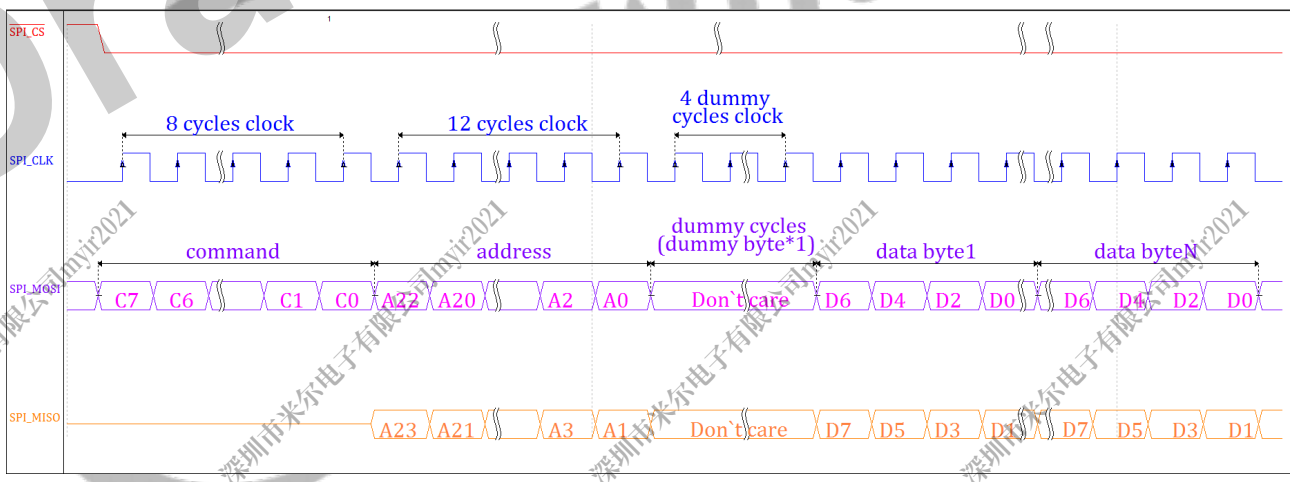
devices, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI

Figure 8-93 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 8-94 SPI Dual I/O Mode



In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

8.17.3.8 SPI Quad-Input/Quad-Output Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC [29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#)

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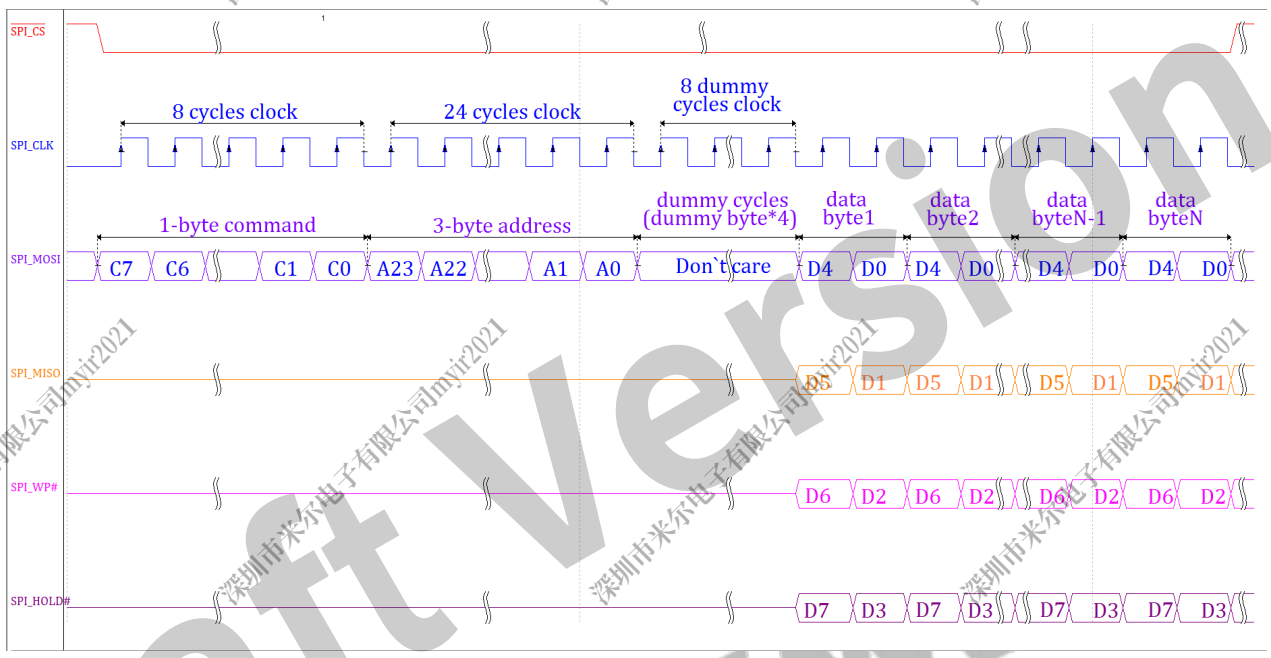
and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Figure 8-95 SPI Quad-Input/Quad-Output Mode



In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

8.17.3.9 Transmission/Reception Bursts in Master Mode

In SPI master mode, the transmission and reception bursts (byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmission bursts are written in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. The transmission bursts in single mode before automatically sending dummy bursts are written in STC (bit [23:0]) of the SPI Master Burst Control Counter Register. For dummy data, the SPI controller can automatically send before receiving by writing DBC (bit [27:24]) in the SPI Master Burst Control Counter Register. If users do not use the SPI controller to send dummy data automatically, then the dummy bursts are used as the transmission counters to write together in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. In master mode, the total burst numbers are written in MBC (bit [23:0]) of the SPI Master Burst Counter Register. When all transmission and reception bursts are transferred, the SPI controller will send a completed interrupt, at the same time, the SPI controller will clear DBC, MWTC, and MBC.

8.17.3.10 SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz–100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in the master mode. The SPI clock is selected from different clock sources, the SPI must configure different work mode. There are three

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work modes: normal sample mode, delay half-cycle sample mode, delay one-cycle sample mode. Delay half-cycle sample mode is the default mode of the SPI controller. When the SPI runs at 40 MHz or below 40 MHz, the SPI can work at normal sample mode or delay half-cycle sample mode. When the SPI runs over 80 MHz, setting the SDC bit in the SPI Transfer Control Register to '1' makes the internal read sample point with a half-cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. The following tables show the different configurations of the SPI sample mode.

Table 8-55 SPI Old Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24 MHz
delay half cycle sample	0	0	<=40 MHz
delay one cycle sample	0	1	>=80 MHz

CAUTION

The remaining spectrum is not recommended. Because when the output delay of SPI flash (refer to the datasheet of the manufactures for the specific delay time) is the same with the half-cycle time of SPI working clock, the variable edge of the output data for the device bumps into the clock sampling edge of the controller, so setting 1 cycle of sampling delay would cause stability problem.

Table 8-56 SPI New Sample Mode

SPI Sample Mode	SDM (bit13)	SDC (bit11)	SDC1 (bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

8.17.3.11 DBI 3-Line Interface Writing and Reading Timing

The 3-line DBI Interface I contains CSX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 3-line DBI Interface II contains CSX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

Since the 3-line display bus mode has no Data/Command data line indicating whether Data or Command is currently being transmitted, an extra bit is added to the data-stream before MSB to indicate whether Data or Command is currently being transmitted. (0: Command, 1: Data)

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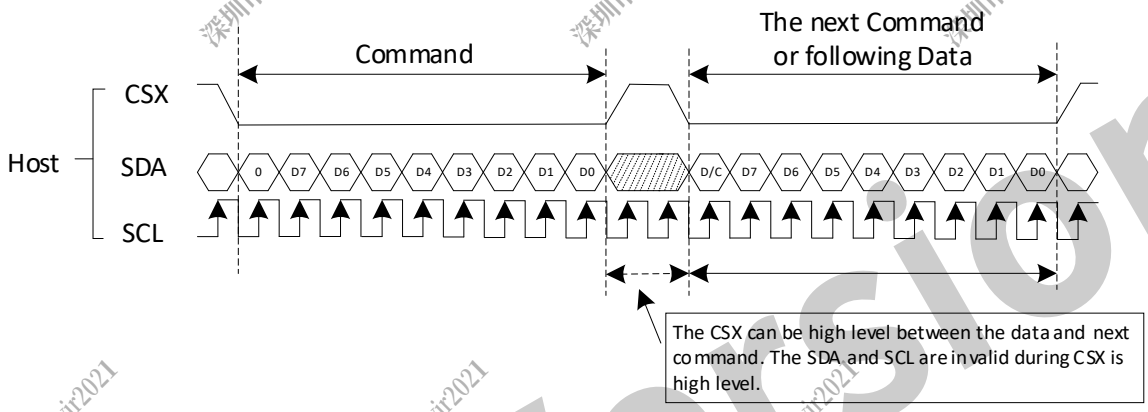
The following figure shows the writing operation format of 3-line DBI Interface I and Interface II.

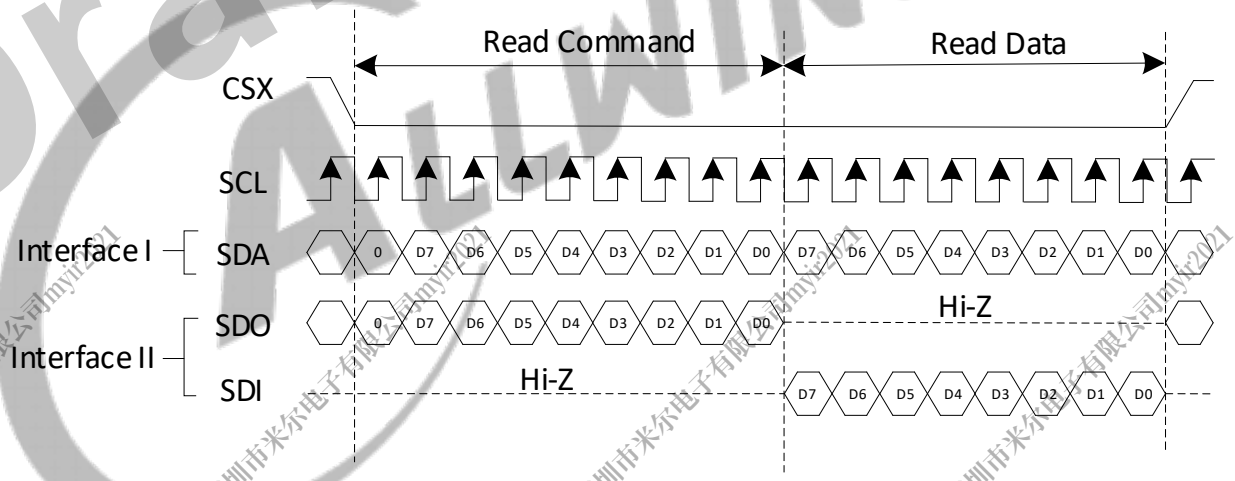
Figure 8-96 DBI 3-Line Display Bus Serial Interface Writing Operation Format



The 3-line DBI Interface I uses the SDA port as bidirectional data input and output port. There are only three cases of data reading volume, 8bits/24bits/32bits, and the first data sampled is high.

The following figure shows the 8 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read immediately with on dummy period.

Figure 8-97 DBI 3-Line Display Bus Serial Interface 8-bit Reading Operation Format



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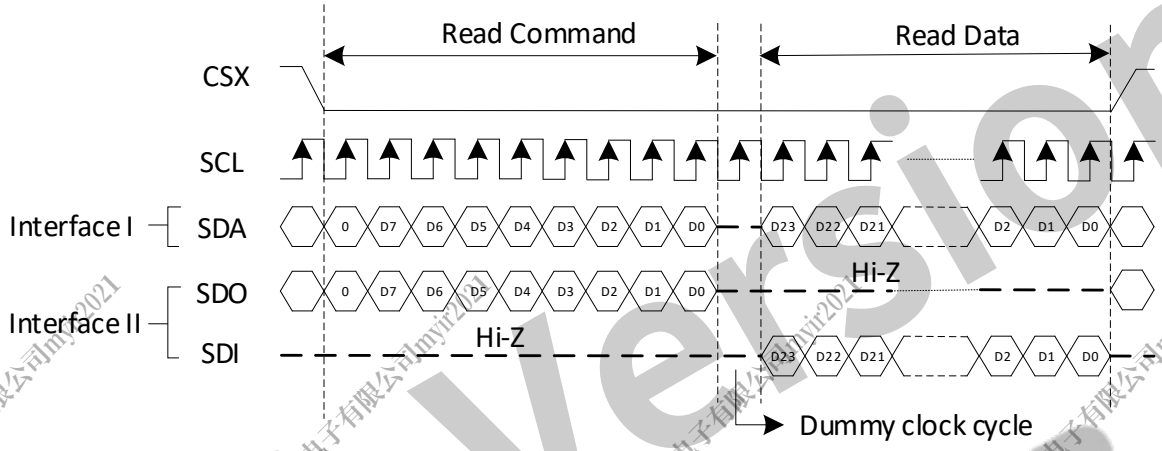
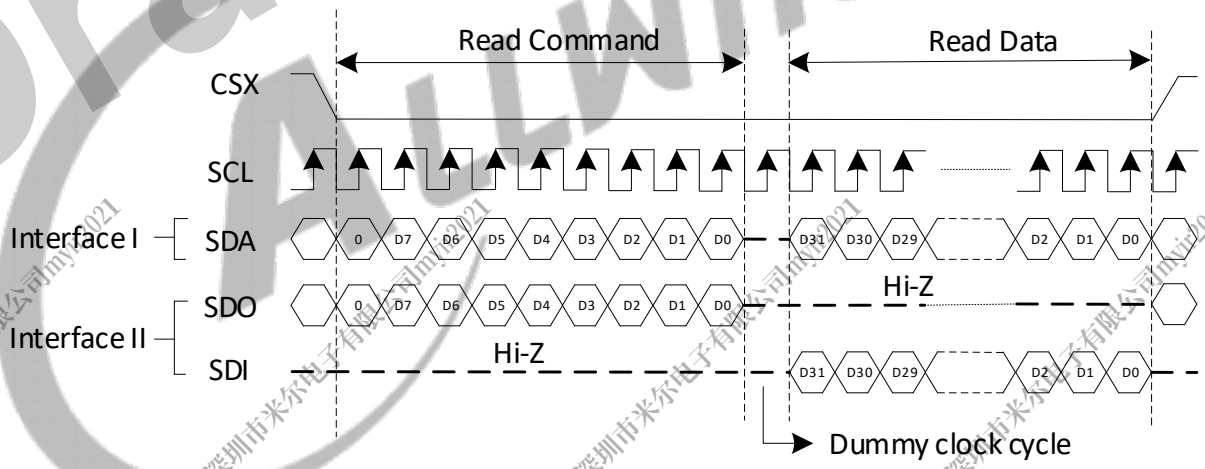
The following figure shows the 24 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read after waiting for the dummy clock cycle.

Figure 8-98 DBI 3-Line Display Bus Serial Interface 24-bit Reading Operation Format



The following figure shows the 32 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read after waiting for the dummy clock cycle.

Figure 8-99 DBI 3-Line Display Bus Serial Interface 32-bit Reading Operation Format



8.17.3.12 DBI 4-Line Interface Writing and Reading Timing

The 4-line DBI Interface I contains CSX, D/CX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 4-line DBI Interface II contains CSX, D/CX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

Since the 4-line display bus mode has a Data/Command data line indicating whether Data or Command is currently being transmitted (0: Command, 1: Data). So there is no need to add an extra bit to data-stream before MSB like the 3-line DBI.

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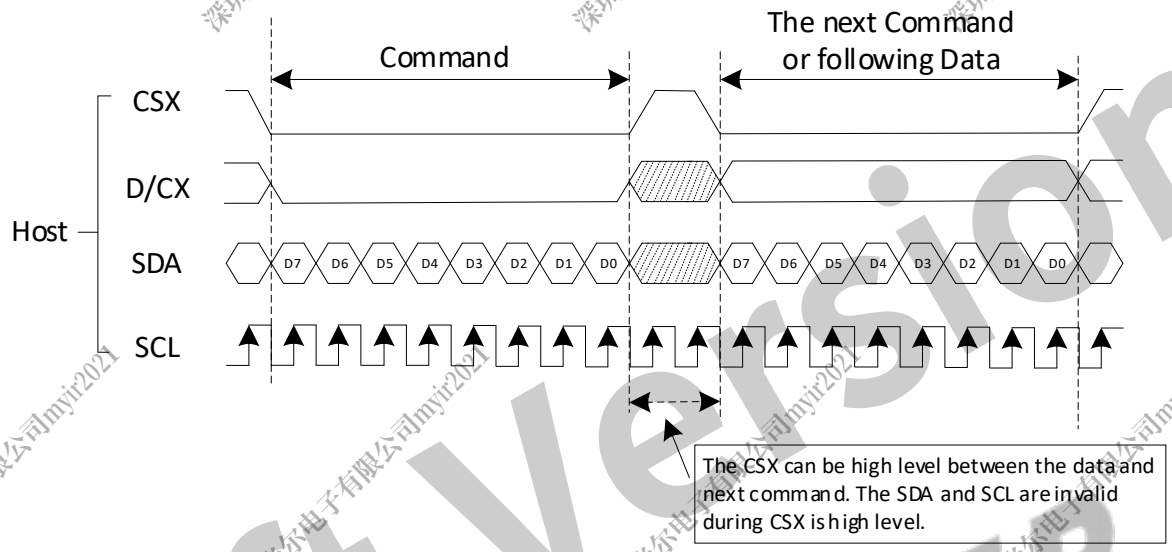
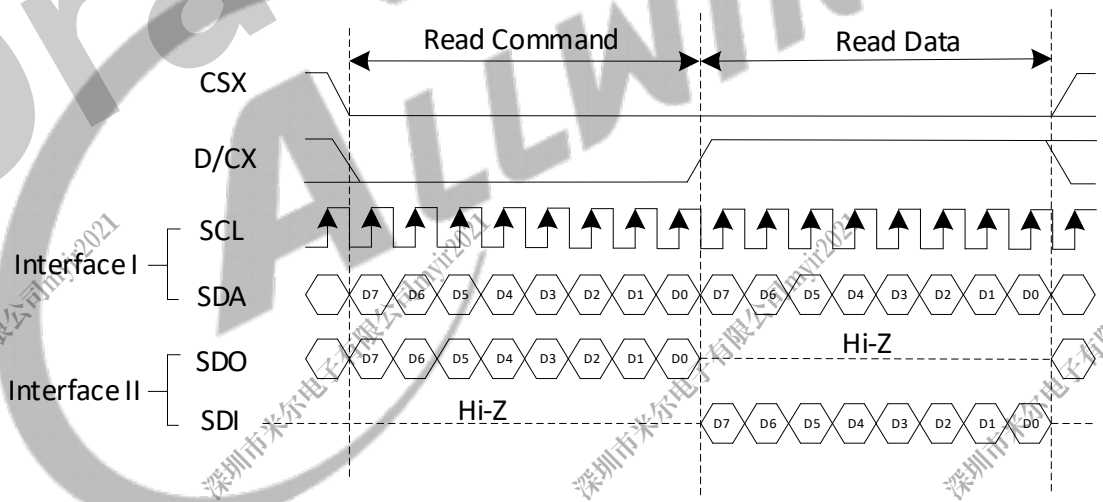
The following figure shows the writing operation format of 4-line DBI Interface I and Interface II.

Figure 8-100 DBI 4-Line Display Bus Serial Interface Writing Operation Format



The following figure shows the 8 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 8-101 DBI 4-Line Display Bus Serial Interface 8-bit Reading Operation Format



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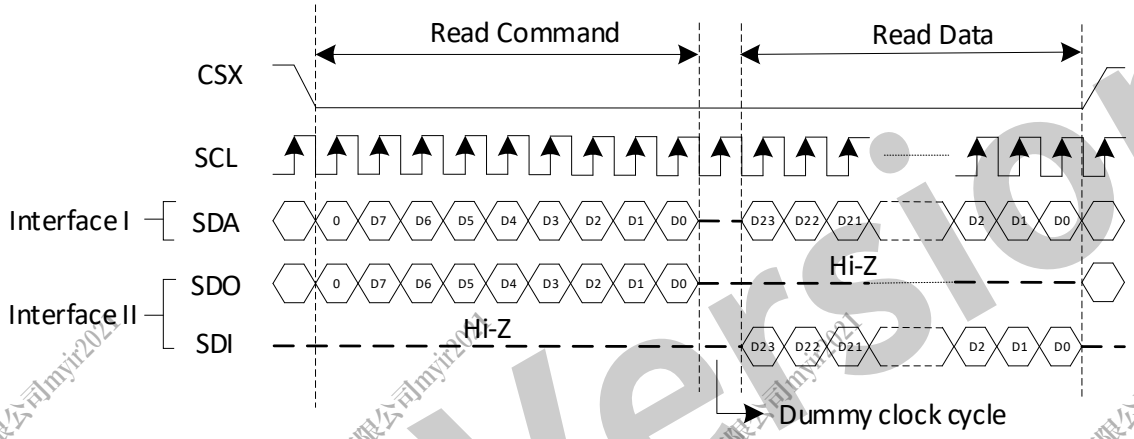
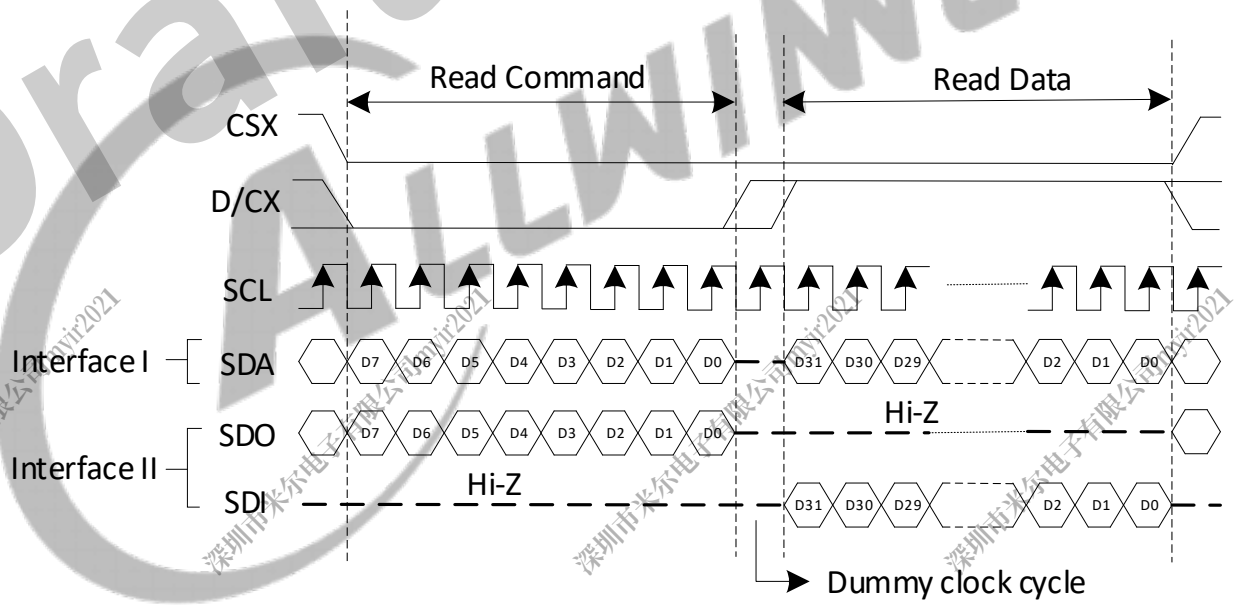
The following figure shows the 24 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 8-102 DBI 4-Line Display Bus Serial Interface 24-bit Reading Operation Format



The following figure shows the 32 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 8-103 DBI 4-Line Display Bus Serial Interface 32-bit Reading Operation Format



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8.17.3.13 DBI 3-Line Interface Transmit Video Format

Figure 8-104 RGB111 3-Line Interface Transmit Video Format

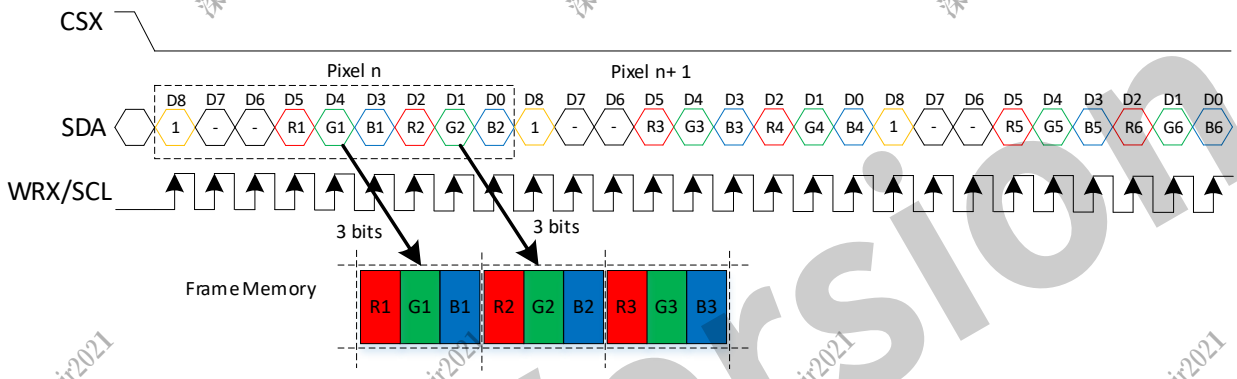
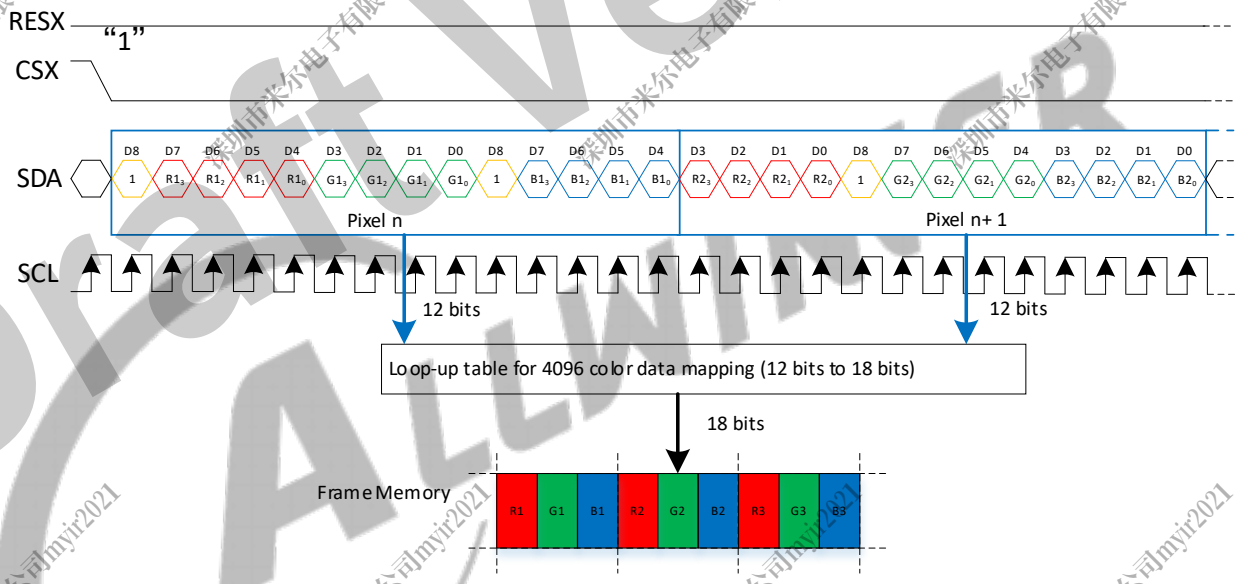


Figure 8-105 RGB444 3-Line Interface Transmit Video Format



Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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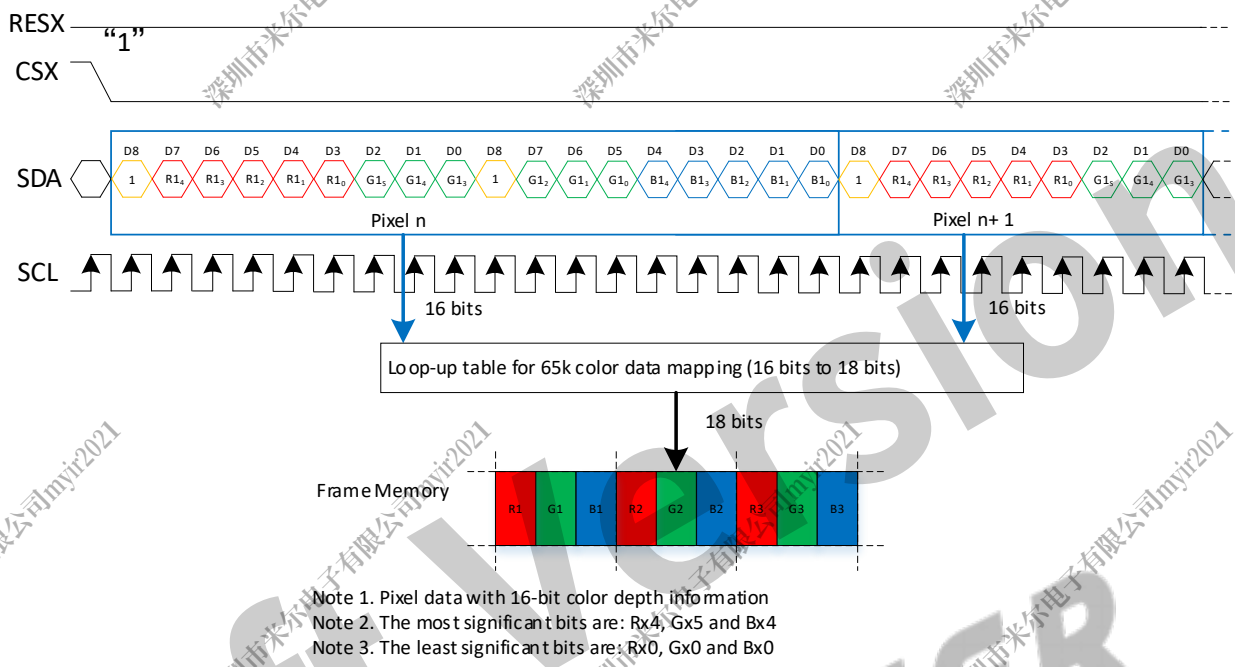
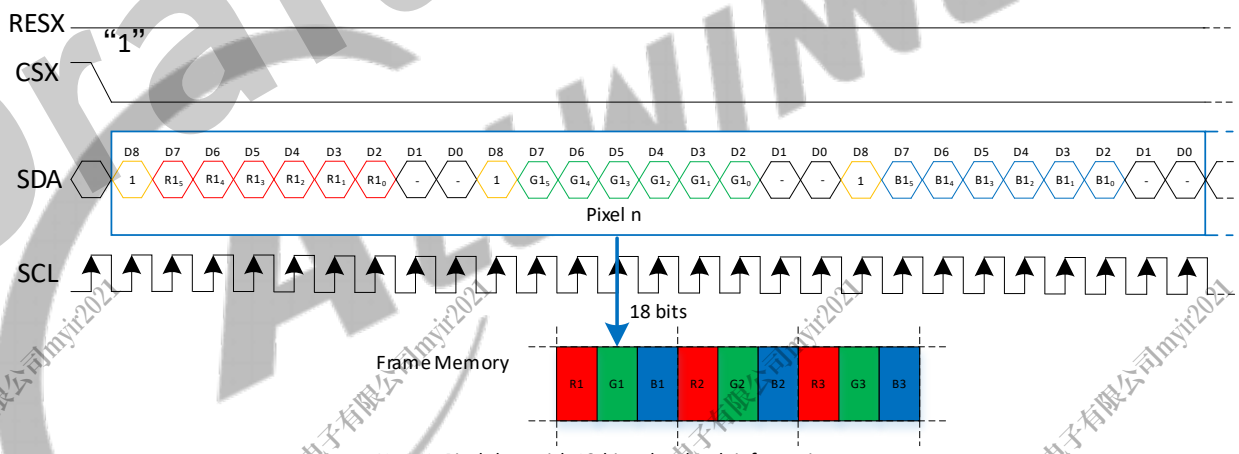
Figure 8-106 RGB565 3-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-107 RGB666 3-Line Interface Transmit Video Format



Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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8.17.3.14 DBI 4-Line Interface Transmit Video Format

Figure 8-108 RGB111 4-Line Interface Transmit Video Format

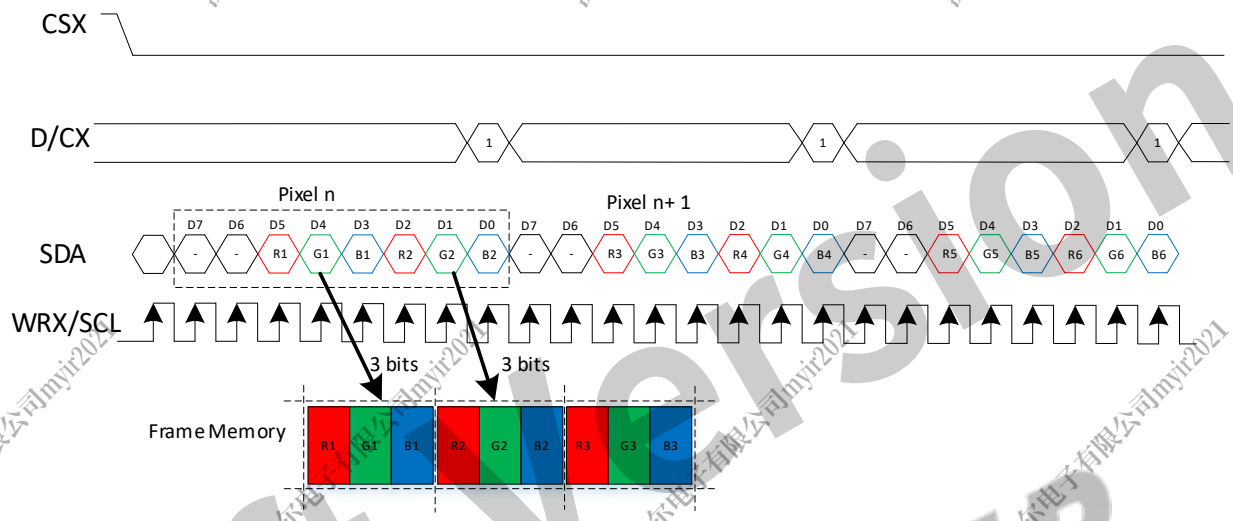
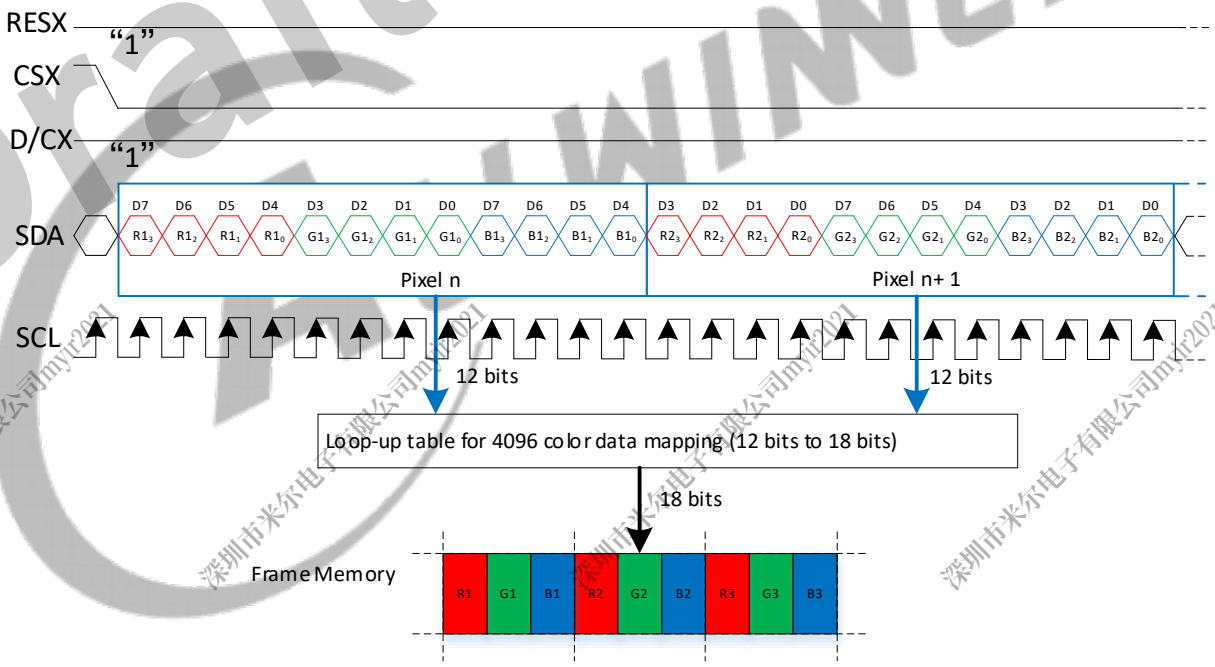


Figure 8-109 RGB444 4-Line Interface Transmit Video Format



Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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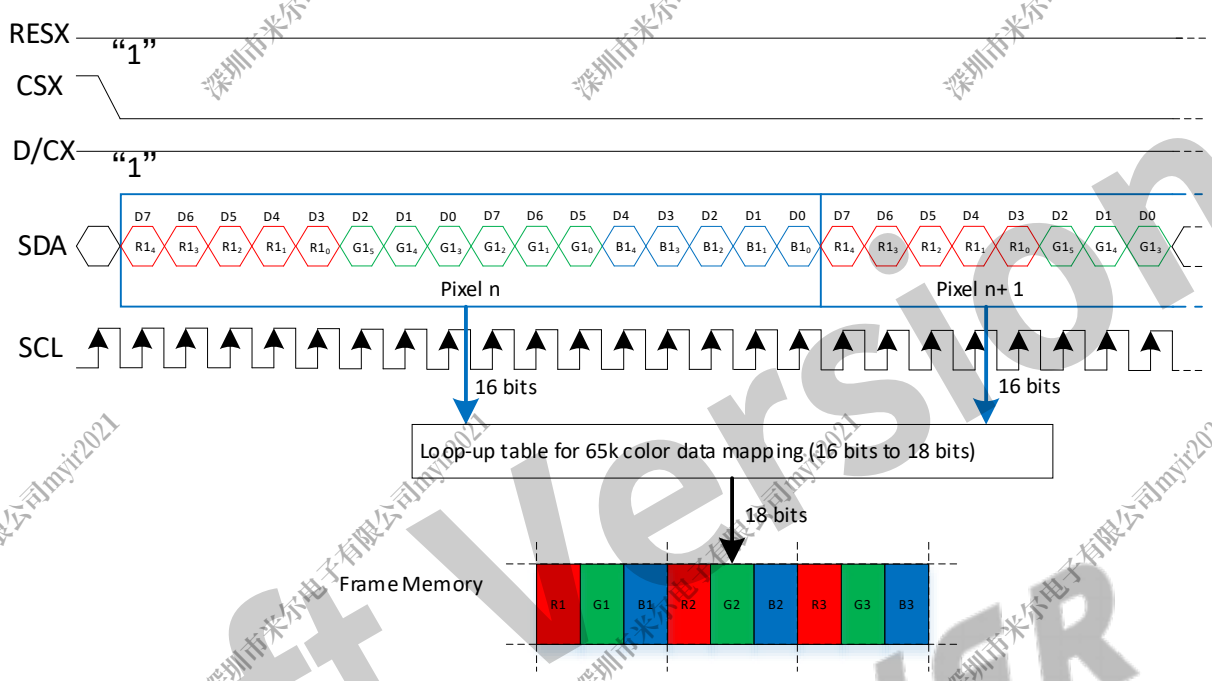
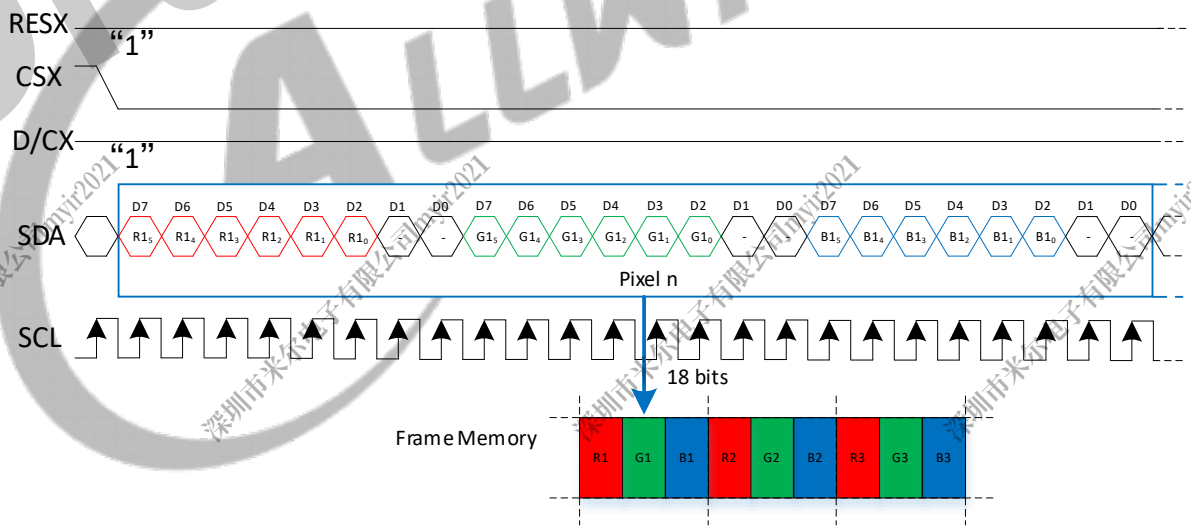
Figure 8-110 RGB565 4-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-111 RGB666 4-Line Interface Transmit Video Format



Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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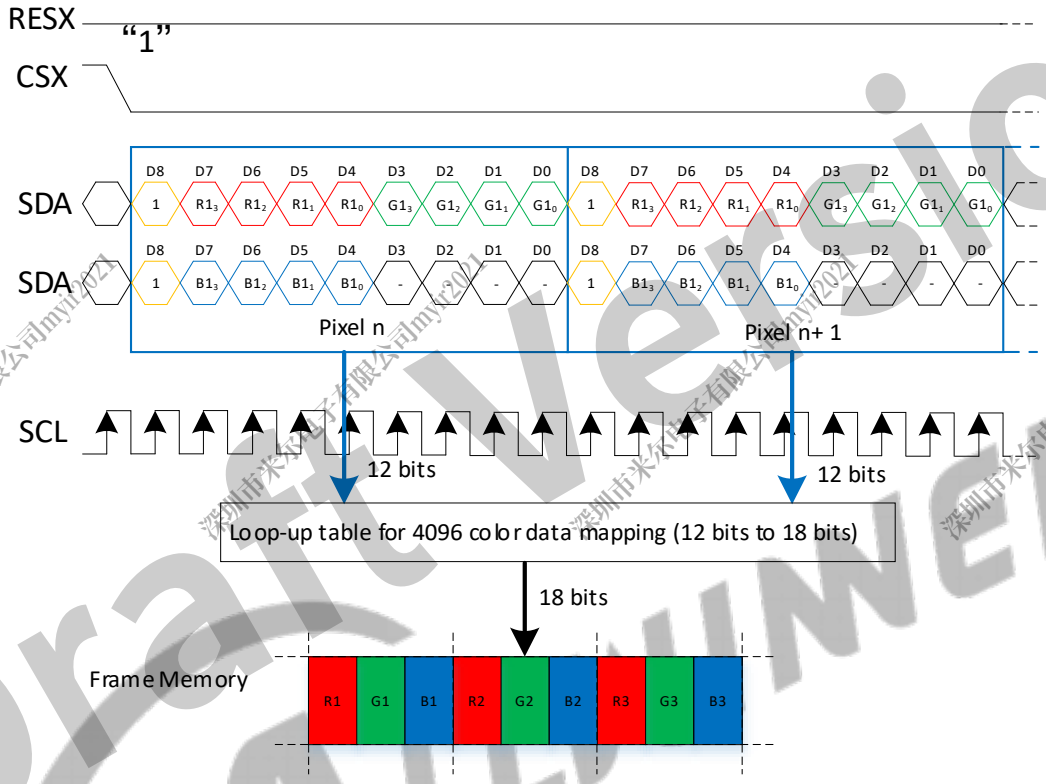
8.17.3.15 DBI 2 Data Lane Interface Transmit Video Format

For RGB444:

Figure 8-112 RGB444 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 12-bit color information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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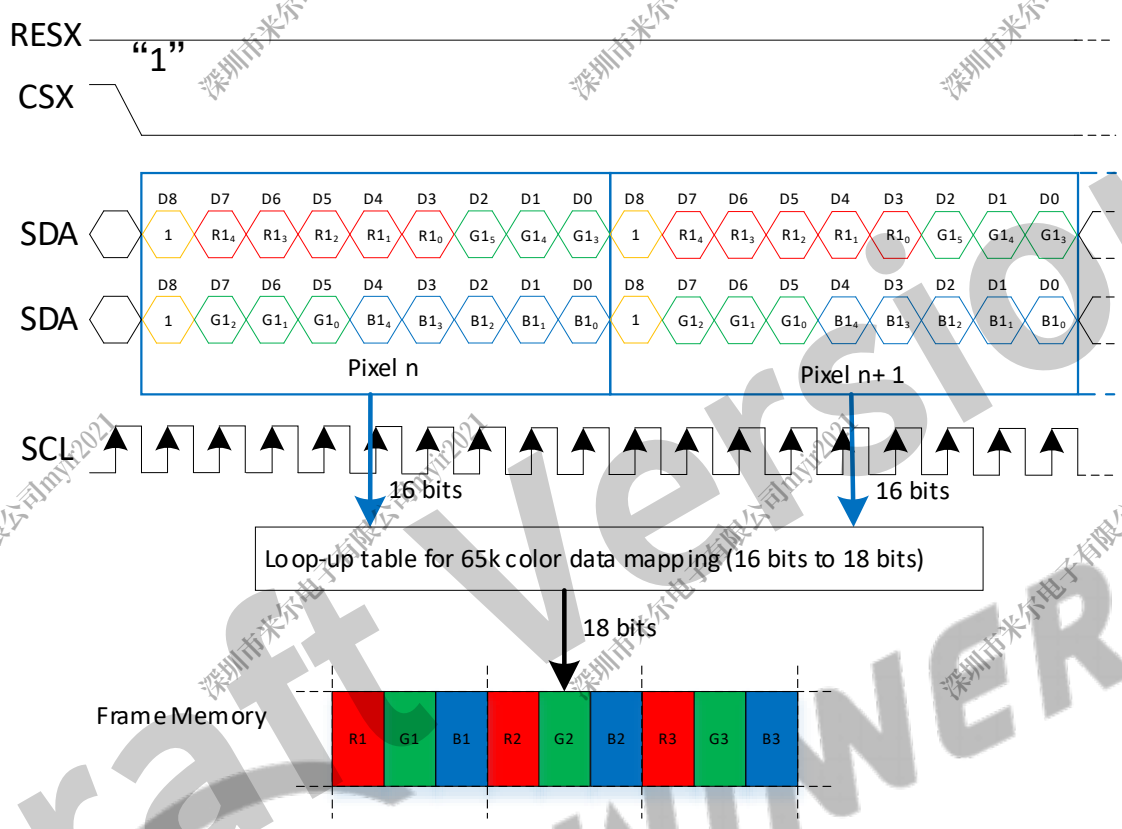
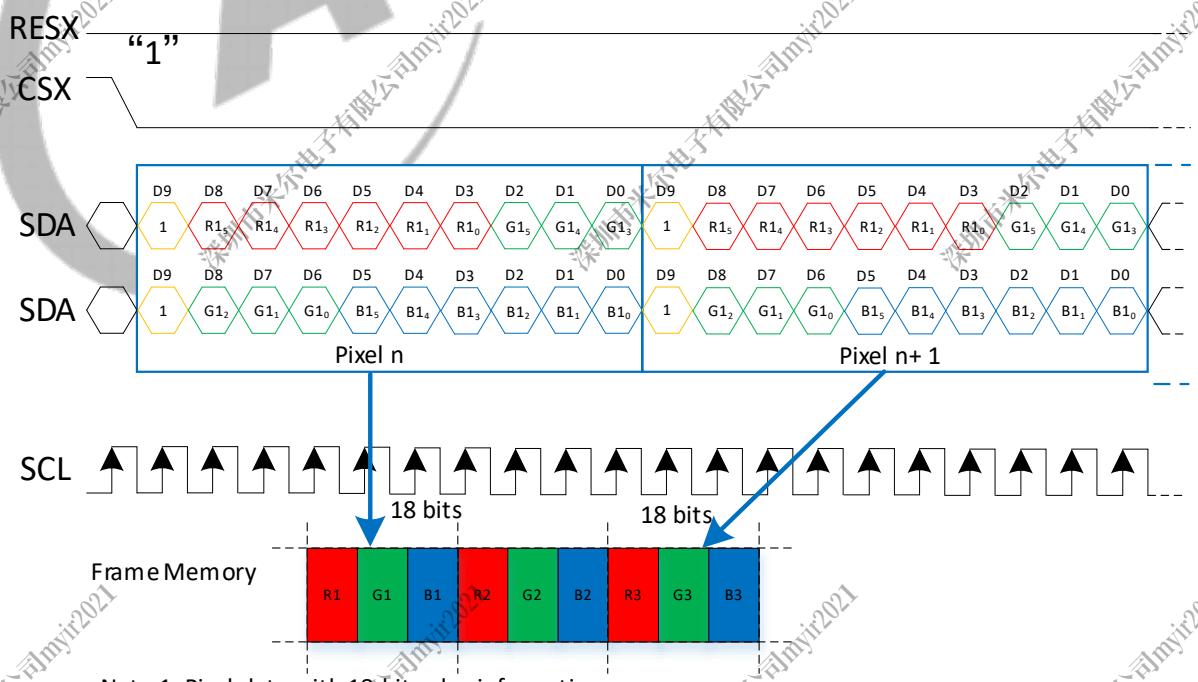
Figure 8-113 RGB565 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 16-bit color information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-114 RGB666 2 Data Lane Interface Transmit Video Format 0



Note 1. Pixel data with 18-bit color information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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Figure 8-115 RGB666 2 Data Lane Interface Transmit Video Format 1 (ilitek)

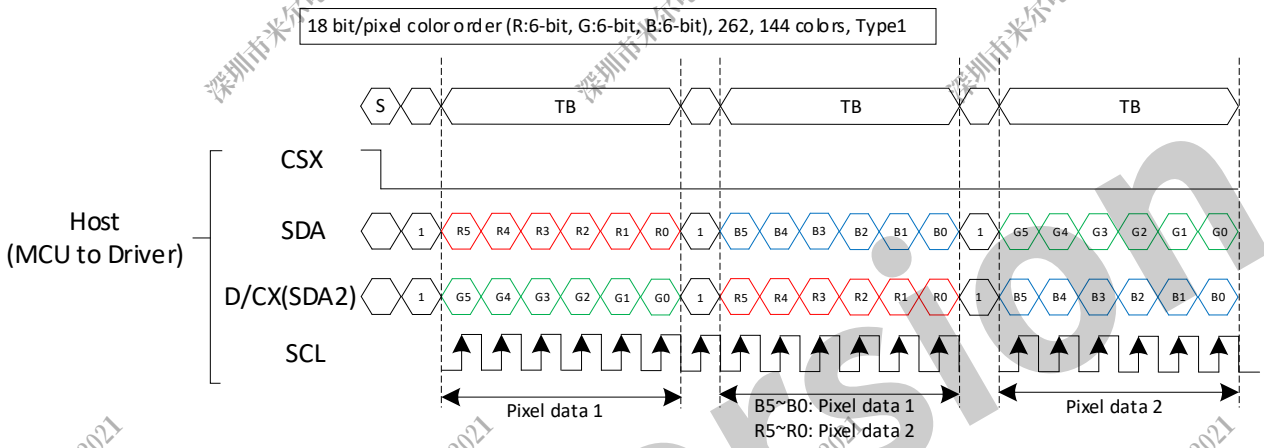


Figure 8-116 RGB666 2 Data Lane Interface Transmit Video Format 2 (New vision)

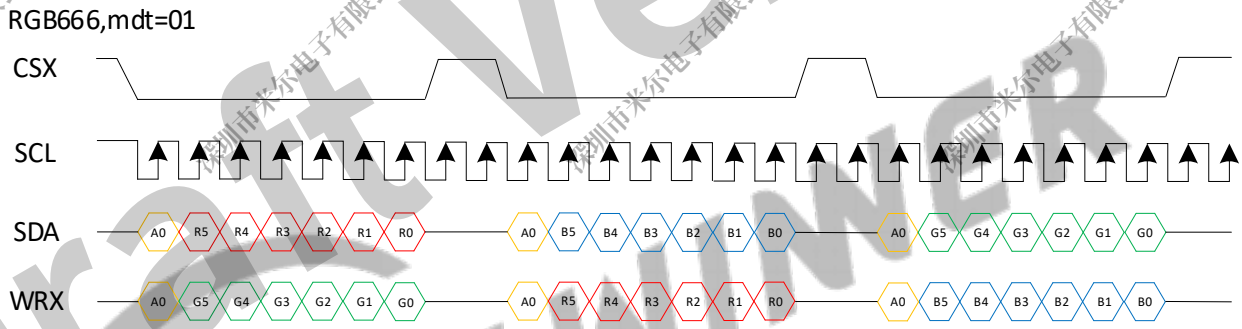
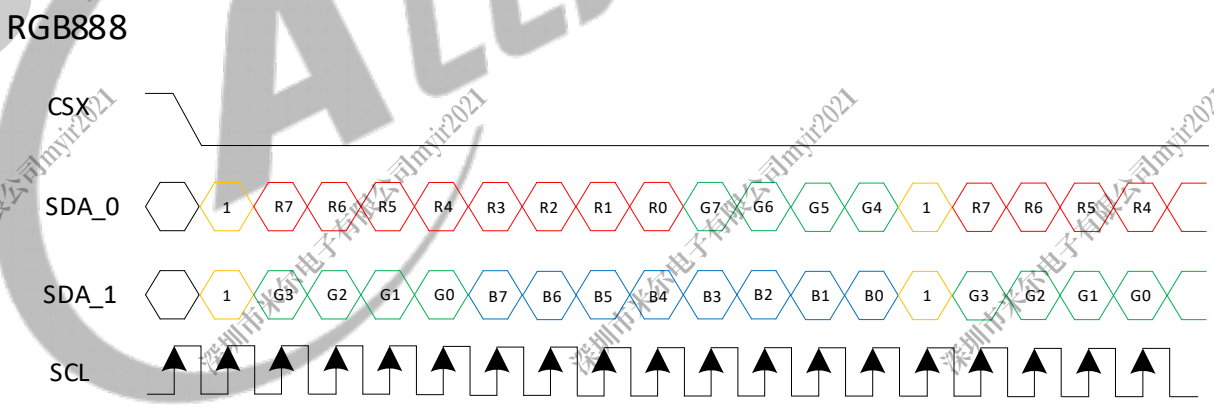


Figure 8-117 RGB888 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 24-bit color information
Note 2. The most significant bits are: R7, G7 and B7
Note 3. The least significant bits are: R0, G0 and B0

8.17.4 Programming Guidelines

8.17.4.1 Writing/Reading Data Process Using SPI Mode

The SPI transfers serial data between the processor and the external device. CPU and DMA are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX channel and

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RX channel. The TX channel has the path from TX FIFO to the external device. The RX channel has the path from the external device to RX FIFO.

Write Data: CPU or DMA must write data on the SPI_TXD register, the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor at the end of each transfer.

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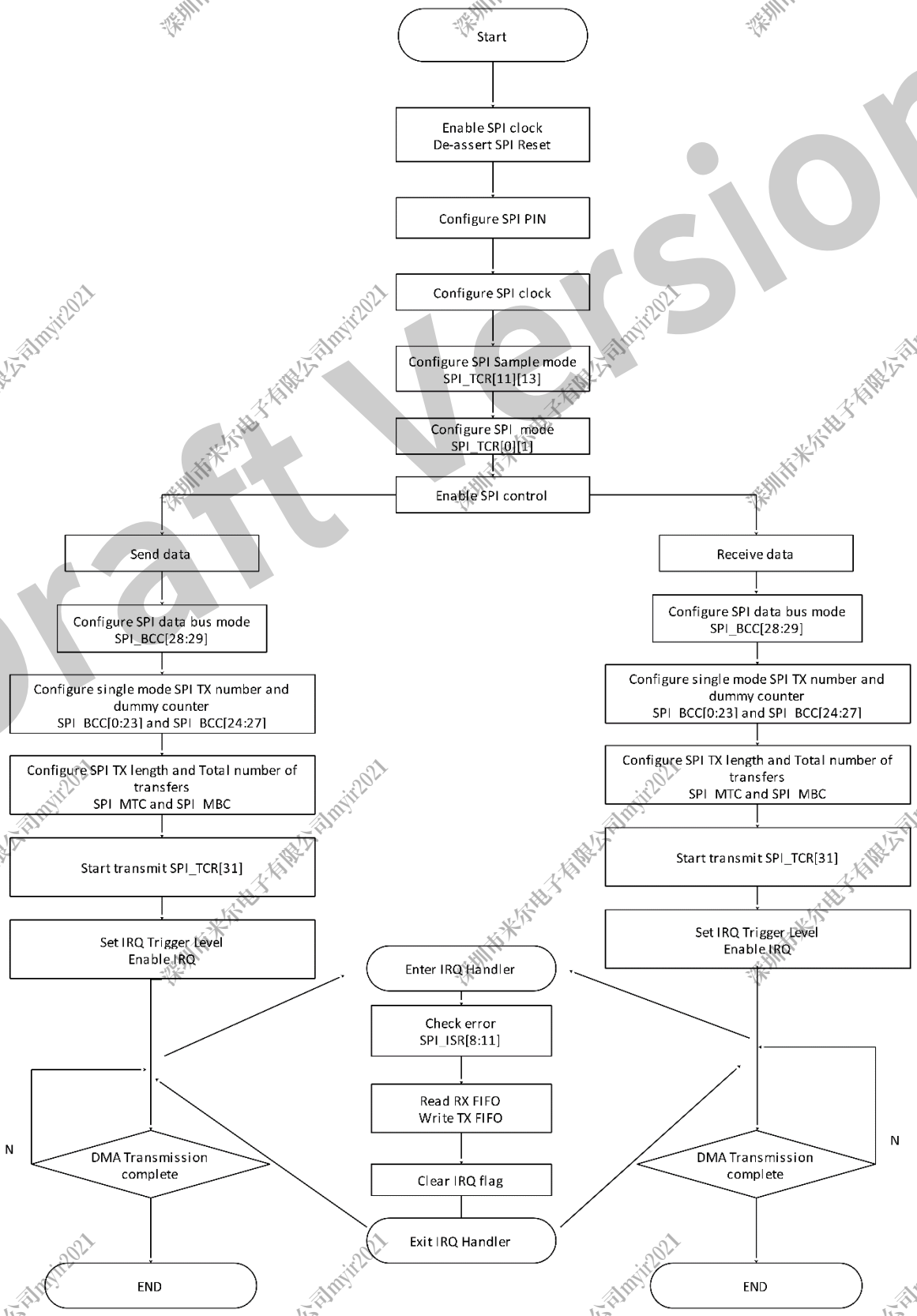
CPU Mode

Figure 8-118 SPI Write/Read Data in CPU Mode



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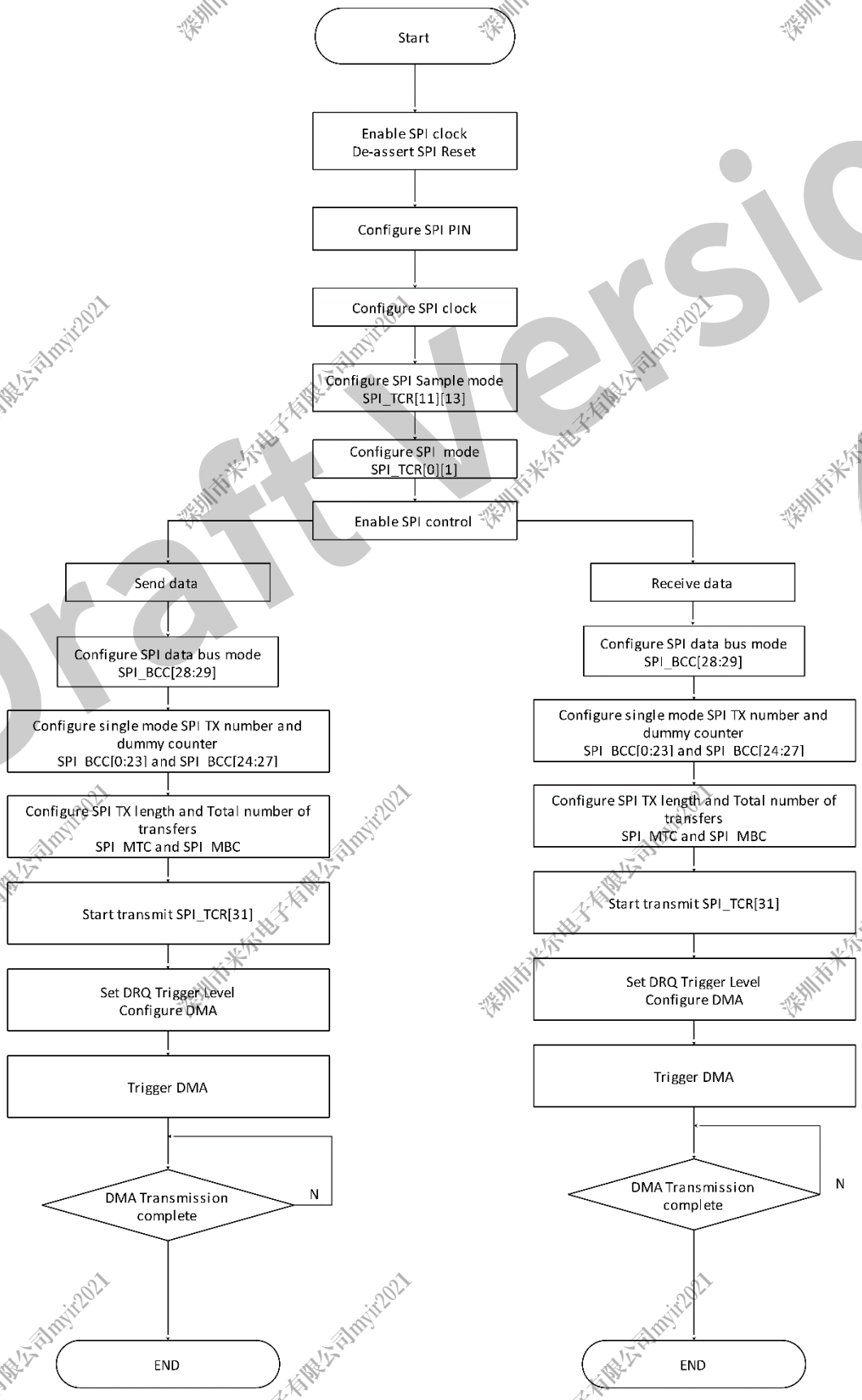
DMA Mode

Figure 8-119 SPI Write/Read Data in DMA Mode



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8.17.4.2 Transmitting Write Command Using DBI Mode

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.

Step 3 Configure the DBI_CTL_0 (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

b) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.

Step 7 Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

8.17.4.3 Transmitting Parameter Using DBI Mode

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

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d) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 1 to send the parameter.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

b) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.

Step 7 Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

8.17.4.4 Transmitting Video Using DBI Mode

Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

If the data is from the CPU path, the controller writes the command to be sent to the 0x0200 address by the AHB bus.

If the data is from the DMA path, configure DBI_CTL_1[DBI_FIFO_DRQ_EN] (bit15) to 1 and DBI_CTL_1[TX_TRIG_LEVEL] (bit[14:8]) to 64, which indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 64.

Software Trigger Mode

The software enables DBI_en_trigger when the edge interrupt of TE is detected.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt and stops transmitting data.

Wait for the edge interrupt of TE, the software needs to enable DBI_en_trigger, in circulation.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 1 to select the software trigger mode.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

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b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111//444/565/666/888.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x110) according to the sent image size.

Step 6 Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

Step 7 Detect the TE interrupt of the DBI_INT (0x0120) register.

Step 8 Configure DBI_CTL_1[DBI_soft_trigger] to 1.

Timer Trigger Mode

The software configures timer_en to enable timer counting, and when the counter reaches the specified value, the DBI_EN automatically can be enabled to start transmitting data.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt, and stops transmitting data.

The timer starts counting again. When the counter reaches the specified value, the controller automatically enables DBI_EN, and in circulation until the software turns off the timer_en.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 2 to select the timer trigger mode.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

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Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x110) to transmit the image size.

Step 6 Configure the related parameter of DBI_Timer (0x10C).

TE Trigger Mode

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN automatically can be enabled to start transmitting data.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt, and stops transmitting data.

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN automatically can be enabled to start transmitting data until the software shuts down TE_EN or the screen no longer sends TE signals.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 3 to select the TE Configure the DBI_CTL_0 register (0x0100).

Step 3 Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

a) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

b) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

c) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

d) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

e) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

f) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x0110) to transmit the image size.

Step 6 Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

8.17.4.5 Transmitting Read Command and Read Data Using DBI Mode

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the reading command.

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b) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

c) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

d) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0.

e) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

f) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Configure the DBI_CTL_1 register (0x0104).

a) Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

b) Configure DBI_CTL_1[Read_MSB_First] (bit20) to select whether the first bit of the read data is the highest or lowest bit of data.

c) Configure DBI_CTL_1[Read Data Number of Bytes] to set the byte number to be read.

d) Configure DBI_CTL_1[Read Command Dummy Cycles] to set the dummy cycle between the read command and the read data, when the dummy cycle is complete, the data starts to be sampled.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[RF_DRQ_EN] (bit8) to 1 to enable RXFIFO DMA.

b) Set SPI_FCR[RX_TRIG_LEVEL] (bit[7:0]) to 32, which indicates the controller requests receiving data from DMA if the data of the RX FIFO is greater than 64.

CPU Path: Read data in RX FIFO from the 0x0300 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting command.

Step 7 Wait until DBI_INT[RD_DONE_INT] is 1. It indicates that the data is read completely.

8.17.5 Register List

Module Name	Base Address
SPI1	0x0402 6000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter register

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Register Name	Offset	Description
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
DBI_CTL_0	0x0100	DBI Control Register 0
DBI_CTL_1	0x0104	DBI Control Register 1
DBI_CTL_2	0x0108	DBI Control Register 2
DBI_TIMER	0x010C	DBI Timer Control Register
DBI_VIDEO_SIZE	0x0110	DBI Video Size Register
DBI_INT	0x0120	DBI Interrupt Register
DBI_DEBUG_0	0x0124	DBI DEBUG Register 0
DBI_DEBUG_1	0x0128	DBI DEBUG Register 1
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register
SPI_BSR	0x0400	SPI BUF Status register

8.17.6 Register Description

8.17.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0s	SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: Stop transmitting data when RXFIFO is full. 0: Normal operation, ignore RXFIFO status. **Note: Can't be written when XCH=1.**
6:5	/	/	/

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Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	DBI_EN DBI Module Enable Control 0: Disable 1: Enable
3	R/W	0x0	SPI_DBI_MODE_SEL SDBISPI_DBI Working Mode Select 0: SPI MODE 1: DBI MODE
2	R/W	0x0	MODE_SELEC Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing **Note: Can't be written when XCH=1.**
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode **Note: Can't be written when XCH=1.**
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable **Note: After transforming from bit_mode to byte_mode, it must Enable the SPI Module again.**

8.17.6.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write "1" to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write "1" to SRST will also clear this bit. Write '0' to this bit has no effect. **Note: Can't be written when XCH=1.**
30:16	/	/	/

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Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: normal operation, do not delay internal read sample point 1: delay internal read sample point **Note：Can't be written when XCH=1.**
14	R/W	0x0	SDDM Sending Data Delay Mode 0:normal sending 1:delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual io mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1: Normal Sample Mode 0: Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first **Note: Can't be written when XCH=1.**

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Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: normal operation, do not delay internal read sample point 1: delay internal read sample point **Note: Can't be written when XCH=1.**
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode **Note: Can't be written when XCH=1.**
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one **Note: Can't be written when XCH=1.**
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. **Note: Can't be written when XCH=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: Can't be written when XCH=1.**

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Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: Can't be written when XCH=1.**
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: Can't be written when XCH=1.**
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts **Note：Can't be written when XCH=1.**
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: Can't be written when XCH=1.**
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: Can't be written when XCH=1.**
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) **Note: Can't be written when XCH=1.**

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8.17.6.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

8.17.6.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed

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Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	TF_UDF TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty

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Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing "1" to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL <= RX_TRIG_LEVEL 1: RX_WL > RX_TRIG_LEVEL This bit is set any time if RX_WL > RX_TRIG_LEVEL. Writing "1" to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.17.6.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write '1' to this bit will reset the control portion of the TX FIFO and auto clear to '0' when completing reset operation, write to '0' has no effect.

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Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable In normal mode, TX FIFO can only be read by SPI controller, write '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

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8.17.6.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO ... 64 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO ... 64: 64 bytes in RX FIFO other: Reserved

8.17.6.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. **Note：Can't be written when XCH=1.**

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Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted **Note: Can't be written when XCH=1.**

8.17.6.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

8.17.6.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst ... N: N bursts **Note:** • **Can't be written when XCH=1;** • **Total transfer data, include the TXD, RXD and dummy burst.**

8.17.6.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

8.17.6.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31: 30	/	/	/

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Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable **Note:** • **Can't be written when XCH=1;** • **Quad mode includes Quad-Input and Quad-Output.**
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode **Note:** • **Can't be written when XCH=1.** • **It is only valid when Quad_Mode_EN=0.**
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don't care by the device. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

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8.17.6.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bits frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Write "1" to this bit will start to transfer serial bits frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode. In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register(or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed **Note: It is only valid when Work Mode Select==0x10/0x11.**
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable **Note: It is only valid when Work Mode Select==0x10/0x11.**

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Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
15:14	/	/	/
13:8	R/W	0x00	TX_FEM_LEN Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**

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Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
1:0	R/W	0x0	WMS Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

8.17.6.13 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first. **Note: This register is only valid when Work Mode Select==0x10/0x11.**

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8.17.6.14 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first. **Note: This register is only valid when Work Mode Select==0x10/0x11.**

8.17.6.15 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: DMA_ACTIVE is low 01: DMA_ACTIVE is high 10: DMA_ACTIVE is controlled by DMA_REQUEST(DRQ) 11: DMA_ACTIVE is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to DMA_ACTIVE high。

8.17.6.16 0x0100 DBI Control Register 0 (Default Value: 0x0010_0000)

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMDT Command Type 0: Write Command 1: Read Command

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Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
30:20	R/W	0x1	WCDC Write Command Dummy Cycles Controls dummy cycles between two write commands Range 1-255 Default Condition: there is a dbi_clk cycle between each command or parameter.
19	R/W	0x0	DAT_SEQ Output Data Sequence 0: MSB First 1: LSB First
18:16	R/W	0x0	RGB_SEQ Output RGB Sequence 0：RGB 1：RBG 2：GRB 3：GBR 4：BRG 5：BGR 6-7 Reserve
15	R/W	0x0	TRAN_MOD Transmit Mode 0：Command / Parameter 1：Video
14:12	R/W	0x0	DAT_FMT Output Data Format 0 : RGB111 1 : RGB444 2 : RGB565 3 : RGB666 4 : RGB888 (only for 2 Data Lane Interface) 5-7 Reserve
11	/	/	/
10:8	R/W	0x0	DBI_INTF DBI Interface 0: 3 Line Interface I 1: 3 Line Interface II 2: 4 Line Interface I 3: 4 Line Interface II 4: 2 Data Lane Interface

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Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	RGB_FMT RGB_Source_Format When Video Source_Type is RGB32 0：RGB 1：RBG 2：GRB 3：GBR 4：BRG 5：BGR Other:Reserve When Video Source_Type is RGB16 0：RGB 1-4:reserve 5：BGR 6：GRBG_0:{G[5:3] R[4:0] B[4:0] G[2:0]} 7：GBRG_0:{G[5:3] B[4:0] R[4:0] G[2:0]} 8：GRBG_1:{G[2:0] R[4:0] B[4:0] G[5:3]} 9：GBRG_1:{G[2:0] B[4:0] R[4:0] G[5:3]} Other:Reserve
3	R/W	0x0	DUM_VAL Dummy Cycle Value Output Value During Dummy Cycle
2	R/W	0x0	RGB_BO RGB Bit Order 0: Remain the sequence of RGB data 1: Swap the higher bit and the lower bit for each component of DRAM RGB
1	R/W	0x0	ELEMENT_A_POS Element A Position Only for RGB32 Data Format 0: A component is in the bit [31:24] of data source 1: A component is in the bit [7:0] of data source
0	R/W	0x0	VI_SRC_TYPE RGB Source Type 0: RGB32 1: RGB16

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8.17.6.17 0x0104 DBI Control Register 1 (Default Value: 0x0000_0001)

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	DBI_SOFT_TRG It is only available for software trigger mode. Write '1' to this bit will start DBI TX module and auto clear to '0' when completing start operation, write to '0' has no effect.
30:29	R/W	0x0	DBI_EN_MOD_SEL DBI Enable Mode Select 0: always on mode 1: software trigger mode 2: timer trigger mode 3: te trigger mode
28	/	/	/
27:26	R/W	0x0	RGB666_FMT 2 Data Lane RGB666 Format 00: Normal Format 01: Special Format for ILITEK 10: Special Format for New Vision
25	R/W	0x0	DBI_RXCLK_INV DBI rx clock inverse 0: Sample data by using the positive edge of the output clock 1: Sample data by using the negative edge of the output clock
24	R/W	0x0	DBI_CLKO_MOD DBI output clock mode 0: DBI clock always on(DCX Setup/hold equals one clock cycle) 1: DBI clock auto gating(DCX Setup/hold equals to a half clock cycle)

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Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	DBI_CLKO_INV DBI clock output inverse When the bit24 (DBI output clock mode) is 0. 0: The falling edge releases the CSX signal, and the falling edge releases data 1: The rising edge releases the CSX signal, and the rising edge releases data When the bit24 (DBI output clock mode) is 1. 0: The rising edge releases the CSX signal, and the falling edge releases data 1: The falling edge releases the CSX signal, and the rising edge releases data
22	R/W	0x0	DCX_DATA DCX Data Value 0：DCX Value equal to 0 1：DCX Value equal to 1
21	R/W	0x0	RGB 16 Data Source Select RGB 16 Data Source Select 0: Pixel1 is stored in the higher bit of address, and Pixel0 is stored in the lower bit of address 1: Pixel0 is stored in the higher bit of address, and Pixel1 is stored in the lower bit of address
20	R/W	0x0	RDAT_LSB Bit Order of Read Data 0: A reading data is the higher bit 1: A reading data is the lower bit
19:16	/	/	/
15:8	R/W	0x0	RCDC Read Command Dummy Cycles The dummy cycle between the read command and read data Reading 1-byte (8 bits) data has not dummy cycle.
7:0	R/W	0x1	RDBN Read Data Number of Bytes Sample Bytes data based on configuration.

8.17.6.18 0x0108 DBI Control Register 2 (Default Value: 0x0000_4000)

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	DBI_FIFO_DRQ_EN DBI FIFO DMA Request Enable 0: Disable 1: Enable
14:8	R/W	0x40	DBI_TRIG_LEVEL DBI FIFO Empty Request Trigger Level
7	/	/	/
6	R/W	0x0	DBI_SDI_OUT_SEL DBI SDI PIN Output Select The signal is used with the DBI SDI PIN Function Sel bit. 0: Output WRX (When DBI DCX PIN Function Sel = 0, the SDI pin outputs data) 1: Output DCX
5	R/W	0x0	DBI_DCX_SEL DBI DCX PIN Function Sel 0: DBI DCX Function 1:WRX(2 Data Lane Interface)
4:3	R/W	0x0	DBI_SDI_SEL DBI SDI PIN Function sel 0: DBI_SDI (Interface II) , WRX(2 Data Lane Interface) 1: DBI_TE 2: DBI_DCX Reserve
2	R/W	0x0	TE_DBC_SEL TE debounce function select 0: debounce 1: no-debounce
1	R/W	0x0	TE_TRIG_SEL TE edge trigger select 0: TE rising edge 1: TE falling edge
0	R/W	0x0	TE_EN TE enable 0: TE Disable 1: TE Enable

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8.17.6.19 0x010C DBI Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: DBI_TIMER
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DBI_TM_EN DBI Timer enable 0: enable 1: disable
30:0	R/W	0x0	DBI Timer Value It sets the time interval between sending data twice, which is frame blanking. It is used to set the time at which the interrupt of the DBI Timer is triggered. When the Timer_EN is 1, the timer starts to count (the clock of the counting is SCLK), and the counter reaches the target value to trigger the Timer_INT of DBI, the data will start to send in series. **Note: Do not count when sending the series data.**

8.17.6.20 0x0110 DBI Video Size Register (Default Value: 0x01e0_0140)

Offset: 0x0110			Register Name: DBI_VIDEO_SIZE
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0x1e0	V_SIZE It is used to generate the Frame int.
15:11	/	/	/
10:0	R/W	0x140	H_SIZE It is used to generate the Line int.

8.17.6.21 0x0120 DBI Interrupt Register (Default Value: 0x0000_4000)

Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W1C	0x1	DBI_FIFO_EMPTY_INT DBI FIFO Empty Interrupt Status 0: DBI_FIFO is not empty 1: DBI_FIFO is empty

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Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	DBI_FIFO_FULL_INT DBI FIFO Full Interrupt Status 0: DBI_FIFO is not full 1: DBI_FIFO is full
12	R/W1C	0x0	TIMER_INT it indicates that timer has been count sclk cycles to the value of DBI_Timer Register[30:0] . Writing 1 to this bit clears it. 0: Timer has no been achieve objective 1: Timer has been achieve objective
11	R/W1C	0x0	RD_DONE_INT it indicates that the number of byte setting in DBI_Control Register 1 [19:8] has been read . Writing 1 to this bit clears it. 0: all of data has been not read 1: all of data has been read
10	R/W1C	0x0	TE_INT it indicates that TE signal has been changed. Writing 1 to this bit clears it. 0: TE signal is no changed 1: TE signal has been changed
9	R/W1C	0x0	FRAM_DONE_INT it indicates that a frame video data has been send. Writing 1 to this bit clears it. 0: a frame video has not been send 1: a frame video has been send
8	R/W1C	0x0	LINE_DONE_INT it indicates that a line of video data has been send. Writing 1 to this bit clears it. 0: a line of video data has not been send 1: a line of video data has been send
7	/	/	/
6	R/W	0x0	DBI_FIFO_EMPTY_INT_EN DBI FIFO Empty Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DBI_FIFO_FULL_INT_EN DBI FIFO Full Interrupt Enable 0: Disable 1: Enable

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Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	TIMER_INT_EN Timer Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RD_DONE_INT_EN Read Done Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	TE_INT_EN TE Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	FRAM_DONE_INT_EN Frame Done Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	LINE_DONE_INT_EN Line Done Interrupt Enable 0: Disable 1: Enable

8.17.6.22 0x0124 DBI Debug Register 0 (Default Value: 0x007F_0000)

Offset: 0x0124			Register Name: DBI_DEBUG_0
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:16	R	0x7F	DBI_FIFO_AVAIL DBI FIFO ROOM VALID 0-127 Words
15:13	/	/	/
12	R	0x0	TE_VAL TE input value 0 : TE not Trigger 1 : TE Trigger
11:8	R	0x0	DBI_RXCS FSM for DBI Receive RX_BS0 - RX_BS6 , Gray - Code
7:4	R	0x0	SH_CS FSM for shifter 0-11 : SH0-SH11

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Offset: 0x0124			Register Name: DBI_DEBUG_0
Bit	Read/Write	Default/Hex	Description
3:2	R	0x0	DBI_TXCS FSM for DBI Transmit 0: IDLE 1: SHIF 2: DUMY 3: READ
1:0	R	0x0	MEM_CS FSM for DBI Memory 0: IDLE_FRM 1: FRM_POS 2: FRM_RDY

8.17.6.23 0x0128 DBI Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: DBI_DEBUG_1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R	0x0	LCNT Line counter The number of pixel lines that are currently sent
15:12	/	/	/
11:0	R	0x0	CCNT Component counter The number of RGB components that are currently sent The field is equal to pixel_cnt *3.

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8.17.6.24 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note: This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

8.17.6.25 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

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8.17.6.26 0x0400 SPI BUF Status Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
15:8	/	/	/
7:0	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer

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8.18 SPI Flash controller (SPIFC)

8.18.1 Overview

The SPI Flash Controller (SPIFC) is a synchronous, serial communication interface which allows rapid data communication with fewer software interrupts. Different from SPI, this IP is typically designed for higher speed Flash devices and it only works at Master mode.

The SPI Flash Controller has the following features:

- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports STR mode and DTR mode, and DTR mode supports DQS signal
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Software Write Protection
  - Write protection for all/portion of memory via software
  - Top/Bottom Block protection
- Programmable delay between transactions
- Support Mode0, Mode1, Mode2 and Mode3
- Support control signal configuration
  - Up to four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

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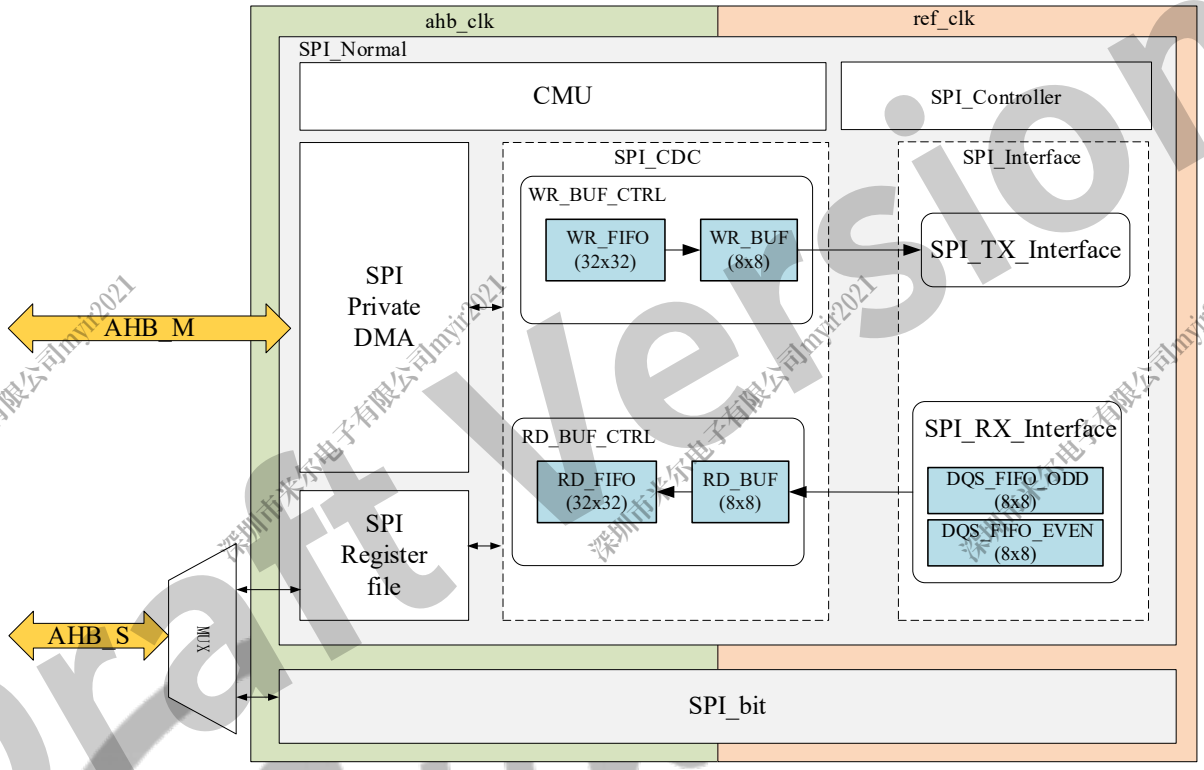
8.18.2 Block Diagram

The following figure shows a block diagram of the SPI Flash Controller.

Figure 8-120 SPI_Flash Block Diagram



SPI Flash Controller contains the following sub-blocks:

Table 8-57 SPI Flash Controller Sub-blocks

Sub-block	Description
SPI_Register_File	Responsible for implementing registers configuration through AHB1 bus.
SPI_Private_DMA	Private DMA for SPI, which contains AHB master and supports TXFIFO(WR_FIFO) and RXFIFO(RD_FIFO).
CMU	Responsible for generating internal clock; Implementing sckr delay, clock sourcess selection, clock gating, and scan; supporting synchronous release of asynchronous reset and scan.
SPI_CDC	SPI cross-clock module, in which bit width transition finishes. (TX: 32bit->8bit; RX: 8bit->32bit) WR_BUF: Cache the write SPI data of AHB, and write them to WR_FIFO. RD_BUF: Cache the read SPI data of RD_FIFO to AHB. WR_FIFO: SPI write data FIFO (SRAM 32x32) RD_FIFO: SPI read data FIFO (SRAM 32x32) in the normal mode.
SPI_Controller	SPI controlling center. It generates TX/RX controlling signal in the course of SPI communication.
SPI_Interface	Standard SPI interface. It is responsible for receiving and transmitting data with Devices.

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Sub-block	Description
SPI_Bit	the processing module in SPI 3-wire mode.

8.18.3 Functional Description

8.18.3.1 External Signals

The following table describes the external signals of SPI Flash Controller. When using SPI Flash Controller, the corresponding PADs are selected as SPI Flash Controller function via section 8.6 GPIO.

Table 8-58 SPI Flash Controller External Signals

Signal Name	Description	Type
SPIF-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF-CLK	SPI Master Mode Clock Output	O
SPIF-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF-DQS	Data Strobe Signal	I
SPIF-D[7:4]	SPI Master Mode Data in Octal Mode	I/O
SPIF-WP	SPI Write Protect, Low Active	I/O
SPIF-HOLD	SPI Hold Signal	I/O

8.18.3.2 Clock Sources

The SPI_Flash controller gets 5 different clock sources and users can select one of them to make SPI Flash Controller clock source. The following table describes the clock sources for SPI Flash Controller. For more details on the clock setting, configuration, and gating information, see section 2.7 Clock Controller Unit (CCU).

Table 8-59 SPI Flash Controller Clock Sources

Clock sources	Description	Clock module
HOSC	24 MHz Crystal	CCU
PERI0_400M	Peripheral Clock, default value is 400 MHz.	
PERI0_300M	Peripheral Clock, default value is 300 MHz.	
PERI1_400M	Peripheral Clock, default value is 400 MHz.	
PERI1_300M	Peripheral Clock, default value is 300 MHz.	

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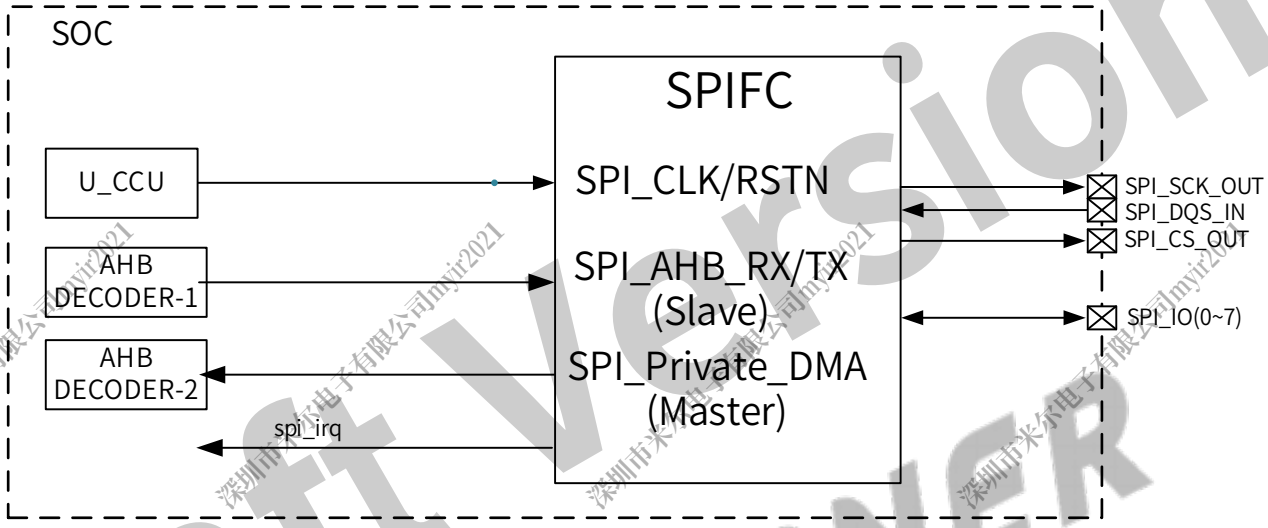
8.18.3.3 Typical Application

The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 8-121 Typical Application



The SPI Flash Controller is running in Master device. SPI_SCK is generated and transmitted to external device. The data from the TX FIFO is routed to the MOSI pin. The data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_CS) signal is active in low level. SPI_CS must be set to low before data are transmitted or received.

8.18.3.4 SPI Flash Controller feature list

Table 8-60 SPI Flash Controller Feature List

SPI mode		Feature List					
		STR	DTR	DTR-RX-DQS	SCK_MODE	Address Size	Description
Bit Mode	3-wire 4-wire	√	×	×	mode0	×	/
Standard SPI	1-1-1-1	√	√	√	• mode 0/1/2/3 (STR) • mode0 (DTR)	24bit/32 bit	• 1-1-1-1: cmd-addr-mode-data. • mode is optional and can be turned off.
Dual SPI	1-1-1-2	√	√	√			

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SPI mode		Feature List					
		STR	DTR	DTR-RX-DQS	SCK_MODE	Address Size	Description
	1-1-2-2						
	1-2-2-2						
	2-2-2-2						
Quad SPI	1-1-1-4	√	√	√			
	1-1-4-4						
	1-4-4-4						
	4-4-4-4						
Octal SPI	1-1-1-8	√	√	√			8-wire DTR only supports the following: ADDR-24+MODE ADDR-32
	1-1-8-8						
	1-8-8-8						
	8-8-8-8						

8.18.3.5 SPI Flash Controller Clock

SPI includes two clock domains: ahb_clk and spi_clk:

- The functions in ahb_clk: parameter analysis (ahb_register) and DMA.
- The functions in spi_clk: cross domain clock, main control unit, the communication between SPI-TX/RX and external devices.

The clock management unit (CMU) divides the external SPI reference clock and gets the o_spi_clk as the internal clock. Based on the clock properties configured by the CPU, the sckt/sckr is gotten to be used as communication clocks for the SPI_TX_INTERFACE/SPI_RX_INTERFACE.

The clock properties include：

- SPI Clock Mode
- DQS EN
- STR or DTR

When the SPI runs at a higher clock frequency, sckr may sample the wrong data because of lane delay. Thus, before sampling, the sckr should be processed by the receive clock latency.

SPI Flash Controller Clock Mode

The SPI Flash controller supports 4 different modes for data transfer. Software can select one of the four modes in which the SPI works by setting the bit5(SPI_CPOL) and bit4(SPI_CPHA) of SPI Global Control Register[0x0004].

The SPI_CPOL defines the signal polarity when SPI_SCLK is in the idle state. The SPI_SCLK is high level when POL is '1 'and it is low level when POL is '0'. The SPI_CPHA decides whether the leading

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edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kind of modes are listed Table:

Table 8-61 SPIFC Modes with Clock Polarity and Phase

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

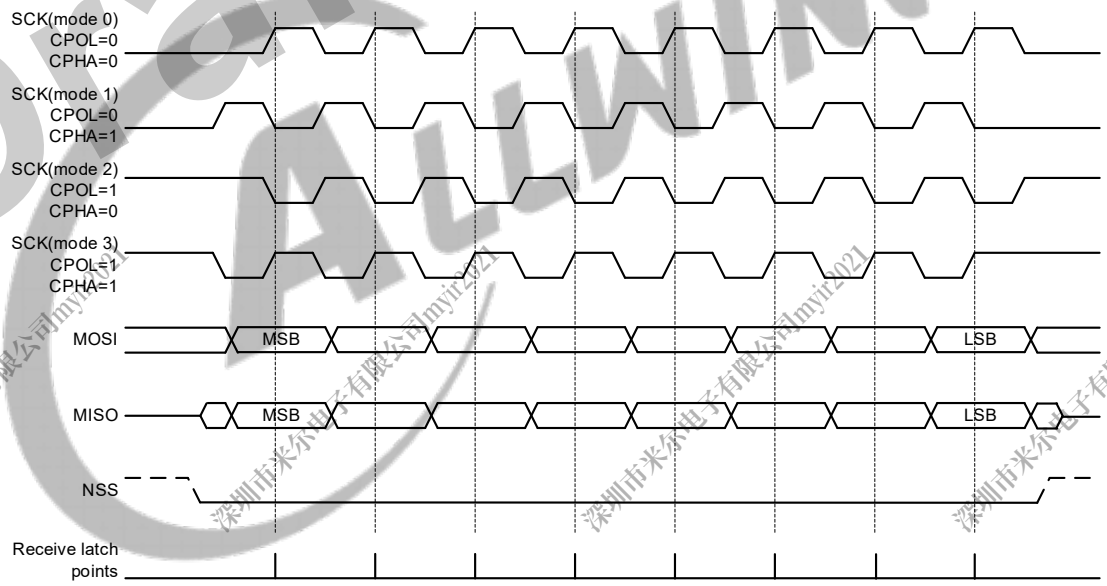
During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges and is shifted in on falling edges.

SPI Bit Mode only supports Phase 0, Polarity 0 operation; the most significant bit (MSB) of data is transmitted first which is not configurable.

The following figure describe four waveforms for SPI_SCLK.

Figure 8-122 SPI Transfer Mode



For MSB first

Single Transfer Rate (STR)

In mode 0 and mode 3, the input data of devices will be latched at the rising edge of SCK, and the output data will be used at the falling edge of SCK.

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Figure 8-123 SPI STR Transfer

Double Transfer Rate (DTR)

As with the STR command, the instruction bit is latched at the rising edge of the clock in the DTR command, but the address and input data are latched at the dual edge. After the instruction bit is latched at the falling edge of SCK, the first address bit will be latched at the next rising edge of SCK. The first output data bit will be sent at the falling edge of the last access latency period.

As with the STR command, the SCK period is the cycle between two adjacent SCK falling edges. In mode 0, the SCK is already at a low level when some command starts to be executed, thus the first SCK period during the command execution indicates the cycle from the falling edge of CS# to the first falling edge of SCK.

Figure 8-124 SPI DTR Transfer Example, 1-4-4

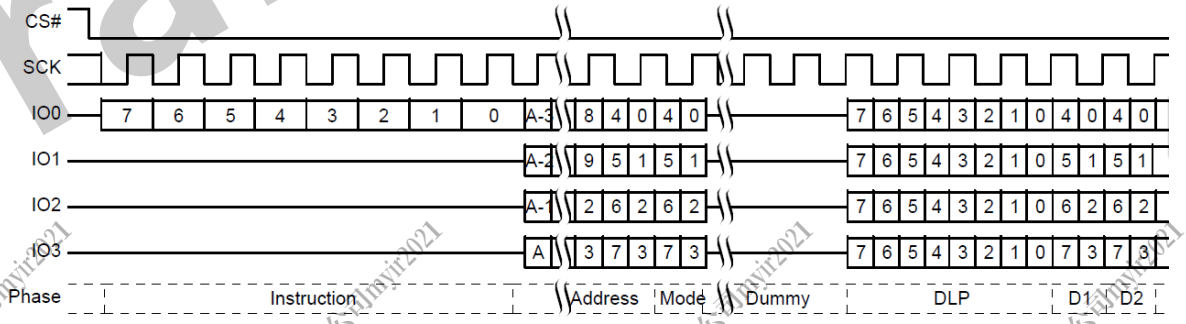
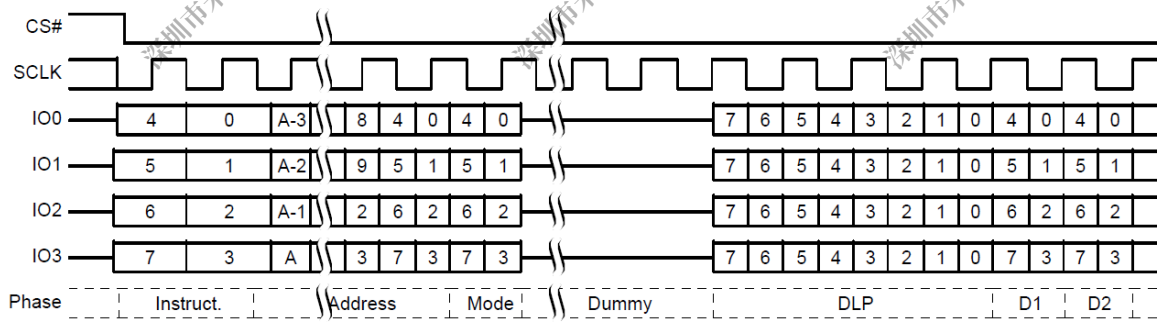


Figure 8-125 SPI DTR Transfer Example, 4-4-4



DQS

DQS（DATA Strobe Signal）signal indicates input/output data valid for DTR modes and is required to support high-speed data. When data strobe function is enabled, DQS signal is driven to ground

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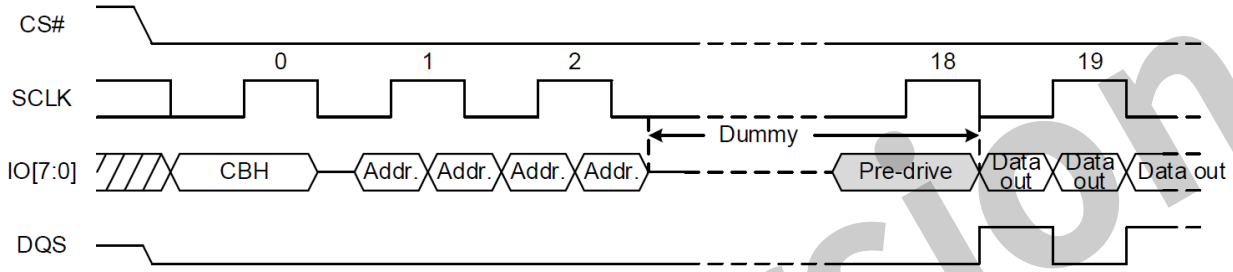
once CS# goes LOW till the device is driving output data, in which case DQS toggles to synchronize data output. When data strobe function is not enabled, DQS signal will not be driven.

Figure 8-126 SPI DTR Transfer with DQS Input Clock Signal



8.18.3.6 SPI Run Clock and Sample Mode

SCKR Delay through Digital Adjustment

To realize the SCKR delay, connect the clk_gate and clk_xor in series to control the opening time of the EN terminal of clk_gate and the polarity of the EN terminal of clk_xor. The specific steps are as follows:

Step 1 Enable the EN terminal delay of the first-level clk_gate module to realize a delay of 1 sclk. (the effective range is 0-3 sclk)

Step 2 Make the EN terminal of the second-level clk_xor module differ in polarity to realize a delay of 0.5 sclk. (the effective values are 0 sclk and 0.5 sclk)

SCKR Delay through Analog Adjustment

There are delay chains in SPI, used to generate delay to make proper timing between internal SPI clock signal and data signals. Delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

Take RX delay chain as an example: the steps to calibrate delay chain are as follows:

Step 1 Configure a proper clock for the SPI Flash Controller. Calibration delay chain is based on the clock for SPI FLASH CONTROLLER from Clock Controller Unit (CCU)

Step 2 Set proper initial delay value to (SPI Timing Configure Register, 0x000C). Write 0x60 to this register to set initial delay value 0x20 to delay chain. Then write 0x0 to delay control register to clear this value.

Step 3 Write 0x80 to SPI Timing Configure Register to start calibrate delay chain.

Step 4 Wait until the flag (Bit7 in SPI Timing Delay State Register 0x0010) of calibration done is set. The number of delay cells is shown at Bit5-Bit0 in SPI Timing Delay State Register. The delay time generated by these delay cells is equal to the cycle of SPI FLASH CONTROLLER's clock nearly. This value is the result of calibration.

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Step 5 Calculate the delay time of one delay cell according to the cycle of SPI FLASH CONTROLLER's clock and the result of calibration.

8.18.3.7 SPI Transfer Mode

SPI supports multiple transfer modes such as SPI Bit Mode, SPI Standard Mode, SPI Dual Mode, SPI Quad Mode, and SPI Octal Mode. Their main differences are the number of wires. Even in the same transfer mode, the detail modes will be derived based on the number of wires used to data transfer. The number of data lines used by Command-Address-Data is indicated on the subdivision pattern heading, expressed as (x-x-x). For example, Command uses one Data line, Address and data both use two data lines, identified by (1-2-2).

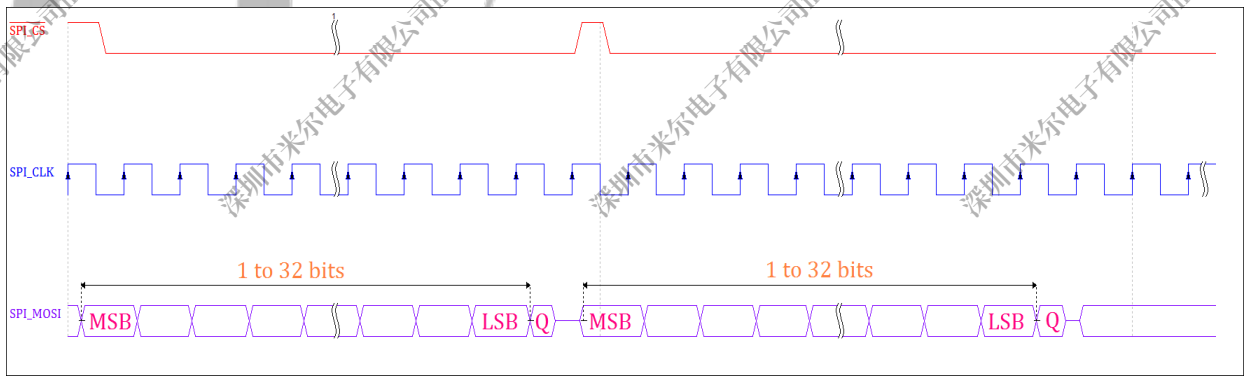
SPI Bit Mode (3-Wire/4-Wire)

For some specific scenarios, some devices such as the sensor use the SPI interfaces as the communication protocol. Generally, their data size is relatively small, and some devices support three wires, so the bit mode is added and 3-wire mode and 4-wire mode are subdivided, which includes SPI_CS, SPI_SCK, and 1/2 wires. The transmission length ranges from 1-32bit.

The 4-Wire Mode is selected when the Work Mode Select(bit[1:0]) is equal to 0x3 in the SPI Bit-Aligned Transfer Configure Register. In SPI 4-Wire Mode, the input data and output data use the independent two data line. The MISO is used for input data, and the MOSI is used for output data.

The SPI 3-Wire Mode is only valid when the SPI controller work as Master Device, and selected when the Work Mode Select(bit[1:0]) is equal to 0x2 in the SPI Bit-Aligned Transfer Configure Register. and in the 3-Wire mode, the input data and the output data use the same single data line. The following figure describe this mode.

Figure 8-127 SPI 3-Wire Mode



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SPI Standard Mode (4-Wire)

Signal Wire: CS#, SCK, IO0, and IO1.

Figure 8-128 SPI CMD with Single IO

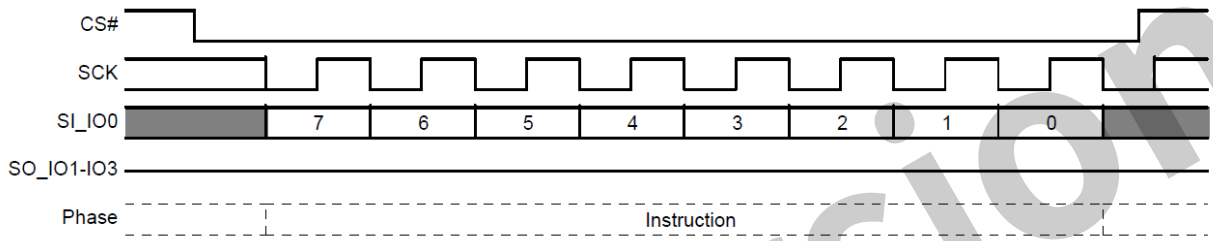


Figure 8-129 SPI Write CMD and DATA with One Wire

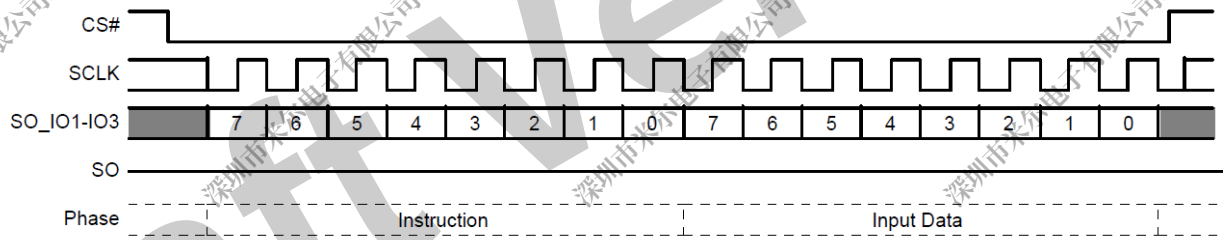


Figure 8-130 SPI Write CMD and Read DATA with One Wire (No Dummy)

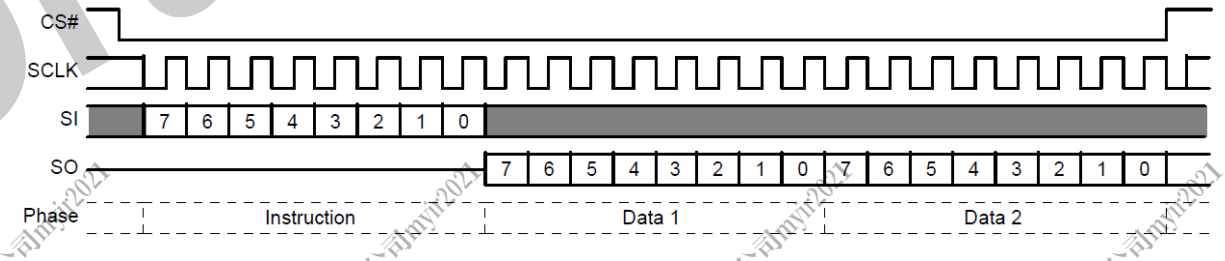
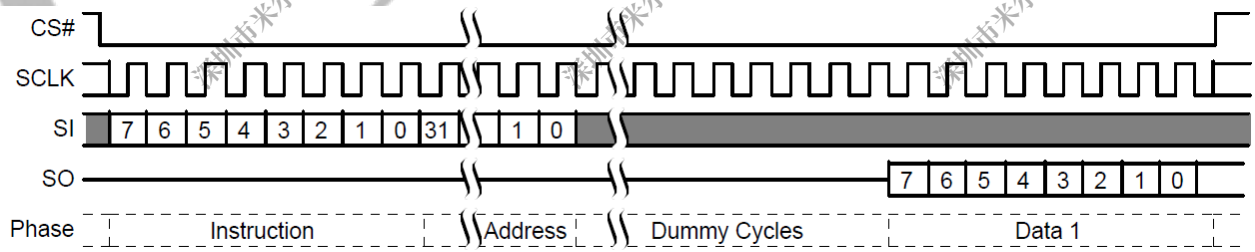


Figure 8-131 SPI Write CMD and Read DATA with One Wire (with Dummy)



SPI Dual Mode

Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices. Data can be read at a faster speed using two data bits (MOSI and MISO) at a time. The following describe the Dual Input/Dual Output SPI (1-1-2), the Dual IO SPI (1-2-2), and the (2-2-2) SPI Mode.

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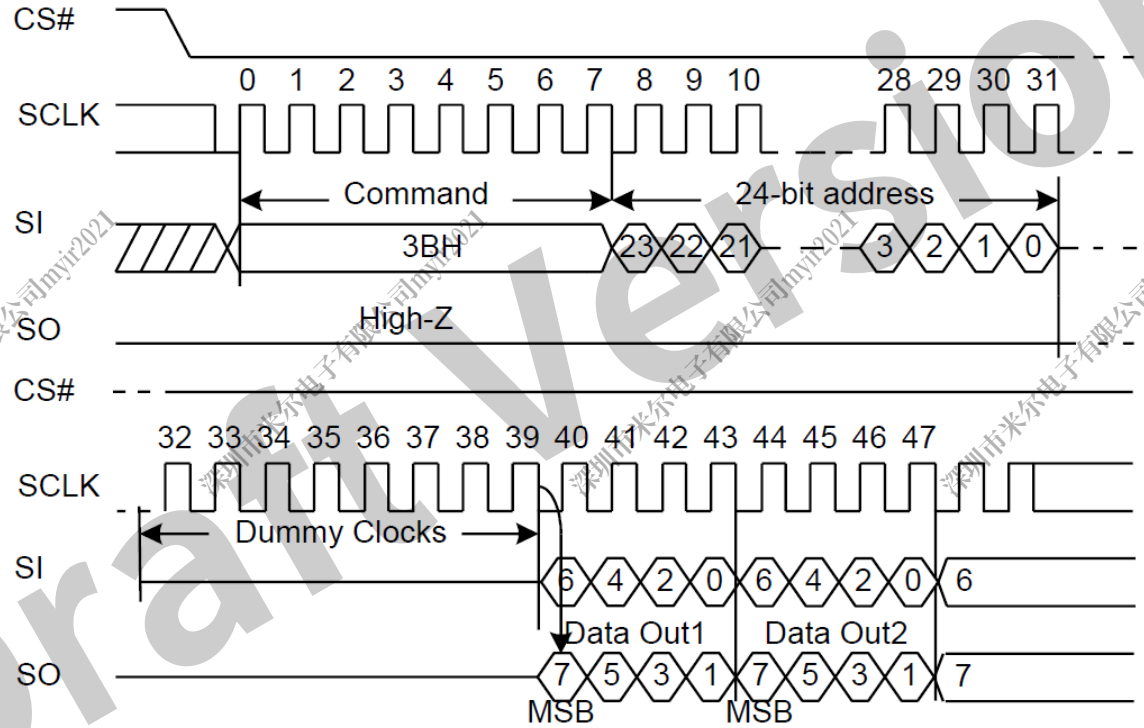
- SPI Dual Input/dual Output Mode (1-1-2)

In the dual Input/dual Output SPI, the command, address, and the dummy bytes are output in the unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output (write) and input (read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

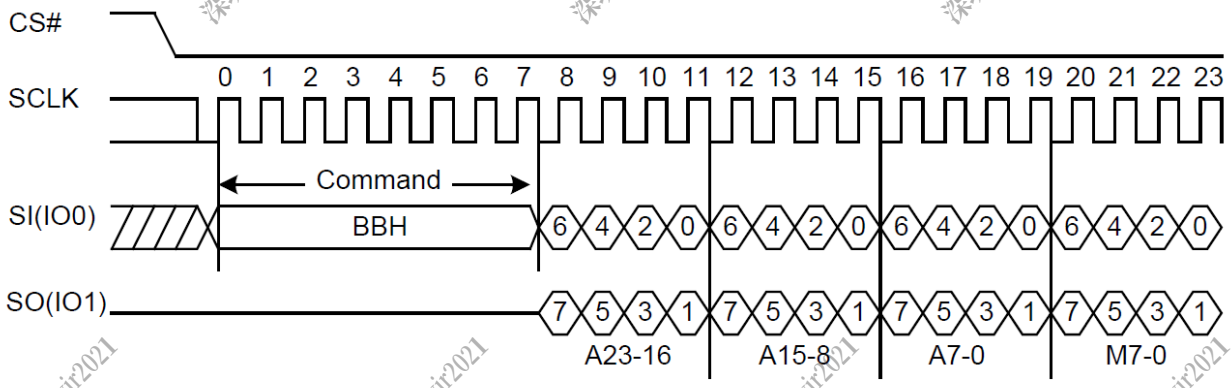
Figure 8-132 SPI Dual Input/Dual Output Mode（1-1-2）



- SPI Dual IO Mode (1-2-2)

In the Dual IO SPI, only the command bytes are output in the unit of a single bit in serial mode through SPI_MOSI line. The address bytes and the dummy bytes are output in the unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes are output (write) and input (read) in the unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 8-133 SPI Dual Input/Dual Output Mode (1-2-2)



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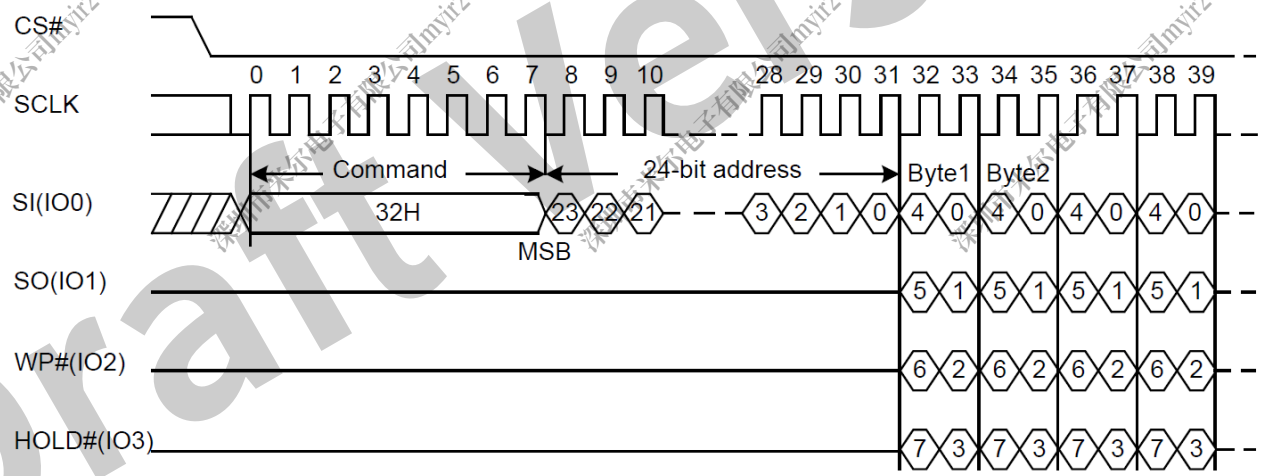
SPI Quad Mode

Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits (MOSI, MISO, IO2(WP#) and IO3(HOLD#)) at the same time. The following describe the Quad Input/Quad Output SPI (1-1-4), 1-4-4 mode, and 4-4-4 mode.

- Quad Input/Quad Output SPI (1-1-4)

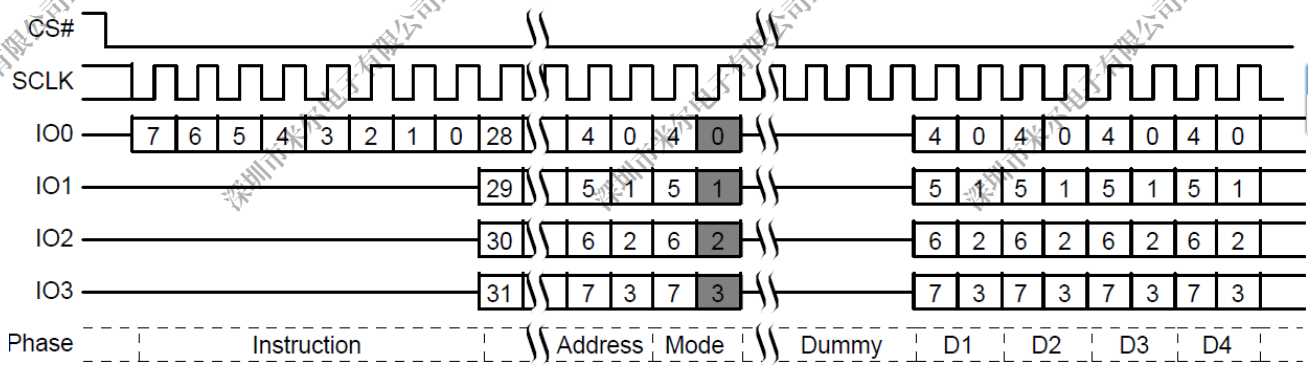
In the Quad Input/Quad Output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output (write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

Figure 8-134 SPI Quad Input/Dual Output Mode (1-1-4)



- 1-4-4 Mode

Figure 8-135 SPI Quad Input/Dual Output Mode (1-4-4)



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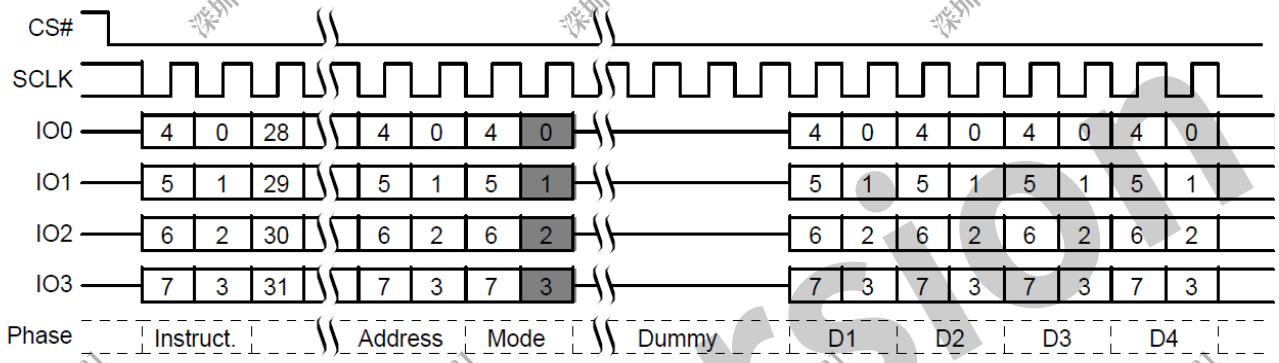
- 4-4-4 Mode

Figure 8-136 SPI Quad Input/Dual Output Mode (4-4-4)

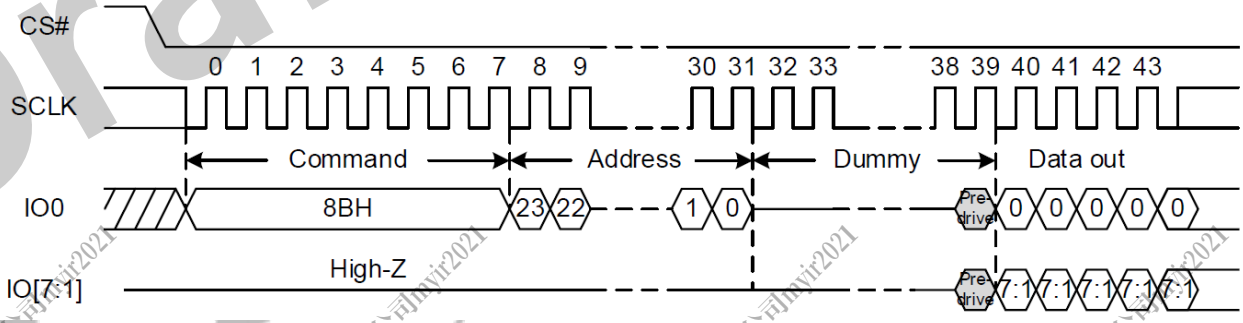


SPI Octal Mode

The Octal SPI Mode allow data to be transferred to or from the device at eight times the rate of the standard SPI. When using the Octal SPI, there are 8 data wires.

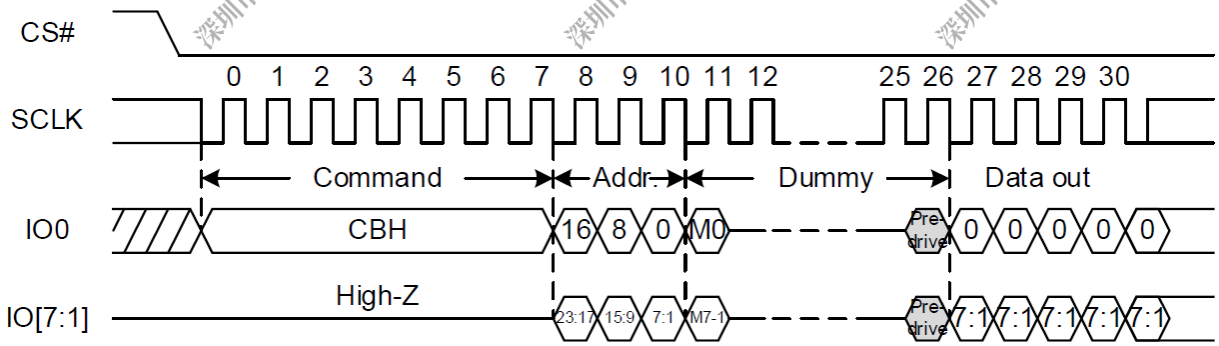
- SPI Octal 1-1-8

Figure 8-137 SPI Octal Input/Dual Output Mode (1-1-8)



- SPI Octal 1-8-8

Figure 8-138 SPI Octal Input/Dual Output Mode (1-8-8)



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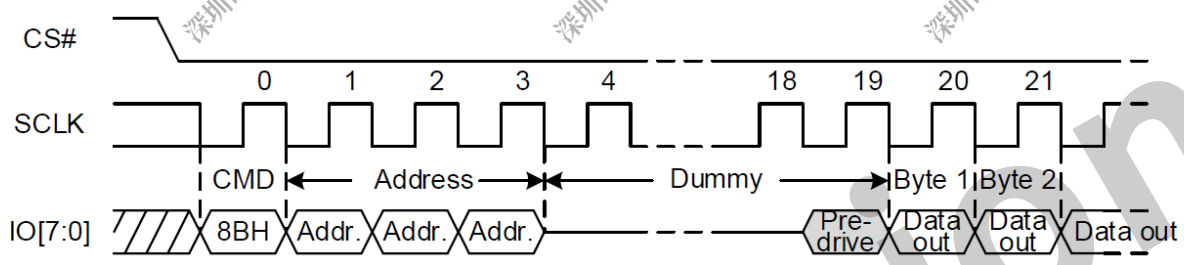
- SPI Octal 8-8-8

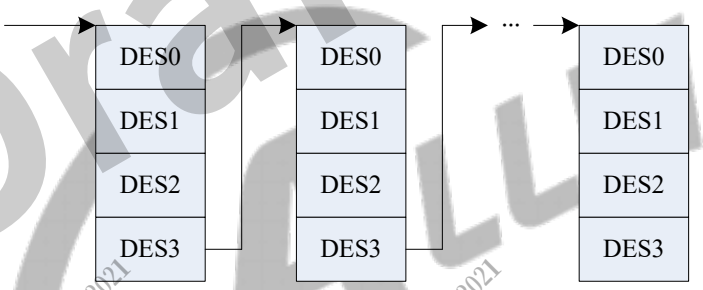
Figure 8-139 SPI Octal Input/dual Output Mode (8-8-8)



8.18.3.8 SPIFC Private DMA

The private DMA adopts the chained descriptor structure. The address and size of the first descriptor are configured by registers. After getting the first descriptor, the hardware will obtain the data from the address recorded in the descriptors. When the current transfer finishes, the hardware will continue to obtain descriptors based on the address of the next descriptor given by the previous descriptor until the terminal character is found. Then, a DMA transfer ends.

Figure 8-140 Descriptor Structure Diagram



The private DMA also supports SPI parameter configuration. The SPI transfer can be configured by the parameters of the descriptors 4-7.

Descriptor0 Definition

Bits	Descriptor
31:7	Reserved
6:4	HBURST_TYPE indicate hburst len 000: SINGLE, hburst_len = 1 011: INCR4, hburst_len = 4 101: INCR8, hburst_len = 8 111: INCR16, hburst_len = 16
3:2	/

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Bits	Descriptor
1	DMA_DIR DMA Write Process or Read Process 0: Read 1:Write
0	DMA_FINISH_FLAG DMA Finish Flag

Descriptor1 Definition

Bits	Descriptor
31:24	DMA_BLK_LEN DMA Block Len Mode 0: 8Byte 1: 16Byte 2: 32Byte 3: 64Byte Recommended Configuration： The data volume of DMA_BLK_LEN is greater than or equal to that of HBURST_TYPE.
23:17	/
16:0	DMA_DATA_LEN Indicate the data byte number of current DMA operation.

Descriptor2 Definition

Bits	Descriptor
31:0	DMA_Buffer_ SADDR The real address is as below The word address is needed, namely, the byte address abandons the low 2 bits.

Descriptor3 Definition

Bits	Descriptor
31:0	NEXT_DESCRIPTOR_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present, which are word (4byte) address (The lower two bits are deleted from the byte address).

Descriptor4 Definition

Bit	Description
31:30	/

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Bit	Description
29	CMD_DTR CMD DTR Control 1: CMD DTR 0: CMD not DTR CAUTION: When CMD DTR, DTR must be on and CMD2 is required.
28	COMMAND_TRANS_EN Set to '1' if command data need trans to device SPI Controller FSM Phase Enable 1: Enable 0:Disable
27:25	/
24	ADDRESS_TRANS_EN Set to '1' if address need trans to device SPI Controller FSM Phase Enable 1: Enable 0:Disable
23:21	/
20	MODE_BIT_TRANS_EN Set to '1' if Mode bit need trans after address SPI Controller FSM Phase Enable 1: Enable 0:Disable
19:17	/
16	DUMMY_BIT_TRANS_EN Dummy Bit State Enable SPI Controller FSM Phase Enable 1: Enable 0:Disable
15:13	/
12	TX_DATA_EN Set to '1' if Data Need Trans SPI Controller FSM Phase Enable 1: Enable 0:Disable
11:9	/
8	RX_DATA_EN Set to '1' if Data Need Receive SPI Controller FSM Phase Enable 1: Enable 0:Disable
7:0	/

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Descriptor5 Definition

Bit	Description
31:0	ADDR_OPCODE Address Content Trans Through SPI

Descriptor6 Definition

This register should be setup while the controller is idle.

Bit	Description
31:24	CMD_OPCODE Command Content Trans Through SPI
23:16	MODE_OPCODE Mode Content Trans Through SPI
15:8	CMD_OPCODE2 Command2 Content Trans Through SPI
7:6	CMD_TRANS_TYPE Command Transfer Type 00: Command can be Shifted to the device on DQ0 01: Command can be Shifted to the device on DQ0 and DQ1 10: Command can be Shifted to the device on DQ0- DQ3 11 : Command can be Shifted to the device on DQ0-DQ7
5:4	ADDR_TRANS_TYPE Address Transfer Type 00: Address can be Shifted to the device on DQ0 01: Address can be Shifted to the device on DQ0 and DQ1 10: Address can be Shifted to the device on DQ0- DQ3 11: Address can be Shifted to the device on DQ0-DQ7
3:2	MODE_BIT_TRANS_TYPE Mode Bit Transfer Type 00: Mode Bit can be Shifted to the device on DQ0 01: Mode Bit can be Shifted to the device on DQ0 and DQ1 10: Mode Bit can be Shifted to the device on DQ0- DQ3 11: Mode Bit can be Shifted to the device on DQ0-DQ7
1:0	DATA_TRANS_TYPE Data Transfer Type 00: Opcode can be Shifted to the device on DQ0 only 01: Opcode can be Shifted to the device on DQ0 and DQ1 only 10: Opcode can be Shifted to the device on DQ0- DQ3 11: Opcode can be Shifted to the device on DQ0-DQ7

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Descriptor7 Definition

Bit	Description
31	DATA_TRANS_NUM[16]
30:29	
28	SPI_NORMAL_EN if dma config spi, this bit start SPI FSM.
27:25	/
24	ADDR_SIZE_MODE Address Size Mode 0: Address Size 24bit. 1: Address Size 32bit.
23:16	DUMMY_TRANS_NUM Number of Dummy Cycles A value of 0 = 1 Cycle A value of 1 = 1 Cycle ... A value of N = N Cycle
15:0	DATA_TRANS_NUM Num of Data Trans Through SPI(Byte) 0: Non-Write. 1: Write 1 Byte. 2: Write 2 Bytes. 3: Write 3 Bytes. ..... 65535: Write 65535 Bytes. **Note: These Bits Indicate number of data bytes in a CHIP SELECT period.** **Notice the difference between DATA_TRANS_NUM here and DMA_DATA_LEN in Descriptor1.**

8.18.4 Programming Guidelines

8.18.4.1 DMA Transfer

The software operation of the SPI DMA transfer is divided into 5 steps. 5 steps are described in detail in the following sections.

Step 1 System Setup

Step 2 SPI Initialization

Step 3 Channel Setup

Step 4 DMA Setup

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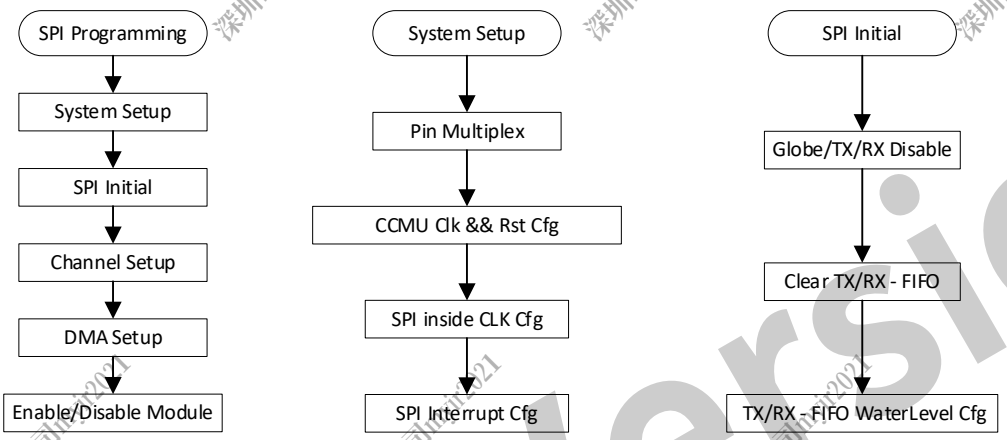
Step 5 Enable SPI

Figure 8-141 SPI Programming flow



8.18.4.2 System Setup

Step 1 Configure SPI Pin

Programming the GPIO.

Step 2 Configure SPI Clock and Reset in CCU

Configure SPI ref clock, AHB Clock, De-assert SPI ref Reset, and AHB reset in Clock Controller Unit (CCU).

Step 3 Configure SPI Internal Working Clock

a) Configure clock source (SPI_TIMING_CFG[0x000C])

- STR Mode

  Write 0 to the CLK_SPI_SRC_SEL bit (bit [24]), the CLK_SCK_SRC_SEL bit (bit [25]) bit, and the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit.

- DTR Mode

  Write 0 to the CLK_SPI_SRC_SEL bit (bit [24]) and the CLK_SCK_SRC_SEL bit (bit [25]) bit.

  Write 1 to the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit.

NOTE

When the value of the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit is 1, the real output clock frequency of SPIF-CLK signal is the SPIFC clock frequency divided by 2.

b) Generate the sckr of SPI data receiving

- Configure SCKR delay mode (SPI_TIMING_CFG[0x000C]). Refer to the section SPI Run Clock and Sample Mode for more details.

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SCKR_DLY_MODE_SEL (bit [20]): Select delay mode. Writing 0 is the digital delay, and writing 1 is the digital and analog delay.

- Configure the digital delay of SCKR

  SPI_TIMING_CFG[0x000C], DIGITAL_SCKR_DELAY_CFG (bit[18:16]): digital delay volume. (step length: 0.5 clock)

- Configure the analog delay of SCKR

  SPI_TIMING_CFG[0x000C], ANALOG_SAMP_DL_SW_VALUE (bit[5:0])

c) Generate SPI output clock

- Select SPI working mode (SPI_MODE). Refer to the section SPI Flash Controller Clock Mode for more details.
- Configure SPI_GLOBAL_CTRL[0x0004]:

  SPI_CPOL (bit [5]): Clock Polarity

  SPI_CPHA (bit [4]): Clock Phase

- DTR switch (SPI_GLOBAL_CTRL[0x0004])

  DTR_EN (bit [16]): It is closed by default.

Step 4 Configure SPI Interrupt

Configure the SPI_INT_EN (0x0014[31:0]) as 0.

8.18.4.3 SPI Initialization

After the system setup, the registers of SPI can be setup. At first, the SPI needs to be initialized.

Step 1 Disable the SPI_GLOBAL_CTRL.

SPI_NMODE_EN (bit [2]): Write 0.

Step 2 Reset TX/RX FIFO (SPI_GLOBAL_CTRL_ADD[0x0008])

Reset the CDC-BUF/FIFO of TX channel: Write 1 to CDC_WF_SRST to reset the WR_BUFF and WR_FIFO in SPI_WR_BUF_CTRL and the SWF in SPI_TX_INTERFACE.

Reset the CDC-BUF/FIFO of RX channel: Write 1 to CDC_RF_SRST.

Step 3 Water Lever

Configure the water level of FIFO.

SPI_CDC_FIFO_TRIG_LEVEL[0x004C]

8.18.4.4 Channel Setup

Select SPI Channel Parameter Resource

- SPI channel parameter resources:

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- CPU is configured by AHB.
- The private DMA fetches descriptors and parses the descriptors 4-7.

- Configure SPI channel parameter sources: SPI_GLOBAL_CTRL[0x0004] and SPI_CFG_MODE(bit[0])
  - 0: Source from CPU
  - 1: Source from DMA descriptor

NOTE

If the parameters source from CPU, configure in reference to all the guidelines in the section Channel Setup. If the parameters source from DMA, configure in reference to the first two guidelines in the section 8.18.4.4 Channel Setup.

SPI Interface Configuration—Public Configuration

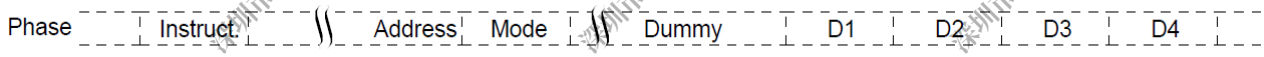
Step 1 CS Delay Configuration: SPI_CS_DELAY[0x001C]

- CSDA (bit [23:16]): The intervals of two adjacent CS enable. The minimum interval is 1sclk. The actual value is CSDA+1.
- CSEOT (bit [15:8]): After the SCLK_OUT is invalid, the CS signal will be de-asserted after CSEOT SCLK. The minimum interval is 1sclk. The actual value is CSEOT+1.
- CSSOT (bit [7:0]): After the SCLK_OUT is valid, the CS signal will be asserted after CSSOT SCLK. The minimum interval is 1sclk. The actual value is CSSOT+1.

Step 2 Activate SPI Trans Phase (SPI_TRANS_PHA_CFG[0x0020])

In a transmission of the SPI interface, the transferring content of I/O wire is as follows. Enable the corresponding Trans Phase based on the content to be transferred.

Figure 8-142 SPI Transfer Phase Flow Diagram



- COMMAND_TRANS_EN (bit [28]): Command (Instruct) Transfer Enable
- ADDRESS_TRANS_EN (bit [24]): Address Transfer Enable
- MODE_BIT_TRANS_EN (bit [20]): Mode Transfer Enable
- DUMMY_BIT_TRANS_EN (bit [16]): Dummy Transfer Enable
- TX_DATA_EN (bit [12]): Enable TX data transfer.
- RX_DATA_EN (bit [8]): Enable RX data transfer.

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NOTE

RX_DATA_EN and TX_DATA_EN cannot be activated at the same time.

Step 3 Configure the number of I/O used by TransPhase. (SPI_TRANS_CFG2[0x0028])

- CMD_TRANS_TYPE (bit [13:12])
- ADDR_TRANS_TYPE (bit [9:8])
- MODE_BIT_TRANS_TYPE (bit [5:4])
- DATA_BIT_TRANS_TYPE (bit [1:0])

Step 4 Configure the transferring number of TransPhase (SPI_TRANS_NUM[0x002C])

SPI Interface Configuration—Normal Mode

Configure the contents of all TransPhase

- ADDR: SPI_TRANS_CFG1[0x0024], ADDR_OPCODE (bit [31:0])
- CMD: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[31:24])
- MODE: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[23:16])

SPI Interface Configuration—BIT Mode

Refer to the functions of SPI Bit Mode (3-Wire/4-Wire).

8.18.4.5 DMA Setup

DMA Configuration Registers

Step 1 Configure the descriptor size and starting address of the first descriptor.

- SPI_DMA_CTRL[0x0040]: DMA_DESCRIPTOR_LEN（bit[11:4]）
- SPI_DESCRIPTOR_SADDR[0x0044]

Step 2 Initiate DMA

SPI_DMA_CTRL[0x0040]，CFG_DMA_START（bit[0]）

DMA Configuration

Step 1 In the DMA register, configure the size and the starting address of storage location for the first descriptor.

Step 2 Configure the first DMA descriptor and store the corresponding address in the step 1.

- Descriptor0
  - AHB Master Burst Configuration

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HBURST_TYPE (bit [6:4]): Support SINGLE/INCR4/INCR8/INCR16 mode.

- DMA Handling Direction Configuration

  DMA_DIR (bit [1]): Read by DMA, or Write by DMA.

- DMA Finish Flag

  DMA_FINISH_FLAG (bit [0]): Currently the memory space allocated by the CPU to DMA may be a part of the total data volume to be transferred. For instance, the 256 Byte memory space is allocated to transfer 1 MB data. In this situation, a DMA descriptor points to the allocated 256 Byte data location and the next descriptor to fetch data. When the data of the last descriptor is fetched by DMA, the stop bit should be pulled up to terminate a DMA handling.

➢ Descriptor1

- DMA_BLK_LEN ([31:16])

  DMA BLK length. It indicates the size of each DMA packet, with multiples of 8 Byte aligned to achieve the optimized rate when accessing storage.

- DMA_DATA_LEN (bit [15:0])

  It indicates the data volume indicated by the current descriptor of DMA

➢ Descriptor2

It indicates the data storage location of current descriptor.

➢ Descriptor3

It indicates the storage location of the next descriptor.

➢ Descriptor4-7

The SPI configuration parameters. When setting parameters with DMA for SPI, the content of descriptors is configured to SPI.

8.18.4.6 Enable SPI

Normal Mode

SPI_GLOBAL_CTRL[0x0004]，SPI_NMODE_EN (bit[2])

Write 1 to the SPI_NMODE_EN, then it will be auto pulled down.

8.18.4.7 CPU Transfer

The software operation of CPU transfer is almost the same as DMA transfer. There are still two main differences. One difference is that when CPU transfer, channel parameter cannot come from DMA descriptors. SPI_GLOBAL_CTRL[0x0004], SPI_CFG_MODE(bit[0]) must be set 0. All parameters should come from REGISTER FILE.

SPI_GLOBAL_CTRL[0x0004], SPI_CPU_MODE_EN(bit[20]) is used to start CPU transfer (Different from descriptor and SPI_GLOBAL_CTRL[0x0004], SPI_NMODE_EN(bit[2])).

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Another difference is that when reading data from Register [0x0210], it is recommended to read SPI_CDC_FIFO_STA[0x0050], RF_CNT([bit5-0]), especially when total read number is not integer multiple of trigger level. When writing data to Register [0x0220], it is always ready as long as trigger level is not reached.

NOTE

Register [0x0040] and [0x0044] are not used in CPU transfer.

8.18.4.8 Status Reading

The software operation of STATUS READING is almost the same as CPU transfer. CMD_TRANS_EN and RX_DATA_EN must be set high because RX data path is used for status reading. MODE_BIT_TRANS_EN and DUMMY_BIT_TRANS_EN should be set accordingly. But STATUS OPCODE will not go through READ_FIFO and READ_BUFFER. Meanwhile, I/O Pins used should be set accordingly. SPI_STATUS_READ[0x0068] and SPI_STATUS_READ_2[0x006C] are used for STATUS READING. And to avoid endless reading and dead lock, CPU should tell the maximum reading times. Then, to start STATUS READING, SPI_READ_STATUS_MODE_EN should be set. In this mode, DATA_TRANS_NUM (002C, [15:0]) is suggested to be 1 and DTR_EN [0x0004, bit 16] is suggested to be 0.

8.18.5 Register List

Module Name	Base Address
SPIFC	0x047F 0000

Register Name	Offset	Description
SPI_GLOBAL_CTRL	0x0004	SPI Global Control Register
SPI_GLOBAL_CTRL_ADD	0x0008	SPI Global Control Additional Register
SPI_TIMING_CFG	0x000C	SPI Timing Configure Register
SPI_TIMING_DLY_STA	0x0010	SPI Timing Delay State Register
SPI_INT_EN	0x0014	SPI Interrupt Enable Register
SPI_INT_STA	0x0018	SPI Interrupt Status Register
SPI_CS_DELAY	0x001C	SPI Chipselect Delay Register
SPI_TRANS_PHA_CFG	0x0020	SPI Trans Phase Configure Register
SPI_TRANS_CFG1	0x0024	SPI Trans Configure1 Register
SPI_TRANS_CFG2	0x0028	SPI Trans Configure2 Register
SPI_TRANS_NUM	0x002C	SPI Trans Number Register
SPI_DMA_CTRL	0x0040	SPI DMA Control Register
SPI_DESCRIPTOR_SADDR	0x0044	SPI DMA Descriptor Start Address Register
SPI_CDC_FIFO_TRIG_LEVEL	0x004C	SPI CDC FIFO Trigger Level Register
SPI_CDC_FIFO_STA	0x0050	SPI CDC FIFO Status Register

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Register Name	Offset	Description
SPI_BATC	0x0054	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0058	SPI Bit-Aligned CLOCK Configuration Register
SPI_TBR	0x005C	SPI TX Bit Register
SPI_RBR	0x0060	SPI RX Bit Register
SPI_STATUS	0x0064	SPI Status Register
SPI_STATUS_READ	0x0068	SPI READ Status Register
SPI_STATUS_READ2	0x006C	SPI READ Status Register_2
SPI_RX_DATA	0x0210	SPI RX Data Register
SPI_TX_DATA	0x0220	SPI TX Data Register

8.18.6 Register Description

8.18.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/W	0x0	START_MODE 0：old start mode 1：new start mode
21	R/WAC	0x0	SPI_READ_STATUS_MODE_EN SPI READ STATUS Mode Enable 0: Disable 1: Enable This bit is not used for data transfer. It is used for status confirm. And when this operation ends, the last returned byte value is sent to 0x0064[31:24].
20	R/WAC	0x0	SPI_CPU_MODE_EN SPI CPU Mode Enable 0: Disable 1: Enable CPU transfer mode.
19	R/W	0x0	SPI_CLK_OUTPUT 0: Disable 1: Enable when the SPI_CLK_OUTPUT is enabled, the SPI FLASH CONTROLLER will convey the sclk from CCU to the spi_sck_out pin. This bit cannot be enabled in the process of data transmission to avoid anomaly.

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Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	SPI_TX_CFG_FBS Transmit Interface First Transmit Bit Select. 0: MSB First 1: LSB First
17	R/W	0x0	SPI_RX_CFG_FBS Receive Interface First Transmit Bit Select. 0: MSB First 1: LSB First
16	R/W	0x0	DTR_EN Double Trans Rate Enable 0: Disable 1: Enable
15	R/W	0x0	SPI_WP_EN 0: Disable 1: Enable In Standard SPI or Dual SPI, SPI PIN Write Protect Function can be Open In the open status, SPI_WP_IO2_OUT is enabled. The exact polarity is decided by the configuration of SPI_WP_POL. In the closed status, SPI_WP_IO2_OUT is controlled by hardware. The exact polarity is decided by the controller.
14	R/W	0x0	SPI_WP_POL SPI PIN Write Protect Polar 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
13	R/W	0x0	SPI_HOLD_EN 0: Disable 1: Enable In Standard SPI or Dual SPI, SPI PIN HOLD Function can be Open In the open status, SPI_HOLD_IO3_OUT is enabled. The exact polarity is decided by the configuration of SPI_HOLD_POL. In the closed status, SPI_HOLD_IO3_OUT is controlled by hardware. The exact polarity is decided by the controller.

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Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	SPI_HOLD_POL SPI PIN HOLD Polar 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
11	/	/	/
10	R/W	0x0	DQS_RX_EN Receive DQS Signal Enable 0: Disable 1: Enable
9	R/W	0x0	DUMMY_BIT_POL Dummy Bit Trans Value 0: Dummy bit Trans 0 1: Dummy bit Trans 1
8	R/W	0x1	SPI_CS_POL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
7:6	R/W	0x0	SPI_CS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted
5	R/W	0x0	SPI_CPOL SPI Clock Polarity Control 0: Active High Polarity. 1: Active Low Polarity.
4	R/W	0x0	SPI_CPHA SPI Clock/Data Phase Control 0: Phase 0(Leading Edge for Sample Data) 1: Phase 1(Leading Edge For Setup Data)
3	/	/	/
2	R/WAC	0x0	SPI_NMODE_EN SPI Normal Mode Enable 0: Disable 1: Enable DMA transfer mode.
1	/	/	/

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Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SPI_CFG_MODE SPI Parameter Config Source in normal(DMA) mode. Set to 0 When CPU Transfer. 0: From REGISTER 1: From DMA Descriptor

8.18.6.2 0x0008 SPI Global Control Additional Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: SPI_GLOBAL_CTRL_ADD
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/WAC	0x0	SPI_FLASH_DMA_END Terminate the DMA Chain after the present BLK is done. After the DMA chain terminates, set 1 to this bit to stop DMA transmission after the DMA module finishes the BLK whether the current chain completes or the finish_flag is set to 1. DMA_END and SPI_SRST should be used together: Enable the DMA_END first, and then enable the SPI_FLASH_SRST after DMA_END is cleared.
3	R/WAC	0x0	SPI_FLASH_SRST Reset All the Logic in SPI Flash (DMA chain is not included)
2	/	/	/
1	R/WAC	0x0	CDC_WF_SRST Transfer FIFO Software Reset, In SPI_WR_BUF_CTRL Module 0: Auto Clear to 0. 1: Reset Transfer FIFO. Writing 1 to this bit will reset the control portion of the transfer FIFO, and auto clear to 0 when completing reset operation. Writing 0 to this bit has no effect.

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Offset: 0x0008			Register Name: SPI_GLOBAL_CTRL_ADD
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	CDC_RF_SRST Receiver FIFO Software Reset, In SPI_RD_BUF_CTRL Module 0: Auto Clear to 0. 1: Reset Receiver FIFO. Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.

8.18.6.3 0x000C SPI Timing Configure Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	CLK_SCKOUT_SRC_SEL SPI Output Clk Select Select the rate of SPI output clock (SCK_OUT). 0: Original Clock 1: Two-frequency Clock
25	R/W	0x0	CLK_SCK_SRC_SEL SPI Interface Clock Select 0: Original Clock 1: Two-frequency Clock
24	R/W	0x0	CLK_SPI_SRC_SEL SPI Inter Process Clock Select 0: Original Clock 1: Two-frequency
23:22	/	/	/
21	R/W	0x0	SCKT_DELAY_MODE_SEL SCKT Delay Mode Select 0: Select the SCKT without delay 1: Select the SCKT after the analog delay chain adjustment
20	R/W	0x0	SCKR_DELAY_MODE_SEL SCKR Delay Mode Select 0: digital delay 1: digital delay + analog delay
19	/	/	/

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Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
18:16	R/W	0x0	DIGITAL_SCKR_DELAY_CFG Digital SCKR Delay Value Config, Step 0.5 spi_clk 000: delay 0 clk 001: delay 0.5 clk 010: delay 1 clk 011: delay 1.5 clk 100: delay 2 clk 101: delay 2.5 clk 110: delay 3 clk 111: delay 3.5 clk
15	R/W	0x0	ANALOG_SAMP_DL_CAL_START_TX Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R/W	0x0	ANALOG_SAMP_DL_SW_EN_TX Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
13:8	R/W	0x0	ANALOG_SAMP_DL_SW_VALUE_TX Sample Delay Software Value The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.
7	R/W	0x0	ANALOG_SAMP_DL_CAL_START_RX Sample Delay Calibration Start When set, start sample delay chain calibration.
6	R/W	0x0	ANALOG_SAMP_DL_SW_EN_RX Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
5:0	R/W	0x0	ANALOG_SAMP_DL_SW_VALUE_RX Sample Delay Software Value The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

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8.18.6.4 0x0010 SPI Timing Delay State Register (Default Value: 0x0000_2020)

Offset: 0x0010			Register Name: SPI_TIMING_DLY_STA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ANALOG_SAMP_DL_CAL_DONE_TX Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
14	/	/	/
13:8	R	0x20	ANALOG_SAMP_DL_TX Sample Delay Value It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R	0x0	ANALOG_SAMP_DL_CAL_DONE_RX Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
6	/	/	/
5:0	R	0x20	ANALOG_SAMP_DL_RX Sample Delay Value It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.

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8.18.6.5 0x0014 SPI Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0014			Name: SPI_INT_EN
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	READ_STATUS_DONE_INT_EN 0: Disable. 1: Enable.
27	R/W	0x0	READ_STATUS_TIME_OUT_INT_EN 0: Disable. 1: Enable.
26	R/W	0x0	SPI_TRANS_DONE_INT_EN SPI Transmit Finish Interrupt Enable 0: Disable. 1: Enable.
25	/	/	/
24	R/W	0x0	DMA_TRANS_DONE_INT_EN DMA Chain Transmit Finish Interrupt Enable 0: Disable. 1: Enable.
23	R/W	0x0	DQS_RF_ODD_UDF_INT_EN DQS Receive FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
22	R/W	0x0	DQS_RF_ODD_OVF_INT_EN DQS Receive FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
21	R/W	0x0	DQS_RF_EVEN_UDF_INT_EN DQS Receive FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
20	R/W	0x0	DQS_RF_EVEN_OVF_INT_EN DQS Receive FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
19:12	/	/	/
11	R/W	0x0	WF_UDF_INT_EN Write FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.

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Offset: 0x0014			Name: SPI_INT_EN
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	WF_OVF_INT_EN Write FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
9	R/W	0x0	RF_UDF_INT_EN Read FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
8	R/W	0x0	RF_OVF_INT_EN Read FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
7:5	/	/	/
4	R/W	0x0	WF_RDY_INT_EN Write FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.
3:1	/	/	/
0	R/W	0x0	RF_RDY_INT_EN Read FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.

8.18.6.6 0x0018 SPI Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W1C	0x0	READ_STATUS_DONE_INT READ_STATUS MODE Done Interrupt. When set, this bit indicates that at least one wanted bit has got expected value.
27	R/W1C	0x0	READ_STATUS_TIME_OUT_INT READ_STATUS MODE TIME OUT Interrupt. When set, this bit indicates that READ_STATUS MODE ends and in the written period, no wanted bit gets expected value.
26	R/W1C	0x0	SPI_TRANS_DONE_INT SPI Transmit Finish Interrupt
25	/	/	/

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Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	DMA_TRANS_DONE_INT DMA Chain Transmit Finish Interrupt Note: When set, this bit indicates that Write FIFO has underflow. Writing "1" to this bit clears it.
23	R/W1C	0x0	DQS_RF_ODD_UDF_INT DQS Receive FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing "1" to this bit clears it.
22	R/W1C	0x0	DQS_RF_ODD_OVF_INT DQS Receive FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing "1" to this bit clears it.
21	R/W1C	0x0	DQS_RF_EVEN_UDF_INT DQS Receive FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing "1" to this bit clears it.
20	R/W1C	0x0	DQS_RF_EVEN_OVF_INT DQS Receive FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing "1" to this bit clears it.
19:12	/	/	/
11	R/W1C	0x0	WF_UDF_INT Write FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing "1" to this bit clears it.
10	R/W1C	0x0	WF_OVF_INT Write FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing "1" to this bit clears it.
9	R/W1C	0x0	RF_UDF_INT Read FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing "1" to this bit clears it.
8	R/W1C	0x0	RF_OVF_INT Read FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing "1" to this bit clears it.
7:5	/	/	/

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Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x1	WF_RDY_INT Write FIFO Ready Request Interrupt Flag 0: WF_WL > WF_EMPTY_TRIG_LEVEL. 1: WF_WL <= WF_EMPTY_TRIG_LEVEL. This bit is set any time if WF_WL <= WF_EMPTY_TRIG_LEVEL. Writing "1" to this bit clears it.
3:1	/	/	/
0	R/W1C	0x0	RF_RDY_INT Read FIFO Ready Request Interrupt Flag 0: RF_WL < RX_EMPTY_TRIG_LEVEL and rest total RX data byte number is larger than RX_EMPTY_TRIG_LEVEL. 1: RF_WL >= RX_EMPTY_TRIG_LEVEL, or rest total RX data byte number is smaller than RX_EMPTY_TRIG_LEVEL meanwhile RF_WL >= 1. This bit is set any time if condition is reached. Writing "1" to this bit clears it.

8.18.6.7 0x001C SPI Chipselect Delay Register (Default Value: 0x0000_0606)

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	DBG_SEL 0: The high 8 bits of debug signal are io*_oen, and the low 8 bits are 0. 1: The high 8 bits are WF_CNT, and the low 8 bits are RF_CNT. 2: The high 8 bits are WB_CNT, and the low 8 bits are RB_CNT. 3: The high 8 bits are DMA state machine, and the low 8 bits are SPI state machine. 4: Debug signal are read DRQ and write DRQ. 2'b0: dqs_rfifo_even water level; 4'b0: dqs_rfifo_odd water level.

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Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x0	CSDA Chip Select De-Assert The interval of two adjacent CS signal enable, namely, the interval of two SPI scheduling. The unit is the i_clk_spi_ref. The minimum interval A (CSDA=0) is 4 clk (used for ending SPI functions) The maximum A (CSDA=FB) is FF clk (used for ending SPI functions) When CSDA is X, the actual interval is X+A.
15:8	R/W	0x6	CSEOT Chip Select End of Transfer The interval between the rising edge of last output clock signal (SPI_CLK_OUT) and the CS signal disable. The unit is the reference clock The minimum interval B (CSEOT=0) is: DTR-TX: 3 clk DTR-RX: 5 clk STR-TX, CPOL=0: 3 clk STR-RX, CPOL=0: 4 clk STR-TX, CPOL=1: 2.5 clk STR-RX, CPOL=1: 3.5 clk When CSEOT is X, the actual interval is X+B. When using delay, the length of CSEOT should be larger than that of delay, or the data will be lost.
7:0	R/W	0x6	CSSOT Chip Select Start of Transfer The interval between the CS signal enable and the rising edge of the first output clock signal (SPI_CLK_OUT). The unit is the reference clock. The minimum interval C (CSSOT=0) is: CPOL=0: 1 clk CPOL=1: 1.5 clk When CSSOT is X, the actual interval is X+C. The minimum interval is recommended to be 6, or the anomaly will occur in some special conditions.。 The minimum interval should be larger than 6 in NEW_START_MODE.

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8.18.6.8 0x0020 SPI Transfer Phase Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_TRANS_PHA_CFG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	CMD_DTR CMD DTR Control 1: CMD DTR 0: CMD not DTR CAUTION: When CMD DTR, DTR_EN must be on and CMD2 is required.
28	R/W	0x0	COMMAND_TRANS_EN Set to 1 if command data need trans to device SPI Controller FSM Phase Enable 1: Enable 0:Disable
27:25	/	/	/
24	R/W	0x0	ADDRESS_TRANS_EN Set to 1 if address need trans to device SPI Controller FSM Phase Enable 1: Enable 0: Disable
23:21	/	/	/
20	R/W	0x0	MODE_BIT_TRANS_EN Set to 1 if Mode bit need trans after address SPI Controller FSM Phase Enable 1: Enable 0:Disable
19:17	/	/	/
16	R/W	0x0	DUMMY_BIT_TRANS_EN Dummy Bit State Enable SPI Controller FSM Phase Enable 1: Enable 0:Disable
15:13	/	/	/
12	R/W	0x0	TX_DATA_EN Set to 1 if Data Need Trans SPI Controller FSM Phase Enable 1: Enable 0: Disable The CPU channels should be configured before writing to this bit out of protection requirements.
11:9	/	/	/

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Offset: 0x0020			Register Name: SPI_TRANS_PHA_CFG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	RX_DATA_EN Set to '1' if Data Need Receive SPI Controller FSM Phase Enable 1: Enable 0: Disable The CPU channels should be configured before reading from this bit out of protection requirements.
7:0	/	/	/

8.18.6.9 0x0024 SPI Trans Configure1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SPI_TRANS_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	ADDR_OPCODE Address Content Trans Through SPI When the length of ADDR is configured as 24bit. To configure MSB first, use the low 24 bits of ADDR_OPCODE. Namely, the sending sequence is from bit23 to bit0 in ADDR_OPCODE [23:0]. To configure LSB first, use the high 24bits of ADDR_OPCODE. Namely, the sending sequence is from bit8 to bit31 in ADDR_OPCODE[31:8].

8.18.6.10 0x0028 SPI Trans Configure2 Register (Default Value: 0x0000_0000)

NOTE

This register should be setup while the controller is idle.

Offset: 0x0028			Register Name: SPI_TRANS_CFG2
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	CMD_OPCODE Command Content Trans Through SPI
23:16	R/W	0x0	MODE_OPCODE Mode Content Trans Through SPI
15:8	R/W	0x0	CMD_OPCODE2 Command2 Content Trans Through SPI

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Offset: 0x0028			Register Name: SPI_TRANS_CFG2
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	CMD_TRANS_TYPE Command Transfer Type 00: Command can be Shifted to the device on DQ0 01: Command can be Shifted to the device on DQ0 and DQ1 10: Command can be Shifted to the device on DQ0-DQ3 11: Command can be Shifted to the device on DQ0-DQ7
5:4	R/W	0x0	ADDR_TRANS_TYPE Address Transfer Type 00: Address can be Shifted to the device on DQ0 01: Address can be Shifted to the device on DQ0 and DQ1 10: Address can be Shifted to the device on DQ0-DQ3 11 : Address can be Shifted to the device on DQ0-DQ7
3:2	R/W	0x0	MODE_BIT_TRANS_TYPE Mode Bit Transfer Type 00: Mode Bit can be Shifted to the device on DQ0 01: Mode Bit can be Shifted to the device on DQ0 and DQ1 10: Mode Bit can be Shifted to the device on DQ0-DQ3 11 : Mode Bit can be Shifted to the device on DQ0-DQ7
1:0	R/W	0x0	DATA_TRANS_TYPE Data Transfer Type 00: Opcode can be Shifted to the device on DQ0 only 01: Opcode can be Shifted to the device on DQ0 and DQ1 only 10: Opcode can be Shifted to the device on DQ0-DQ3 11 : Opcode can be Shifted to the device on DQ0-DQ7

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8.18.6.11 0x002C SPI Trans Number Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SPI_TRANS_NUM
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DATA_TRANS_NUM[16]
30:25	/	/	/
24	R/W	0x0	ADDR_SIZE_MODE Address Size Mode 0: Address Size 24bit. 1: Address Size 32bit.
23:16	R/W	0x0	DUMMY_TRANS_NUM Number of Dummy Cycles A value of 0 = 1 Cycle A value of 1 = 1 Cycle ... A value of N = N Cycle
15:0	R/W	0x0	DATA_TRANS_NUM Num of Data Trans Through SPI(Byte) 0: Non-Write. 1: Write 1 Byte. 2: Write 2 Bytes. 3: Write 3 Bytes. ..... 65535: Write 65535 Bytes. Note: These Bits Indicate Current Operation is Write Data To Flash.

8.18.6.12 0x0040 SPI DMA Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPI_DMA_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	DMA_DESCRIPTOR_LEN DMA Descriptor Length In the initial design, there are eight DMA descriptors and the length of each descriptor is 4 Byte. In this bit, the length of descriptor is set to 32=8*4Byte.
3:1	/	/	/

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Offset: 0x0040			Register Name: SPI_DMA_CTRL
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	CFG_DMA_START Config DMA Start Signal When all the DMA parameters are configured well, pull up a pulse of this signal to enable DMA chain.

8.18.6.13 0x0044 SPI DMA Descriptor Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_DESCRIPTOR_SADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FIRST_DESCRIPTOR_SADDR First Descriptor Start Address The WORD address is needed.

8.18.6.14 0x004C SPI CDC FIFO Trigger Level Register (Default Value: 0x1001_1a10)

Offset: 0x004C			Name: SPI_CDC_FIFO_TRIG_LEVEL
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x10	WF_DMA_TRIG_LEVEL Write FIFO DMA Request Trigger Level (WORD) In the case of DMA conveying, WF_DMA_TRIG_LEVEL should be set to be less than or equal to 16 to avoid the efficiency reduction.
23:22	/	/	/
21:16	R/W	0x01	WF_CPU_TRIG_LEVEL Write FIFO CPU Request Trigger Level (WORD) In the case of DMA conveying, when WF_CNT is less than WF_CPU_TRIG_LEVEL, WF_RDY interrupts will be sent out.
15:14	/	/	/
13:8	R/W	0x1a	RF_FULL_TRIG_LEVEL Read FIFO Full Request Trigger Level (WORD) RF_FULL_TRIG_LEVEL is recommended to be less than or equal to 26 to avoid FIFO anomaly. RF_FULL_TRIG_LEVEL only decides the volume of RX_FIFO, not influencing the RX_RDY_INT.
7:6	/	/	/

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Offset: 0x004C			Name: SPI_CDC_FIFO_TRIG_LEVEL
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x10	RF_RDY_TRIG_LEVEL Read FIFO RDY Request Trigger Level (WORD). In the case of CPU reading data, when the rest data volume is larger than RF_RDY_TRIG_LEVEL, and RF_CN is greater than RF_RDY_TRIG_LEVEL; or the rest data volume is less than RF_RDY_TRIG_LEVEL, and RF_CNT is larger than 1, the RF_RDY_INT will be sent out.

8.18.6.15 0x0050 SPI CDC FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050			Name: SPI_CDC_FIFO_STA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R	0x0	Flash Controller State Debug Reg.
25	R	0x0	WB_WR Write Buffer Could or Not Write.
24:21	R	0x0	WB_CNT Write Buffer Counter(Byte) These Bits Indicate Number of Bytes in Write Buffer.
20	R	0x0	RB_RD_RDY_STATE Read Buffer Could or Not Read
19:16	R	0x0	RB_CNT Read Buffer Counter(Byte) These Bits Indicate Number of Bytes in Read Buffer.
15:14	/	/	/
13:8	R	0x0	WF_CNT Write FIFO Counter (Level) These Bits Indicate Water Level in Write FIFO. 0: 0 level in Write FIFO. 1: 1 level in Write FIFO. ... 32: 32 level in Write FIFO.
7:6	/	/	/

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Offset: 0x0050			Name: SPI_CDC_FIFO_STA
Bit	Read/Write	Default/Hex	Description
5:0	R	0x0	RF_CNT Read FIFO Counter (Level) These Bits Indicate Water Level in Read FIFO. 0: 0 level in Read FIFO. 1: 1 level in Read FIFO. ... 32: 32 level in Read FIFO.

8.18.6.16 0x0054 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bit's frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Write "1" to this bit will start to transfer serial bits' frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0 - Standard Sample Mode 1 - Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	

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Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed Note: It is only valid when Work Mode Select==0x10/0x11.
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable Note: It is only valid when Work Mode Select==0x10/0x11.
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
15:14	/	/	/
13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**

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Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**

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Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

8.18.6.17 0x0058 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select==0x10/0x11.

Offset: 0x0058			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)).

8.18.6.18 0x005C SPI TX Bit Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select==0x10/0x11.

Offset: 0x005C			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. Note: In the process of transmission, the LSB is transmitted first.

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8.18.6.19 0x0060 SPI RX Bit Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select==0x10/0x11.

Offset: 0x0060			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. Note: In the process of transmission, the LSB is transmitted first.

8.18.6.20 0x0064 SPI STATUS Register (Default Value: 0x0000_0885)

Offset: 0x0064			Register Name: SPI_STATUS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	READ_STATUS_RESULT
23:12	/	/	/
11:8	R	0x8	DQS_RF_ODD_WL Rest of space.
7：4	R	0x8	DQS_RF_EVEN_WL Rest of space.
3	R	0x0	WF_FULL Write FIFO Full Interrupt Flag 0: Write FIFO is Not Full. 1: Write FIFO is Full. Note: This bit is set when the Write FIFO is full.
2	R	0x1	WF_EMPTY Write FIFO Empty Request Interrupt Flag 0: Write FIFO always contains one or more bytes. 1: Write FIFO has been empty. Note: This bit is set if the Write FIFO is empty.
1	R	0x0	RF_FULL Read FIFO Full Interrupt Flag 0: Not Full. 1: Read FIFO has been Full. Note: This bit is set when Read FIFO is full.

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Offset: 0x0064			Register Name: SPI_STATUS
Bit	Read/Write	Default/Hex	Description
0	R	0x1	RF_EMPTY Read FIFO Empty Interrupt Flag 0: Not Empty. 1: Read FIFO has been Empty. Note: This bit is set if the Read FIFO is empty.

8.18.6.21 0x0068 SPI STATUS READ Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: SPI_STATUS_READ
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	SPI_READ_STATUS_DETECTED_BIT_POSITION These 8 bits are used to distinguish the wanted bit in a STATUS BYTE. For every bit that CPU cares, put a high level in the corresponding bit position.
15:8	/	/	/
7:0	R/W	0x0	SPI_READ_STATUS_DETECTED_BIT_VALUE These 8 bits are used to distinguish the wanted bit in a STATUS BYTE. For every bit that CPU cares, put the level that CPU wants in the corresponding bit position. And when one bit is detected the same value, READ_STATUS_MODE shall stop and return a DONE interrupt. Then CPU shall check the exact result in 0x0068[31:24].

8.18.6.22 0x006C SPI STATUS READ Register_2(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: SPI_STATUS_READ2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x0	MAXIMUM_STATUS_READ_TIME These 14 bits are used to tell the module that when reading FLASH status, how many times it should read before it stops reading and instead return a TIME_OUT INTERRUPT to avoid dead lock. NOTE：Suggested minimum value is 1.
15:14	/	/	/

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Offset: 0x006C			Register Name: SPI_STATUS_READ2
Bit	Read/Write	Default/Hex	Description
13:0	R/W	0x0	READ_STATUS_INTERVAL The INTERVAL is counted with 32KHz clock. These 14 bits are used to tell that when READING STATUS, after how many rising edge of the 32K clock should the module start a READ STATUS visit to the connected FLASH. NOTE：Suggested minimum value is 1.

8.18.6.23 0x0210 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: SPI_RX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_RX_DATA SPI RX Data.Non read when DMA transfer.

8.18.6.24 0x0220 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: SPI_TX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_TX_DATA SPI TX Data. Non write when DMA transfer.

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8.19 UART

8.19.1 Overview

The universal asynchronous receiver transmitter (UART) provides an asynchronous serial communication with external devices, modem (data carrier equipment, DCE). It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals.

The UART has the following features:

- Up to 10 UART controllers
  - 8 UART controllers in CPUX domain: UART0, UART1, UART2, UART3, UART4, UART5, UART6, and UART7
  - 2 UART controllers in CPUS domain: S_UART0 and S_UART1
- Compatible with industry-standard 16450/16550 UARTs
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes for UART0, S_UART0, and S_UART1
  - Each of them is 128 bytes for UART1, UART2, UART3, UART4, UART5, UART6, and UART7
- The working reference clock is from the APB bus clock
  - Speed up to 10 Mbit/s with 160 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 5 Mbit/s with 80 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 3.75 Mbit/s with 60 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 format, or 9 bits RS-485 format
- 1, 1.5 or 2 stop bit(s)
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports IrDA-compatible slow infrared (SIR) format
- Supports auto-flow by using CTS & RTS (excluding UART0, S_UART0, and S_UART1)

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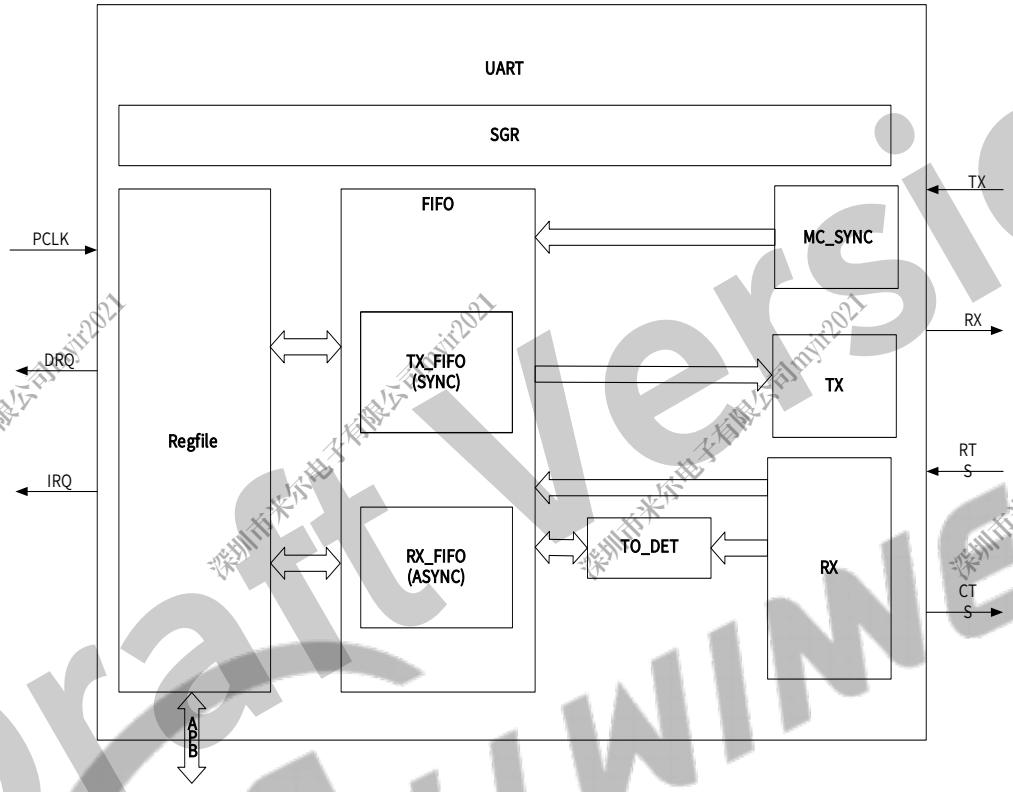
8.19.2 Block Diagram

The following figure shows a block diagram of the UART.

Figure 8-143 UART Block Diagram



8.19.3 Functional Description

8.19.3.1 External Signals

The following table describes the external signals of UART.

Table 8-62 UART External Signals

Signal Name	Description	Type
UART0-TX	UART0 Data Transmitter	O
UART0-RX	UART0 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART1-CTS	UART1 Data Clear to Send	I
UART1-RTS	UART1 Data Request to Send	O
UART2-TX	UART2 Data Transmitter	O
UART2-RX	UART2 Data Receiver	I
UART2-CTS	UART2 Data Clear to Send	I
UART2-RTS	UART2 Data Request to Send	O
UART3-TX	UART3 Data Transmitter	O
UART3-RX	UART3 Data Receiver	I

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Signal Name	Description	Type
UART3-CTS	UART3 Data Clear to Send	I
UART3-RTS	UART3 Data Request to Send	O
UART4-TX	UART4 Data Transmitter	O
UART4-RX	UART4 Data Receiver	I
UART4-CTS	UART4 Data Clear to Send	I
UART4-RTS	UART4 Data Request to Send	O
UART5-TX	UART5 Data Transmitter	O
UART5-RX	UART5 Data Receiver	I
UART5-CTS	UART5 Data Clear to Send	I
UART5-RTS	UART5 Data Request to Send	O
UART6-TX	UART6 Data Transmitter	O
UART6-RX	UART6 Data Receiver	I
UART6-CTS	UART6 Data Clear to Send	I
UART6-RTS	UART6 Data Request to Send	O
UART7-TX	UART7 Data Transmitter	O
UART7-RX	UART7 Data Receiver	I
UART7-CTS	UART7 Data Clear to Send	I
UART7-RTS	UART7 Data Request to Send	O
S-UART0-TX	S-UART0 Data Transmitter	O
S-UART0-RX	S-UART0 Data Receiver	I
S-UART1-TX	S-UART1 Data Transmitter	O
S-UART1-RX	S-UART1 Data Receiver	I

8.19.3.2 Clock Sources

The following table describes the clock sources of UART.

Table 8-63 UART Clock Sources

UART Interfaces	Clock Source	Description	Clock Module
UART0 to UART7	APB1 Bus	UART clock source. Refer to CCU for details on APB1.	CCU
S_UART0, S_UART1	APBS1 Bus	S_UART clock source. Refer to PRCM for details on APB1.	PRCM

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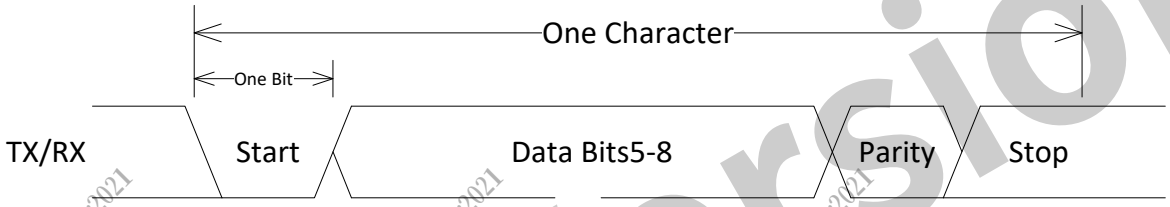
8.19.3.3 Typical Applications and Timing Diagram

UART Serial Data Format

The following figure shows the UART serial data format. The start bit, data bit, parity bit, and stop bit can be configured.

Figure 8-144 UART Serial Data Format



Using UART for RTS/CTS Autoflow Control

Figure 8-145 shows the typical application diagram for RTS/CTS autoflow control. Figure 8-146 shows the data format of the RTS/CTS autoflow control.

Figure 8-145 Application Diagram for RTS/CTS Autoflow Control

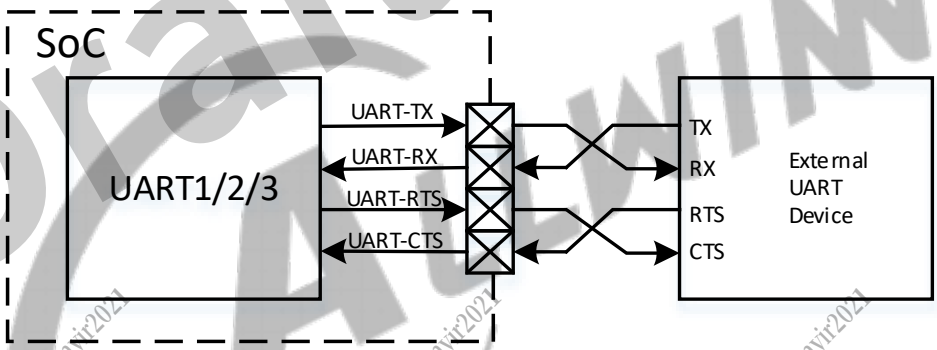
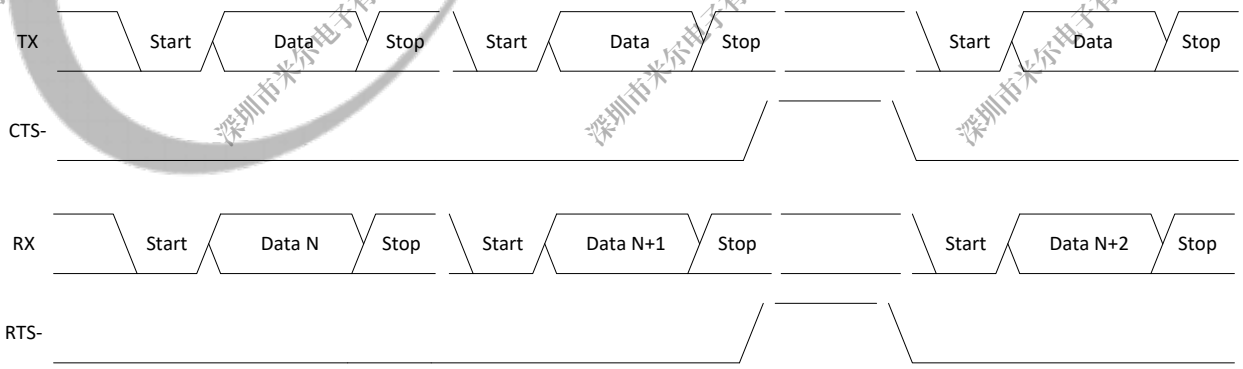


Figure 8-146 RTS/CTS Autoflow Control Data Format



Using UART for Serial IrDA

Figure 8-147 shows the application diagram for the IrDA transceiver. Figure 8-148 shows the data format of the serial IrDA.

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Figure 8-147 Application Diagram for IrDA Transceiver

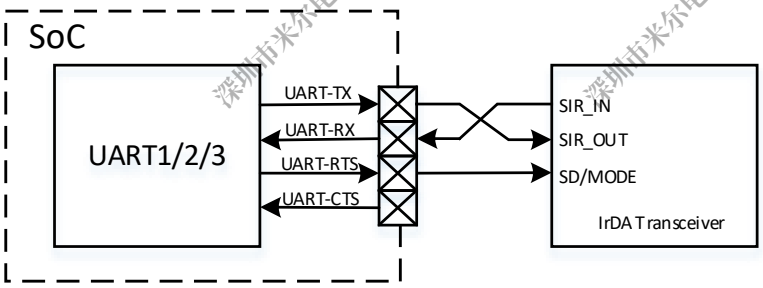
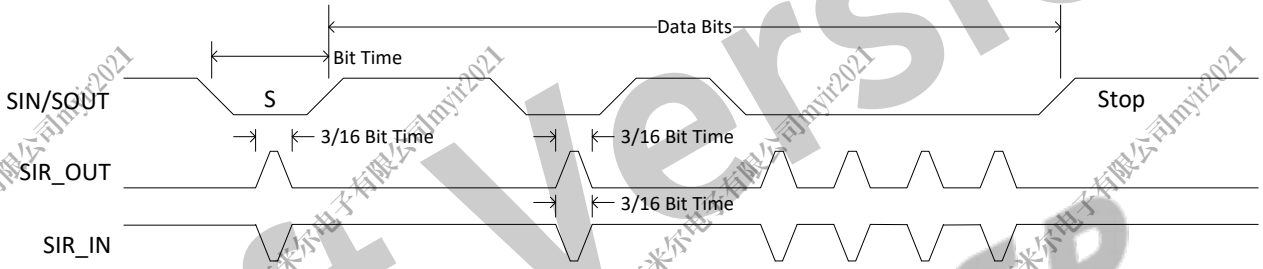


Figure 8-148 Serial IrDA Data Format



Using UART for RS-485

Figure 8-149 shows the application diagram for the RS-485 transceiver. Figure 8-150 shows the data format of the RS-485.

Figure 8-149 Application Diagram for RS-485 Transceiver

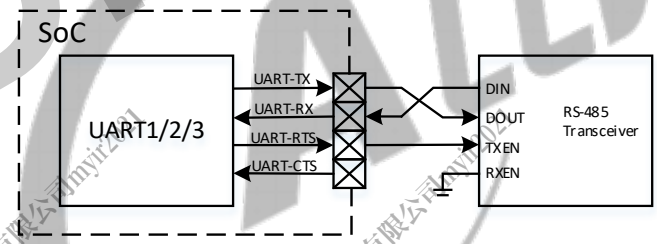
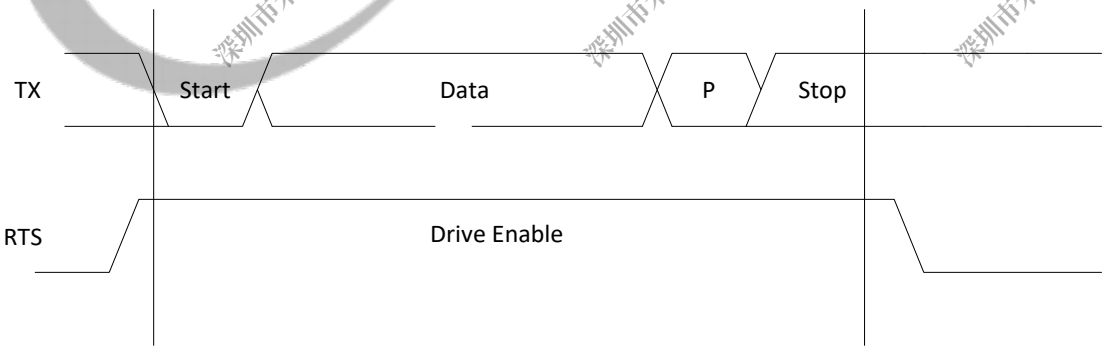


Figure 8-150 RS-485 Data Format



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8.19.3.4 UART Operating Mode

Data Frame Format

The UART_LCR register can set the basic parameter of a data frame: data width (5 to 8 bits), stop bit number (1/1.5/2), parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit, and stop signal. The LSB is transmitted first.

- Start signal (start bit): It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART transmits data, the level needs to hold high.
- Data signal (data bit): The data bit width can be configured as 5-bit, 6-bit, 7-bit, and 8-bit through different applications. If RS-485 mode is enabled, th data bit width is 8-bit.
- Parity bit: It is a 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the UART_LCR register. If RS-485 mode is enabled, the parity bit must be keep enabled.
- Stop Signal (stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit, 1.5-bit, and 2-bit by the UART_LCR register. The high level of the TXD signal indicates the end of a data frame.

Baud and Error Rates

The baud rate is calculated as follows: Baud rate = SCLK/(16 * divisor).

The SCLK is usually APB1 and can be set in section 2.7 Clock Controller Unit (CCU).

The divisor is frequency divider of UART. The frequency divider has 16-bit, the low 8-bit is in the UART_DLL register, the high 8-bit is in the UART_DLH register.

The relationship between the different UART mode and the error rate is as follows.

Table 8-64 UART Mode Baud and Error Rates

Clock Source	Divisor	Baud Rate	Over Sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
60000000	1	3750000	16	0

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Clock Source	Divisor	Baud Rate	Over Sampling	Error(%)
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
80000000	1	5000000	16	0
160000000	1	10000000	16	0

Table 8-65 IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 8-66 RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
60000000	1	3750000	16	0
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
80000000	1	5000000	16	0
160000000	1	10000000	16	0

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DLAB Definition

The DLAB control bit (UART_LCR[7]) is the access control bit of the divisor Latch register.

If DLAB is 0, then the 0x00 offset address is the UART_RBR/UART_THR (RX/TX FIFO) register, and the 0x04 offset address is the UART_IER register.

If DLAB is 1, then the 0x00 offset address is the UART_DLL register, and the 0x04 offset address is the UART_DLH register.

When the UART initials, the divisor needs to be set. That is, writing 1 to DLAB can access the UART_DLL and UART_DLH register, after finished the configuration, writing 0 to DLAB can access the UART_RBR/UART_THR register.

CHCFG_AT_BUSY Definition

The function of the CHCFG_AT_BUSY (UART_HALT [1]) and CHANGE_UPDATE (UART_HALT[2]) are as follows.

CHCFG_AT_BUSY: Enable the bit, the software can also set the UART controller when UART is busy, such as the UART_LCR, UART_DLH, UART_DLL register.

CHANGE_UPDATE: If CHCFG_AT_BUSY is enabled, and CHANGE_UPDATE is written to 1, the configuration of the UART controller can be updated. After completed the update, the bit is cleared to 0 automatically.

Setting divisor performs the following steps:

Write 1 to CHCFG_AT_BUSY to enable "configure at busy".

Write 1 to DLAB (UART_LCR[7]) and set the UART_DLH and UART_DLL registers.

Write 1 to CHANGE_UPDATE to update the configuration. The bit is cleared to 0 automatically after completing the update.

UART Busy Flag

The UART_USR [0] is a busy flag of the UART controller.

When the TX transmits data, or the RX receives data, or the TX FIFO is not empty, or the RX FIFO is not empty, then the busy flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

8.19.4 Programming Guidelines

The following takes the UART module in the CPUX domain as an example.

8.19.4.1 Initialization

Step 1 System Initialization

- Configure APB1_CLK_REG in the CCU module to set the APB1 bus clock (The clock is 24MHz by default).

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- Set UART_BGR_REG[UARTx_GATING] to 1 to enable the module clock, and set UART_BGR_REG[UARTx_RST] to 1 to de-assert the module.

Step 2 UART Controller Initialization

- IO configuration: Configure GPIO multiplex as UART function, and set UART pins to internal pull-up mode (For detail, see the description in section 8.6 GPIO).
- Baud-rate configuration:
  - Set UART baud-rate (refer to section 8.19.3.4);
  - Write UART_FCR[FIFOE] to 1 to enable TX/RX FIFO;
  - Write UART_HALT[HALT_TX] to 1 to disable TX transfer;
  - Set UART_LCR[DLAB] to 1, remain default configuration for other bits; set 0x00 offset address to the UART_DLL register, set 0x04 offset address to the UART_DLH register;
  - Write the high 8-bit of divisor to the UART_DLH register, and write the low 8-bit of divisor to the UART_DLL register;
  - Set UART_LCR[DLAB] to 0, remain default configuration for other bits; set 0x00 offset address to the UART_RBR/UART_THR register, set 0x04 offset address to the UART_IER register;
  - Set UART_HALT[HALT_TX] to 0 to enable TX transfer.

Step 3 Controller Parameter Configuration

- Set data width, stop bits, and even/odd parity type by writing the UART_LCR register.
- Reset, enable FIFO and set FIFO trigger condition by writing the UART_FCR register.
- Set the flow control parameter by writing the UART_MCR register.

Step 4 Interrupt Configuration

- Configure UART interrupt vector number to request UART interrupt (Refer to section 2.9 Generic Interrupt Controller (GIC) for interrupt vector number).
- In DMA mode, write UART_IER to 0 to disable interrupt; write UART_HSK[Handshake configuration] to 0xE5 to set DMA handshake mode; write UART_FCR[DMAM] to 1 to set DMA transmission/reception mode; set DMA parameter and request DMA interrupt according to DMA configuration process.
- In Interrupt mode, configure UART_IER to enable the corresponding interrupt according to requirements: such as transmit (TX) interrupt, receive (RX) interrupt, receive line status interrupt, RS48 interrupt, etc. (Here TX/RX interrupt is usually used).

8.19.4.2 Transferring/Receiving Data in DMA Mode

Step 1 Initialize UART model. Refer to section 8.19.4.1 Initialization for initialization steps.

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Step 2 Configure UART_TFL and UART_RFL to set DRQ trigger level for DMA.

Step 3 Configure UART_HALT to set PTE and DMA_PTE_RX.

Step 4 DMA data channel, including the transfer source address, the transfer destination address, the number of data to be transferred, and the transfer type, and so on. For details, see section 2.8 DMA Controller (DMAC).

Step 5 Enable the DMA transfer or receive function of the UART by setting the register of the DMA module.

Step 6 Determine whether UART data is transferred or received completely based on the DMA status. If all data is transferred or received completely, disable the DMA transfer or receive function of the UART.

8.19.4.3 Transferring/Receiving Data in Interrupt Mode

- Data transfer

Step 1 Initialize UART model. Refer to section 8.19.4.1 for initialization steps.

Step 2 Configure UART_TFL and UART_RFL to set DRQ trigger level for DMA.

Step 3 Configure UART_HALT to set PTE and DMA_PTE_RX.

Step 4 Set UART_IER[ETBEI] to 1 to enable the UART transmission interrupt.

Step 5 Write the data to be transmitted to UART_THR.

Step 6 When the data of TX_FIFO meets trigger condition (such as FIFO/2, FIFO/4), the UART transfer interrupt is generated.

Step 7 Check UART_USR[TFE] and determine whether TX_FIFO is empty. If UART_USR[TFE] is 1, it indicates that the data in TX_FIFO is transmitted completely.

Step 8 Clear UART_IER[ETBEI] to 0 to disable transfer interrupt.

- Data receive

Step 1 Initialize UART model. Refer to section 8.19.4.1 for initialization steps.

Step 2 Configure UART_TFL and UART_RFL to set DRQ trigger level for DMA.

Step 3 Configure UART_HALT to set PTE and DMA_PTE_RX.

Step 4 Set UART_IER[ERBFI] to 1 to enable the UART reception interrupt.

Step 5 When the received data from RX_FIFO meets trigger condition (such as FIFO/2, FIFO/4), the UART receive interrupt is generated.

Step 6 Read data from UART_RBR.

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Step 7 Check RX_FIFO status by reading UART_USR[RFNE] and determine whether to read data. If the bit is 1, continue to read data from UART_RBR until UART_USR[RFNE] is cleared to 0, which indicates data is received completely.

8.19.4.4 Transferring/Receiving Data in RS485 Mode

Step 1 Initialize UART model. Refer to section 8.19.4.1 for initialization steps.

Step 2 Configure UART_485_CTL [1:0] to select UART RS485 receive data format.

Step 3 If AAD receive data mode is choosed, configure UART_RS485_ADDR_MATCH register to set receive address in AAD mode.

Step 4 If DMA mode is selected, perform Step2 to Step6 in section 8.19.4.2. Otherwise, perform Step2 to Step7 in section 8.19.4.3.

8.19.5 Register List

Module Name	Base Address
UART0	0x02500000
UART1	0x02500400
UART2	0x02500800
UART3	0x02500C00
UART4	0x02501000
UART5	0x02501400
UART6	0x02501800
UART7	0x02501C00
S_UART0	0x07080000
S_UART1	0x07080400

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register

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Register Name	Offset	Description
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_DMA_REQ_EN	0x008C	UART DMA Request Enable Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control Configure and Status Register
UART_RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHECK	0x00C8	BUS IDLE CHECK Register
TX_DELAY	0x00CC	TX_DELAY Register
UART_FCC	0x00F0	UART FIFO Clock Control Register

8.19.6 Register Description

8.19.6.1 0x0000 UART Receiver Buffer Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

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8.19.6.2 0x0000 UART Transmit Holding Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

8.19.6.3 0x0000 UART Divisor Latch Low Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

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8.19.6.4 0x0004 UART Divisor Latch High Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.19.6.5 0x0004 UART Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable

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Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
3	R/W	0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

8.19.6.6 0x0008 UART Interrupt Identity Register (Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

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Offset: 0x0008			Register Name: UART_IIR
Bit	Read/Write	Default/Hex	Description
7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt（pending by UART_485_CTL[6:5]） 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)

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Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

8.19.6.7 0x0008 UART FIFO Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

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Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full

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Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
3	W	0	DMAM DMA Mode 0: Mode 0 In this mode, when PTE is high and TX FIFO is enable, the TX DMA request will be set when TFL is less than or equal to FIFO Trigger Level(otherwise it will be cleared). When PTE is high and TX FIFO is disabled, the TX DMA request will be set only if THR is empty. If PTE is low, the TX DMA request will be set only if the TX FIFO(TX FIFO Enabled) or THR(TX FIFO Disabled) is empty. When dma_pte_rx is high and RX FIFO is enabled, the rx drq will be set only if RFL is equal to or more than FIFO Trigger Level, otherwise it will be cleared. 1: Mode 1 In this mode, TX FIFO should be enable. If the PTE is high, the TX DMA request will be set when TFL is less than or equal to FIFO Trigger Level; If PTE is low, the TX DMA request will be set when TX FIFO is empty. Once the request is set, it is cleared only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level or there is a character timeout , the rx drq will be set; Once the rx drq is set, it is cleared only when RX FIFO(RX FIFO enabled) or RBR(RX FIFO disabled) is empty.
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.

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Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

8.19.6.8 0x000C UART Line Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.

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Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0	EPS Even Parity Select It is writable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 0, indicates that this is a data byte. 10:9th bit = 1, indicates that this is an address byte. Note: When use this function, PEN(LCR[3]) must set to 1.
3	R/W	0	PEN Parity Enable It is writable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits It is writable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit

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Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0	DLS Data Length Select It is writable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

8.19.6.9 0x0010 UART Modem Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0	UART_FUNCTION Select IrDA or RS485 0:UART Mode 1:IrDA SIR Mode 2:RS485 Mode 3:Reverse
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled

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Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
4	R/W	0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	/	/	/
2	/	/	/

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Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
1	R/W	0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n。 0：dtr_n de-asserted (logic 1) 1：dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

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8.19.6.10 0x0014 UART Line Status Register (Default Value: 0x0000_0060)

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.

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Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.

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Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
2	RC	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	RC	0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

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8.19.6.11 0x0018 UART Modem Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).

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Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	RC	0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.

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Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
1	RC	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RC	0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

8.19.6.12 0x001C UART Scratch Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: UART_SCH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

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8.19.6.13 0x007C UART Status Register (Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

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8.19.6.14 0x0080 UART Transmit FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

8.19.6.15 0x0084 UART Receive FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0	RFL Receive FIFO Level This indicates the number of data entries in the receive FIFO.

8.19.6.16 0x0088 UART DMA Handshake Configuration Register (Default Value: 0x0000_00A5)

Offset: 0x0088			Register Name: UART_HSK
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xA5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

8.19.6.17 0x008C UART DMA Request Enable Register (Default Value: 0x0000_0003)

Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0	DMA Timeout Enable 0: disable 1: enable
1	R/W	1	DMA TX REQ Enable 0: disable 1: enable

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Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	Read/Write	Default/Hex	Description
0	R/W	1	DMA RX REQ Enable 0: disable 1: enable

8.19.6.18 0x00A4 UART Halt TX Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, when DMA_PTE_RX = 1 and FIFO on, if RFL is more than or equal to trig, send DRQ, else DRQ is cleared. In other cases, once the receive data is valid, send DRQ.
6	R/W	0	PTE The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set 1, when TFL is less than or equal to trig, send the DMA request. If PTE is set 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set 1 and FIFO on, when TFL is less than or equal to trig, send DMA request. If PTE is set 1 and FIFO off, when THR is empty, send DMA request. If PTE is set 0, when FIFO(FIFO Enable) or THR(FIFO Enable) is empty, send DMA request. Otherwise, DMA request is cleared.
5	R/W	0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/

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Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
2	R/WAC	0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled Note: If FIFOs are not enabled, the setting has no effect on operation.

8.19.6.19 0x00B0 UART DBG DLL Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: UART_DBG_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0	DEBUG DLL

8.19.6.20 0x00B4 UART DBG DLH Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: UART_DBG_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0	DEBUG DLH

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8.19.6.21 0x00C0 UART RS485 Control Configure and Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: UART_485_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	Add_bit_polarity Address bit polarity 0: The address bit is 1 representative the data is address 1: The address bit is 0 representative the data is address
6	R/W1C	0	AAD_ADDR_Detecte AAD Mode Receive address detecte 0:Receive address is different with set 1:Receive address is same with set
5	R/W1C	0	Address_detected RS485 Address detect 0: No address detected 1: address detected
4:2	/	/	/
1:0	R/W	0	RCM RS485 Receive mode This is used to chose the RS485 Receive mode 00: RS_9BITM 01: AAD

8.19.6.22 0x00C4 UART RS485 Address Match Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: UART_RS485_ADDR_MATCH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	AAD_Receive _ADDR AAD Mode Receive address

8.19.6.23 0x00C8 UART RS485 Bus idle Check Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: BUS_IDLE_CHECK
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	BUS_IDLE_CHK_EN 1: Enable bus idle check function 0: Disable bus idle check function

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Offset: 0x00C8			Register Name: BUS_IDLE_CHECK
Bit	Read/Write	Default/Hex	Description
6	R	0	BUS_STATUS The flag of bus status 1:busy 0:idle
5:0	R	0	ADJ_TIME How long the bus is idle.The unit is 8*16*Tclk

8.19.6.24 0x00CC UART TX Delay(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: TX_DELAY
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLY The delay time between the last stop bit and the next start bit. The uint is 16*Tclk. It is use to control the space between tow bytes in TX.

8.19.6.25 0x00F0 UART FIFO Clock Control Register (Default Value: 0x0000_0003)

Offset: 0x00F0			Register Name: UART_FCC
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	FIFO Depth Indicates the depth of TX/RX FIFO
7:3	/	/	/
2	R/W	0	RXFIFO Clock Mode 0: Sync mode, R/W clocks use apb clock 1:Sync mode, write clock uses apb clock, read clock uses ahb clock
1	R/W	1	TX FIFO Clock Enable 0: clock disable 1: clock enable
0	R/W	1	RX FIFO Clock Enable 0: clock disable 1: clock enable

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9 Security System

9.1 Crypto Engine (CE)

9.1.1 Overview

The Crypto Engine (CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RBG algorithms. There are two software interfaces for secure and non-secure world each. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world and 4 different types of algorithms simultaneously. This module also has an internal DMA controller to transfer data between CE and memory. It supports parallel running for symmetric, HASH, asymmetric algorithms.

The CE has the following features:

- Symmetrical algorithm:
  - AES symmetrical algorithm
    - Key size: 28/192/256 bits
    - CFB mode includes: CFB1, CFB8, CFB64, and CFB128
    - CTR mode includes: CTR16, CTR32, CTR64, and CTR128
    - Supports ECB, CBC, CTS, OFB, CBC-MAC, and GCM modes
  - DES symmetrical algorithm
    - CTR mode, includes: CTR16, CTR32, and CTR64
    - Supports ECB, CBC, and CBC-MAC mode
  - Supports 3DES
  - SM4 symmetrical algorithm supports ECB and CBC mode
- Hash algorithms
  - Support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
  - Support HMAC-SHA1, HMAC-SHA256
  - Support multi-package[1] mode for these ones
  - Support hardware padding

[1] If not last package, input should aligned with computation block, namely 512bits or 1024bit

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- Random bit generator algorithms
  - Support PRNG, 175 bits seed width, and output with multiple of 5 words
  - Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words
  - Support Instantiate/Reseed/Generate/Uninstantiate 4 process
  - Support prediction resistance requests
  - Support 8 separate suits of Internal State
  - Maxim 2^32 BYTE length of Entropy input, Nonce, Personalization, Additional input. And length is multiple of word
- Public key algorithms
  - Supports RSA public key algorithms: 512/1024/2048/3072/4096-bit width
  - Supports ECC public key algorithms: 160/224/256/384/521-bit width
  - Supports SM2 algorithms
- Security Strategy and System Feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time.
  - Support task chain mode for each request. Task or task chain are executed at request order.
  - multi- scatter group(sg) are supported for both input and output data
  - Support secure and non-secure interfaces respectively, each world issues task request through its own interface, don't know each other's existence.
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other.
  - Supports byte-aligned address for all configurations

NOTE

The total length of data_length in the CBC and ECB modes of the symmetric channels needs to be aligned according to the algotithm granularity. For example, in the AES-128 algorithm, the total length of data_length needs to be an integer multiple of 128 bits

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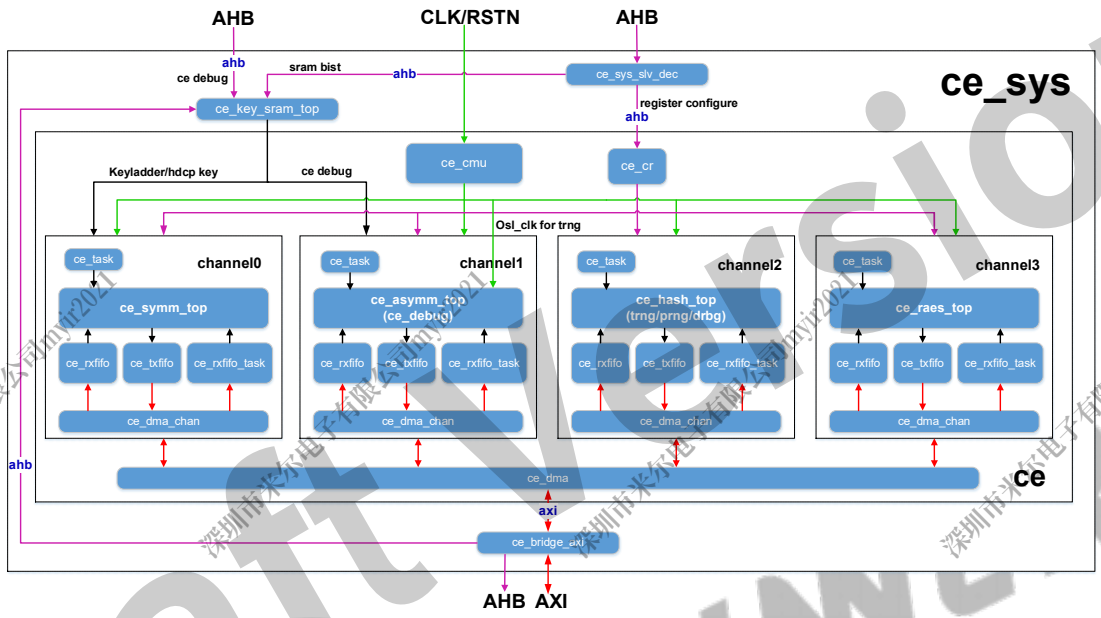
9.1.2 Block Diagram

The following figure shows a block diagram of CE.

Figure 9-1 CE Block Diagram

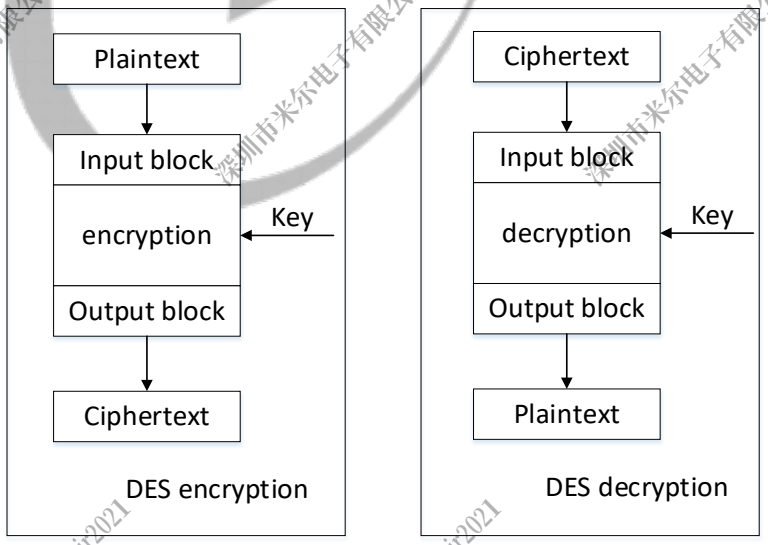


9.1.3 Functional Description

9.1.3.1 DES Algorithm

The following figure shows the DES encryption and decryption operation.

Figure 9-2 DES Encryption and Decryption



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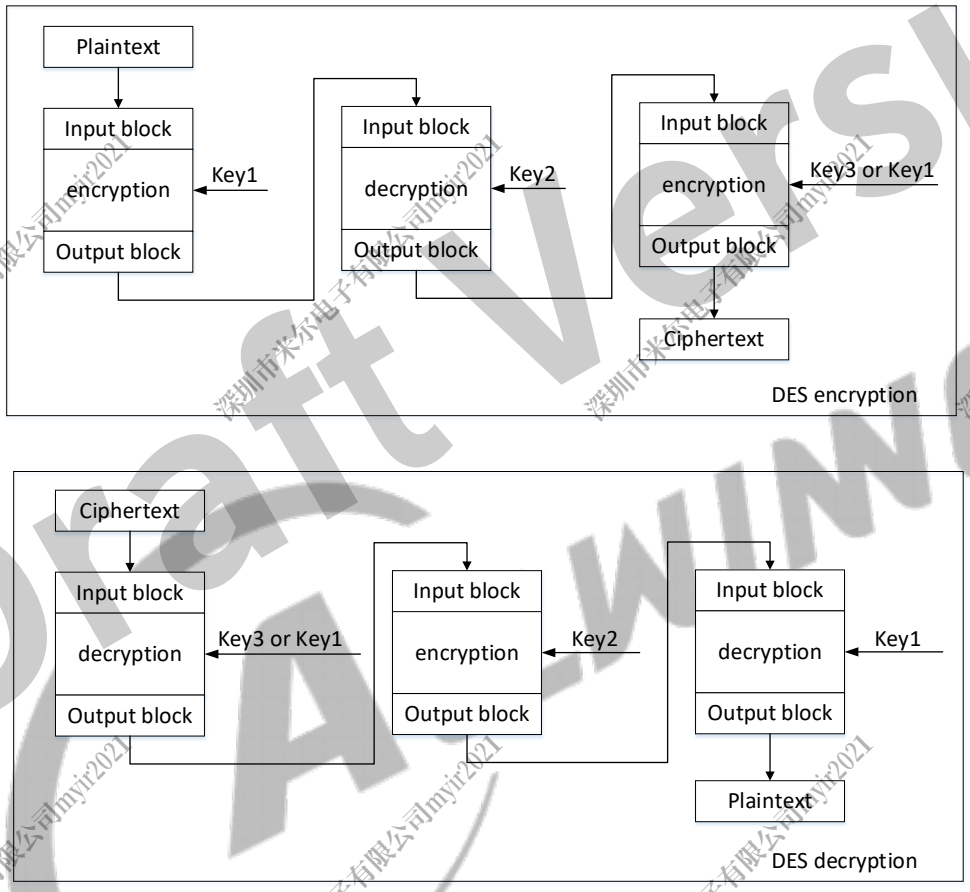
9.1.3.2 3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation. The following figure shows the 3DES encryption and decryption operation of a 3-key operation and a 2-key operation.

Figure 9-3 3DES Encryption and Decryption of a 3-key Operation and a 2-key Operation



9.1.3.3 ECB Mode

The ECB mode is a confidentiality mode that features, for a given key, the assignment of a fixed ciphertext block to each plaintext block, analogous to the assignment of code words in a codebook.

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent, so the plaintext encryption and ciphertext decryption can be performed concurrently.

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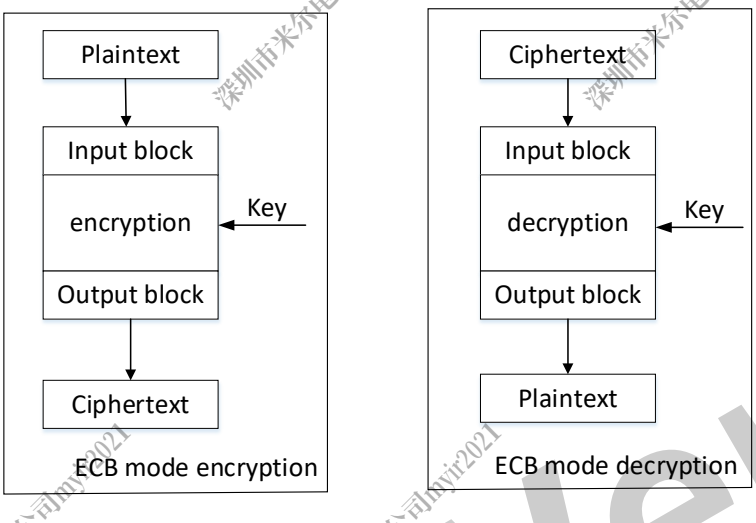
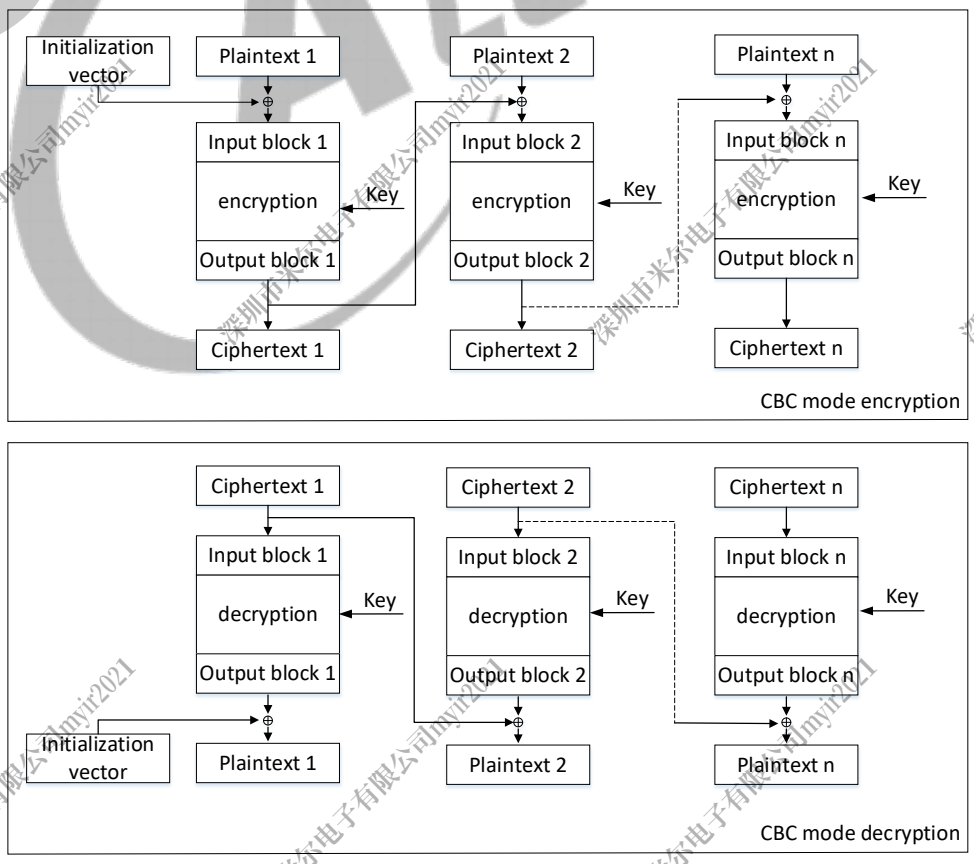
Figure 9-4 ECB Mode Encryption and Decryption



9.1.3.4 CBC Mode

The CBC mode is a confidentiality mode whose encryption process features the combining of the plaintext blocks with the previous ciphertext blocks. The CBC mode requires an initialization vector (IV) to combine with the first plaintext block. The encryption process of each plaintext block is related to the block processing result of the previous ciphertext blocks, so encryption operations cannot be concurrently performed in CBC mode. The decryption operation is independent of output plain text of the previous block, so decryption operations can be performed concurrently.

Figure 9-5 CBC Mode Encryption and Decryption



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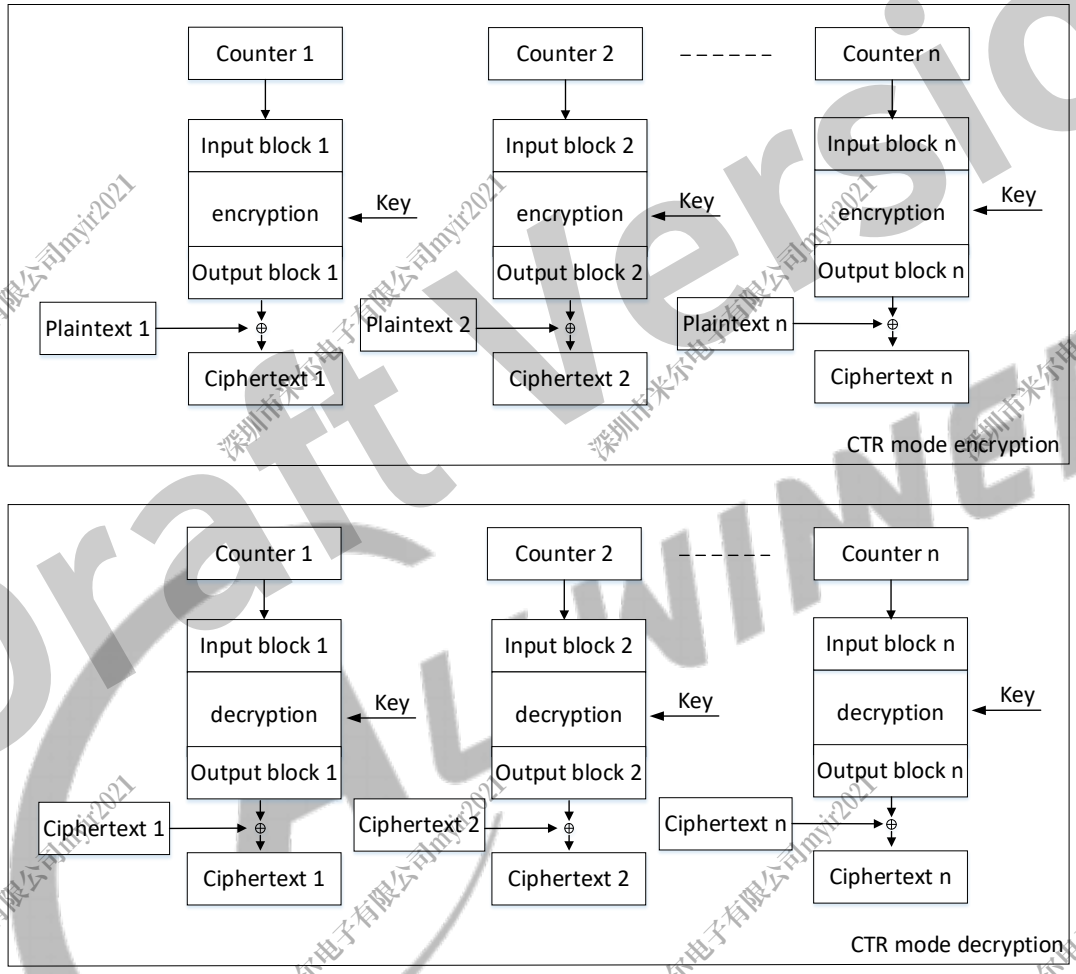
9.1.3.5 CTR Mode

The CTR mode is a confidentiality mode that features the application of the forward cipher to a set of input blocks, called counters, to produce a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. All of the counters must be distinct.

Figure 9-6 CTR Mode Encryption and Decryption



9.1.3.6 CFB Mode

The CFB mode is a confidentiality mode that features the feedback of successive ciphertext segments into the input blocks of the forward cipher to generate output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The CFB mode requires an IV as the initial input block, and the forward cipher operation is applied to the IV to produce the first output block. The first ciphertext segment is produced by exclusive-ORing the first plaintext segment with the s most significant bits of the first output block. The value of s is 1 bit, 8 bits, 64 bits, or 128 bits.

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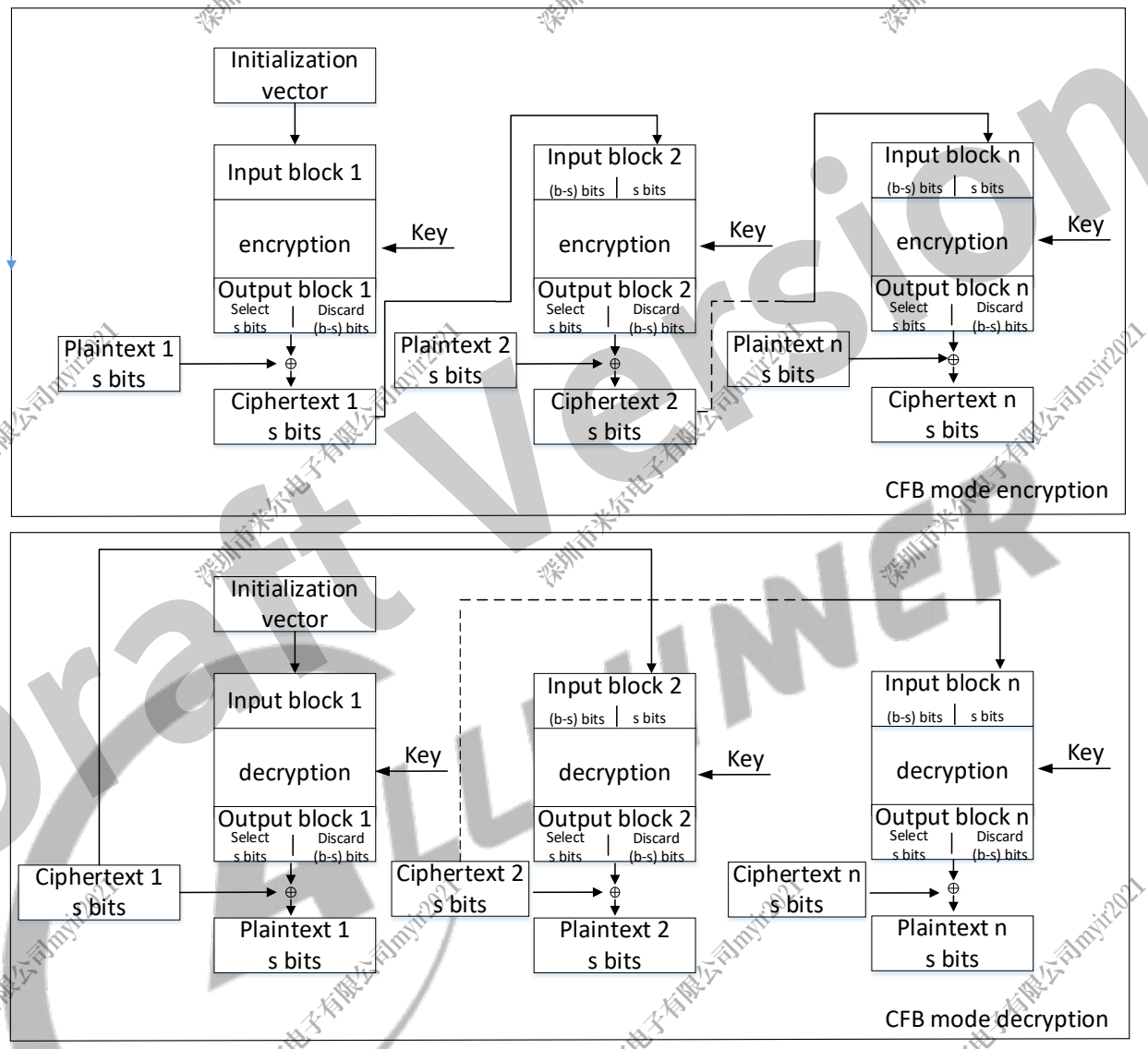
The following figure shows the s-bit CFB mode of the AES algorithms.

Figure 9-7 CFB Mode Encryption and Decryption



9.1.3.7 OFB Mode

The OFB mode is a confidentiality mode that features the iteration of the forward cipher on an IV to generate a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. If a same key is used, different IVs must be used to ensure operation security.

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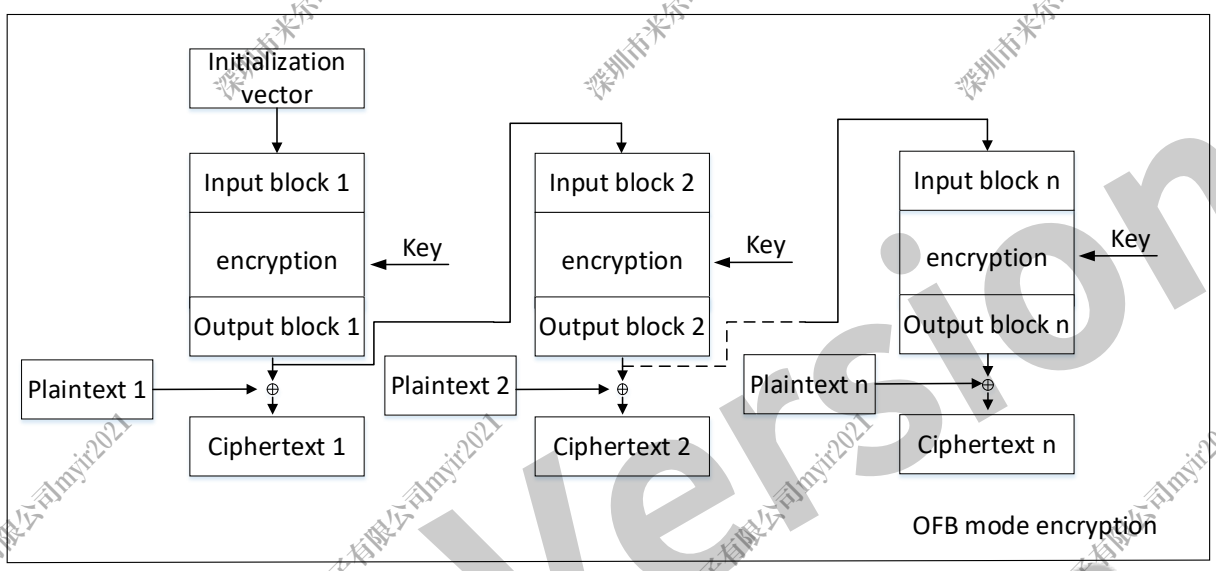
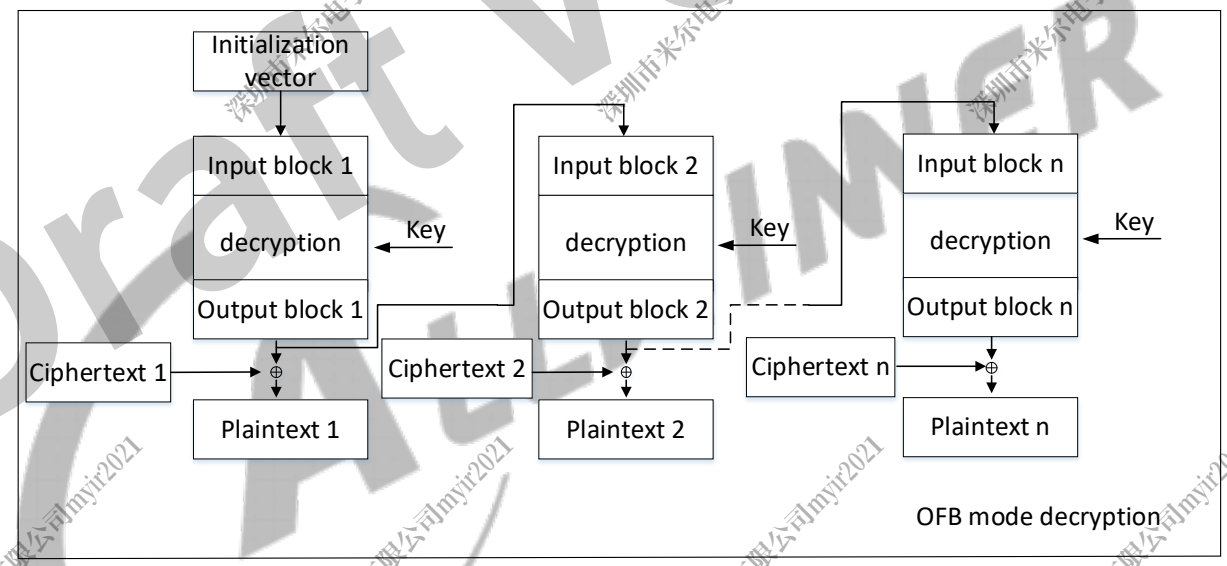
Figure 9-8 OFB Mode Encryption and Decryption





9.1.3.8 CTS Mode

The CTS mode is a confidentiality mode that accepts any plaintext input whose bit length is greater than or equal to the block size but not necessarily a multiple of the block size. Below are the diagrams for CTS encryption and decryption.

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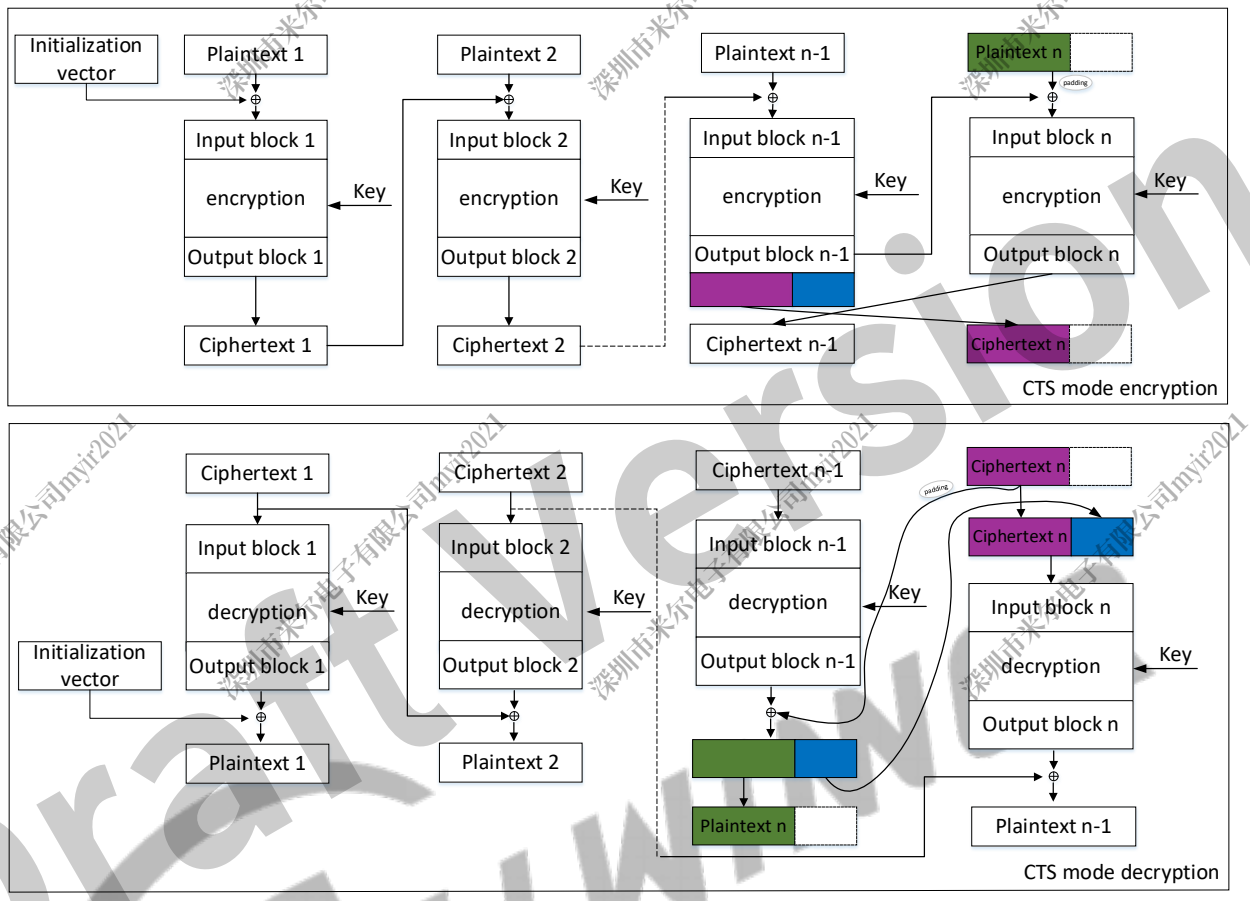
Figure 9-9 CTS Mode Encryption and Decryption



9.1.3.9 HASH Algorithm

The hash algorithms support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC-SHA1, and HMAC-SHA256. All algorithms are iterative, one-way hash functions that can process a message to produce a condensed representation called a message digest. When a message is received, the message digest can be used to verify whether the data has changed, that is, to verify its integrity.

The hash algorithm of the CE supports block-aligned total length of the input data (padded by software), that is, a multiple of 64 bytes. The message length after padding by software is used as the configured data length for the hash algorithm.

9.1.3.10 RSA Algorithm

The RSA is a public key encryption/decryption algorithm implemented through the modular exponentiation operation.

The ciphertext is obtained as follows: C = ME mod N. The plaintext is obtained as follows: M = CD mod N.

M indicates the plaintext, C indicates the ciphertext, (N, E) indicates the public key, and (N, D) indicates the private key.

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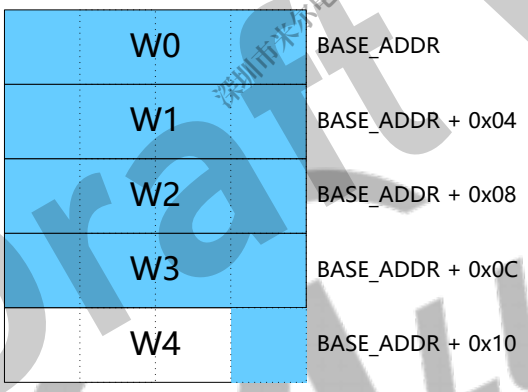
9.1.3.11 Storing Message

In the application, a message may not be stored contiguously in the memory, but divided into multiple segments. Or a piece of continuously stored messages can be artificially split into multiple pieces as needs. Then each segment corresponds to a set of the source address and source length in the descriptor. Multiple segments correspond to groups 0-7 source address/source length in sequence.

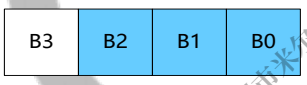
Each task supports up to 8 message segments, and the data volume of each message segment supports up to 4 GWord (AES-CTS is 1 GByte). The total amount of all segments in a task (that is a package) supports up to 4 GWord (AES-CTS is 1 GByte). If a message is divided into multiple packages, all others are required to be whole words; when the last package of AES-CTS is less than one word, 0 needs to be padded, and those less than one word are counted as one word. The following figure shows the address order structure.

Figure 9-10 Word Address of Message



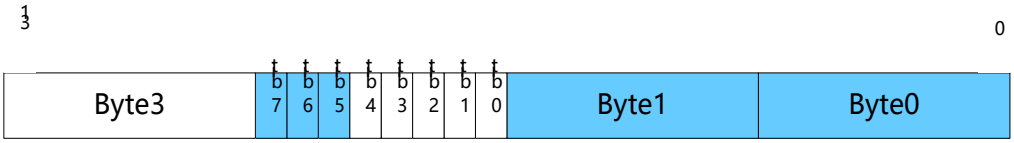
Byte order: low byte first, high byte last. When the data is less than one word, the low byte is filled first. The following figure shows the byte order structure (blue means it is filled by the message).

Figure 9-11 Byte Order



Bit order: high bit first, low bit last. When the data is less than one Byte, the high bit is filled first. The following figure shows the bit order structure.

Figure 9-12 Bit Order



9.1.3.12 Storing Key

The length of KEY must be an integer multiple of word.

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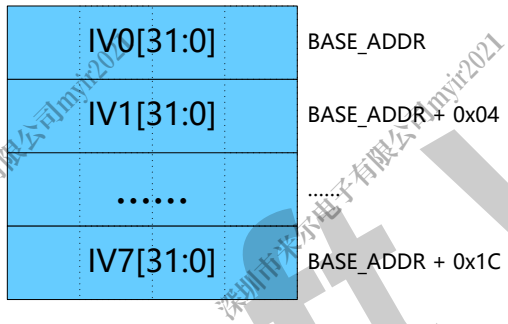
9.1.3.13 Storing IV

For different algorithms, the length of IV is different. But they are integer multiples of word. To keep the byte order of IV and HASH digest output consistent, the byte order of IV is different from that of the message. For the multi-packet operation, the first address of the digest output result of the previous HASH can be directly configured to the first address of the next IV, and the software does not need to do any processing on the digest.

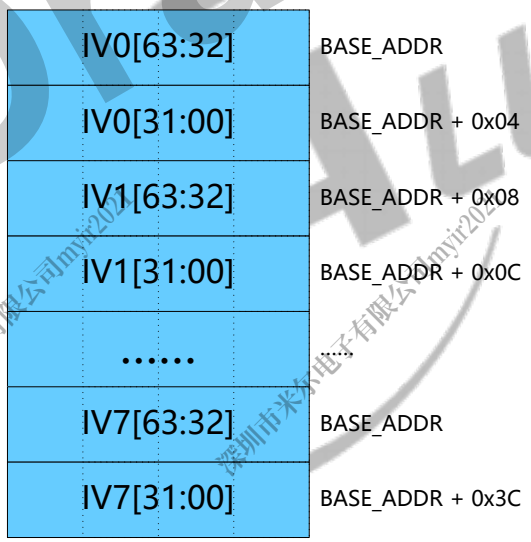
The following figure shows the storage method of 32-bit IV value.

Figure 9-13 The Storage Method of 32-bit IV



The following figure shows the storage method of 64-bit IV value.

Figure 9-14 The Storage Method of 64-bit IV



9.1.3.14 Task Descriptor of Hash Algorithms and RBG Algorithms

The task descriptor is data written by software to a contiguous space in memory. The data describes the various properties of a task, such as algorithm type, mode, subcommand, key address, data source address, the data size read from data source, abstract destination address, the written destination data size, and the information of other tasks. First, we configure the task descriptor by software; then we operates the registers of CE to start this task. After the task starts, CE will read task descriptor based on the address of the task descriptor configured in register, and perform the task one time based on the described properties.

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In applications, the “NEXT TASK ADDR” field can be configured as the starting address of the next task descriptor, to concatenate multi task descriptors into a task chain. After starting the first task, CE will perform every task in order until the “NEXT TASK ADDR” field is invalid (that is 0).

The HASH/RBG algorithms and Symmetrical/Asymmetrical algorithms use the different descriptor structure, separately.

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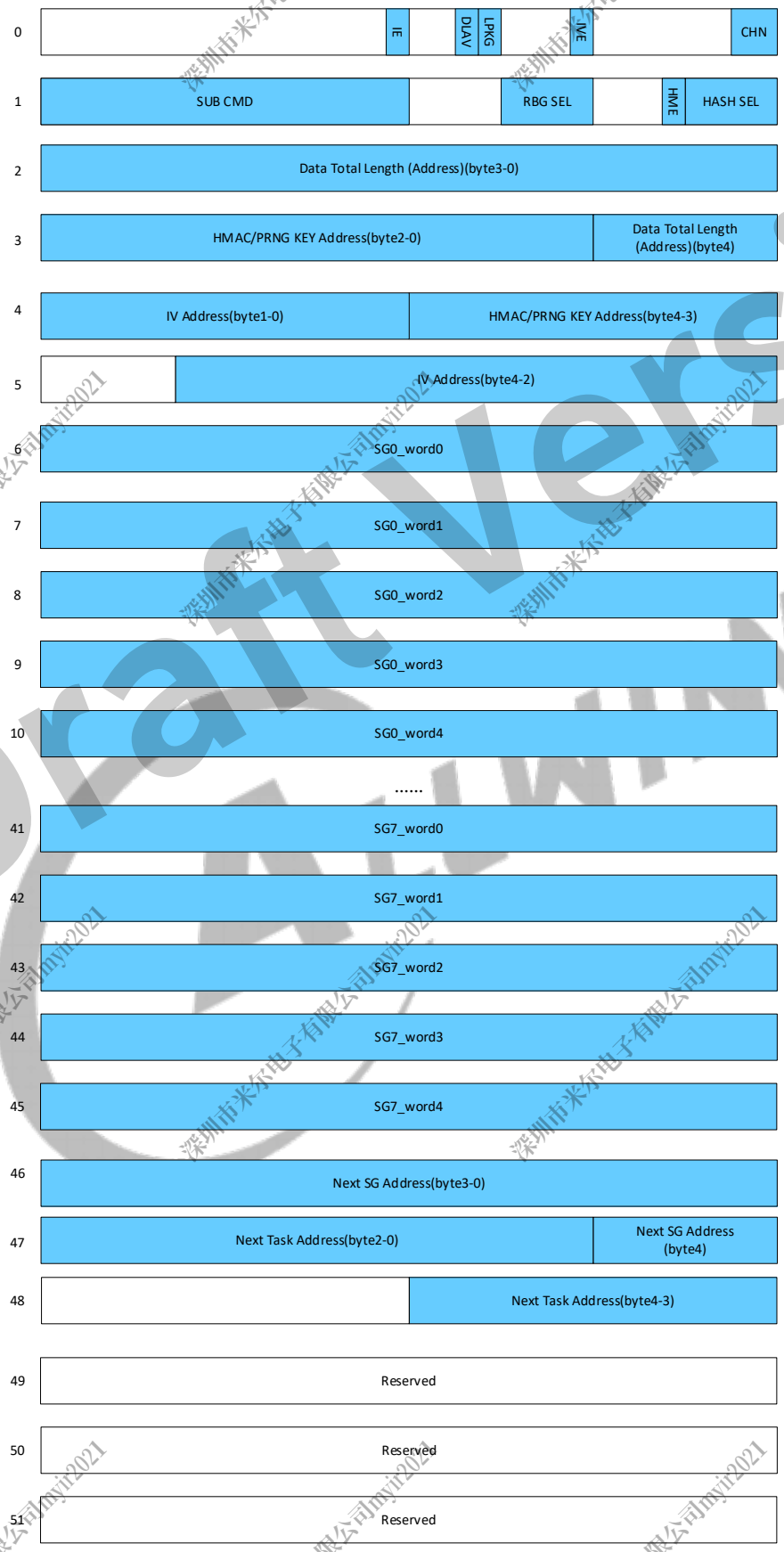
Figure 9-15 Task Chaining of Hash Algorithms and Random Bit Generator Algorithms



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The detail structures are as follows.

No.	Descriptor	Name	Width	Description
0	CTRL	CHN	[1:0]	Channel ID
		IVE	[8]	IV mode enable, active high
		LPKG	[12]	1: Multi-SG enable. This bit needs to be fixed as 1.
		DLAV	[13]	Data length valid For last package, the bit needs be configured. For non last package, the bit needs not be configured. (Please configure it as 0 in PRNG/TRNG) 1: DLA means the WORD address where data total length (by bits) is saved. 0: DLA means the value of message total length (by bits).
		IE	[16]	Interrupt enable for current task, active high
1	CMD	HASH SEL	[3:0]	Hash algorithms select 0: MD5 1: SHA1 2: SHA224 3: SHA256 4: SHA384 5: SHA512 6: SM3 Other: Reserved
		HME	[4]	HMAC mode enable, active high
		RGB SEL	[11:8]	RGB algorithms select 0: No RGB use 1: PRNG 2: TRNG Other: Reserved
		SUB CMD	[31:16]	Sub-command in a specific algorithms When using PRNG, sub_cmd[15] means PRNG seed reload; sub_cmd[14:0] means PRNG linearly shifted seed

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No.	Descriptor	Name	Width	Description
2	DLA	DLA	[31:0]	Data length OR its address. For last package, the field needs be configured. For non last package, the field needs not be configured. (Not used in PRNG/TRNG) When DLAV=1, here is the WORD address where data total length (by bits) is saved. When DLAV=0, here is the value of message total length (by bits)
3	DLA	DLA	[7:0]	When DLAV=1, here is the byte address bit[39:32] where data total length (by bits) is saved.
	KA	KA	[31:8]	KEY Address: The byte address bit[23:0].where HMAC KEY or PRNG KEY is saved.
4	KA	KA	[15:0]	KEY Address: The byte address bit[39:24].where HMAC KEY or PRNG KEY is saved.
	IVA	IVA	[31:16]	IV Address: The byte address bit[15:0] where IV is saved.
5	IVA	IVA	[23:0]	IV Address: The byte address bit[39:16] where IV is saved.
	Reversed	Reversed	[31:24]	/
6+5*x	SGx_W0	SGx_WORD 0	[31:0]	Source Data Address x: The byte address bit[31:0] where Source Datax is saved.
7+5*x	SGx_W1	SGx_WORD 1	[7:0]	Source Data Address x: The byte address bit[39:32] where Source Datax is saved.
			[31:8]	Output Data Address x: The byte address bit[23:0]where Output Datax to be saved.
8+5*x	SGx_W2	SGx_WORD 2	[15:0]	Output Data Address x: The byte address bit[39:24]where Output Datax to be saved.
	Reversed	Reversed	[31:16]	/
9+5*x	SGx_W3	SGx_WORD 3	[31:0]	Source Data length x: The Length (by bytes) of Source Datax.
10+5*x	SGx_W4	SGx_WORD 4	[31:0]	Output Data length x: The Length (by bytes) of output Datax.

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No.	Descriptor	Name	Width	Description
46	NSA	NSA	[31:0]	Next SG Address: The byte address bit[31:0].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 32'h0.
47	NSA	NSA	[7:0]	Next SG Address: The byte address bit[39:32].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 8'h0. The [38] indicate whether the next set of source sg exists.[39] bit indicate whether the next set of output（dst）sg exists.
	NTA	NTA	[31:8]	Next task Address: The byte address bit[23:0] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 24'h0.
48	NTA	NTA	[7:0]	Next task Address: The byte address bit[39:24] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 16'h0.
	Reversed	Reversed	[31:8]	/
49	Reversed	Reversed	/	/
50	Reversed	Reversed	/	/
51	Reversed	Reversed	/	/

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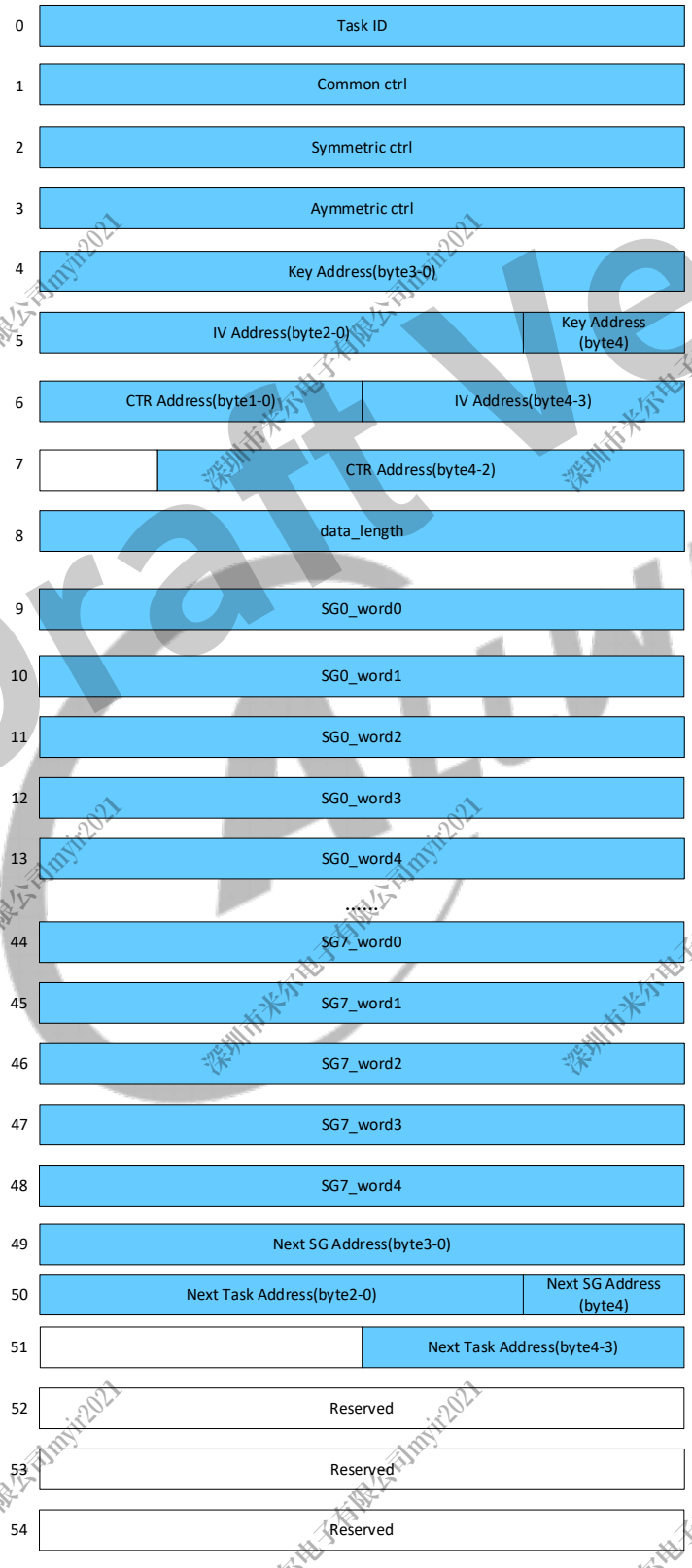
9.1.3.15 Other Algorithms Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination sg address and size, etc. The task descriptor is as follows.

Figure 9-16 Task Chaining of Other Algorithms



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Channel id supports 0-3 for each world.

- Common ctrl

Bit	Read/Write	Default	Description
31	R/W	0	interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:25	/	/	/
24:17	R/W	0	cbc_mac_len the outcome bit length of CBC-MAC when in CBC-MAC mode. The part also be used as gcm/ocb mode tag_len.
16:9	/	/	/
8	R/W	0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0	Algorithm type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x3： SM4 others: reserved 0x20: RSA 0x21: ECC 0x22: SM2 others: reserved 0x30: RAES Others: reserved

- Symmetric ctrl

Bit	Read/Write	Default	Description
31:30	/	/	/
29:28	R/W	0	SCK_SEL 0: use sck0/maskkey0 1: use sck1/maskkey1 2: use sck2/maskkey2 3: reserved
27:24	/	/	/

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Bit	Read/Write	Default	Description
23:20	R/W	0	KEY Select key select for AES/SM4/TDES（TDES only configured as 0/8-15） 0: Select input CE_KEYx (Normal Mode) 1: Select {SSK} 2: Select {HUK} 3: Select {RSSK}, used for decrypt EK, BSSK 4-7: Reserved 8-15: Select internal Key n (n from 0 to 7)
19:18	R/W	0	cfb_width For AES-CFB width 0: CFB1 1: CFB8 2: CFB64 3: CFB128
17	/	/	/
16	R/W	0	AES CTS last package flag When set to ‘1’, it means this is the last package for AES-CTS mode(the size of the last package >128bit). The part also be used as gcm/ocb mode gcm_last/ocb_last .
15:12	/	/	/
11:8	R/W	0	AES/DES/3DES/RAES modes. DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC operation mode for symmetric 0: Electronic Code Book (ECB) mode 1: Cipher Block Chaining (CBC) mode 2: Counter (CTR) mode 3: CipherText Stealing (CTS) mode 4: Output feedback (OFB)mode 5: Cipher feedback (CFB)mode 6: CBC-MAC mode 7: OCB mode 8: GCM mode 9: Reserved Other: reserved
7:6	/	/	/

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Bit	Read/Write	Default	Description
5:4	R/W	0	gcm_iv_mode[1:0] gcm_iv_mode[0]:value 1 show the last req for iv calculate gcm_iv_mode[1]: 0 :no GHASH calculate mode 1: GHASH calculate mode gcm_iv_mode[1:0]: 00: IDLE state ,this calculate do not have the process from iv to J0. 01: by iv padding generating J0. On the mode ,iv padding is 96 bits, so iv_length will be 96bits. 10: by GHASH calculate for iv generating J0, and this is not the last req for iv calculate. 11: by GHASH calculate for iv generating J0, and this is the last req for iv calculate
3:2	R/W	0	CTR Width Counter Width for CTR Mode 0: 16-bits Counter 1: 32-bits Counter, gcm mode always use this setting without software 2: 64-bits Counter 3: 128-bits Counter
1:0	R/W	0	AES Key Size 0: 128-bits 1: 192-bits 2: 256-bits 3: Reserved

- Asymmetric ctrl

Bit	Read/Write	Default	Description
31:21	/	/	/

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Bit	Read/Write	Default	Description
20:16	R/W	0	PKC algorithm mode. For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved For SM2： 00000: encryption 00001: decryption 00010: sign 00011: sign verify 00100: key exchange
15:8	/	/	/
7:0	R/W	0	Asymmetric algorithms operation width field. It indicates how much width this request apply, as words.

key addr field is address for each algorithm's key, also for extension feature micro codes address. (By byte)

ctr addr is address for next block's IV. (By byte)

src/dst sgX addr field indicate 40bits address for source and destination data. (By byte)

src/dst sgX size field indicates size for each sg respectively(by byte)

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For SG, the detail as flow:

byte3	byte2	byte1	byte0	
SRC_ADDR0 [B3]	SRC_ADDR0 [B2]	SRC_ADDR0 [B1]	SRC_ADDR0 [B0]	SG_WORD0
DST_ADDR0 [B2]	DST_ADDR0 [B1]	DST_ADDR0 [B0]	SRC_ADDR0 [B4]	SG_WORD1
		DST_ADDR0 [B4]	DST_ADDR0 [B3]	SG_WORD2
SRC_SIZE0 [B3]	SRC_SIZE0 [B2]	SRC_SIZE0 [B1]	SRC_SIZE0 [B0]	SG_WORD3
DST_SIZE0 [B3]	DST_SIZE0 [B2]	DST_SIZE0 [B1]	DST_SIZE0 [B0]	SG_WORD4

1 group SG has 8 sg, each sg has 5 words, the ADDR is 40 bits and byte-addr; the SIZE is 32bits nad byte-unit. We will support unlimited SG number,but the 1860 just use for test. This can has many group SG in a task, using the next_sg_addr to create the new SG information in the task.

Next sg field should be set to 0 when no next group sg, else set to next sg's descriptor.

next task field should be set to 0 when no next task, else set to next task's descriptor.

9.1.3.16 PKC Microcode

PKC module supports RSA, ECC, SM2 algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC/SM2 encryption, decryption, sign, verify are implemented with these microcode.

Asymmetric algorithms RSA/ECC/SM2 are implemented as microcode in PKC module. The encryption, decryption, sign, verify operations of asymmetric algorithms are composed with certain fixed microcode with hardware.

9.1.3.17 PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.

For RSA, parameters should be at the order of key, modulus, plaintext.

For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.

For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.

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For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.

For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.

For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.

For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.

For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

9.1.3.18 Error Check

After CE reads the task descriptor, CE can monitor error during algorithm operation. When the error is monitored, CE will do the following operations:

The task will pause immediately

Generates interrupt

The corresponding channel of the task status register is Fail

The corresponding channel bit of error status register can be read error number

The error number has the following types.

Code	Name	Description	Algorithms Type
0x01	algorithm not support	The algorithm type is not supported.	All
0x11	KEYSRAM access error	In AES decryption task, RSSK is used as plaintext, the DST address is not in KEYSRAM space.	AES decryption
0x21	key ladder configuration error	/	KL
0x31	data length error	Input size or output size configuration size error.	All

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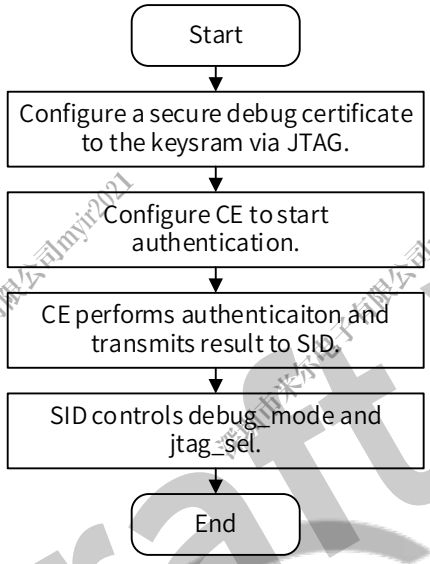
9.1.4 Programming Guidelines

9.1.4.1 Processing Secure Debug

The following figure shows the secure debug process.

Figure 9-17 Secure Debug Process



In secure debug process, CE mainly performs the following operatioins:

- Signature authentication
- Comparision of hash values of public key and chip_id
- Transmission of debug mode and transmission of authentification result

9.1.5 Register List

There are tree groups of registers in

Module Name	Base Address	Comments
CE_NS	0x03040000	Non-Security CE
CE_S	0x03040800	Security CE
SECURE_DEBUG_CFG	0x03042000	Secure Debug Configuration

9.1.5.1 CE_NS Register List

Module Name	Base Address	Comments
CE_NS	0x03040000	Non-Security CE

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Register Name	Offset	Description
CE_TDA0_NS	0x0000	Non-Security CE Task Descriptor Address0 Register
CE_TDA1_NS	0x0004	Non-Security CE Task Descriptor Address1 Register
CE_ICR_NS	0x0008	Non-Security CE Interrupt Control Register
CE_ISR_NS	0x000C	Non-Security CE Interrupt Status Register
CE_TLR_NS	0x0010	Non-Security CE Task Load Register
CE_TSR_NS	0x0014	Non-Security CE Task Status Register
CE_ESR_NS	0x0018	Non-Security CE Error Status Register

9.1.5.2 CE_S Register List

Module Name	Base Address	Comments
CE_S	0x03040800	Security CE

Register Name	Offset	Description
CE_TDA0_S	0x0000	Security CE Task Descriptor Address0 Register
CE_TDA1_S	0x0004	Security CE Task Descriptor Address1 Register
CE_ICR_S	0x0008	Security CE Interrupt Control Register
CE_ISR_S	0x000C	Security CE Interrupt Status Register
CE_TLR_S	0x0010	Security CE Task Load Register
CE_TSR_S	0x0014	Security CE Task Status Register
CE_ESR_S	0x0018	Security CE Error Status Register
CE_SCSA0_S	0x0020	Security CE Symmetric algorithm DMA Current Source Address0 Register
CE_SCSA1_S	0x0024	Security CE Symmetric algorithm DMA Current Source Address1 Register
CE_SCDA0_S	0x0028	Security CE Symmetric algorithm DMA Current Destination Address0 Register
CE_SCDA1_S	0x002C	Security CE Symmetric algorithm DMA Current Destination Address1 Register
CE_ACSA0_S	0x0030	Security CE Asymmetric algorithm DMA Current Source Address0 Register
CE_ACSA1_S	0x0034	Security CE Asymmetric algorithm DMA Current Source Address1 Register
CE_ACDA0_S	0x0038	Security CE Asymmetric algorithm DMA Current Destination Address0 Register
CE_ACDA1_S	0x003C	Security CE Asymmetric algorithm DMA Current Destination Address1 Register
CE_HCSA0_S	0x0040	Security CE HASH algorithm DMA Current Source Address0 Register
CE_HCSA1_S	0x0044	Security CE HASH algorithm DMA Current Source Address1 Register

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Register Name	Offset	Description
CE_HCDA0_S	0x0048	Security CE HASH algorithm DMA Current Destination Address0 Register
CE_HCDA1_S	0x004C	Security CE HASH algorithm DMA Current Destination Address1 Register
CE_XCSA0_S	0x0050	Security CE RAES algorithm DMA Current Source Address0 Register
CE_XCSA1_S	0x0054	Security CE RAES algorithm DMA Current Source Address1 Register
CE_XCDA0_S	0x0058	Security CE RAES algorithm DMA Current Destination Address0 Register
CE_XCDA1_S	0x005C	Security CE RAES algorithm DMA Current Destination Address1 Register

9.1.5.3 SECURE_DEBUG_CFG Register List

Module Name	Base Address	Comments
SECURE_DEBUG_CFG	0x03042000	Secure Debug Configuration

Register Name	Offset	Description
DEBUG_CTRL_AUTH	0x0000	Debug Authentication control Register

9.1.6 CE_NS Register Descrption

9.1.6.1 0x0000 Non-Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_NS
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_Address0 Task Descriptor Address0 is bit[31:0] (byte addr)

9.1.6.2 0x0004 Non-Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

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Offset: 0x0004			Register Name: CE_TDA1_NS
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	TASK_DES_Address1 Task Descriptor Address is bit[39:32] (byte addr)

9.1.6.3 0x0008 Non-Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_NS
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	/	/	HASH_PADDING 0: Hardware padding, perform one hash operation within a task. 1: Software padding, perform one hash operation in multiple tasks.
4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

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9.1.6.4 0x000C Non-Security CE Interrupt Status Register (Default Value: 0x0000_0000)

NOTE

The tasks of 4 channels can be calculated in parallel. Therefore, 4 types of interrupts can be pulled high at the same time.

Offset: 0x000C			Register Name: CE_ISR_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

9.1.6.5 0x0010 Non-Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_NS
Bit	Read/Write	Default	Description
31	R	0	TASK3_F_FULL task FIFO is not full. 0：channel 3 is ready to load task. 1：channel 3 is busy, can not load task.

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Offset: 0x0010			Register Name: CE_TLR_NS
Bit	Read/Write	Default	Description
30	R	0	TASK2_F_FULL task FIFO is not full. 0：channel 2 is ready to load task. 1：channel 2 is busy, can not load task.
29	R	0	TASK1_F_FULL task FIFO is not full. 0：channel 1 is ready to load task. 1：channel 1 is busy, can not load task.
28	R	0	TASK0_F_FULL task FIFO is not full. 0：channel 0 is ready to load task. 1：channel 0 is busy, can not load task.
27:20	/	/	/
19:16	R/W	0	Channel Task Load enable When set, channel load task . 0001：channel 0 load task enable 0010：channel 1 load task enable 0100：channel 2 load task enable 1000：channel 3 load task enable **Note: only when the corresponding bit is enabled, the task load signal can be loaded into the channel.**
15	R/W	0	TASK_LOAD_RAES When set, channel 3 can load the descriptor. 1：load ares task 0：no effect
14:11	/	/	/
10	R/W	0	TASK_LOAD_HASH When set, channel 2 can load the descriptor of task. 1：load hash task 0：no effect
9:6	/	/	/
5	R/W	0	TASK_LOAD_ASYMM When set, channel 1 can load the descriptor of task. 1：load asymm task 0：no effect
4:1	/	/	/
0	R/W	0	TASK_LOAD_SYMM When set, channel 0 can load the descriptor of task. 1：load symm task 0：no effect

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9.1.6.6 0x0014 Non-Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR_NS
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R	0x0	TASK_CHAN_RAES indicate which channel in run for RAES. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
23:19	/	/	/
18:16	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
15:11	/	/	/
10:8	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
7:3	/	/	/
2:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

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9.1.6.7 0x0018 Non-Security CE Error Status Register (Default Value: 0x0000_0000)

NOTE

If data length error occurs, CE needs to be reset. Because, in this case, the computation has already started. In order to ensure that the data FIFO and algorithm state machine are cleared after the error stauts is cleared, CE needs to be reset to ensure the normal calculation of the next task.

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved

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9.1.7 CE_S Register Descrption

9.1.7.1 0x0000 Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_ADDR0 Task Descriptor Address is bit[31:0] (byte addr)

9.1.7.2 0x0004 Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_ADDR1 Task Descriptor Address is bit[39:32] (byte addr)

9.1.7.3 0x0008 Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_S
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	HASH_PADDING 0: Hardware padding, perform one hash operation within a task. 1: Software padding, perform one hash operation in multiple tasks.
4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

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Offset: 0x0008			Register Name: CE_ICR_S
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

9.1.7.4 0x000C Security CE Interrupt Status Register (Default Value: 0x0000_0000)

NOTE

The tasks of 4 channels can be calculated in parallel. Therefore, 4 types of interrupts can be pulled high at the same time.

Offset: 0x000C			Register Name: CE_ISR_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

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9.1.7.5 0x0010 Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_S
Bit	Read/Write	Default	Description
31	R	0	CHANNEL3_F_FULL task FIFO is not full. 0：channel 3 is ready to load task. 1：channel 3 is busy，can not load task.
30	R	0	CHANNEL2_F_FULL task FIFO is not full. 0：channel 2 is ready to load task. 1：channel 2 is busy，can not load task.
29	R	0	CHANNEL1_F_FULL task FIFO is not full. 0：channel 1 is ready to load task. 1：channel 1 is busy，can not load task.
28	R	0	CHANNEL0_F_FULL task FIFO is not full. 0：channel 0 is ready to load task. 1：channel 0 is busy，can not load task.
27:20	/	/	/
19:16	R/W	0	Channel Task Load enable When set, channel load task . 0001：channel 0 load task enable 0010：channel 1 load task enable 0100：channel 2 load task enable 1000：channel 3 load task enable **Note: only when the corresponding bit is enabled, the task load signal can be loaded into the channel.**
15	R/W	0	TASK_LOAD_RAES When set, ares can load the descriptor. 1：load ares task 0：no effect
14:11	/	/	/
10	R/W	0	TASK_LOAD_HASH When set, hash can load the descriptor of task. 1：load hash task 0：no effect
9:6	/	/	/

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Offset: 0x0010			Register Name: CE_TLR_S
Bit	Read/Write	Default	Description
5	R/W	0	TASK_LOAD_ASYMM When set, asymm can load the descriptor of task. 1：load asymm task 0：no effect
4:1	/	/	/
0	R/W	0	TASK_LOAD_SYMM When set, symm can load the descriptor of task. 1：load symm task 0：no effect

9.1.7.6 0x0014 Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR_S
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R	0x0	TASK_CHAN_RAES indicate which channel in run for RAES. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
23:19	/	/	/
18:16	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
15:11	/	/	/
10:8	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
7:3	/	/	/

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Offset: 0x0014			Register Name: CE_TSR_S
Bit	Read/Write	Default/Hex	Description
2:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

9.1.7.7 0x0018 Security CE Error Status Register (Default Value: 0x0000_0000)

NOTE

If data length error occurs, CE needs to be reset. Because, in this case, the computation has already started. In order to ensure that the data FIFO and algorithm state machine are cleared after the error stauts is cleared, CE needs to be reset to ensure the normal calculation of the next task.

Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved

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Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved

9.1.7.8 0x0020 Security CE Symmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CE_SCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_SRC_ADDR0 Symmetric algorithm current source address DMA reads. Bit[31:0], byte addr.

9.1.7.9 0x0024 Security CE Symmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_SRC_ADDR1 Symmetric algorithm current source address DMA reads. Bit[39:32], byte addr.

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9.1.7.10 0x0028 Security CE Symmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_DST_ADDR0 Symmetric algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.11 0x002C Security CE Symmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_SCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_DST_ADDR1 Symmetric algorithm current destination address DMA writes. Bit[39:32], byte addr.

9.1.7.12 0x0030 Security CE Asymmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CE_ACSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_SRC_ADDR0 Asymmetric algorithm current source address DMA reads. Bit[31:0], byte addr.

9.1.7.13 0x0034 Security CE Asymmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_ACSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_SRC_ADDR1 Asymmetric algorithm current source address DMA reads. Bit[39:32], byte addr.

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9.1.7.14 0x0038 Security CE Asymmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_ACDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_DST_ADDR0 Asymmetric algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.15 0x003C Security CE Asymmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CE_ACDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_DST_ADDR1 Asymmetric algorithm current destination address DMA writes. Bit[39:32], byte addr.

9.1.7.16 0x0040 Security CE HASH algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CE_HCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_SRC_ADDR0 HASH algorithm current source address DMA reads. Bit[31:0], byte addr.

9.1.7.17 0x0044 Security CE HASH algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_HCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_SRC_ADDR1 HASH algorithm current source address DMA reads. Bit[39:32], byte addr.

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9.1.7.18 0x0048 Security CE HASH algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_HCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_DST_ADDR0 HASH algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.19 0x004C Security CE HASH algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CE_HCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_DST_ADDR1 HASH algorithm current destination address DMA writes. Bit[39:32], byte addr.

9.1.7.20 0x0050 Security CE RAES algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CE_XCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RAES_CUR_CUR_ADDR0 RAES algorithm current source address DMA reads.

9.1.7.21 0x0054 Security CE RAES algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RAES_CUR_CUR_ADDR1 RAES algorithm current source address DMA reads.

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9.1.7.22 0x0058 Security CE RAES algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RAES_CUR_DST_ADDR0 RAES algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.23 0x005C Security CE RAES algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: CE_XCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RAES_CUR_DST_ADDR1 RAES algorithm current destination address DMA writes. Bit[39:32], byte addr.

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Appendix: Glossary

The following table contains acronyms and abbreviations used in this document.

Term	Meaning
A	
ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
AMBA	Advanced Microcontroller Bus Architecture
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Synchronization
AWB	Automatic White Balance
AXI	Advanced eXtensible Interface
B	
BROM	Boot ROM
C	
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
D	
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
E	
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge

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Term	Meaning
F	
FEL	Fireware Exchange Launch
FIFO	First In First Out
G	
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
I	
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor
J	
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
L	
LRADC	Low Rate Analog to Digital Converter
LSB	Least Significant Bit
M	
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N	
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
O	
OHCI	Open Host Controller Interface
OTP	One Time Programmable
OWA	One Wire Audio
P	
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
PPU	Power Policy Unit
POR	Power-On Reset
PRCM	Power Reset Clock Management

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Term	Meaning
PWM	Pulse Width Modulation
R	
R	Read only/non-Write
RGB	Red Green Blue
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
S	
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
T	
TDES	Triple Data Encryption Standard
TWI	Two Wire Interface
U	
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB DRD	Universal Serial Bus Dual Role Device
UTMI	USB2.0 Transceiver Macrocell Interface

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