MYiR 米尔电子
Make Your Idea Real

MYC-LT527M Product Manual

Version：V1.0

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MYIR Electronics Limited

History

Version	Author	Participants	Date	Description
V1.0	MHW0097		20240125	Official release

Contents

1. Overview

The T527M series high-performance processor is based on eight core Cortex-A55 + HiFi4 DSP+RISC-V multi-core heterogeneous industrial processor, optional support AI 2 Tops model; LPDDR4/LPDDR4x Max. 4GB 32bits; Support H.265 4K@60fps and H.264 4K@30fps video decoding, H.264 1080P@60fps video coding, with rich multimedia interface HDMI、eDP、MIPI-DSI、RGB、LVDS、MIPI CSI、Parallel CSI, Support 4K@60Hz display, support three screen display; The processor also supports dual gigabit Ethernet interfaces, PCIE2.1 and USB3.1 high-speed interfaces, 2 CAN interfaces, 2 USB2.0 interfaces, and 10 UART functional interfaces. Suitable for industrial, automotive, power, medical, education and other application scenarios.

The T527M supports H.265, H.264, MJPEG-1/2/4, JPEG and other full-format decoding, MJPEG encoder up to 4K@15fps, JPEG encoder up to 8K x 8K resolution. The T527M processor has rich interfaces RGB*2, LVDS *2, MIPI DSI*2, Parallel CSI*2, DAC*2, ADC*3, I2S/PCM*4, USB*3, SDIO*3, Ethernet*2, TWI*6, UART*10, SPI*3, PWM*20, LRADC*2, GPADC*10, CAN*2, etc. Chip package HS-FCBGA664, 17mmx17mm.

Based on the T527 chip as the main processor, Mill Electronics has launched a new core board series: MYC-LT527M-I. MYC-LT527M-I has a good software development environment, the kernel supports the open source operating system Linux. The processor is a high-performance octa-core Cortex-A55CPU designed for intelligent control and human-machine interface in areas such as automotive and industrial applications, with a high price/performance ratio for entry-level Linux embedded ARM applications. Simplify hardware design and shorten development cycle.

Product introduction link: https://www.myirtech.com/list.asp?id=749

Download link: http://d.myirtech.com/MYD-LT527/

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Figure 1-1 MYC-LT527M Core board

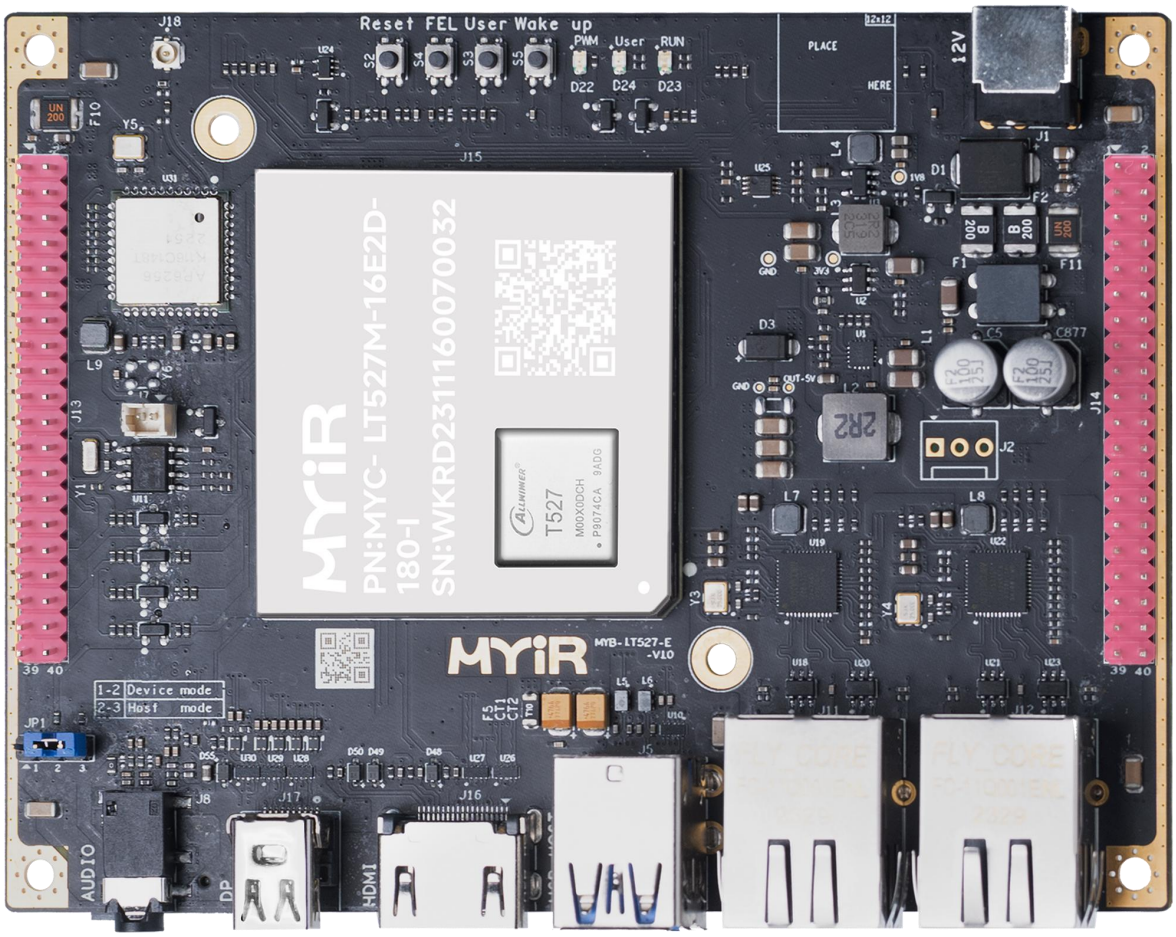

Figure 1-2 MYD-LT527M Kit

2. Product introduction

MYC-LT527M core board adopts high-density high-speed circuit board design, and integrates T527, DDR, eMMC, E2PROM, PMIC power supply and other circuits on the 45mm*43mm board.

The MYC-LT527M series core board includes 4 standard product models: they have some differences in storage configuration, and customers can choose the right model according to their needs. For the differences between product models, see Section 2.4.

2.1. CPU Introduction

The T527M is an eight-core 64-bit AI platform processor that delivers efficient computing power and is designed for intelligent control and human-machine interfaces in areas such as automotive and industrial applications.

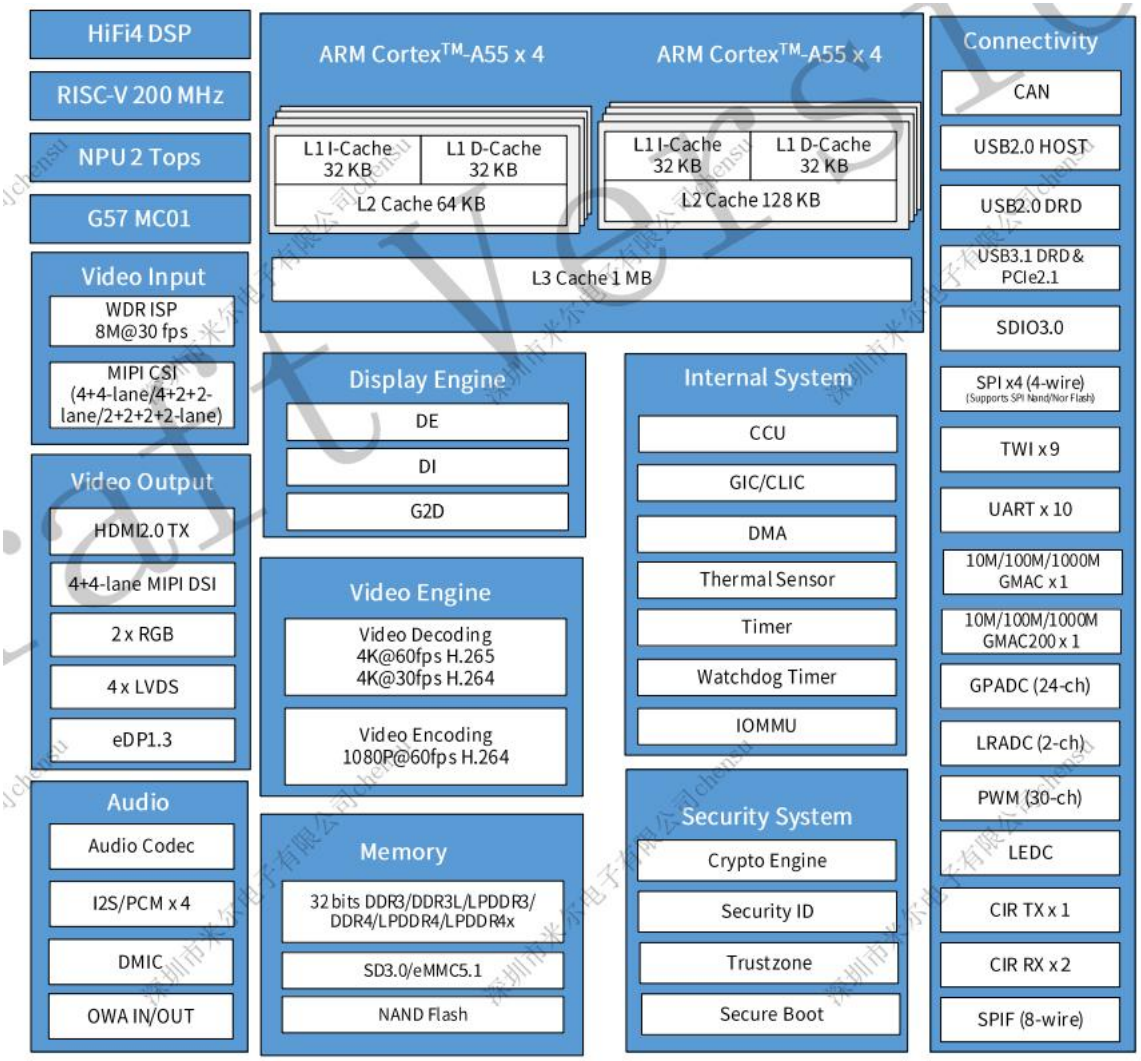

Figure 2-1 LT527M Resource block diagram

Resource	Parameter description
CPU	● 8 ARM CortexTM-A55x4，Up to 1.8 GHz ● 32 KB L1 cache + 32 KB L1 D-cache per core, and 128 KB L2 cache + 1MB L3cache
DSP	● HiFi4
External storage	**Three SD/MMC host controller (SMHC) interfaces** ● The SMHCO controls the devices that comply with the protocol Secure Digital Memory (SD mem-version3.0) ● The SMHC1 controls the device that complies with the protocol Secure Digital I/0 (SDIO-version 3.0) ● The SMHC2 controls the device that complies with the protocol Multimedia Card (eMMC-version 5.1)
Video engine	**Video Encoder / Decoder support** ● H.265 ITU-T.H@L6.1 up to 3840p@2160fps ● H.264 BP/MP/HP@L4.2 up to 1080p@60fps ● MPEG up to 4kp@15fps ● JPEG/MJPEG up to 8kp@8kfps
Video input	**Parallel CSI** ● Supports 16-bit digital camera interface ● Supports 8/10/12/16-bit width ● Supports BT656,BT601,BT.1120 interface ● Dual Data Rate(DDR) sample mode with pixel clock up to 148.5 MHz ● Supports ITU-R BT.656 up to 4*720p@30fps ● Supports ITU-R BT.1120 up to 4*1080p@30fps **MIPI CSI** ● 8M@30fps RAW12 2F-WDR,size up to 3264(H)x2448(V) ● 4+4-lane 4+2+2-lane,or2+2+2+2-lane MIPI Interface ● MIPI CSI2 V1.1　MIPI DPHY V1.1　1.5Gbit/S per lane ● Crop function ● Frame-rate decreasing via software ● 6 DMA controllers for 6 video stream storage ● Data conversion supports:YUV422 to YUV420,YUV422 to YUV400,YUV420 to YUV400, **VIPP** ● Four VIPP YUV422 or YUV420 outputs ● Maximum resolution of 3264x4224 ● Each VIPP has one sub-VIPP in online mode

	ISP ● Maximum frame rate of 8M@30fps 2F-WDR ● Supports off-line mode
Audio	● Two audio digital-to-analog converter (DAC) channels ● One audio output：One stereo headphone output: HPOUTL/R ● Three audio analog-to-digital converter (ADC) channels ● Three audio inputs: - Three differential microphone input: MICIN1P/1N,MICIN2P/2N,MICIN3P/3N (for echo reduction) - One differential lineout output: LINEOUTLP/N、LINEOUTRP/N
Display output	**HDMI** ● One HDMI2.0 TX interface,supporting HDCP1.4 ● Supports several data formats including RGB888,YUV444,YUV422,and YUV200 ● Supports I2S,192KHz sampling rate,8sound channels ● Supports up to 3840x2160@60 10bit input,3Data lanes,6Gbit/s per lane for YUV422 ● Supports DDC/CEC,5V tolerant voltage ● Supports 3840x2160,1920x1080,and 1280x720 resolution **MIPI DSI** ● Compliance with MIPI DSI V1.02 ● Up to 1.5Gbit/s for each lane ● Supports 4-lane MIPI DSl, up to 1280 x 720@60fps and 1920 x 1200@60fps ● Supports non-burst mode with sync pulse/sync event and burst 、command mode ● Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565 ● Supports continuous and non-continuous lane clock modes ● Supports bidirectional communication of all generic commands in LP through data lane 0 ● Supports low power data transmission ● Supports ULPS and escape modes ● Supports haedware checksum
Safety Engine	**Crypto Engine (CE)** ● Supports Symmetrical algorithm for encryption and decryption: AES, DES, 3TDES and SM4 . ● Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC. ● Supports Asymmetrical algorithm for signature verification: RSA,ECC.

connection	● 3 x USB （USB2.0 OTG+USB2.0 HOST+USB3.1DRD&PCIe2.1 Combo) ● 2x Gigabit Ethernet Interface -10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces ● 2 x CAN Interface ● 9 x TWI ● 10 x UART ● 4 x SPI ● 3 x SD/MMC ● 20 x PWM ● 24 x GPADC ● 2 x TPADC
package	● HS-FCBGA664, package ● 17 mm x 17 mm size

Table 2-1 LT527M resources

Refer to the chip manual for details.

2.2. Core Board Features

Item	features
CPU series	T527M
CPU Chip type	LT527M/MN
DDR storage	1/2/4GB LPDDR4
eMMC	8/16/32GB eMMC
CPU Processor	4xCortex-A55@1.8GHz+4xCortex-A55@1.4GHz
Core board size	45mm x 43mm
interface type	LGA：381PIN
PCB board specifications	12 layer plate design, gold sinking process production

Table 2-2 Core board features

2.3. Block Diagram

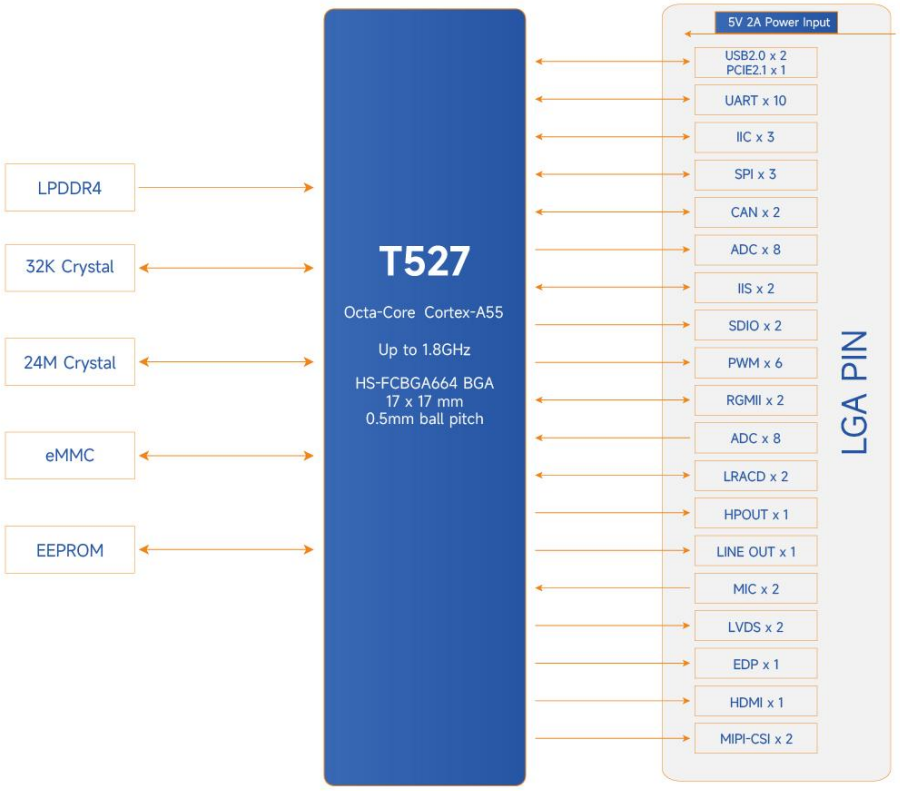

Figure 2-2 Core board block diagram

2.4. Core Board Ordering Information

The MYC-LT527M series core board consists of 4 standard product models: they have some differences in operating temperature parameters, and customers can choose the appropriate model according to their needs. For batch requirements, MYIR provides customized services with optional core board parameters. Low configuration model:MYC-LT527M/MN-8E1/2D-180-I-G, Frequency: 4*Cortex-A55@1.8GHz + 4*Cortex-A55@1.4GHz。

Part No. / Item	MYC-LT527M/MN-16E2D-180-I-G	MYC-LT527M/MN-32E4D-180-I-G
CPU	T527M/MN	T527M/MN
CPU series	T527	T527
DDR	2GB LPDDR4	4GB LPDDR4
eMMC	16GB EMMC	32GB EMMC
Core	8 CortexTM-A55x4	8 CortexTM-A55x4
Frequency	1.8GHz	1.8GHz
Video output	LVDS x 1 HDMI x1 MIPI DSI x1 EDP x1	LVDS x 1 HDMI x1 MIPI DSI x1 EDP x1
Audio	HPOUTL/R x1 MICIN/P x2 LINEINL/R x1	HPOUTL/R x1 MICIN/P x2 LINEINL/R x1
Parallel CSI	2	2
uSDHC	2	2
USB	USB2.0 OTG x 1 USB2.0 Host x 1 USB3.0 OTG x 1	USB2.0 OTG x 1 USB2.0 Host x 1 USB3.0 OTG x 1
Ethernet	RGMII x 2	RGMII x 2
UART	10	10
TWI	3	3
CAN	2	2
SPI	3	3
ADC	LRADC x1 GPADC x10	LRADC x1 GPADC x10
PWM	6	6

GPIO	203	203
System	Linux 5.4.61	Linux 5.4.61
Power Supply	+5V	+5V
Mechanical size	45mm x 43mm	45mm x 43mm
Operating temperature	-40℃ - +85℃	-40℃ - +85℃
Connector	LGA (total 381 pins)	LGA (total 381 pins)
Certification	CE ROHS	CE ROHS

Table 2-3 MYC-LT527M core board ordering information

***Note**: The blue background represents the interface type supported by the core board module; The gray background represents the others. The selection table is the maximum resource extracted from the core board, and there may be a reuse relationship.*

3. Pin Description

3.1. Pin Out

The MYC-LT52/M core board is soldered to the base plate in the form of an SMD patch, and the front pins are LGA with 381 pins. For details about the baseboard package design, see Section 7.2.

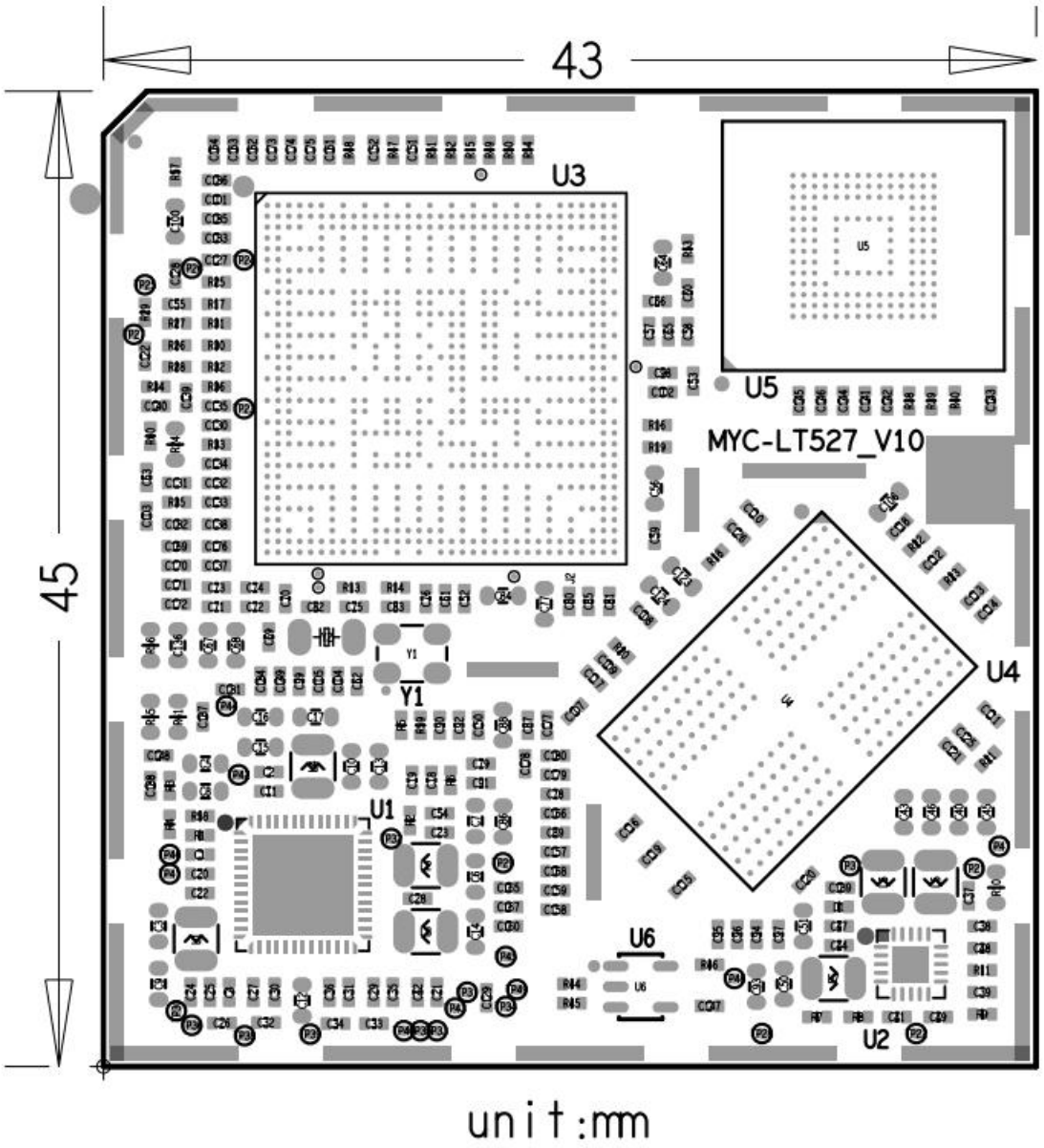

Figure 3-1 Module Pin map (Top side)

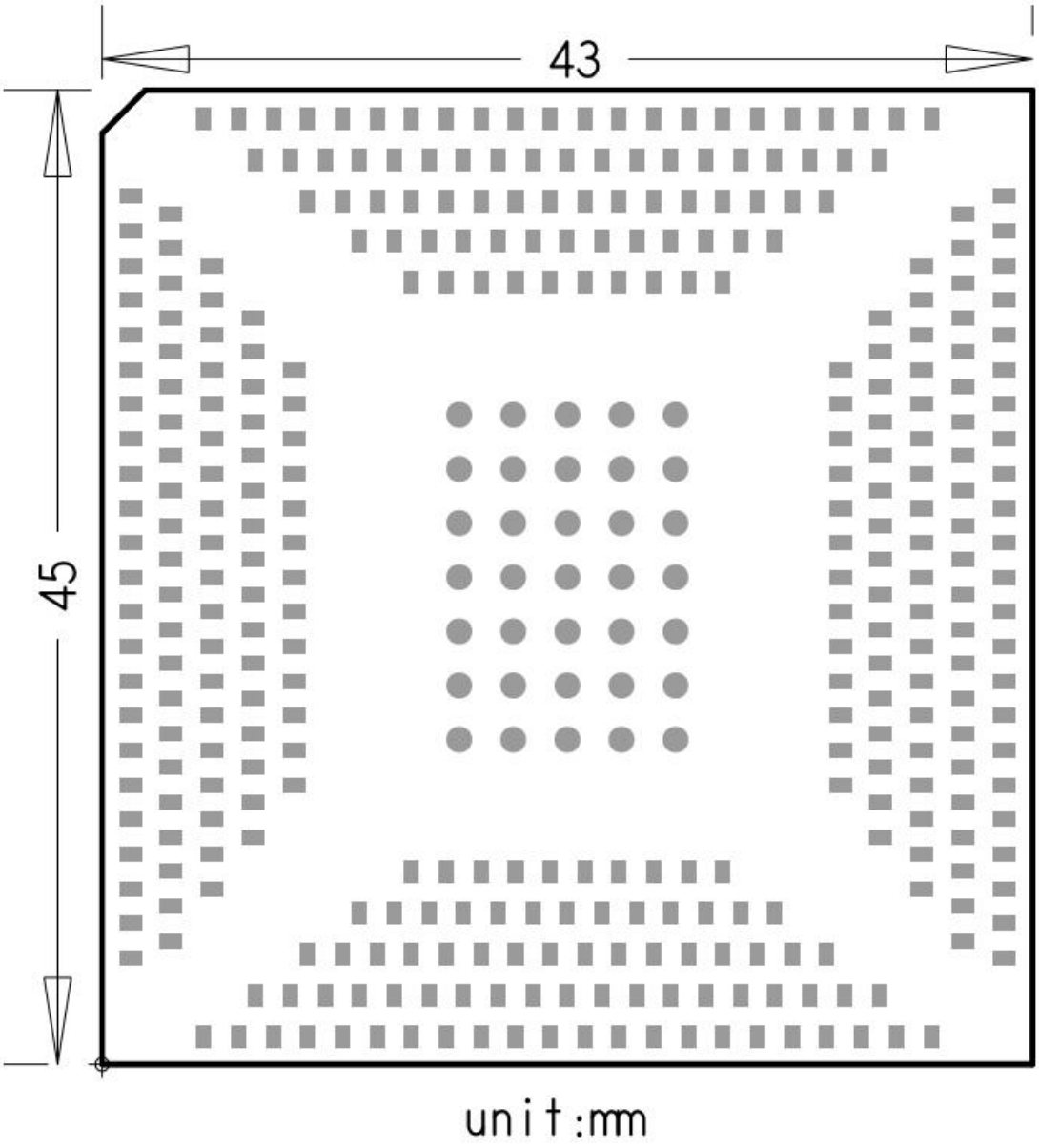

Figure 3-2 Module pin map（Bottom side）

3.2. Pin List

The following table shows the definition of the interface pins of the MYC-LT527M core board. The pin functions of the BSP development kit are configured according to "Default functions" in the following table. If you need to change the default pin functions, please modify the related driver configuration code.

-	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	A1	MCSIC-D0P	CSI	CSI differential signal +	1.8V	I/O	
	A2	MCSIC-D0N	CSI	CSI differential signal -	1.8V	I/O	
	A24	MCSIC-D1P	CSI	CSI differential signal +	1.8V	I/O	
	A25	MCSIC-D1N	CSI	CSI differential signal -	1.8V	I/O	
	A46	MCSIC-CKP	CSI	CSI differential CLK signal+	1.8V	I/O	
	A47	MCSIC-CKN	CSI	CSI differential CLK signal -	1.8V	I/O	
	A4	MCSID-D0P	CSI	CSI differential signal +	1.8V	I/O	
	A5	MCSID-D0N	CSI	CSI differential signal -	1.8V	I/O	
	A27	MCSID-D1P	CSI	CSI differential signal +	1.8V	I/O	
	A28	MCSID-D1N	CSI	CSI differential signal -	1.8V	I/O	
	A65	MCSID-CKP	CSI	CSI differential CLK signal+	1.8V	I/O	
	A66	MCSID-CKN	CSI	CSI differential CLK signal -	1.8V	I/O	
	A49	RGMII1-MDC	RGMII1	RGMII1 clock signal	3.3V	I/O	
	A50	RGMII1-MDIO	RGMII1	RGMII1 data signal	3.3V	I/O	
	A81	RGMII1-TXCK	RGMII1	RGMII1 TX clock signal	3.3V	I/O	
	A82	RGMII1-TXCTL	RGMII1	RGMII1 enable signal	3.3V	I/O	
	A83	RGMII1-TXD0	RGMII1	RGMII1 data signal	3.3V	I/O	
	A84	RGMII1-TXD1	RGMII1	RGMII1 data signal	3.3V	I/O	
	A67	RGMII1-TXD2	RGMII1	RGMII1 data signal	3.3V	I/O	
	A68	RGMII1-TXD3	RGMII1	RGMII1 data signal	3.3V	I/O	
	A69	RGMII1-EPHY-25M	RGMII1	RGMII1 25M signal	3.3V	I/O	
	A51	RGMII1-CLKIN	RGMII1	RGMII1-clock signal input	3.3V	I/O	
	A52	RGMII1-RXCTL	RGMII1	RGMII1 enable signal	3.3V	I/O	
	A29	RGMII1-RXCK	RGMII1	RGMII1 RX clock signal	3.3V	I/O	
	A30	RGMII1-RXD0	RGMII1	RGMII1 data signal	3.3V	I/O	
	A31	RGMII1-RXD1	RGMII1	RGMII1 data signal	3.3V	I/O	
	A7	RGMII1-RXD2	RGMII1	RGMII1 data signal	3.3V	I/O	
	A8	RGMII1-RXD3	RGMII1	RGMII1 data signal	3.3V	I/O	

A53	SDC1-CLK	SDIO	SDC1 clock signal	1.8V	I/O	
A54	SDC1-CMD	SDIO	SDC1detection signal	1.8V	I/O	
A71	SDC1-D0	SDIO	SDIO data signal	1.8V	I/O	
A72	SDC1-D1	SDIO	SDIO data signal	1.8V	I/O	
A85	SDC1-D2	SDIO	SDIO data signal	1.8V	I/O	
A86	SDC1-D3	SDIO	SDIO data signal	1.8V	I/O	
A10	I2S1-MCLK	I2S1	I2S master clock signal	1.8V	I/O	
A11	I2S1-BCLK	I2S1	The Bit signal of I2S	1.8V	I/O	
A12	I2S1-LRCK	I2S1	I2S frame clock signal	1.8V	I/O	
A33	I2S1-DIN1	I2S1	I2S serial data input	1.8V	I/O	
A34	I2S1-DOUT1	I2S1	I2S serial data output	1.8V	I/O	
A13	MICIN1N	MIC	MIC differential signal-	1.8V	AI	
A14	MICIN1P	MIC	MIC differential signal+	1.8V	AI	
A35	MICIN2N	MIC	MIC differential signal-	1.8V	AI	
A36	MICIN2P	MIC	MIC differential signal+	1.8V	AI	
A37	MBIAS	MIC	First Bias Voltage Output For Main Microphone	1.8V	AO	
A55	HPOUTFB	HP	Pseudo Differential Headphone Ground Reference	/	AI	
A56	HPOUTL	HP	Headphone Light Output	1.8V	AO	
A57	HPOUTR	HP	Headphone Right Output	1.8V	AO	
A73	HP-DET	JACK	Headphone Jack Detect	1.8V	AI	
A74	LINEOUTLP	LINE	Lineout Left Channel Positive Differential Output	1.8V	AO	
A75	LINEOUTLN	LINE	Lineout Left Channel Negative Differential Output	1.8V	AO	
A88	LINEOUTRP	LINE	Lineout Right Channel Positive Differential Output	1.8V	AO	
A89	LINEOUTRN	LINE	Lineout Right Channel Negative Differential Output	1.8V	AO	
A16	GPADC3	GPADC	General Purpose ADC Input	1.8V	AI	
A59	GPADC4	GPADC	General Purpose ADC Input	1.8V	AI	

A91	GPADC5	GPADC	General Purpose ADC Input	1.8V	AI	
A39	GPADC6	GPADC	General Purpose ADC Input	1.8V	AI	
A77	GPADC7	GPADC	General Purpose ADC Input	1.8V	AI	
A17	GPADC8	GPADC	General Purpose ADC Input	1.8V	AI	
A60	GPADC9	GPADC	General Purpose ADC Input	1.8V	AI	
A92	GPADC10	GPADC	General Purpose ADC Input	1.8V	AI	
A40	LRADC0	LRADC	Low Rate ADC	1.8V	AI	
A78	LRADC1	LRADC	Low Rate ADC	1.8V	AI	
A19	I2S2-MCLK	I2S2	I2S master clock signal	3.3V	I/O	
A20	I2S2-BCLK	I2S2	The Bit signal of I2S	3.3V	I/O	
A21	I2S2-LRCK	I2S2	I2S frame clock signal	3.3V	I/O	
A42	I2S2-DOUT0	I2S2	I2S serial data output	3.3V	I/O	
A43	I2S2-DIN0	I2S2	I2S serial data input	3.3V	I/O	
A41	PE0	IO	general purpose in/output	3.3V	I/O	
A79	PE10	IO	general purpose in/output	3.3V	I/O	
A62	NC	/	/	/	/	
A80	PL6	IO	general purpose in/output	3.3V	I/O	
A64	PL7	IO	general purpose in/output	3.3V	I/O	
A22	PL10	IO	general purpose in/output	3.3V	I/O	
A23	PL11	IO	general purpose in/output	3.3V	I/O	
B1	UART4-TX	UART	UART Data transmit	3.3V	I/O	
B2	UART4-RX	UART	UART Data receive	3.3V	I/O	
B23	UART4-RTS	UART	Flow control signal of serial port	3.3V	I/O	
B3	UART4-CTS	UART	Flow control signal of serial port	3.3V	I/O	
B24	UART6-TX	UART	UART Data transmit	3.3V	I/O	
B4	UART6-RX	UART	UART Data receive	3.3V	I/O	
B42	UART5-TX	UART	UART Data transmit	3.3V	I/O	
B25	UART5-RX	UART	UART Data receive	3.3V	I/O	

B5	UART3-RTS	UART	Flow control signal of serial port	3.3V	I/O	
B43	UART3-CTS	UART	Flow control signal of serial port	3.3V	I/O	
B26	UART3-TX	UART	UART Data transmit	3.3V	I/O	
B58	UART3-RX	UART	UART Data receive	3.3V	I/O	
B6	S-UART0-TX	UART	UART Data transmit	3.3V	I/O	
B44	S-UART0-RX	UART	UART Data receive	3.3V	I/O	
B27	S-UART1-TX	UART	UART Data transmit	3.3V	I/O	
B59	S-UART1-RX	UART	UART Data receive	3.3V	I/O	
B45	UART1-TX	UART	UART Data transmit	1.8V	I/O	
B71	UART1-RX	UART	UART Data receive	1.8V	I/O	
B7	UART1-RTS	UART	Flow control signal of serial port	1.8V	I/O	
B60	UART1-CTS	UART	Flow control signal of serial port	1.8V	I/O	
B29	SPI1-CS0	SPI1	SPI slice selection signal	3.3V	I/O	
B30	SPI1-CLK	SPI1	SPI clock signal	3.3V	I/O	
B47	SPI1-MOSI	SPI1	The main output of SPI is from the input	3.3V	I/O	
B48	SPI1-MISO	SPI1	SPI main input from output	3.3V	I/O	
B61	PJ18	IO	general purpose in/output	3.3V	I/O	
B9	PJ16	IO	general purpose in/output	3.3V	I/O	
B73	PJ17	IO	general purpose in/output	3.3V	I/O	
B62	PJ19	IO	general purpose in/output	3.3V	I/O	
B46	PJ24	IO	general purpose in/output	3.3V	I/O	
B72	PJ25	IO	general purpose in/output	3.3V	I/O	
B10	SPI2-CS0	SPI2	SPI slice selection signal	3.3V	I/O	
B11	SPI2-CLK	SPI2	SPI clock signal	3.3V	I/O	
B31	SPI2-MOSI	SPI2	The main output of SPI is from the input	3.3V	I/O	
B32	SPI2-MISO	SPI2	SPI main input from output	3.3V	I/O	
B75	CK32K-OUT	CLK	32M clock output	3.3V	I/O	
B76	CK24M-OUT	CLK	24M clock output	3.3V	I/O	
B12	TWI4-SCK	TWI4	12C clock signal	3.3V	I/O	
B13	TWI4-SDA	TWI4	12C data signal	3.3V	I/O	

B50	TWI5-SCK	TWI5	12C clock signal	3.3V	I/O	
B51	TWI5-SDA	TWI5	12C data signal	3.3V	I/O	
B64	S-TWI1-SCK	S-TWI1	12C clock signal	3.3V	I/O	
B65	S-TWI1-SDA	S-TWI1	12C data signal	3.3V	I/O	
B77	PWM-2	PWM	Pulse width modulation signal	3.3V	I/O	
B34	PWM-10	PWM	Pulse width modulation signal	3.3V	I/O	
B66	PWM-11	PWM	Pulse width modulation signal	3.3V	I/O	
B14	PWM-12	PWM	Pulse width modulation signal	3.3V	I/O	
B52	PWM-15	PWM	Pulse width modulation signal	3.3V	I/O	
B78	PWM-14	PWM	Pulse width modulation signal	3.3V	I/O	
B35	PM0	IO	Pulse width modulation signal	1.8V	I/O	
B67	PM1	IO	Pulse width modulation signal	1.8V	I/O	
B15	PM2	IO	Pulse width modulation signal	1.8V	I/O	
B53	PM3	IO	Pulse width modulation signal	1.8V	I/O	
B63	PM4	IO	Pulse width modulation signal	1.8V	I/O	
B49	PM5	IO	Pulse width modulation signal	1.8V	I/O	
B79	VCC-CARD	3V3	core board outputs 3V3	3.3V	P	
B80	VCC-CARD	3V3	core board outputs 3V3	3.3V	P	
B56	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B39	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B19	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B57	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B40	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B20	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B41	VDD_CORE_5V	5V	Base Board output 5V	5V	P	

B21	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B22	VDD_CORE_5V	5V	Base Board output 5V	5V	P	
B36	GND	/	/	0V	G	
B68	GND	/	/	0V	G	
B69	GND	/	/	0V	G	
B54	GND	/	/	0V	G	
B37	GND	/	/	0V	G	
B16	GND	/	/	0V	G	
B17	GND	/	/	0V	G	
B55	GND	/	/	0V	G	
B38	GND	/	/	0V	G	
B70	GND	/	/	0V	G	
B18	GND	/	/	0V	G	
C1	UART0-TX	UART	UART Data transmit	3.3V	I/O	
C24	UART0-RX	UART	UART Data receive	3.3V	I/O	
C2	UART7-RTS	UART	Flow control signal of serial port	3.3V	I/O	
C25	UART7-CTS	UART	Flow control signal of serial port	3.3V	I/O	
C3	UART7-TX	UART	UART Data transmit	3.3V	I/O	
C46	UART7-RX	UART	UART Data receive	3.3V	I/O	
C26	UART2-TX	UART	UART Data transmit	3.3V	I/O	
C4	UART2-RX	UART	UART Data receive	3.3V	I/O	
C47	UART2-RTS	UART	Flow control signal of serial port	3.3V	I/O	
C27	UART2-CTS	UART	Flow control signal of serial port	3.3V	I/O	
C65	RESET	RESET	Reset signal	1.8V	I/O,OD	
C48	PD22	IO	general purpose in/output	3.3V	I/O	
C28	PD23	IO	general purpose in/output	3.3V	I/O	
C66	PD20	IO	general purpose in/output	3.3V	I/O	
C6	PD21	IO	general purpose in/output	3.3V	I/O	
C49	CAN-TX	CAN	CAN Data transmit	3.3V	I/O	
C50	CAN-RX	CAN	CAN Data receive	3.3V	I/O	
C30	NC	/	/	/	/	

C51	WREQIN	DCXO	WREQIN signal from DCXO	3.3V	AI	
C9	PB8	IO	general purpose in/output	3.3V	I/O	
C52	PB6	IO	general purpose in/output	3.3V	I/O	
C84	PB7	IO	general purpose in/output	3.3V	I/O	
C70	CAN0-CPUS-TX	CAN	CAN Data transmit	3.3V	I/O	
C71	CAN0-CPUS-RX	CAN	CAN Data receive	3.3V	I/O	
C11	PWRON	POWER	Power start enable signal	3.3V	I/O	
C86	FEL	System	Force burn pin	3.3V	I/O	
C55	AP-NMI	System	AP-NMI	3.3V	I/O,OD	
C87	PH19	IO	general purpose in/output	3.3V	I/O	
C73	PH8	IO	general purpose in/output	3.3V	I/O	
C56	PH11	IO	general purpose in/output	3.3V	I/O	
C88	PH12	IO	general purpose in/output	3.3V	I/O	
C42	LVDS0-D0P	LVDS0	LVDS differential signal+	1.8V	I/O	
C41	LVDS0-D0N	LVDS0	LVDS differential signal-	1.8V	I/O	
C61	LVDS0-D1P	LVDS0	LVDS differential signal+	1.8V	I/O	
C60	LVDS0-D1N	LVDS0	LVDS differential signal-	1.8V	I/O	
C93	LVDS0-D2P	LVDS0	LVDS differential signal+	1.8V	I/O	
C92	LVDS0-D2N	LVDS0	LVDS differential signal-	1.8V	I/O	
C17	LVDS0-CKP	LVDS0	LVDS differential clock signal+	1.8V	I/O	
C16	LVDS0-CKN	LVDS0	LVDS differential clock signal-	1.8V	I/O	
C39	LVDS0-D3P	LVDS0	LVDS differential signal+	1.8V	I/O	
C38	LVDS0-D3N	LVDS0	LVDS differential signal-	1.8V	I/O	
C77	LVDS1-D0P	LVDS1	LVDS differential signal+	1.8V	I/O	
C76	LVDS1-D0N	LVDS1	LVDS differential signal-	1.8V	I/O	
C90	LVDS1-D1P	LVDS1	LVDS differential signal+	1.8V	I/O	
C89	LVDS1-D1N	LVDS1	LVDS differential signal-	1.8V	I/O	
C58	LVDS1-D2P	LVDS1	LVDS differential signal+	1.8V	I/O	
C57	LVDS1-D2N	LVDS1	LVDS differential signal-	1.8V	I/O	
C14	LVDS1-CKP	LVDS1	LVDS differential clock signal+	1.8V	I/O	
C13	LVDS1-CKN	LVDS1	LVDS differential clock signal-	1.8V	I/O	

C36	LVDS1-D3P	LVDS1	LVDS differential signal+	1.8V	I/O	
C35	LVDS1-D3N	LVDS1	LVDS differential signal-	1.8V	I/O	
C20	EDP-AUXP	EDP	EDP differential clock signal+	1.8V	I/O	
C19	EDP-AUXN	EDP	EDP differential clock signal-	1.8V	I/O	
C80	EDP-TX0P	EDP	EDP differential signal+	1.8V	I/O	
C79	EDP-TX0N	EDP	EDP differential signal-	1.8V	I/O	
C21	EDP-HPD	EDP	EDP hot swap	1.8V	I/O	
C64	EDP-TX1P	EDP	EDP differential signal+	1.8V	I/O	
C63	EDP-TX1N	EDP	EDP differential signal-	1.8V	I/O	
C45	EDP-TX2P	EDP	EDP differential signal+	1.8V	I/O	
C44	EDP-TX2N	EDP	EDP differential signal-	1.8V	I/O	
C23	EDP-TX3P	EDP	EDP differential signal+	1.8V	I/O	
C22	EDP-TX3N	EDP	EDP differential signal-	1.8V	I/O	
C32	SPI0-CS0	SPI2	SPI slice selection signal	1.8V	I/O	
C33	SPI0-CS1	SPI2	SPI clock signal	1.8V	I/O	
C34	SPI0-CLK	SPI2	SPI clock signal	1.8V	I/O	
C53	SPI0-MOSI	SPI2	The main output of SPI is from the input	1.8V	I/O	
C54	SPI0-MISO	SPI2	SPI main input from output	1.8V	I/O	
D1	HTX0P	HDMI	HDMI differential signal+	1.8V	AO	
D2	HTX0N	HDMI	HDMI differential signal-	1.8V	AO	
D23	HTX1P	HDMI	HDMI differential signal+	1.8V	AO	
D24	HTX1N	HDMI	HDMI differential signal-	1.8V	AO	
D4	HTX2P	HDMI	HDMI differential signal+	1.8V	AO	
D5	HTX2N	HDMI	HDMI differential signal-	1.8V	AO	
D43	HTXCP	HDMI	HDMI differential clock signal+	1.8V	AO	
D44	HTXCN	HDMI	HDMI differential clock signal-	1.8V	AO	
D27	HSCL	HDMI	12C clock signal	1.8V	O	
D26	HSDA	HDMI	12C data signal	1.8V	I/O	
D58	HCEC	HDMI	HCEC	1.8V	I/O	
D6	HHPD	HDMI	HDMI hot swappable	1.8V	I/O	

D8	USB0-DP	USB	USB data signal +	3.3V	AI/O	
D9	USB0-DM	USB	USB data signal -	3.3V	AI/O	
D46	USB2-DP	USB	USB data signal +	3.3V	AI/O	
D47	USB2-DM	USB	USB data signal -	3.3V	AI/O	
D29	USB1-DP	USB	USB data signal +	3.3V	AI/O	
D30	USB1-DM	USB	USB data signal -	3.3V	AI/O	
D73	PCIE-CLKP	PCIE	PCIE differential clock signal+	1.8V	AI/O	
D74	PCIE-CLKN	PCIE	PCIE differential clock signal-	1.8V	AI/O	
D59	PCIE-TX0-DP	PCIE	PCIE differential signal+	1.8V	AO	
D60	PCIE-TX0-DN	PCIE	PCIE differential signal-	1.8V	AO	
D62	PCIE-RX0-DP	PCIE	PCIE differential signal+	1.8V	AI	
D63	PCIE-RX0-DN	PCIE	PCIE differential signal-	1.8V	AI	
D11	SDC0-CLK	SDC0	SDC clock signal	3.3V	O	
D12	SDC0-CMD	SDC0	SDC command signal	3.3V	O	
D13	SDC0-D0	SDC0	SDIO data signal	3.3V	I/O	
D32	SDC0-D1	SDC0	SDIO data signal	3.3V	I/O	
D33	SDC0-D2	SDC0	SDIO data signal	3.3V	I/O	
D49	SDC0-D3	SDC0	SDIO data signal	3.3V	I/O	
D50	SDC0-DET	SDC0	SDC detection signal	3.3V	O	
D34	RGMII0-MDC	RGMII0	RGMII0 clock signal	3.3V	I/O	
D35	RGMII0-MDIO	RGMII0	RGMII0 data signal	3.3V	I/O	
D52	RGMII0-TXD0	RGMII0	RGMII0 data signal	3.3V	I/O	
D53	RGMII0-TXD1	RGMII0	RGMII0 data signal	3.3V	I/O	
D54	RGMII0-TXD2	RGMII0	RGMII0 data signal	3.3V	I/O	
D69	RGMII0-TXD3	RGMII0	RGMII0 data signal	3.3V	I/O	
D70	RGMII0-TXCK	RGMII0	RGMII0 TX clock signal	3.3V	I/O	
D68	RGMII0-TXCTL	RGMII0	RGMII0 enable signal	3.3V	I/O	
D67	RGMII0-RXCTL	RGMII0	RGMII0 enable signal	3.3V	I/O	
D65	RGMII0-RXCK	RGMII0	RGMII0 RX clock signal	3.3V	I/O	
D66	RGMII0-RXD0	RGMII0	RGMII0 data signal	3.3V	I/O	
D76	RGMII0-RXD1	RGMII0	RGMII0 data signal	3.3V	I/O	
D77	RGMII0-RXD2	RGMII0	RGMII0 data signal	3.3V	I/O	

	D78	RGMII0-RXD3	RGMII0	RGMII0 data signal	3.3V	I/O	
	D79	EPHY-CLK-25M	RGMII0	RGMII0 25M signal	3.3V	I/O	
	D80	RGMII0-CLKIN-125M	RGMII0	RGMII0 125Mclock signal input	3.3V	I/O	
	D15	MCSIA-D0N	CSI	CSI differential signal-	1.8V	I/O	
	D16	MCSIA-D0P	CSI	CSI differential signal+	1.8V	I/O	
	D37	MCSIA-D1N	CSI	CSI differential signal-	1.8V	I/O	
	D38	MCSIA-D1P	CSI	CSI differential signal+	1.8V	I/O	
	D18	MCSIA-CKN	CSI	CSI differential signal-	1.8V	I/O	
	D19	MCSIA-CKP	CSI	CSI differential signal+	1.8V	I/O	
	D56	MCSIB-D0N	CSI	CSI differential signal-	1.8V	I/O	
	D57	MCSIB-D0P	CSI	CSI differential signal+	1.8V	I/O	
	D40	MCSIB-D1N	CSI	CSI differential signal-	1.8V	I/O	
	D41	MCSIB-D1P	CSI	CSI differential signal+	1.8V	I/O	
	D21	MCSIB-CKN	CSI	CSI differential clock signal-	1.8V	I/O	
	D22	MCSIB-CKP	CSI	CSI differential clock signal+	1.8V	I/O	

Table 3-1 MYC-LT527M Core board Pin List

4. Electrical Characteristics

4.1. Primary System Power (VDD_5V)

The main power supply of the MYC-LT527M core board is VDD_5V, which corresponds to 9 pins such as B56, B39, B19 of the stamp hole SMD pad. In order to ensure normal operation, the base plate must provide a voltage of 5V±5%, a current of about 2-3A, and ensure that the output capacity of the power supply circuit can meet the power consumption of the core board. This section lists the power consumption and current of the core board under various conditions. Please reserve an appropriate margin when designing the power supply circuit.

Name	Description	Recommended Voltage
VDD_CORE_5V	Main supply voltage, 5V input, 2A	5V
VCC-CARD	3.3V output，500mA	3.3V

Table 4-1 External input / output voltage

4.2. Power Consumption

Conditon	Voltage(V)	Average Current(A)	Power Consumption (W)
no-load	4.96	0.4	1.984
Full-load (ENET*1+USB*2+Type-C*1+SD Card*1+aging)	4.96	1.1	5.456
mem (echo mem)	4.96	0.01	0.0496
freeze (echo freeze)	4.96	0.14	0.6944

Table 4-2 Power consumption parameters

4.3. GPIO DC Parameters

Parameter	Symbol	Min	Typical	Max	Units	description
High-lever DC input voltage	V_{IH}	0.7*VCC_{IO}	—	VCC_{IO}+0.3	V	—
Low-lever DC input voltage	V_{IL}	-0.3	—	0.3*VCC_{IO}	V	—
High-lever DC output voltage	V_{OH}	VCC_{IO}-0.3	—	VCC_{IO}	V	—
Low-lever DC output voltage	V_{OL}	0	—	0.2	V	—

Table 4-3 GPIO DC Parameters

5. System necessary circuit design

5.1. Boot

With the MYC-LT527M core board, you do not need to pay attention to the boot bit configuration when designing the baseboard. SD card is inserted and the card surface has been burned mirror, the development board will boot from SD card preferentially. After removing the MicroSD card, the development board can be booted from eMMC .

5.2. Burning firmware

Micro SD card circuit is recommended for the core board of MYC-LT527M to burn and update the firmware of the core board, and SMHC0 is recommended for signal interface. Please refer to Section 6.1.

5.3. Debug

It is recommended that the core board of MYC-LT527M use UART interface circuit to debug the software program of the core board. It is recommended that the signal interface use UART0. For details, please refer to Section 6.2.

5.4. Reset

With the MYC-LT527M core board, the RESET signal is led out by the PIN C65 pin of the core board, which is used for the hardware system of the core board to reset the input signal, The core board pulls down the 1nF capacitor, and the logic chip is used to open the leakage output of the core board to isolate external interference. Please refer to Section 4 for details.

6. Interfaces

6.1. SD

The MYC-LT527M core board is equipped with three SD/MMC interfaces, SMHC0, SMHC1 and SMHC2. SMHC0 is commonly used to design MicroSD card signals; SMHC2 has been used to connect EMMC signals on the core board. SMHC1 is 1V8 level, and the chip supports SD3.0 protocol.

6.1.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	D11	SDC0-CLK	SDC0	SDIO clock signal	3.3V	O	
	D12	SDC0-CMD	SDC0	SDIO command signal	3.3V	O	Pull up inside the chip
	D13	SDC0-D0	SDC0	SDIO data signal	3.3V	I/O	
	D32	SDC0-D1	SDC0	SDIO data signal	3.3V	I/O	
	D33	SDC0-D2	SDC0	SDIO data signal	3.3V	I/O	
	D49	SDC0-D3	SDC0	SDIO data signal	3.3V	I/O	
	D50	SDC0-DET	SDC0	SDC detection signal	3.3V	O	Pull up inside the chip,A series 1K resistor is required

Table 6-1 SD/MMC PIN description

6.2. UART

The MYC-LT527M core board processor has up to 10 serial ports. UART1 is at 1V8 level, where UART1-4 and UART7 are 4-wire with flow control (RTS and CTS signals) functions.

6.2.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	B1	UART4-TX	UART	UART Data transmit	3.3V	I/O	
	B2	UART4-RX	UART	UART Data receive	3.3V	I/O	
	B23	UART4-RTS	UART	Flow control signal of serial port	3.3V	I/O	
	B3	UART4-CTS	UART	Flow control signal of serial port	3.3V	I/O	
	B24	UART6-TX	UART	UART Data transmit	3.3V	I/O	
	B4	UART6-RX	UART	UART Data receive	3.3V	I/O	
	B25	UART5-TX	UART	UART Data transmit	3.3V	I/O	
	B5	UART5-RX	UART	UART Data receive	3.3V	I/O	
	B43	UART3-RTS	UART	Flow control signal of serial port	3.3V	I/O	
	B26	UART3-CTS	UART	Flow control signal of serial port	3.3V	I/O	
	B58	UART3-TX	UART	UART Data transmit	3.3V	I/O	
	B6	UART3-RX	UART	UART Data receive	3.3V	I/O	
	B44	S-UART0-TX	UART	UART Data transmit	3.3V	I/O	
	B26	S-UART0-RX	UART	UART Data receive	3.3V	I/O	
-	B59	S-UART1-TX	UART	UART Data transmit	3.3V	I/O	
	B45	S-UART1-RX	UART	UART Data receive	3.3V	I/O	
	B45	UART1-TX	UART	UART Data transmit	1.8V	I/O	
	B71	UART1-RX	UART	UART Data receive	1.8V	I/O	
	B7	UART1-RTS	UART	Flow control signal of serial port	1.8V	I/O	
	B60	UART1-CTS	UART	Flow control signal of serial port	1.8V	I/O	
	C1	UART0-TX	UART	UART Data transmit	3.3V	I/O	
	C24	UART0-RX	UART	UART Data receive	3.3V	I/O	
	C2	UART7-RTS	UART	Flow control signal of serial port	3.3V	I/O	
	C25	UART7-CTS	UART	Flow control signal of serial port	3.3V	I/O	
	C3	UART7-TX	UART	UART Data transmit	3.3V	I/O	
	C46	UART7-RX	UART	UART Data receive	3.3V	I/O	
	C26	UART2-TX	UART	UART Data transmit	3.3V	I/O	
	C4	UART2-RX	UART	UART Data receive	3.3V	I/O	

	C47	UART2-RTS	UART	Flow control signal of serial port	3.3V	I/O	
	C27	UART2-CTS	UART	Flow control signal of serial port	3.3V	I/O	

Table 6-2 UART PIN description

6.3. USB

The MYC-LT527M core board provides two USB2.0 channels and one USB3.1 DRD. USB0 supports HOST and Device modes, and the burning program can only use the USB0 port. The USB1 only supports HOST mode, and the USB0-1 has a maximum speed of 480Mbps. The USB2 supports HOST and Device modes, and the USB3.1 rate can reach 5Gbps.

6.3.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	D8	USB0-DP	USB	USB data signal +	3.3V	AI/O	
	D9	USB0-DM	USB	USB data signal -	3.3V	AI/O	
	D46	USB2-DP	USB	USB data signal +	3.3V	AI/O	
	D47	USB2-DM	USB	USB data signal -	3.3V	AI/O	
	D29	USB1-DP	USB	USB data signal +	3.3V	AI/O	
	D30	USB1-DM	USB	USB data signal -	3.3V	AI/O	
	D73	PCIE-CLKP	PCIE	PCIE differential clock signal+	3.3V	AI/O	
	D74	PCIE-CLKN	PCIE	PCIE differential clock signal-	3.3V	AI/O	
	D59	PCIE-TX0-DP	PCIE	PCIE differential signal+	3.3V	AO	
	D60	PCIE-TX0-DN	PCIE	PCIE differential signal-	3.3V	AO	
	D62	PCIE-RX0-DP	PCIE	PCIE differential signal+	3.3V	AI	
	D63	PCIE-RX0-DN	PCIE	PCIE differential signal-	3.3V	AI	

Table 6-3 USB PIN description

6.4. Ethernet

Two RGMII signals are extracted from the MYC-LT527M core board. CPU Ethernet interfaces support only RGMII and RMII. Support 10/100/1000M transmission speed. The core board can output 25MHz clock signal to the external PHY chip for use, which can save the external 25MHz crystal oscillator. RGMII-TXCK is recommended to reserve RC for EMI suppression debugging and place it on the SOC end.

6.4.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	A49	RGMII1-MDC	RGMII1	RGMII1 clock signal	3.3V	I/O	
	A50	RGMII1-MDIO	RGMII1	RGMII1 data signal	3.3V	I/O	
	A81	RGMII1-TXCK	RGMII1	RGMII1 TX clock signal	3.3V	I/O	
	A82	RGMII1-TXCTL	RGMII1	RGMII1 enable signal	3.3V	I/O	
	A83	RGMII1-TXD0	RGMII1	RGMII1 data signal	3.3V	I/O	
	A84	RGMII1-TXD1	RGMII1	RGMII1 data signal	3.3V	I/O	
	A67	RGMII1-TXD2	RGMII1	RGMII1 data signal	3.3V	I/O	
	A68	RGMII1-TXD3	RGMII1	RGMII1 data signal	3.3V	I/O	
	A69	RGMII1-EPHY-25M	RGMII1	RGMII1 25M signal	3.3V	I/O	
	A51	RGMII1-CLKIN	RGMII1	RGMII1-clock signal input	3.3V	I/O	
	A52	RGMII1-RXCTL	RGMII1	RGMII1 enable signal	3.3V	I/O	
	A29	RGMII1-RXCK	RGMII1	RGMII1 RX clock signal	3.3V	I/O	
	A30	RGMII1-RXD0	RGMII1	RGMII1 data signal	3.3V	I/O	
	A31	RGMII1-RXD1	RGMII1	RGMII1 data signal	3.3V	I/O	
	A7	RGMII1-RXD2	RGMII1	RGMII1 data signal	3.3V	I/O	
	A8	RGMII1-RXD3	RGMII1	RGMII1 data signal	3.3V	I/O	
	D34	RGMII0-MDC	RGMII0	RGMII0 clock signal	3.3V	I/O	
	D35	RGMII0-MDIO	RGMII0	RGMII0 data signal	3.3V	I/O	
	D52	RGMII0-TXD0	RGMII0	RGMII0 data signal	3.3V	I/O	
	D53	RGMII0-TXD1	RGMII0	RGMII0 data signal	3.3V	I/O	
	D54	RGMII0-TXD2	RGMII0	RGMII0 data signal	3.3V	I/O	
	D69	RGMII0-TXD3	RGMII0	RGMII0 data signal	3.3V	I/O	
	D70	RGMII0-TXCK	RGMII0	RGMII0 TX clock signal	3.3V	I/O	
	D68	RGMII0-TXCTL	RGMII0	RGMII0 enable signal	3.3V	I/O	

	D67	RGMII0-RXCTL	RGMII0	RGMII0 enable signal	3.3V	I/O	
	D65	RGMII0-RXCK	RGMII0	RGMII0 RX clock signal	3.3V	I/O	
	D66	RGMII0-RXD0	RGMII0	RGMII0 data signal	3.3V	I/O	
	D76	RGMII0-RXD1	RGMII0	RGMII0 data signal	3.3V	I/O	
	D77	RGMII0-RXD2	RGMII0	RGMII0 data signal	3.3V	I/O	
	D78	RGMII0-RXD3	RGMII0	RGMII0 data signal	3.3V	I/O	
	D79	EPHY-CLK-25M	RGMII0	RGMII0 25M signal	3.3V	I/O	
	D80	RGMII0-CLKIN-125M	RGMII0	RGMII0 125Mclock signal input	3.3V	I/O	

Table 6-4 PHY PIN description

6.5. I2C

The MYC-LT527M core board processor supports four I2C (TWI) buses, among which I2C1 is used for E2PROM chip in the core board, and three I2C interfaces are led out to the core board for use.

If you want to use more I2C bus interfaces, consult the chip manual or Pin List and modify the pin configuration in the driver

6.5.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	B12	TWI4-SCK	TWI4	12C clock signal	3.3V	I/O	
	B13	TWI4-SDA	TWI4	12C data signal	3.3V	I/O	
	B50	TWI5-SCK	TWI5	12C clock signal	3.3V	I/O	
	B51	TWI5-SDA	TWI5	12C data signal	3.3V	I/O	
	B64	S-TWI1-SCK	S-TWI1	12C clock signal	3.3V	I/O	
	B65	S-TWI1-SDA	S-TWI1	12C data signal	3.3V	I/O	

Table 6-5 I2C PIN description

6.6. PWM

The MYC-LT527M core board leads to six PWM interfaces, which can also be used as a general I/O port. Up to 16 independent PWM channels for the PWM controller, supporting PWM continuous mode output; Support PWM pulse mode output, pulse number can be configured. Up to 8 pairs of complementary output PWM controllers.

6.6.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	B77	PWM-2	PWM	Pulse width modulation signal	3.3V	I/O	
	B34	PWM-10	PWM	Pulse width modulation signal	3.3V	I/O	
	B66	PWM-11	PWM	Pulse width modulation signal	3.3V	I/O	
	B14	PWM-12	PWM	Pulse width modulation signal	3.3V	I/O	
	B52	PWM-15	PWM	Pulse width modulation signal	3.3V	I/O	
	B78	PWM-14	PWM	Pulse width modulation signal	3.3V	I/O	

Table 6-6 Audio PIN description

6.7. LVDS

The MYC-LT527M core board has two LVDS display and output interfaces. Supports dual LVDS0+LVDS1 display interfaces. Support dual screen display, resolution 1920x1080@60Hz. Where, when LVDS1 serves as MIPI DSI, the resolution is 1920x1080@60Hz; LVDS0 supports the display of a single LVDS interface. The resolution is 1366x768@60Hz. It is 3V3 level for normal IO and 1V8 level for LVDS

6.7.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	C42	LVDS0-D0P	LVDS0	LVDS differential signal+	1.8V	I/O	
	C41	LVDS0-D0N	LVDS0	LVDS differential signal-	1.8V	I/O	
	C61	LVDS0-D1P	LVDS0	LVDS differential signal+	1.8V	I/O	
	C60	LVDS0-D1N	LVDS0	LVDS differential signal-	1.8V	I/O	
	C93	LVDS0-D2P	LVDS0	LVDS differential signal+	1.8V	I/O	
	C92	LVDS0-D2N	LVDS0	LVDS differential signal-	1.8V	I/O	
	C17	LVDS0-CKP	LVDS0	LVDS differential clock signal+	1.8V	I/O	
	C16	LVDS0-CKN	LVDS0	LVDS differential clock signal-	1.8V	I/O	
	C39	LVDS0-D3P	LVDS0	LVDS differential signal+	1.8V	I/O	
	C38	LVDS0-D3N	LVDS0	LVDS differential signal-	1.8V	I/O	
-							
	C77	LVDS1-D0P	LVDS1	LVDS differential signal+	1.8V	I/O	
	C76	LVDS1-D0N	LVDS1	LVDS differential signal-	1.8V	I/O	
	C90	LVDS1-D1P	LVDS1	LVDS differential signal+	1.8V	I/O	
	C89	LVDS1-D1N	LVDS1	LVDS differential signal-	1.8V	I/O	
	C58	LVDS1-D2P	LVDS1	LVDS differential signal+	1.8V	I/O	
	C57	LVDS1-D2N	LVDS1	LVDS differential signal-	1.8V	I/O	
	C14	LVDS1-CKP	LVDS1	LVDS differential clock signal+	1.8V	I/O	
	C13	LVDS1-CKN	LVDS1	LVDS differential clock signal-	1.8V	I/O	
	C36	LVDS1-D3P	LVDS1	LVDS differential signal+	1.8V	I/O	
	C35	LVDS1-D3N	LVDS1	LVDS differential signal-	1.8V	I/O	

Table 6-7 LVDS PIN description

6.8. AUDIO

The MYC-LT527M core board contains an analog audio CODE-C interface, which can provide 1 HPOUT L/R interface, 1 LINEOUT L/R, and 2 MICIN1/2 P/N.

6.8.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	A13	MICIN1N	MIC	MIC differential signal-	1.8V	AI	
	A14	MICIN1P	MIC	MIC differential signal+	1.8V	AI	
	A35	MICIN2N	MIC	MIC differential signal-	1.8V	AI	
	A36	MICIN2P	MIC	MIC differential signal+	1.8V	AI	
	A37	MBIAS	MIC	First Bias Voltage Output For Main Microphone	1.8V	AO	
	A55	HPOUTFB	HP	Pseudo Differential Headphone Ground Reference	1.8V	AI	
	A56	HPOUTL	HP	Headphone Light Output	1.8V	AO	
	A57	HPOUTR	HP	Headphone Right Output	1.8V	AO	
	A73	HP-DET	JACK	Headphone Jack Detect	1.8V	AI	
	A74	LINEOUTLP	LINE	Lineout Left Channel Positive Differential Output	1.8V	AO	
	A75	LINEOUTLN	LINE	Lineout Left Channel Negative Differential Output	1.8V	AO	
	A88	LINEOUTRP	LINE	Lineout Right Channel Positive Differential Output	1.8V	AO	
	A89	LINEOUTRN	LINE	Lineout Right Channel Negative Differential Output	1.8V	AO	

Table 6-8 Audio PIN description

6.9. ADC

The MYC-LT527M core board supports 8 GPADC and 2 LRADC. GPADC has a 12/10-bit resolution, a maximum 1Mhz sampling rate, and supports signal input ranges from 0 to 1.8V. LRADC has a 6-bit resolution, a maximum 2Khz sampling rate, and supports signal input ranges from 0 to 1.35V.

6.9.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	A16	GPADC3	GPADC	General Purpose ADC Input	1.8V	AI	
	A59	GPADC4	GPADC	General Purpose ADC Input	1.8V	AI	
	A91	GPADC5	GPADC	General Purpose ADC Input	1.8V	AI	
	A39	GPADC6	GPADC	General Purpose ADC Input	1.8V	AI	
	A77	GPADC7	GPADC	General Purpose ADC Input	1.8V	AI	
	A17	GPADC8	GPADC	General Purpose ADC Input	1.8V	AI	
	A60	GPADC9	GPADC	General Purpose ADC Input	1.8V	AI	
	A92	GPADC10	GPADC	General Purpose ADC Input	1.8V	AI	
	A40	LRADC0	LRADC	General Purpose ADC Input	1.8V	AI	
	A78	LRADC1	LRADC	General Purpose ADC Input	1.8V	AI	

Table 6-9 ADC PIN description

6.10. MIPI CSI

The MYC-LT527M core board supports two MIPI CSI interfaces with a level of 1V8. The maximum input for CSI is 8M@30fps, the maximum pixel clock for parallel CSI interface is 148.5MHz, and the maximum input for BT656 interface is 4*720P@30fps in clock dual-edge sampling mode.

6.10.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	A1	MCSIC-D0P	CSI	CSI differential signal +	1.8V	I/O	
	A2	MCSIC-D0N	CSI	CSI differential signal -	1.8V	I/O	
	A24	MCSIC-D1P	CSI	CSI differential signal +	1.8V	I/O	
	A25	MCSIC-D1N	CSI	CSI differential signal -	1.8V	I/O	
	A46	MCSIC-CKP	CSI	CSI differential CLK signal+	1.8V	I/O	
	A47	MCSIC-CKN	CSI	CSI differential CLK signal -	1.8V	I/O	
	A4	MCSID-D0P	CSI	CSI differential signal +	1.8V	I/O	
	A5	MCSID-D0N	CSI	CSI differential signal -	1.8V	I/O	
	A27	MCSID-D1P	CSI	CSI differential signal +	1.8V	I/O	
	A28	MCSID-D1N	CSI	CSI differential signal -	1.8V	I/O	
	A65	MCSID-CKP	CSI	CSI differential CLK signal+	1.8V	I/O	
	A66	MCSID-CKN	CSI	CSI differential CLK signal -	1.8V	I/O	
	D15	MCSIA-D0N	CSI	CSI differential signal-	1.8V	I/O	
	D16	MCSIA-D0P	CSI	CSI differential signal+	1.8V	I/O	
	D37	MCSIA-D1N	CSI	CSI differential signal-	1.8V	I/O	
	D38	MCSIA-D1P	CSI	CSI differential signal+	1.8V	I/O	
	D18	MCSIA-CKN	CSI	CSI differential signal-	1.8V	I/O	
	D19	MCSIA-CKP	CSI	CSI differential signal+	1.8V	I/O	
	D56	MCSIB-D0N	CSI	CSI differential signal-	1.8V	I/O	
	D57	MCSIB-D0P	CSI	CSI differential signal+	1.8V	I/O	
	D40	MCSIB-D1N	CSI	CSI differential signal-	1.8V	I/O	
	D41	MCSIB-D1P	CSI	CSI differential signal+	1.8V	I/O	
	D21	MCSIB-CKN	CSI	CSI differential clock signal-	1.8V	I/O	
	D22	MCSIB-CKP	CSI	CSI differential clock signal+	1.8V	I/O	

Table 6-10 CSI PIN description

6.11. I2S

Signal MYC-LT527M core board leads to two I2S interface, I2S1 is 1V8, I2S interface supports a variety of clocks, 24.576MHz/12.288MHz. Has adjustable widths from 8 bit to 32 bit sampling rates from 8-384 KHZ.

6.11.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	A10	I2S1-MCLK	I2S1	I2S master clock signal	1.8V	I/O	
	A11	I2S1-BCLK	I2S1	The Bit signal of I2S	1.8V	I/O	
	A12	I2S1-LRCK	I2S1	I2S frame clock signal	1.8V	I/O	
	A33	I2S1-DIN1	I2S1	I2S serial data input	1.8V	I/O	
	A34	I2S1-DOUT1	I2S1	I2S serial data output	1.8V	I/O	
	A19	I2S2-MCLK	I2S2	I2S master clock signal	3.3V	I/O	
	A20	I2S2-BCLK	I2S2	The Bit signal of I2S	3.3V	I/O	
	A21	I2S2-LRCK	I2S2	I2S frame clock signal	3.3V	I/O	
	A42	I2S2-DOUT0	I2S2	I2S serial data output	3.3V	I/O	
	A43	I2S2-DIN0	I2S2	I2S serial data input	3.3V	I/O	

Table 6-11 I2S PIN description

6.12. SPI

MYC-LT527M core board leads to 3 SPI interfaces, SPI0 is 1V8 level. SPI1-2 is 3V3 level, the main mode is 3-wire SPI, and has programmable serial data frame lengths from 1 to 32 bits. The maximum clock is 100MHz.

6.12.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	B29	SPI1-CS0	SPI1	SPI slice selection signal	3.3V	I/O	
	B30	SPI1-CLK	SPI1	SPI clock signal	3.3V	I/O	
	B47	SPI1-MOSI	SPI1	SPI main output from input	3.3V	I/O	
	B48	SPI1-MISO	SPI1	SPI main input from output	3.3V	I/O	
	B10	SPI2-CS0	SPI2	SPI slice selection signal	3.3V	I/O	
	B11	SPI2-CLK	SPI2	SPI clock signal	3.3V	I/O	
	B31	SPI2-MOSI	SPI2	The main output of SPI is from the input	3.3V	I/O	
	B32	SPI2-MISO	SPI2	SPI main input from output	3.3V	I/O	

Table 6-12 SPI PIN description

6.13. eDP

The MYC-LT527M core board leads to one EDP interface, resolution 2.5k@60Hz. 1, 2, and 4 lane transfers with a maximum transfer rate of 2.7 Gbit/s. Color depth: 8bit and 10bit per channel.

6.13.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	C20	EDP-AUXP	EDP	EDP differential clock signal+	1.8V	I/O	
	C19	EDP-AUXN	EDP	EDP differential clock signal-	1.8V	I/O	
	C80	EDP-TX0P	EDP	EDP differential signal+	1.8V	I/O	
	C79	EDP-TX0N	EDP	EDP differential signal-	1.8V	I/O	
	C21	EDP-HPD	EDP	EDP hot swap	1.8V	I/O	
	C64	EDP-TX1P	EDP	EDP differential signal+	1.8V	I/O	
	C63	EDP-TX1N	EDP	EDP differential signal-	1.8V	I/O	
	C45	EDP-TX2P	EDP	EDP differential signal+	1.8V	I/O	
	C44	EDP-TX2N	EDP	EDP differential signal-	1.8V	I/O	
	C23	EDP-TX3P	EDP	EDP differential signal+	1.8V	I/O	
	C22	EDP-TX3N	EDP	EDP differential signal-	1.8V	I/O	

Table 6-13 eDP PIN description

6.14. HDMI

The MYC-LT527M core board leads to 1 HDMI interface. The 5V power supply of HDMI must be connected with a Schottky diode in series to prevent leakage at the end of the device after shutdown. Please choose a Schottky diode with reduced on-voltage. Support 3840x2160, 1920x1080, 1280x720 resolution.

6.14.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	D1	HTX0P	HDMI	HDMI differential signal+	1.8V	AO	
	D2	HTX0N	HDMI	HDMI differential signal-	1.8V	AO	
	D23	HTX1P	HDMI	HDMI differential signal+	1.8V	AO	
	D24	HTX1N	HDMI	HDMI differential signal-	1.8V	AO	
	D4	HTX2P	HDMI	HDMI differential signal+	1.8V	AO	
	D5	HTX2N	HDMI	HDMI differential signal-	1.8V	AO	
	D43	HTXCP	HDMI	HDMI differential clock signal+	1.8V	AO	
	D44	HTXCN	HDMI	HDMI differential clock signal-	1.8V	AO	
	D27	HSCL	HDMI	12C clock signal	1.8V	O	
	D26	HSDA	HDMI	12C data signal	1.8V	I/O	
	D58	HCEC	HDMI	HCEC	1.8V	I/O	
	D6	HHPD	HDMI	HDMI hot swappable	1.8V	I/O	

Table 6-14 HDMI PIN description

7. Package Information

7.1. Package Dimensions

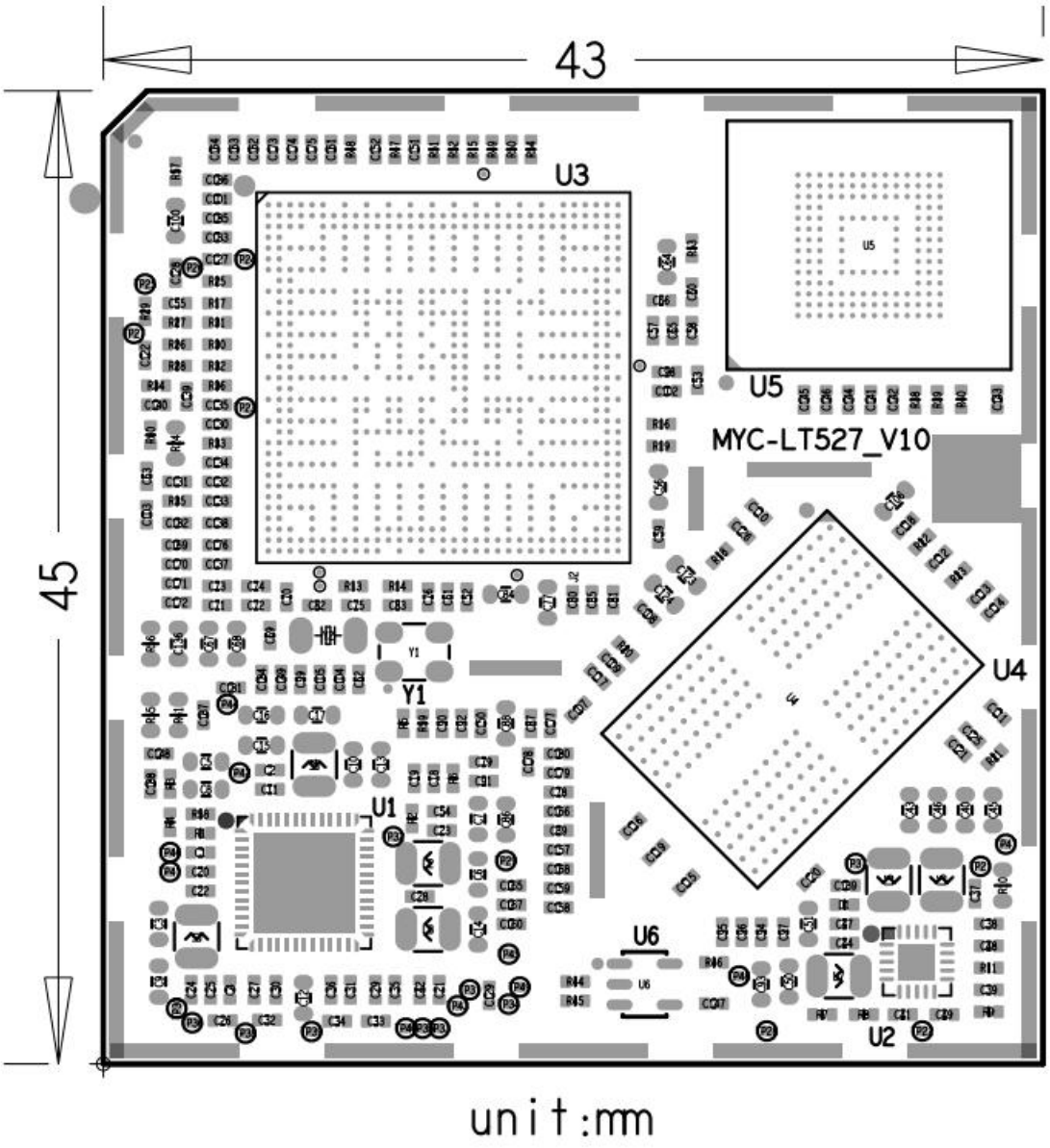

Figure 7-1 MYC-LT527M Top View

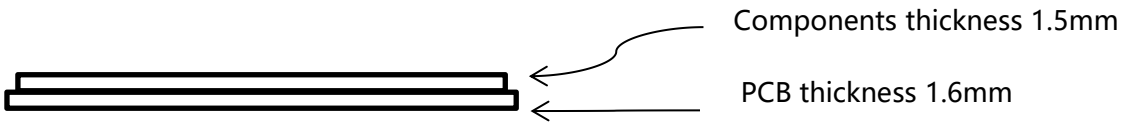

Figure 7-2 MYC-LT527M Side View

7.2. Carrier Board PCB Design

a. PCB thickness is recommended to be at least 1.6mm. Pay attention to the balance of copper coating. If PCB deformation occurs in the over furnace, it is recommended to use a carrier to fix the over furnace.

b. To ensure the quality of mounting and tinning, ensure that the PCB module is at least 3mm away from other components.

c. PCB packaging provided by MYIR Electronics is recommended.

8. Mount and storage requirements

8.1. Steel mesh design

1) It is recommended to open holes at a ratio of 1:1 for the circular pad with a thickness of 0.15mm tin; With a thickness of 0.18mm, the opening ratio is 1:0.8.

8.2. Storage requirement

Modules are shipped in vacuum sealed form, and the following conditions are required for storage:

1) The vacuum-sealed bag can be stored for 12 months when the ambient temperature is lower than 40℃ and the air humidity is less than 90%.

2) After opening the vacuum sealing bag, reflow welding can be carried out directly within 72 hours when the ambient temperature is lower than 30℃ and the air humidity is less than 10%.

Note: If the above conditions are not met, baking should be carried out before applying.

8.3. Baking method

Because the module packaging material cannot withstand high temperature, if necessary, please choose one of the following two methods to bake, to avoid affecting the welding quality of the module.

1) Baking in the original package: baking temperature is 40 ~ 60℃ and time is 5 ~ 7 days.

2) Transfer to high temperature resistant dish baking: baking temperature is 100 ~ 120, baking time is more than 48 hours.

8.4. Welding technology

1) If the plate to be mounted is double-sided device layout, it is recommended to put the core plate mounting process in the last stage.

2) It is recommended to set the preheating time of 160 ~ 200℃ to 60 ~ 120 seconds.

3) It is recommended that the temperature of reflow welding should be 235 ~ 245℃, and the maximum temperature should not exceed 250℃, and the reflow time should be controlled within 40 ~ 60 seconds.

4) The recommended temperature rise rate is 1-3 ℃/ s, and the temperature drop rate is 2-4 ℃/ s.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR’ s products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.

- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

MYIR Tech Limited

Headquarter Address: Room 04, 6th Floor, Building No.2, Fada Road, Yunli Smart Park, Bantian, Longgang District, Shenzhen, Guangdong, China 518129

Factory Address: Room 201, Block C, Shengjianli Industrial Park, Dafu Industrial Zone, Guanlan, Longhua District, Shenzhen, 518110, China

Website: www.myir.cn
Email: sales.en@myir.cn
Tel: +86-755-22984836