# MYC-YF13X Product Manual


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| | **Author:** | Dana |
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| | **Updated:** | 2024-10-18 |

# History

| Version | Author | Participants | Date | Description |
|---|---|---|---|---|
| V1.0 | TOM | | 20230527 | Initial Version |
| V1.1 | Bai | | 20241018 | Updated PWM1/PWM2 pin IO input/output definition |



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# 1. Overview

STM32MP135 Series processor is a cost-effective industrial processor based on single-core Cortex-A7; equipped with LCD-TFT parallel display interface and 16-bit parallel camera interface; The processor also supports 2-channel Gigabit Ethernet interfaces, 2-channel CAN interfaces, 2-channel USB2.0 interfaces and 8-channel UART functional interfaces, suitable for energy and power, industrial control, industrial gateway, industrial HMI and other scenarios.

MYIR Electronics has launched a new series of ST STM32MP13X chips as the main processor: MYC-YF13X. MYC-YF13X core board has the most stringent quality standards, ultra-high performance, rich peripheral resources, high cost performance and long supply time, which is suitable for the core board requirements required by high-performance intelligent equipment. In order to ensure the quality of products, through rigorous testing, to ensure the quality of products.

Product introduction link: https://www.myirtech.com/list.asp?id=727

Download link: http://d.myirtech.com/MYD-YF13X/


**Figure 1-1 The MYC-YF13X core board**

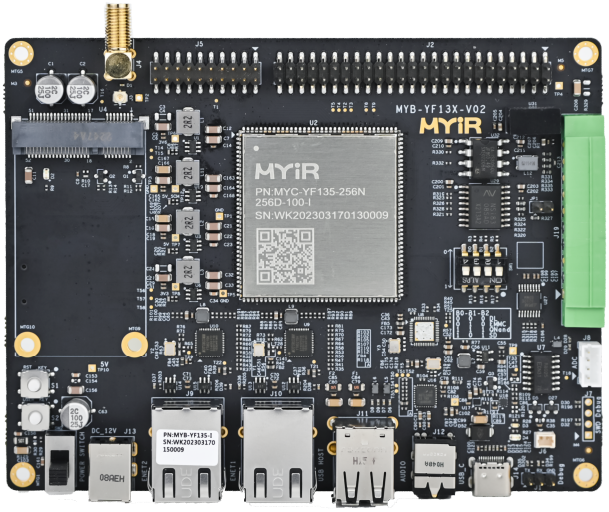


**Figure 1-2 The MYD-YF13X Kit**



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# 2. Product introduction

The MYC-YF13X core board adopts high-density high-speed circuit board design, with STM32MP135, DDR3L and Rand integrated on the 37mm * 39mm board card Flash / eMMC, E2PROM, discrete power supply, etc. The MYC-YF13X core board is welded to the bottom board as an SMD patch with stamp hole packaging pins. The board adopts 10 layers of high density PCB design, gold sinking process production, independent grounding signal layer, lead free.

## 2.1. CPU Introduction

STM32MP13X Series processor is a single-core Cortex-A7 processor with high operating frequency of 1GHz, equipped with dual-channel Gigabit Ethernet interface to provide high-cost and energy efficient processing power. This product line has advanced security functions, including: encryption algorithm accelerator, hardware robustness; memory protection against illegal access; code isolation mechanism to protect data security during runtime; multiple functions for platform authentication in the product life cycle; and a complete security ecosystem. STM32MP13X Microprocessors are designed for entry-level Linux, bare or RTOS systems, allowing MCU developers to friendly transition to MPU platform design.


**Figure 2-1 STM32MP135 Resource block diagram**

| Resource | Parameter description |
|---|---|
| CPU | ● 32-bit Arm® Cortex®-A7 1GHz |
| External storage | ● up to LPDDR2/LPDDR3-1066 16-bit<br>● up to DDR3/DDR3L-1066 16-bit<br>● Dual Quad-SPI memory interface<br>● 16-bit data bus: parallel interface to connect external ICs and SLC NAND memories with up to 8-bit ECC |
| Video engine | ● Video E ncoder / D ecoder support<br>● up to WXGA (1366 × 768) @60 fps or up to Full HD (192 0 x 1080) @ 30 fps<br>● pixel clock up to 90 MHz<br>● two layers (incl.1 secured) with programmable color |
| Simulation peri pherals | ● 2 × ADCs with 12-bit max.resolution up to 5 Msps<br>● 1 x temperature sensor<br>● 1 x digital filter for sigma-delta modulator (DFSDM) with 4 channels and 2 filters<br>● Internal or external ADC reference V REF+<br>● |
| Clock managem ent | ● Internal oscillators: 64 MHz HSI oscillator, 4 MHz CSI oscill ator, 32 kHz LSI oscillator<br>● External oscillators: 8-48 MHz HSE oscillator, 32.768 kHz LS E oscillator<br>● 4 × PLLs with fractional mode |
| Controller | ● 56 physical channels in total<br>● 1 x high-speed general-purpose master direct memory access c ontroller (MDMA)<br>● 3 × dual-port DMAs with FIFO and request router capabilities for optimal peripheral management |
| Security engine | ● TrustZone ® peripherals, 12 x tamper pins including 5 x acti ve tampers<br>● Temperature, voltage, frequency and 32 kHz monitoring |
| Peripherals | ● 5 × I2C FM+ (1 Mbit/s, SMBus/PMBus™)<br>● 4 x UART + 4 x USART (12.5 Mbit/s, ISO7816 interface, L IN, IrDA, SPI slave)<br>● 5 × SPI (50 Mbit/s, including 4 with full-duplex I 2S audio class accuracy via internal audio PLL or external clock )<br>● 2 × SAI (stereo audio: I 2S, PDM, SPDIF Tx)<br>● SPDIF Rx with 4 inputs<br>● 2 × SDMMC up to 8 bits (SD/e•MMC™/SDIO)<br>● 2 × CAN controllers supporting CAN FD protocol<br>● 2 × USB 2.0 high-speed Host – or 1 × USB 2.0 high-speed Host +1 × USB 2.0 high-speed OTG simultaneously |



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| | |
|---|---|
| | ● 2 x Ethernet MAC/GMAC – IEEE 1588v2 hardware, MII/RMII/RGMII<br>● 8to 16-bit camera interface, 3 Mpix @30 fps or 5Mpix @15 fps incolor or monochrome with pixel clock @120 MHz (max freq) |
| package | ● BGA 320 balls<br>● 11 mm x 11 mm size,0.5 mm ball pitch, |

**Table 2-1 YF13X Resources**

Please refer to the chip manual for more details.

## 2.2. Core Board Features

| Item | features |
|---|---|
| CPU series | STM32MP13X |
| CPU Chip type | STM32MP135D AF7 |
| DDR storage | 256MB/512MB DDR3L |
| EMMC | eMMC : 4GB.<br>QSPI-NAND : 256MB<br>E2PROM : 32KBit |
| CPU Processor | Arm® Cortex®-A7 up to 1 GHz |
| Core board size | 37mmx 39mm |
| interface type | Stamp hole |
| PCB board specifications | 10 layer board design, gold immersion process |

**Table 2-2 Core board features**

## 2.3. Block Diagram

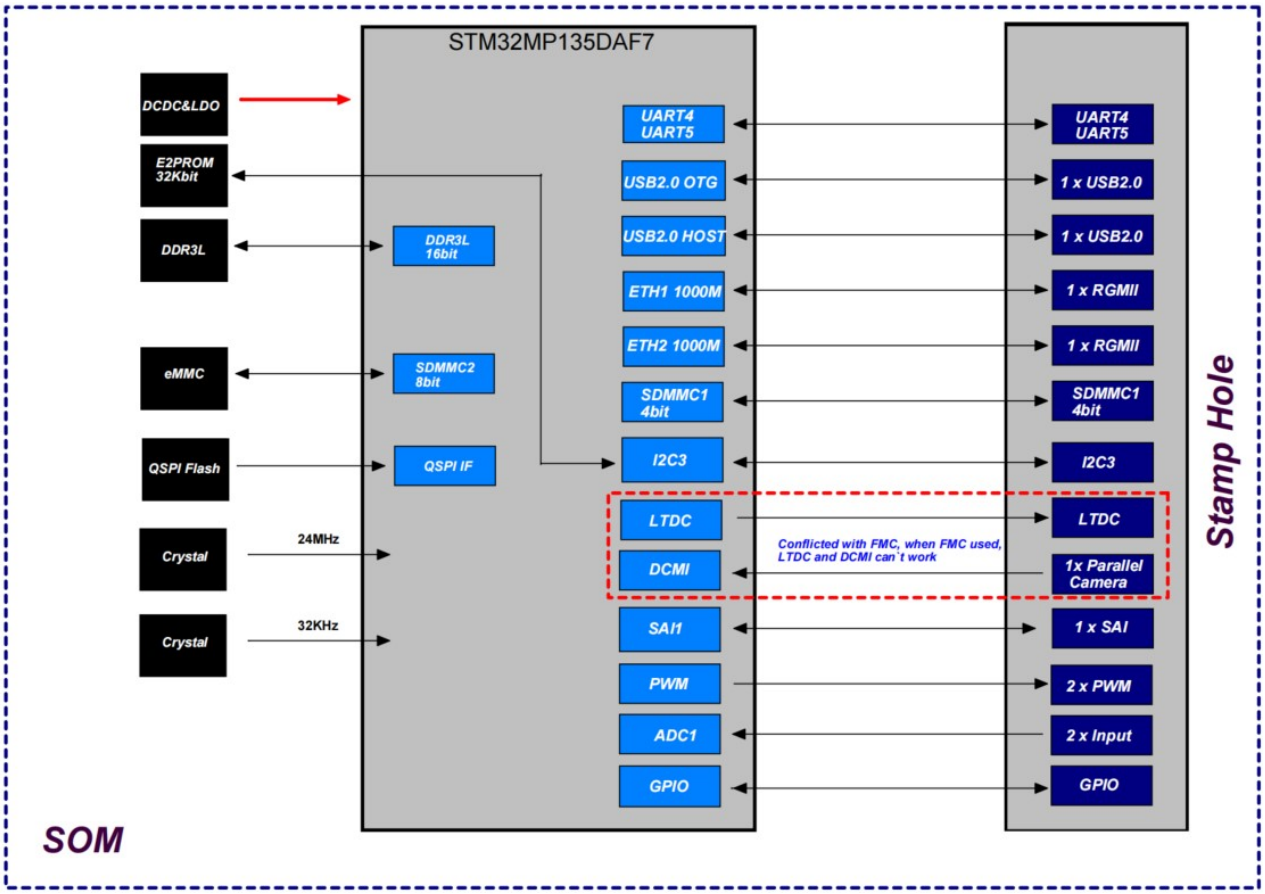


**Figure 2-2 Core board block diagram**

## 2.4. Core Board Ordering Information

The MYC-YF13X series core board contains 2 standard product models: the customer can choose the appropriate model according to the demand. For the batch requirements, MYIR provides customized services, you can choose the core board parameters.

| Part No. / Item | MYC-YF135-256N256D-100-I | MYC-YF135-4E512D-100-I |
|---|---|---|
| **CPU** | STM32MP135DAF7 | STM32MP135DAF7 |
| **CPU series** | STM32MP13X | STM32MP13X |
| **DDR** | 256MB DDR3L | 512MB DDR3L |
| **Memorizer** | 256MB Nand Flash | 4GB eMMC |
| **Core** | Single-nuclear Cortex-A7 | Single-nuclear Cortex-A7 |
| **Frequency** | 1 GHz | 1 GHz |
| **System** | Linux 5.15 | Linux 5.15 |
| **Power Supply** | +5V | +5V |
| **Mechanical size** | 37mmx 39mm | 37mmx 39mm |
| **Operating temperature** | -40℃ - +85℃ | -40℃ - +85℃ |
| **Connector** | Stamp hole 148 PIN | Stamp hole 148 PIN |
| **Certification** | CE<br>ROHS | CE<br>ROHS |
| **Camera** | DCMI X 1 | DCMI X 1 |
| **RGB** | Support capacitive screen | Support capacitive screen<br>Support four-wire resistance screen (need additi onal touch chip) |
| **Audio** | I2S | I2S |
| **SD/MMC** | 1 | 1 |
| **USB** | USB 2.0 OTG Type C x 1<br>USB 2.0 HOST Type A x 1 | USB 2.0 OTG Type C x 1<br>USB 2.0 HOST Type A x 1 |
| **Ethernet** | RGMII x2 | RGMIIx2 |
| **UART** | 8 | 8 |
| **I2C** | 5 | 5 |

| | | |
|---|---|---|
| **CAN** | 2 | 2 |
| **QSPI** | 2 | 2 |
| **SPI** | 5 | 5 |
| **ADC** | 6 | 6 |
| **SWD** | 1 | 1 |

**Table 2-3 MYC-YF13X core board ordering information**

***Note:*** *The blue background represents the interface type supported by the core module; the gray background represents others.*

# 3. Pin Description

## 3.1. Pin Out

STM32MP135 The core board is welded on the bottom board in the form of SMD patch, and the pin is a stamp hole design.

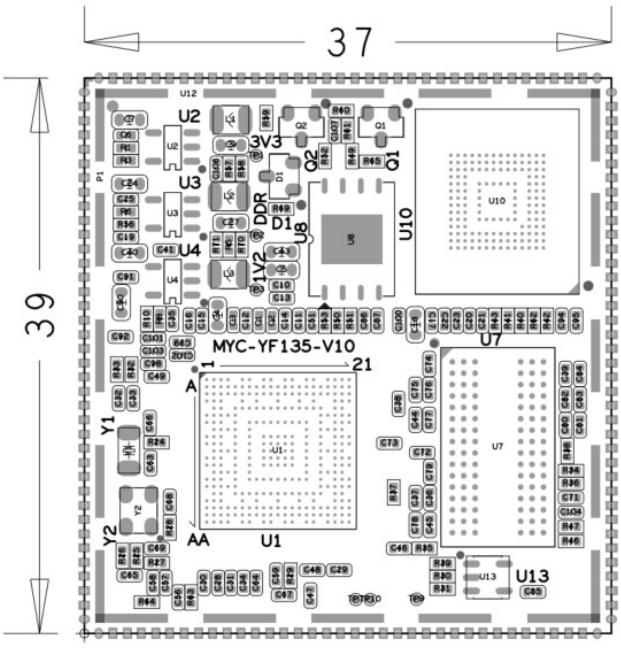


**Figure 3-1 Mechanical Structure of MYC-YF13X Core board (Unit: mm)**

## 3.2. Pin List

The interface pin of the MYC-YF13X core board is defined as shown in the following table. The pin functions of the BSP development package are configured according to the "default function" in the following table. If you need to change the default function of the pin, please modify the relevant driver configuration code, otherwise there will be uncertain exceptions such as driver conflict.

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 1 | GND | | | | 0V | | |
| | 2 | DCMIPP_D0 | PA9 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 3 | DCMIPP_D4 | PE13 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 4 | DCMIPP_D1 | PD0 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 5 | DCMIPP_D5 | PD3 | DCMI | Data Center Manageability Interface | 3.3V | I | |

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 6 | DCMIPP_D7 | PE9 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 7 | DCMIPP_D2 | PH14 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 8 | DCMIPP_D6 | PB8 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 9 | DCMIPP_D3 | PE4 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 10 | DCMIPP_PIXCLK | PB7 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 11 | DCMIPP_VS | PG9 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 12 | DCMIPP_HS | PH8 | DCMI | GPIO | 3.3V | I | |
| | 13 | GND | | | | 0V | | |
| | 14 | VSOM_5V | | | | 5V | I | |
| | 15 | VSOM_5V | | | | 5V | I | |
| | 16 | VDD_3V3 | | | | 3.3V | O | |
| | 17 | VBAT | | | | 3.3V | I | |
| | 18 | GND | | | | 0V | | |
| | 19 | GND | | | | 0V | | |
| | 20 | ETH2_MDIO | PB6 | ETH2 | ETH2 MDIO data | 3.3V | I/0 | |
| | 21 | ETH2_MDC | PG5 | ETH2 | ETH2 MDIO clock | 3.3V | I | |
| | 22 | ETH2_TXCTL | PF6 | ETH2 | ETH2 Data transmit control bit | 3.3V | I | |
| | 23 | ETH2_TXD3 | PE6 | ETH2 | ETH2 Data transmit 3 | 3.3V | O | |
| | 24 | ETH2_TXD2 | PG1 | ETH2 | ETH2 Data transmit 2 | 3.3V | O | |
| | 25 | ETH2_TXD1 | PG11 | ETH2 | ETH2 Data transmit 1 | 3.3V | O | |
| | 26 | ETH2_TXD0 | PF7 | ETH2 | ETH2 Data transmit 0 | 3.3V | O | |
| | 27 | GND | | | | 0V | | |
| | 28 | ETH2_TXC | PG3 | ETH2 | ETH2 Send clock | 3.3V | O | |
| | 29 | GND | | | | 0V | | |
| | 30 | ETH2_RXCTL | PA12 | ETH2 | ETH2 Data reception control bit | 3.3V | I | |
| | 31 | ETH2_RXC | PH11 | ETH2 | ETH2 Receive clock | 3.3V | I | |
| | 32 | ETH2_RXD2 | PH6 | ETH2 | ETH2 Data Receive 2 | 3.3V | I | |
| | 33 | ETH2_RXD3 | PA8 | ETH2 | ETH2 Data Receive 3 | 3.3V | I | |
| | 34 | ETH2_RXD0 | PF4 | ETH2 | ETH2 Data Receive 0 | 3.3V | I | |
| | 35 | ETH2_RXD1 | PE2 | ETH2 | ETH2 Data Receive 1 | 3.3V | I | |
| | 36 | GND | | | | 0V | | |
| | 37 | ETH2_CLK125 | PH2 | ETH2 | ETH2 CLK | 3.3V | I | |
| | 38 | GND | | | | 0V | | |
| | 39 | GND | | | | 0V | | |
| | 40 | SPI5_SCK | PG10 | SPI5 | SPI5 clock | 3.3V | I | |

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 41 | SPI5_MOSI | PH12 | SPI5 | SPI5 data in | 3.3V | I | |
| | 42 | SPI5_MISO | PG8 | SPI5 | SPI5 data out | 3.3V | O | |
| | 43 | GND | | | | 0V | | |
| | 44 | ETH1_CLK125 | PF12 | SPI5 | ETH1 CLK | 3.3V | I | |
| | 45 | GND | | | | 0V | | |
| | 46 | ETH1_MDC | PG2 | ETH1 | ETH1 MDIO clock | 3.3V | I | |
| | 47 | ETH1_MDIO | PA2 | ETH1 | ETH1 MDIO data | 3.3V | I/0 | |
| | 48 | ETH1_RXC | PA1 | ETH1 | ETH1 Receive clock | 3.3V | I | |
| | 49 | ETH1_RXD2 | PB0 | ETH1 | ETH1 Data Receive 2 | 3.3V | I | |
| | 50 | ETH1_RXD1 | PC5 | ETH1 | ETH1 Data Receive 1 | 3.3V | I | |
| | 51 | ETH1_RXD3 | PB1 | ETH1 | ETH1 Data Receive 3 | 3.3V | I | |
| | 52 | ETH1_RXCTL | PA7 | ETH1 | ETH1 Data reception control bit | 3.3V | I | |
| | 53 | ETH1_RXD0 | PC4 | ETH1 | ETH1 Data Receive 0 | 3.3V | I | |
| | 54 | GND | | | | 0V | | |
| | 55 | ETH1_TXC | PC1 | ETH1 | ETH1 Send clock | 3.3V | O | |
| | 56 | GND | | | | 0V | | |
| | 57 | ETH1_TXD1 | PG14 | ETH1 | ETH1 Data transmit 1 | 3.3V | O | |
| | 58 | ETH1_TXD2 | PC2 | ETH1 | ETH1 Data transmit 2 | 3.3V | O | |
| | 59 | ETH1_TXD0 | PG13 | ETH1 | ETH1 Data transmit 0 | 3.3V | O | |
| | 60 | ETH1_TXCTL | PB11 | ETH1 | ETH1 Data transmit control bit | 3.3V | O | |
| | 61 | ETH1_TXD3 | PE5 | ETH1 | ETH1 Data transmit 3 | 3.3V | O | |
| | 62 | | | | | | | |
| | 63 | GND | | | | 0V | | |
| | 64 | UART4_RX | PD8 | UART4 | UART4 Data receive | 3.3V | I | |
| | 65 | UART4_TX | PD6 | UART4 | UART4 Data transmit | 3.3V | O | |
| | 66 | UART5_RX | PF13 | UART5 | UART5 Data receive | 3.3V | I | |
| | 67 | UART5_TX | PA0 | UART5 | UART5 Data transmit | 3.3V | O | |
| | 68 | GND | | | | 0V | | |
| | 69 | USB_D2_P | USB_DP2 | USB2 | USB2 Data+ | 3.3V | I/0 | |
| | 70 | USB_D2_N | USB_DM2 | USB2 | USB2 Data- | 3.3V | I/0 | |
| | 71 | GND | | | | 0V | | |
| | 72 | USB_D1_P | USB_DP1 | USB1 | USB1 Data+ | 3.3V | I/0 | |
| | 73 | USB_D1_N | USB_DM1 | USB1 | USB1 Data- | 3.3V | I/0 | |
| | 74 | GND | | | | 0V | | |
| | 75 | GND | | | | 0V | | |
| | 76 | I2S1_MCLK | PC0 | I2S1 | I2S Main clock | 3.3V | I | |
| | 77 | I2S1_SDI | PA6 | I2S1 | I2S data input | 3.3V | I | |

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 78 | I2S1_SDO | PA3 | I2S1 | I2S data output | 3.3V | O | |
| | 79 | I2S1_CK | PC3 | I2S1 | I2S clock | 3.3V | I | |
| | 80 | I2S1_WS | PA4 | I2S1 | I2S SELECT | 3.3V | I | |
| | 81 | SWCLK | PF14 | SW | SWD | 3.3V | I | |
| | 82 | SWDIO | PF15 | SW | SWD | 3.3V | I/0 | |
| | 83 | BOOT2 | PI6 | BOOT2 | Boot configuration bit 2 | 3.3V | O | |
| | 84 | BOOT1 | PI5 | BOOT1 | Boot configuration bit 1 | 3.3V | O | |
| | 85 | BOOT0 | PI4 | BOOT0 | Boot configuration bit 0 | 3.3V | O | |
| | 86 | GND | | | | 0V | | |
| | 87 | PI1 | PI1 | GPIO | GPIO | 3.3V | O | |
| | 88 | NRST | NRST | NRST | NRST | 3.3V | O | |
| | 89 | PWM2 | PA11 | PWM2 | Pulse Width Modulation 2 | 3.3V | O | |
| | 90 | PWM1 | PA10 | PWM1 | Pulse Width Modulation 1 | 3.3V | O | |
| | 91 | ADC1_INP8 | PF11 | ADC1 | ADC1 channel 8 | 3.3V | I | |
| | 92 | ADC1_INP2 | PA5 | ADC1 | ADC1 channel 2 | 3.3V | I | |
| | 93 | I2C3_SCL | PH3 | I2C3 | IIC3 bus clock | 3.3V | I | |
| | 94 | I2C3_SDA | PH7 | I2C3 | IIC3 bus data | 3.3V | I/0 | |
| | 95 | FDCAN2_TX | PB13 | CAN2 | CAN1 data transmit | 3.3V | I | |
| | 96 | FDCAN2_RX | PB5 | CAN2 | CAN1 data receive | 3.3V | O | |
| | 97 | PI7 | PI7 | GPIO | GPIO | 3.3V | I/0 | |
| | 98 | PH4 | PH4 | GPIO | GPIO | 3.3V | I/0 | |
| | 99 | PH5 | PH5 | GPIO | GPIO | 3.3V | I/0 | |
| | 100 | GND | | | | 0V | | |
| | 101 | PB10 | PB10 | GPIO | GPIO | 3.3V | I/0 | |
| | 102 | PI3 | PI3 | GPIO | GPIO | 3.3V | I/0 | |
| | 103 | PI2 | PI2 | GPIO | GPIO | 3.3V | I/0 | |
| | 104 | PC13 | PC13 | GPIO | GPIO | 3.3V | I/0 | |
| | 105 | PE10 | PE10 | GPIO | GPIO | 3.3V | I/0 | |
| | 106 | PE8 | PE8 | GPIO | GPIO | 3.3V | I/0 | |
| | 107 | PI0 | PI0 | GPIO | GPIO | 3.3V | I/0 | |
| | 108 | PA13 | PA13 | GPIO | GPIO | 3.3V | I/0 | |
| | 109 | PG12 | PG12 | GPIO | GPIO | 3.3V | I/0 | |
| | 110 | PD12 | PD12 | GPIO | GPIO | 3.3V | I/0 | |
| | 111 | | | | | | | |
| | 112 | GND | | | | 0V | | |
| | 113 | SDMMC1_D0 | PC8 | SD | SD1 data 0 | 3.3V | I/0 | |
| | 114 | SDMMC1_CMD | PD2 | SD | SD1 CMD | 3.3V | I/0 | |
| | 115 | SDMMC1_D1 | PC9 | SD | SD1 data 1 | 3.3V | I/0 | |
| | 116 | SDMMC1_D3 | PC11 | SD | SD1 data 3 | 3.3V | I/0 | |
| | 117 | SDMMC1_D2 | PC10 | SD | SD1 data 2 | 3.3V | I/0 | |
| | 118 | SDMMC1_CK | PC12 | SD | SD1 clock | 3.3V | I | |
| | 119 | GND | | | | 0V | | |



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| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 120 | LTDC_CLK | PD9 | RGB | RGB | 3.3V | I | |
| | 121 | LTDC_DE | PH9 | RGB | RGB | 3.3V | I | |
| | 122 | LTDC_HS | PE1 | RGB | RGB | 3.3V | I | |
| | 123 | LTDC_VS | PG4 | RGB | RGB | 3.3V | I | |
| | 124 | LTDC_R2 | PH10 | RGB | RGB | 3.3V | I | |
| | 125 | LTDC_R3 | PB12 | RGB | RGB | 3.3V | I | |
| | 126 | LTDC_R7 | PD11 | RGB | RGB | 3.3V | I | |
| | 127 | LTDC_R0 | PE11 | RGB | RGB | 3.3V | I | |
| | 128 | LTDC_R1 | PG7 | RGB | RGB | 3.3V | I | |
| | 129 | LTDC_R6 | PD4 | RGB | RGB | 3.3V | I | |
| | 130 | LTDC_R4 | PD14 | RGB | RGB | 3.3V | I | |
| | 131 | LTDC_R5 | PF5 | RGB | RGB | 3.3V | I | |
| | 132 | LTDC_G3 | PF3 | RGB | RGB | 3.3V | I | |
| | 133 | LTDC_G2 | PH13 | RGB | RGB | 3.3V | I | |
| | 134 | LTDC_G4 | PF2 | RGB | RGB | 3.3V | I | |
| | 135 | LTDC_G1 | PF1 | RGB | RGB | 3.3V | I | |
| | 136 | LTDC_G5 | PG0 | RGB | RGB | 3.3V | I | |
| | 137 | LTDC_G7 | PA15 | RGB | RGB | 3.3V | I | |
| | 138 | LTDC_G6 | PE12 | RGB | RGB | 3.3V | I | |
| | 139 | LTDC_G0 | PE14 | RGB | RGB | 3.3V | I | |
| | 140 | LTDC_B0 | PD5 | RGB | RGB | 3.3V | I | |
| | 141 | LTDC_B7 | PE15 | RGB | RGB | 3.3V | I | |
| | 142 | LTDC_B3 | PE7 | RGB | RGB | 3.3V | I | |
| | 143 | LTDC_B2 | PD10 | RGB | RGB | 3.3V | I | |
| | 144 | LTDC_B5 | PD15 | RGB | RGB | 3.3V | I | |
| | 145 | LTDC_B4 | PG15 | RGB | RGB | 3.3V | I | |
| | 146 | LTDC_B1 | PE0 | RGB | RGB | 3.3V | I | |
| | 147 | LTDC_B6 | PD1 | RGB | RGB | 3.3V | I | |
| | 148 | GND | | | | 0V | | |

**Table 3-1 MYC-YF13X Core board PIN LIST**

# 4. Electrical Characteristics

## 4.1. Primary System Power (VDD_5V)

The main power supply for the MYC-YF13X core board is VDD _ 5 V, corresponding to the PIN 14-17 pin of the SMD pad in the stamp hole. In order to ensure normal operation, the bottom board must provide a voltage of 5V ± 5%, 1A current, and ensure that the output capacity of the power supply circuit can meet the power consumption of the core board. The power consumption and current of the core board are listed in this section. Please reserve the appropriate allowance for the design of the power supply circuit.

| Name | Description | Recommended Voltage |
|---|---|---|
| VDD_5V | Main supply voltage, 5V input, 1A | 5V |
| VDD_3V3 | 3.3V output,1A | 3.3V |

**Table 4-1 External input / output voltage**

## 4.2. Power Consumption

| Conditon | Voltage(V) | Average Current(A) | Power Consumption (W) |
|---|---|---|---|
| no-load | 5V | 0.1 | 0.50 |
| Full-load | 5V | 0.20 | 1.00 |
| Mem Hibernation state | 5V | 0.02 | 0.1 |
| Freeze Hibernation state | The software does not support the Freeze sleep mode | The software does not support the Freeze sleep mode | The software does not support the Freeze sleep mode |

**Table 4-2 Power consumption parameters**

## 4.3. GPIO DC Parameters

| Parameter | Symbol | Min | Typical | Max | Units | description |
|---|---|---|---|---|---|---|
| High-lever DC output voltage | $V_{OH\ (1.8V)}$ | 1.4 | — | 1.8 | V | |
| | $V_{OH\ (3.3V)}$ | 2.8 | — | 3.3 | V | |
| Low-lever DC output voltage | $V_{OL\ (1.8V)}$ | — | — | 0.4 | V | |
| | $V_{OL\ (3.3V)}$ | 0 | — | 0.4 | V | |
| High-lever DC input voltage | $V_{I\ H\ (1.8V)}$ | 1.17 | — | 2.1 | V | |
| | $V_{IH(3.3V)}$ | 2 | — | 3.6 | V | |
| Low-lever DC input voltage | $V_{IL(1.8V)}$ | -0.3 | — | 0.36 | V | |
| | $V_{I\ L\ (3.3V)}$ | -0.3 | — | 0.63 | V | |

**Table 4-3 GPIO DC Parameters**

# 5. System Start-up Configuration

The MYC-YF13X core board supports the following startup sources: UART and USB download, EMMC startup, NAND FLASH startup, and Micro SD startup. At startup, the boot source used by the internal BootROM is selected by the BOOT Pin and OTP bytes.

The MYC-YF13X core board has pulled down BOOT0, BOOT1 and BOOT2 inside the CPU.

## 5.1. Start-up Configuration

| BOOT[2:1:0] | Boot Device | Remarks |
|---|---|---|
| 000 | UART and USB | Download image |
| 010 | eMMC | Boot from eMMC |
| 011 | Nand Flash | Boot from Nand Flash |
| 101 | SD Card | Boot from Micro SD |
| 111 | QSPI Nand Flash | BOOT from QSPI Nand Flash |

**Table 5-1 Start mode configuration**

# 6. Interfaces

## 6.1. SD

The MYC-YF13X core board is equipped with a 1-channel SD / MMC interface to design the communication interface between modules with SDIO interface.

### 6.1.1. Pin Description

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| - | 113 | SDMMC1_D0 | PC8 | SD | SD data 0 | 3.3V | I/O | |
| | 114 | SDMMC1_CMD | PD2 | SD | SD command | 3.3V | I | |
| | 115 | SDMMC1_D1 | PC9 | SD | SD data 1 | 3.3V | I/O | |
| | 116 | SDMMC1_D3 | PC11 | SD | SD data 3 | 3.3V | I/O | |
| | 117 | SDMMC1_D2 | PC10 | SD | SD data 2 | 3.3V | I/O | |
| | 118 | SDMMC1_CK | PC12 | SD | SD clock | 3.3V | I/O | |

**Table 6-1 SD PIN description**

## 6.2. UART

The MYC-YF13X core board has up to 8 channels. The core board is configured with 2 serial ports by default.

### 6.2.1. Pin Description

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| - | 64 | UART4_RX | PD8 | UART4 | UART 4 Data receive | 3.3V | I | |
| | 65 | UART4_TX | PD6 | UART4 | UART 4 Data transmit | 3.3V | O | |
| | 66 | UART5_RX | PF13 | UART5 | UART 5 Data receive | 3.3V | I | |
| | 67 | UART5_TX | PA0 | UART5 | UART 5 Data transmit | 3.3V | O | |

**Table 6-2 UART PIN description**



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## 6.3. USB

The MYC-YF13X core board provides two high-speed USB2.0. USB1 is used for HOST and USB2 is used for OTG.

### 6.3.1. Pin Description

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| - | 69 | USB_DP2 | AA13 | USB2 | USB 2 Data+ | 3.3V | I/0 | |
| | 70 | USB_DM2 | Y13 | USB2 | USB 2 Data - | 3.3V | I/0 | |
| | 72 | USB_DP1 | Y16 | USB1 | USB1 Data+ | 3.3V | I/0 | |
| | 73 | USB_DM1 | AA16 | USB1 | USB 1 Data - | 3.3V | I/0 | |

**Table 6-3 USB PIN description**

## 6.4. Ethernet

A 2-way RGMII signal was elicited in the MYC-YF13X core board. When the user designs the floor circuit, design the Ethernet PHY circuit, transformer isolation circuit and RJ 45 part circuit. The CPU Ethernet interface supports three modes: MII / RMII / RGMII.

### 6.4.1. Pin Description

| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 20 | ETH2_MDIO | PB6 | ETH2 | ETH2 MDIO data | 3.3V | I/0 | |
| | 21 | ETH2_MDC | PG5 | ETH2 | ETH2 MDIO clock | 3.3V | I | |
| | 22 | ETH2_TXCTL | PF6 | ETH2 | ETH2 Data transmit control bit | 3.3V | O | |
| | 23 | ETH2_TXD3 | PE6 | ETH2 | ETH2 Data transmit 3 | 3.3V | O | |
| | 24 | ETH2_TXD2 | PG1 | ETH2 | ETH2 Data transmit 2 | 3.3V | O | |
| | 25 | ETH2_TXD1 | PG11 | ETH2 | ETH2 Data transmit 1 | 3.3V | O | |
| | 26 | ETH2_TXD0 | PF7 | ETH2 | ETH2 Data transmit 0 | 3.3V | O | |
| | 28 | ETH2_TXC | PG3 | ETH2 | ETH2 Send clock | 3.3V | O | |
| | 30 | ETH2_RXCTL | PA12 | ETH2 | ETH2 Data reception control bit | 3.3V | I | |
| | 31 | ETH2_RXC | PH11 | ETH2 | ETH2 Receive clock | 3.3V | I | |
| | 32 | ETH2_RXD2 | PH6 | ETH2 | ETH2 Data Receive 2 | 3.3V | I | |
| | 33 | ETH2_RXD3 | PA8 | ETH2 | ETH2 Data Receive 3 | 3.3V | I | |
| | 34 | ETH2_RXD0 | PF4 | ETH2 | ETH2 Data Receive 0 | 3.3V | I | |
| | 35 | ETH2_RXD1 | PE2 | ETH2 | ETH2 Data Receive 1 | 3.3V | I | |
| | 37 | ETH2_CLK125 | PH2 | ETH2 | ETH2 CLK | 3.3V | I | |
| | 44 | ETH1_CLK125 | PF12 | SPI5 | ETH1 CLK | 3.3V | I | |



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| | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 46 | ETH1_MDC | PG2 | ETH1 | ETH1 MDIO clock | 3.3V | I | |
| | 47 | ETH1_MDIO | PA2 | ETH1 | ETH1 MDIO data | 3.3V | I/0 | |
| | 48 | ETH1_RXC | PA1 | ETH1 | ETH1 Receive clock | 3.3V | I | |
| | 49 | ETH1_RXD2 | PB0 | ETH1 | ETH1 Data Receive 2 | 3.3V | I | |
| | 50 | ETH1_RXD1 | PC5 | ETH1 | ETH1 Data Receive 1 | 3.3V | I | |
| | 51 | ETH1_RXD3 | PB1 | ETH1 | ETH1 Data Receive 3 | 3.3V | I | |
| | 52 | ETH1_RXCTL | PA7 | ETH1 | ETH1 Data reception control bit | 3.3V | I | |
| | 53 | ETH1_RXD0 | PC4 | ETH1 | ETH1 Data Receive 0 | 3.3V | I | |
| | 55 | ETH1_TXC | PC1 | ETH1 | ETH1 Send clock | 3.3V | O | |
| | 57 | ETH1_TXD1 | PG14 | ETH1 | ETH1 Data transmit 1 | 3.3V | O | |
| | 58 | ETH1_TXD2 | PC2 | ETH1 | ETH1 Data transmit 2 | 3.3V | O | |
| | 59 | ETH1_TXD0 | PG13 | ETH1 | ETH1 Data transmit 0 | 3.3V | O | |
| | 60 | ETH1_TXCTL | PB11 | ETH1 | ETH1 Data transmit control bit | 3.3V | O | |
| | 61 | ETH1_TXD3 | PE5 | ETH1 | ETH1 Data transmit 3 | 3.3V | O | |

**Table 6-4 Ethernet PIN description**

## 6.5. LCD

The MYC-YF13X core board supports 1-channel RGB display output interface, and the reference screen is 7-inch capacitive touch LCD screen MY-TFT070CV2, link: https://www.myirtech.com/list.asp?id=477

### 6.5.1. Pin Description

| item | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| — | 120 | LTDC_CLK | PD9 | GPIO | RGB | 3.3V | I | |
| | 121 | LTDC_DE | PH9 | GPIO | RGB | 3.3V | I | |
| | 122 | LTDC_HS | PE1 | GPIO | RGB | 3.3V | I | |
| | 123 | LTDC_VS | PG4 | GPIO | RGB | 3.3V | I | |
| | 124 | LTDC_R2 | PH10 | GPIO | RGB | 3.3V | I | |
| | 125 | LTDC_R3 | PB12 | GPIO | RGB | 3.3V | I | |
| | 126 | LTDC_R7 | PD11 | GPIO | RGB | 3.3V | I | |
| | 127 | LTDC_R0 | PE11 | GPIO | RGB | 3.3V | I | |
| | 128 | LTDC_R1 | PG7 | GPIO | RGB | 3.3V | I | |
| | 129 | LTDC_R6 | PD4 | GPIO | RGB | 3.3V | I | |
| | 130 | LTDC_R4 | PD14 | GPIO | RGB | 3.3V | I | |

| item | pin | grade | MPU | Default function | Default feature description | electrical level | IO | remarks |
|---|---|---|---|---|---|---|---|---|
| | 131 | LTDC_R5 | PF5 | GPIO | RGB | 3.3V | I | |
| | 132 | LTDC_G3 | PF3 | GPIO | RGB | 3.3V | I | |
| | 133 | LTDC_G2 | PH13 | GPIO | RGB | 3.3V | I | |
| | 134 | LTDC_G4 | PF2 | GPIO | RGB | 3.3V | I | |
| | 135 | LTDC_G1 | PF1 | GPIO | RGB | 3.3V | I | |
| | 136 | LTDC_G5 | PG0 | GPIO | RGB | 3.3V | I | |
| | 137 | LTDC_G7 | PA15 | GPIO | RGB | 3.3V | I | |
| | 138 | LTDC_G6 | PE12 | GPIO | RGB | 3.3V | I | |
| | 139 | LTDC_G0 | PE14 | GPIO | RGB | 3.3V | I | |
| | 140 | LTDC_B0 | PD5 | GPIO | RGB | 3.3V | I | |
| | 141 | LTDC_B7 | PE15 | GPIO | RGB | 3.3V | I | |
| | 142 | LTDC_B3 | PE7 | GPIO | RGB | 3.3V | I | |
| | 143 | LTDC_B2 | PD10 | GPIO | RGB | 3.3V | I | |
| | 144 | LTDC_B5 | PD15 | GPIO | RGB | 3.3V | I | |
| | 145 | LTDC_B4 | PG15 | GPIO | RGB | 3.3V | I | |
| | 146 | LTDC_B1 | PE0 | GPIO | RGB | 3.3V | I | |
| | 147 | LTDC_B6 | PD1 | GPIO | RGB | 3.3V | I | |

**Table 6-5 LCD PIN description**

## 6.6. SPI

The MYC-YF13X core board supports a maximum 5-channel SPI controller and supports primary / slave modes. SPI signals include SPI _ CLK, SPI _ MOSI and SPI _ MISO. First, confirm the relationship between primary and slave devices, and then confirm the direction of MOSI and MISO signals. Due to the pin multiplexing relationship, the core board has the SPI 5 interface configured by default. If you want to use more SPI interfaces, check the chip manual and modify the pin configuration in the driver.

### 6.6.1. Pin Description

| item | pin | grade | MPU | Default function | Default feature description | electrical level | IO | remarks |
|---|---|---|---|---|---|---|---|---|
| - | 40 | SPI5_SCK | PG10 | SPI5 | SPI5 clock | 3.3V | I | |
| | 41 | SPI5_MOSI | PH12 | SPI5 | SPI5 data in | 3.3V | O | |
| | 42 | SPI5_MISO | PG8 | SPI5 | SPI5 data out | 3.3V | O | |

**Table 6-6 SPI PIN description**

## 6.7. I2S

MYC-YF13X core board supports 4-channel I2S. At present, the core board leads to the first road I2S1.

### 6.7.1. Pin Description

| item | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| – | 76 | I2S1_MCLK | PC0 | I2S1 | I2S Main clock | 3.3V | I | |
| | 77 | I2S1_SDI | PA6 | I2S1 | I2S data input | 3.3V | I | |
| | 78 | I2S1_SDO | PA3 | I2S1 | I2S data output | 3.3V | O | |
| | 79 | I2S1_CK | PC3 | I2S1 | I2S clock | 3.3V | I | |
| | 80 | I2S1_WS | PA4 | I2S1 | I2S SELECT | 3.3V | I | |

**Table 6-7 I2S PIN description**

## 6.8. DCMI

The MYC-YF13X core board leads to a digital camera interface, which can be externally connected to a 16-bit parallel camera interface, and you can buy the corresponding camera module for testing (suitable for module MY-CAM011B (OV2659)).Link: https://www.myirtech.com/list.asp?id=534

### 6.8.1. Pin Description

| item | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| – | 2 | DCMIPP_D0 | PA9 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 3 | DCMIPP_D4 | PE13 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 4 | DCMIPP_D1 | PD0 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 5 | DCMIPP_D5 | PD3 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 6 | DCMIPP_D7 | PE9 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 7 | DCMIPP_D2 | PH14 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 8 | DCMIPP_D6 | PB8 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 9 | DCMIPP_D3 | PE4 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 10 | DCMIPP_PIXCLK | PB7 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 11 | DCMIPP_VS | PG9 | DCMI | Data Center Manageability Interface | 3.3V | I | |
| | 12 | DCMIPP_HS | PH8 | DCMI | Data Center Manageability Interface | 3.3V | I | |

**Table 6-8 DCMI PIN description**

## 6.9. MISC

The MYC-YF13X core board is connected to a series of MISC interfaces as follows.

### 6.9.1. Pin Description

| item | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 81 | SWCLK | PF14 | SW | SWD | 3.3V | I | |
| | 82 | SWDIO | PF15 | SW | SWD | 3.3V | I/0 | |
| | 83 | BOOT2 | PI6 | BOOT2 | Boot configuration bit 2 | 3.3V | O | |
| | 84 | BOOT1 | PI5 | BOOT1 | Boot configuration bit 1 | 3.3V | O | |
| | 85 | BOOT0 | PI4 | BOOT0 | Boot configuration bit 0 | 3.3V | O | |
| | 87 | PI1 | PI1 | GPIO | GPIO | 3.3V | O | |
| | 88 | NRST | Y11 | NRST | NRST | 3.3V | O | |
| - | 89 | PWM2 | PA11 | PWM2 | Pulse Width Modulation 2 | 3.3V | I | |
| | 90 | PWM1 | PA10 | PWM1 | Pulse Width Modulation 1 | 3.3V | I | |
| | 91 | ADC1_INP8 | PF11 | ADC1 | ADC channel 1 | 3.3V | O | |
| | 92 | ADC1_INP2 | PA5 | ADC1 | ADC channel 1 | 3.3V | O | |
| | 93 | I2C3_SCL | PH3 | I2C3 | IIC2 bus clock | 3.3V | I | |
| | 94 | I2C3_SDA | PH7 | I2C3 | IIC2 bus data | 3.3V | I/0 | |
| | 95 | FDCAN2_TX | PB13 | CAN2 | CAN1 data transmit | 3.3V | I | |
| | 96 | FDCAN2_RX | PB5 | CAN2 | CAN1 data receive | 3.3V | O | |

**Table 6-9 MISC PIN description**

## 6.10. GPIO

The MYC-YF13X core board introduces some GPIO pins that are not defined by the cust omer according to the chip manual.

### 6.10.1. Pin Description

| item | Pin | Signal | MPU Pin | Default Function | Description | Voltage | IO | Comments |
|---|---|---|---|---|---|---|---|---|
| | 101 | PB10 | PB10 | GPIO | GPIO | 3.3V | I/0 | |
| | 102 | PI3 | PI3 | GPIO | GPIO | 3.3V | I/0 | |
| | 103 | PI2 | PI2 | GPIO | GPIO | 3.3V | I/0 | |
| | 104 | PC13 | PC13 | GPIO | GPIO | 3.3V | I/0 | |
| | 105 | PE10 | PE10 | GPIO | GPIO | 3.3V | I/0 | |
| - | 106 | PE8 | PE8 | GPIO | GPIO | 3.3V | I/0 | |
| | 107 | PI0 | PI0 | GPIO | GPIO | 3.3V | I/0 | |
| | 108 | PA13 | PA13 | GPIO | GPIO | 3.3V | I/0 | |
| | 109 | PG12 | PG12 | GPIO | GPIO | 3.3V | I/0 | |
| | 110 | PD12 | PD12 | GPIO | GPIO | 3.3V | I/0 | |

**Table 6-10 GPIO PIN description**

# 7. Package Information

## 7.1. Package Dimensions

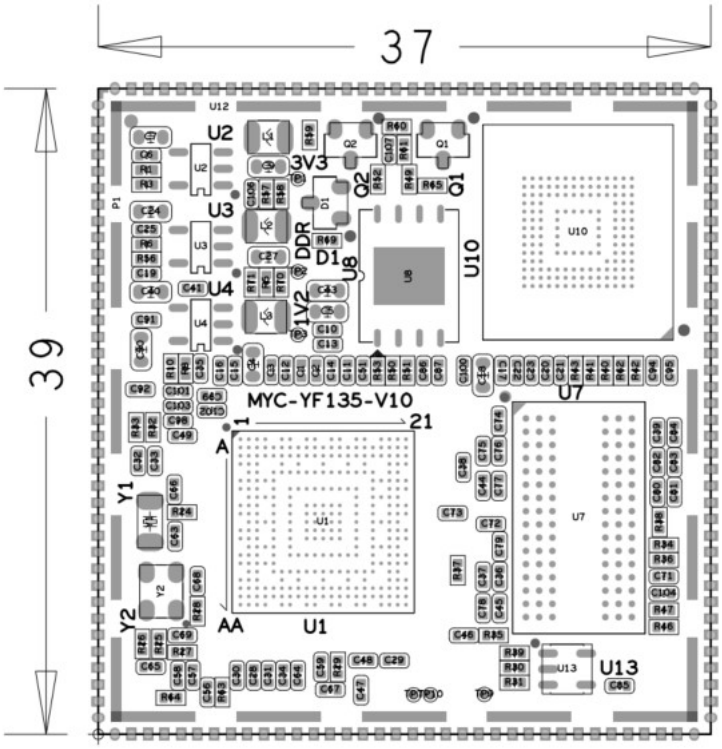


**Figure 7-1 MYC-YF135X Top View**

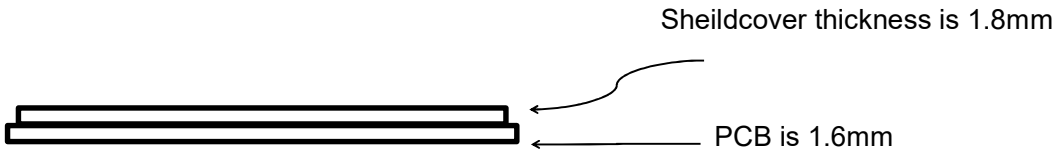


**Figure 7-2 MYC-YF135X Side View**



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## 7.2. Carrier Board PCB Design

a) PCB thickness is recommended to be at least 1.6mm. Pay attention to the balance of c opper coating. If PCB deformation occurs in the over furnace, it is recommended to use a carrier to fix the over furnace.

b) To ensure the quality of mounting and tinning, please ensure that the distance between the PCB module and other components is at least 3mm.

c) Please design the package of the core board module according to Section 7.2, or use t he PCB package provided by MYIR Electronics.

# 8. Mount and storage requirements

## 8.1. Steel mesh design

1) It is recommended to open holes at a ratio of 1:1 for the circular pad with a thickness of 0.15mm tin; With a thickness of 0.18mm, the opening ratio is 1:0.8.

2) The requirements for the opening of the stamp hole welding plate steel mesh are suggested to shrink the inside of the plate by 10%, expand the outside by 20%, and the thickness is 0.18mm step.

## 8.2. Storage requirement

Modules are shipped in vacuum sealed form, and the following conditions are required for storage:

1) The vacuum-sealed bag can be stored for 12 months when the ambient temperature is lower than 40℃ and the air humidity is less than 90%.

2) After opening the vacuum sealing bag, reflow welding can be carried out directly within 72 hours when the ambient temperature is lower than 30℃ and the air humidity is less than 10%.

Note: If the above conditions are not met, baking should be carried out before applying.

## 8.3. Baking method

Because the module packaging material cannot withstand high temperature, if necessary, please choose one of the following two methods to bake, to avoid affecting the welding quality of the module.

1) Baking in the original package: baking temperature is 40 ~ 60℃ and time is 5 ~ 7 days.

2) Transfer to high temperature resistant dish baking: baking temperature is 100 ~ 120, baking time is more than 48 hours.

## 8.4. Welding technology

1) If the plate to be mounted is double-sided device layout, it is recommended to put the core plate mounting process in the last stage.

2) It is recommended to set the preheating time of 160 ~ 200℃ to 60 ~ 120 seconds.

3) It is recommended that the temperature of reflow welding should be 235 ~ 245℃, and the maximum temperature should not exceed 250℃, and the reflow time should be controlled within 40 ~ 60 seconds.

4) The recommended temperature rise rate is 1-3 ℃/ s, and the temperature drop rate is 2-4 ℃/ s.

# Appendix A

## Warranty & Technical Support Services

**MYIR Electronics Limited** is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

### Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

### Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

### Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

### Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

### After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

### Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;

- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

## After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

## Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

## Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service

but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

## Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

## Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

## Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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