

Product Overview

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050 device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps, and it can support at least 110 CAN nodes. The NSi1050 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000V_{rms} Insulation voltage
- Power supply voltage
VDD1: 2.5V to 5.5V
VDD2: 4.5V to 5.5V
- Bus fault protection of -40V to +40V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Date rate: up to 1Mbps
- High CMTI: 80kV/us
- Low loop delay: <200ns
- High system level EMC performance:
Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
WB SOIC-16
DUB-8



Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Functional Block Diagrams

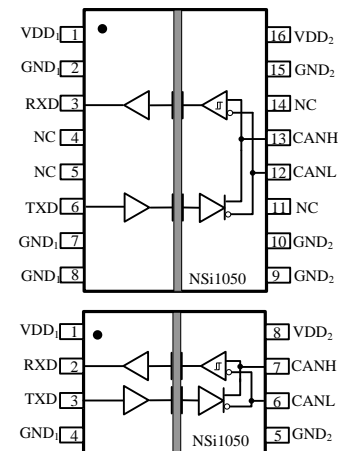


Figure 1. NSi1050 Block Diagram

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD ₁ VDD ₂	-0.5		6.5	V	
Maximum Input Voltage	V _{TXD}	-0.4		VDD ₁ +0.4	V	
Maximum BUS Pin Voltage	V _{CANH} , V _{CANL}	-40		+40	V	
Common-Mode Transients	CMTI	±80		±100	kV/us	
Output current	I _o	-15		15	mA	
Maximum Surge Isolation Voltage	V _{IOSM}			8	kV	
Operating Temperature	T _{opr}	-40		125	°C	
Storage Temperature	T _{stg}	-40		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

2.0 SPECIFICATIONS

2.1. ELECTRICAL CHARACTERISTICS

(VDD₁=2.5V~5.5V, VDD₂=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD₁ = 5V, VDD₂ = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDD ₁	2.5		5.5	V	
	VDD ₂	4.5	5	5.5	V	
Logic side supply current	IDD ₁		1.95		mA	VDD ₁ =3.3V
			2.01		mA	VDD ₁ =5V
Bus side supply current	IDD ₂		46	70	mA	VI=0V, R _{Load} =60Ω
			4.49	10	mA	VI=VDD ₂ ,
Thermal-Shutdown Threshold	T _{TS}	155	165	180	°C	
Common Mode Transient Immunity	CMTI	±100		±150	kV/us	
Logic Side						
High level input voltage	V _{IH}	2			V	TXD pin
Low level input voltage	V _{IL}			0.8	V	TXD pin

High level input current	I _{IH}			10	uA	TXD pin
Low level input current	I _{IL}	-10			uA	TXD pin
Output Voltage High	V _{OH}	VDD ₁ -0.4			V	I _{OH} = -4mA, RXD pin
Output Voltage Low	V _{OL}			0.4	V	I _{OL} = 4mA, RXD pin
Input Capacitance	C _{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	V _{OH(D)}	2.9	3.03	4.5	V	V _I =0V, R _{Load} =60Ω
CANL output voltage (Dominant)	V _{OL(D)}	0.8	1.5	2	V	V _I =0V, R _{Load} =60Ω
CAN bus output voltage (Recessive)	V _{O(R)}	2	2.5	3	V	V _I =3V, R _{Load} =60Ω
Differential output voltage(Dominant)	V _{OD(D)}	1.5	1.53	3	V	V _I =3V, R _{Load} =60Ω
Differential output voltage(Recessive)	V _{OD(R)}	-0.012		0.012	V	V _I =3V, R _{Load} =60 Ω , see Figure x
		-0.5		0.05	V	V _I =3V, NO Load
Common-mode output voltage	V _{OC}	2	2.5	3	V	
Peak-to-peak Common-mode output voltage	V _{OC(PP)}		30		mV	
Short- circuit output current	I _{OS}	-105	-22		mA	CANH=-12V, CANL open, see Figure x
			0.28	1	mA	CANH=12V, CANL open, see Figure x
		-1	-0.44		mA	CANL=-12V, CANH open, see Figure x
			21	105	mA	CANL=12V, CANH open, see Figure x
Receiver						
Positive-going bus input threshold voltage	V _{IT+}		800	900	mV	
Negative-going bus input threshold voltage	V _{IT-}	500	650		mV	
Hysteresis voltage	V _{HYS}	100	125		mV	
Power-off bus input current	I _(OFF)			5	uA	
Input capacitance to ground	C _I		13		pF	CANH or CANL

Differential input	C _{ID}		5		pF	
Differential input resistance	R _{ID}	30		80	kΩ	V _I =3V
Input resistance	R _{IN}	15	30	40	kΩ	
Input resistance matching	R _{I_{match}}	-3		+3	%	CANH=CANL
Common-mode voltage range	V _{COM}	-12		+12	V	

2.2. SWITCHING ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T _{loop1}	100	165	200	ns	Driver input to receiver output, Recessive to Dominant
Loop delay2	T _{loop2}	100	125	200	ns	Driver input to receiver output, Dominant to Recessive
Driver						
Propagation delay time, recessive -to- dominant output	t _{PLH}	45	37	140	ns	
Propagation delay time, dominant -to- recessive output	t _{PHL}	45	82	110	ns	
Differential output signal rise time	t _r		42		ns	
Differential output signal fall time	t _f		24		ns	
Bus dominant time-out time	t _{TXD.DTO}	300	468	700	us	See Figure x
Receiver						
Propagation delay time, low-to-high-level output	t _{PLH}	80	100	150	ns	
Propagation delay time, high-to-low-level output	t _{PHL}	65	94	110	ns	
RXD signal rise time	t _r		3		ns	
RXD signal fall time	t _f		3		ns	
Fail-Safe output delay time from bus-side power loss	t _{fs}	6			us	VDD ₁ =5V

2.3. TYPICAL PERFORMANCE CHARACTERISTICS

2.4. PARAMETER MEASUREMENT INFORMATION

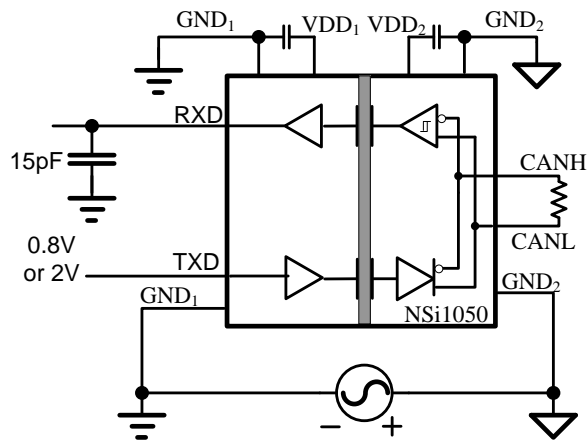


Figure 2.8 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value		Unit	Comments
		DUB-8	SOIC-16		
Minimum External Air Gap (Clearance)	L(I01)	6.5	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	6.5	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II			

3.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARATERISTICS

Description	Test Condition	Symbol	Value		Unit
			DUB-8	SOIC-16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	I to IV	

For Rated Mains Voltage $\leq 300V_{rms}$			I to III	I to III	
For Rated Mains Voltage $\leq 400V_{rms}$			I to III	I to III	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		VIORM	560	1100	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	840	1650	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	1320	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	1320	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	VIOTM	4242	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, $V_{TEST} = V_{IOSM} \times 1.3$	VIOSM	5384	5384	Vpeak
Isolation resistance	$V_{IO} = 500V$	RIO	$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	CIO	0.8	0.8	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25°C		Ps	1.5	1.5	W
Safety input, output, or supply current	$\theta_{JA} = 72^\circ C/W$, $V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	Is	310		mA
Safety input, output, or supply current	$\theta_{JA} = 84^\circ C/W$, $V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	Is		299	mA
Case Temperature		Ts	150	150	°C

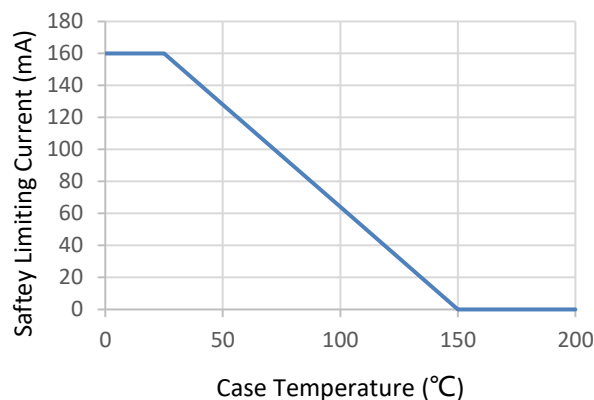


Figure 3.1 NSi1050-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.3. REGULATORY INFORMATION

The NSi1050-DBBR is approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01 ²	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V _{rms} Isolation voltage	Single Protection, 3000V _{rms} Isolation voltage	Basic Insulation 560V _{peak} , V _{IOSM} =5384V _{peak}	Basic insulation at 400V _{rms} (1103V _{peak})
File (pending)	File (pending)	File (pending)	File (pending)

¹ In accordance with UL 1577, each NSi1050-DBBR is proof tested by applying an insulation test voltage ≥ 3600 V_{rms} for 1 sec.

² In accordance with DIN VDE V 0884-11, each NSi1050-DBBR is proof tested by applying an insulation test voltage ≥ 840 V_{peak} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

The NSi1050-DSWR is approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01 ²	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Basic Insulation 1103V _{peak} , V _{IOSM} =5384V _{peak}	Basic insulation at 780V _{rms} (1103V _{peak})
File (pending)	File (pending)	File (pending)	File (pending)

¹ In accordance with UL 1577, each NSi1050-DSWR is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 sec.

² In accordance with DIN VDE V 0884-11, each NSi1050-DSWR is proof tested by applying an insulation test voltage ≥ 1320 V_{peak} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

4.0 FUNCTION DESCRIPTION

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050W device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while the NSi1050U device is safety certified by UL1577 support 3kV_{rms} insulation withstand voltages. The NSi1050 is providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps, and it can support at least 110 CAN nodes. The NSi1050 provides thermal protection and transmit data dominant time out function.

4.1. DEVICE FUNCTIONAL MODES

Table x. Driver Function Table

TXD	CANH	CANL	BUS STATE
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

¹ H= high level; L=low level; Z= high impedance

Table x. Receiver Function Table

V _{ID} =CANH-CANL	RXD	BUS STATE
V _{ID} ≥ 0.9V	L	Dominant
0.5 < V _{ID} < 0.9V	X	Uncertain
V _{ID} ≤ 0.5V	H	Recessive
Open	H	Recessive

¹ H= high level; L=low level; X= uncertain

4.2. TXD DOMINANT TIME-OUT FUNCTION

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

4.3. CURRENT PROTECTION

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

4.4. OVER TEMPERATURE PROTECTION

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

5.0 APPLICATION NOTE

5.1. TYPICAL APPLICATION

The NSi1050 requires a 0.1 μF bypass capacitors between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. The figure5.1 is the basic schematic of NSi1050.

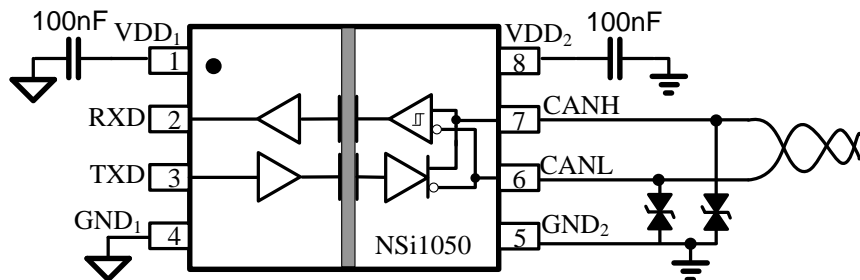


Figure5.1 Basic schematic of NSi1050

5.2. PCB LAYOUT

The recommended PCB layout shown below.

Figure5.1 Recommended PCB Layout — Top Layer

Figure5.2 Recommended PCB Layout — Bottom Layer

6.0 PACKAGE INFORMATION

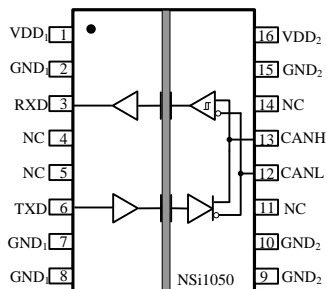


Figure 6.1 NSi1050W Package

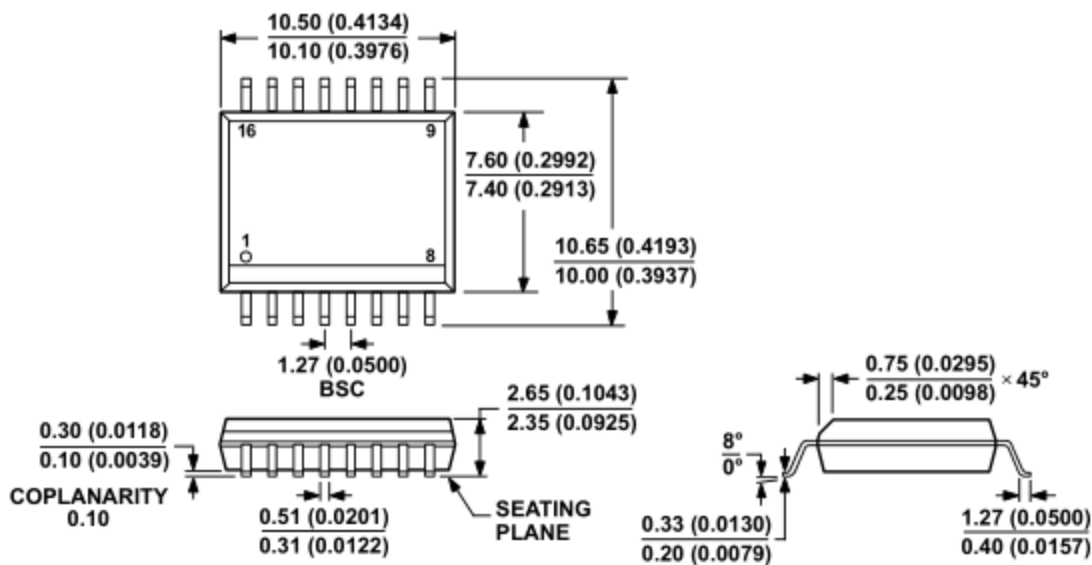


Figure 6.2 WB SOIC-16 Package Shape and Dimension in millimeters (inches)

Table6.1 NSi1050-DSWR Pin Configuration and Description

NSi1050- DSWR PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	GND1	Ground 1, the ground reference for Isolator Side 1
8	GND1	Ground 1, the ground reference for Isolator Side 1
9	GND2	Ground 2, the ground reference for Isolator Bus Side
10	GND2	Ground 2, the ground reference for Isolator Bus Side
11	NC	No Connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND2	Ground 2, the ground reference for Isolator Bus Side
16	VDD ₂	Power supply for Bus Side

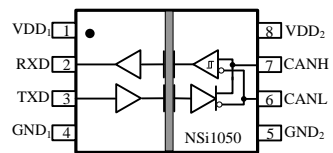
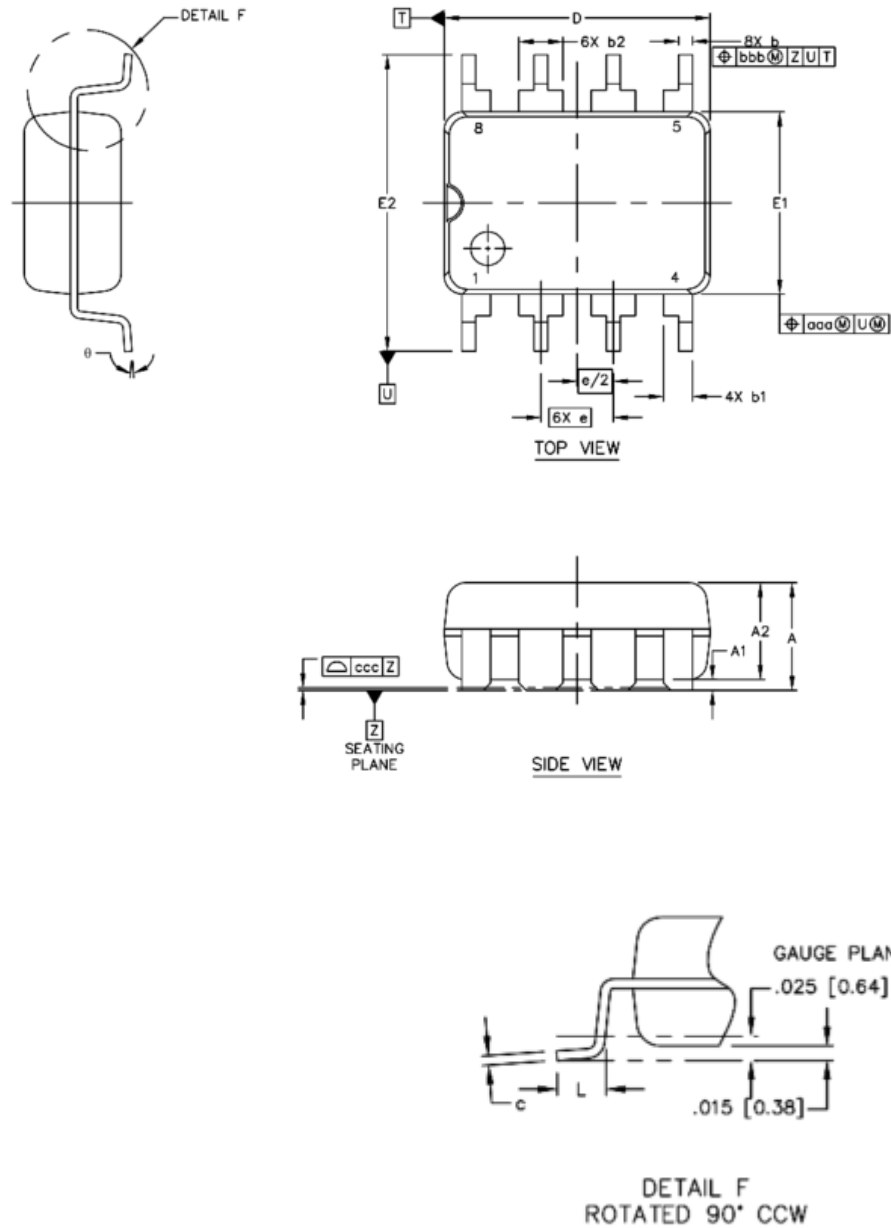


Figure 6.3 NSi1050U Package

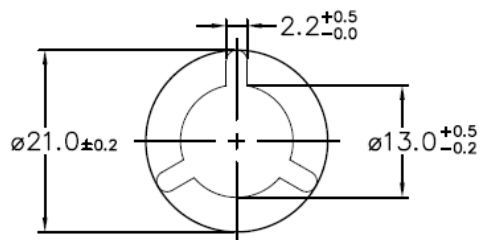
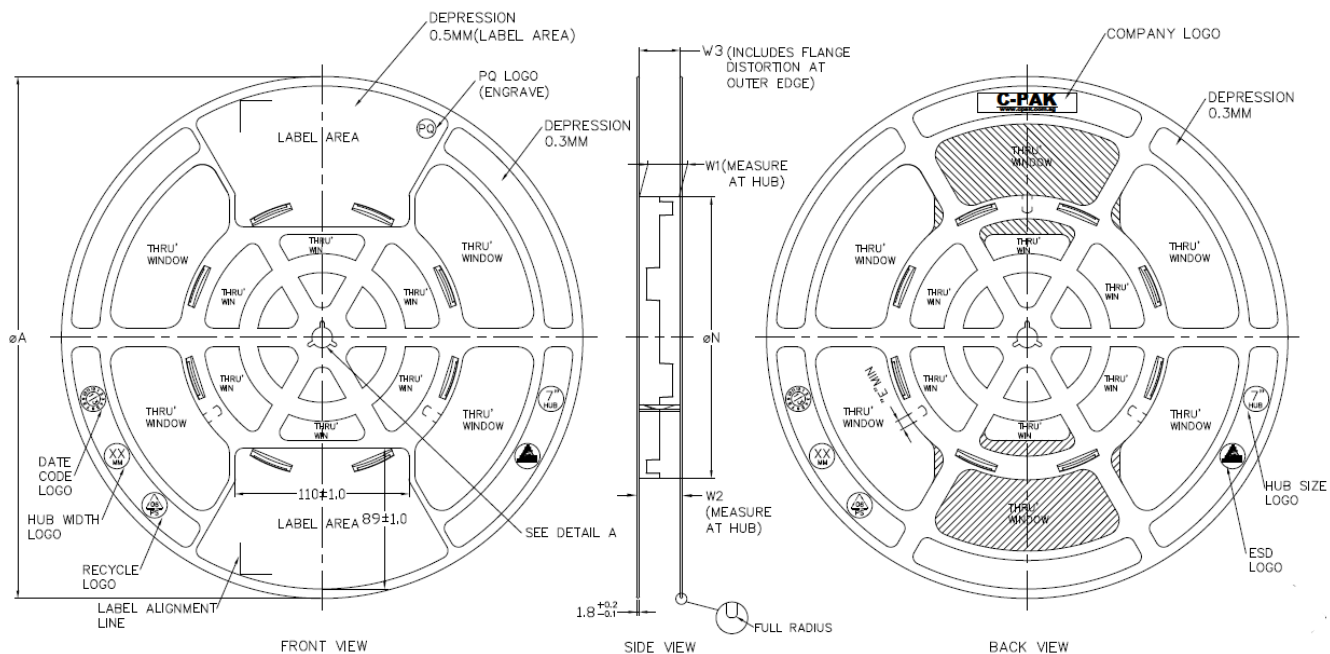


	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	.191	---	---	4.85
STAND OFF	A1	.015	---	---	0.38	---	---
MOLD THICKNESS	A2	.126	---	.142	3.20	---	3.61
LEAD WIDTH	b	.014	---	.022	0.36	---	0.56
	b1	---	0.039 REF	---	---	0.99 REF	---
	b2	---	0.06 REF	---	---	1.524 REF	---
L/F THICKNESS	c	.008	---	.014	0.20	---	0.36
BODY SIZE	D	.365	---	.369	9.27	---	9.37
	E1	.244	---	.260	6.20	---	6.60
	E	.398	---	.421	10.11	---	10.69
LEAD PITCH	e	.100 BSC			2.54 BSC		
LEAD LENGTH	L	.0453	---	.0571	1.15	---	1.45
	θ	0°	---	8°	0°	---	8°
LEAD OFFSET	aaa	.010			0.254		

Table6.2 NSi1050-DDBR Pin Configuration and Description

NSi1050-DDBR PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Side 1
2	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD ₂	Power supply for Bus Side

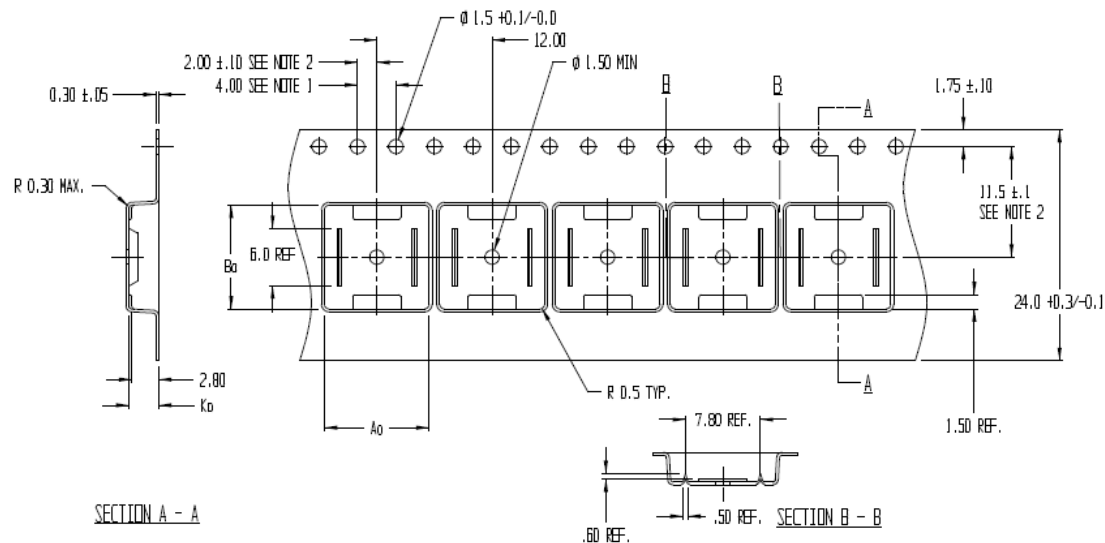
7.0 TAPE AND REEL INFORMATION



ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 ^{+0.5} _{-0.5}	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ^{+2.0} _{-0.5}	18.4		5.5
16MM	330	178	16.4 ^{+2.0} _{-0.5}	22.4		5.5
24MM	330	178	24.4 ^{+2.0} _{-0.5}	30.4		5.5
32MM	330	178	32.4 ^{+2.0} _{-0.5}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ¹²	ANTISTATIC	ALL TYPES
B	10 ⁸ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁵ & BELOW 10 ⁵	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 ⁸ TO 10 ¹¹	ANTISTATIC (COATED)	ALL TYPES



NOTES:

1. TO SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. A_0 AND B_0 ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

$A_0 = 10.90$
 $B_0 = 10.80$
 $K_0 = 3.1$

Figure 7.1 Tape and Reel Information of WB SOIC-16

8.0 ORDER INFORMATION

Part No.	Isolation Rating(kV)	Max Data Rate (Mbps)	MSL	Temperature	Automotive	Package
NSi1050-DDBR	3	1	MSL3	-40 to 125°C	NO	DUB-8
NSi1050-DSWR	5	1	MSL2	-40 to 125°C	NO	SOIC-16

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

9.0 REVISION HISTORY

Revision	Description	Date
0.0	Original	2019/9/15