

# MYC-YM62X Product Manual



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**MYIR Electronics Limited**

# History

Version	Author	Participants	Date	Description
V1.0	MYIR		20230825	Official release



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# 1. Overview

AM62x is a new generation of high-performance and ultra-efficient processor in the field of intelligent industrial control. TI AM62x Integrated ARM Cortex-A53 high-performance CPU and ARM Cortex-M4F real-time CPU, including 3 D GPU graphics accelerator (AM625X only), support dual-screen display, support 1080P HD display. Support OpenGL 3.x/2.0/1.1, Vulkan 1.2 graphics acceleration engine. TI AM62x The processor has rich interfaces UARTx9, CAN-FDx 3, I2Cx 6, SPIx 4, GPMC, dual-channel DPI + LVDS, the highest 2K, ETHx2, OSPI, CSI, USB2.0x2, etc.

MYIR Electronics has launched a new series of core panels: MYC-YM62X. MYC-YM62X has a good software development environment, and the kernel supports the open source operating system Linux. The processor is a dual-core Cortex-A53 processor designed for industrial HMI, medical, industrial automation, power, graphics and control terminals. It has high cost performance and is suitable for entry-level Linux embedded ARM applications. At the same time, the built-in EMMC, DDR 4, PMIC chip and other integrated circuits can simplify the hardware design and shorten the research and development cycle..

Product introduction link: <https://www.myirtech.com/list.asp?id=730>

Download link: <http://d.myirtech.com/MYD-YM62X/>





Figure 1-1 MYC-YM62X Core board

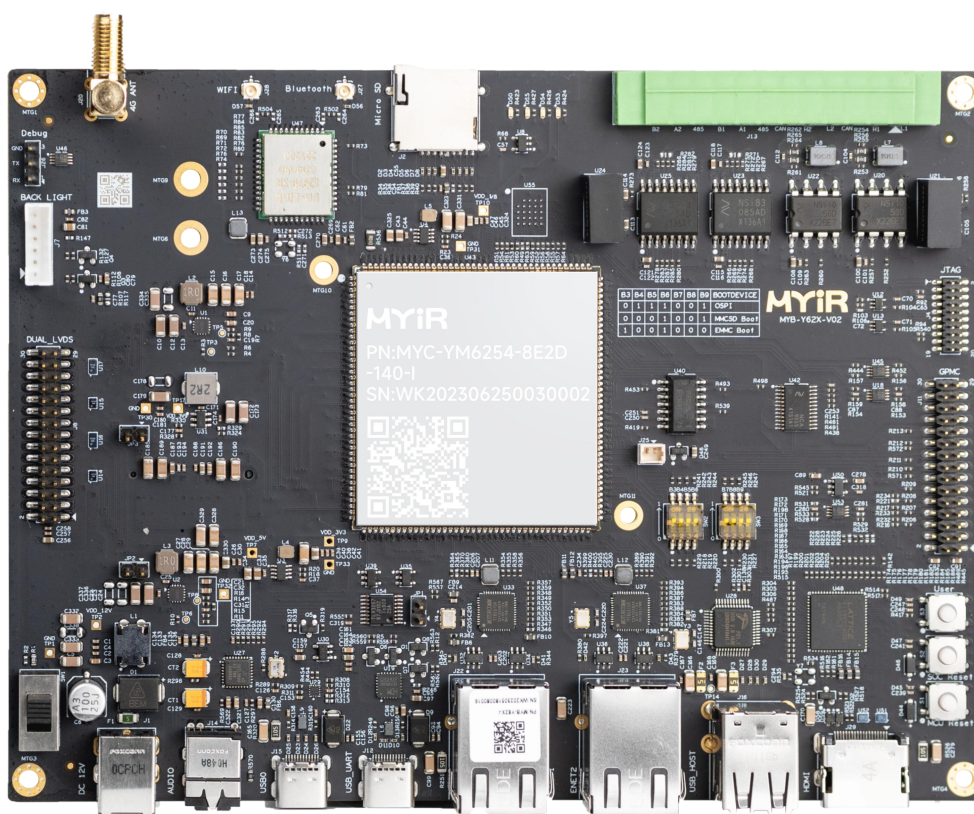


Figure 1-2 MYC-YM62X Kit



## 2. Product introduction

MYC-YM62X core board adopts high density and high speed circuit board design, and integrates AM62x、DDR4、eMMC、E2PROM、PMIC , discrete power supply and other circuits on the 43mm\*45mm board card.

MYC-YM62X series core board includes three standard product models: they have some differences in storage configuration, customers can choose the appropriate model according to their needs. For details about the differences between product models, see Section 2.4.

### 2.1. CPU Introduction

The TI AM62x integrates a Cortex-A53 and Cortex-M4F CPU to provide efficient computing power and is designed for intelligent control and human-machine interface in areas such as automotive and industrial applications.

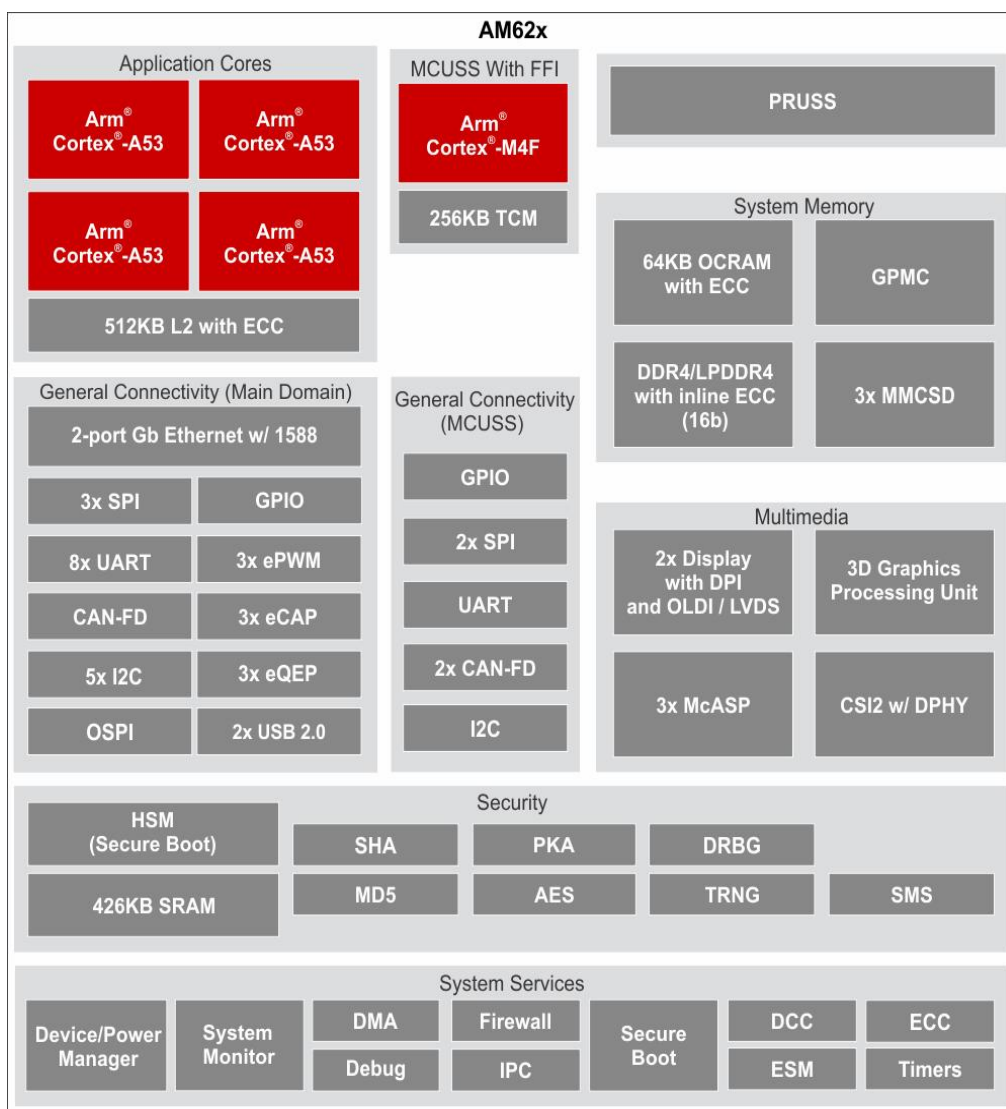


Figure 2-1 TI AM62x Resource block diagram





resource	Description
CPU	<ul style="list-style-type: none"> <li>● Quad-core Cortex-A53 cluster with 512KB L2 shared cache with SECDED ECC</li> <li>● Each A53 Core has 32KB L1 DCache with SECDED ECC and 32KB L1 I Cache with Parity protection</li> <li>● Single-core Arm® Cortex®-M4F MCU at up to 400 MHz</li> <li>● 256KB SRAM with SECDED ECC Dedicated Device and Power Manager</li> </ul>
Multi Media	<ul style="list-style-type: none"> <li>● Display subsystem</li> <li>● 3D Graphics Processing Unit</li> <li>● One Camera Serial interface (CSI-Rx) - 4 Lane with DPHY</li> </ul>
Memory Subsystem	<ul style="list-style-type: none"> <li>● Up to 816KB of On-chip RAM</li> <li>● DDR Subsystem (DDRSS)</li> </ul>
Functional Safety	<ul style="list-style-type: none"> <li>● Functional Safety-Compliant targeted [Industrial]</li> <li>● Functional Safety-Compliant targeted [Automotive]</li> <li>● AEC-Q100 qualified</li> </ul>
Security	<ul style="list-style-type: none"> <li>●</li> <li>● Hardware Security Module</li> <li>● Secure boot supported</li> <li>● Cryptographic acceleration supported</li> <li>● Debugging security</li> <li>● Trusted Execution Environment (TEE) supported</li> <li>● Secure storage support</li> <li>● On-the-Fly encryption support for OSPI interface in XIP mode</li> <li>●</li> </ul>
PRU Subsystem	<ul style="list-style-type: none"> <li>● Dual-core Programmable Real-Time Unit running up to 333 MHz and Industrial Communication Subsystem (PRU-ICSS)</li> <li>● Intended for driving GPIO for cycle accurate protocols</li> <li>● 16KByte program memory per PRU with SECDED ECC</li> <li>● 8KB data memory per PRU with SECDED ECC</li> <li>● 32KB general purpose memory with SECDED ECC</li> <li>● CRC32/16 HW accelerator</li> <li>● Scratch PAD memory with 3 banks of 30 x 32-bit registers 1 Industrial 64-bit timer with 9 capture and 16 compare events, along with slow and fast compensation</li> </ul>





	<ul style="list-style-type: none"> <li>● 1 interrupt controller (INTC), minimum of 64 input events supported</li> <li>●</li> </ul>
High-Speed Interfaces	<ul style="list-style-type: none"> <li>●</li> <li>● Integrated Ethernet switch supporting (total 2 external ports)</li> <li>● Two USB2.0 Ports</li> </ul>
Media and Data Storage	<ul style="list-style-type: none"> <li>● 3x Secure Digital® (SD®) (4b+4b+8b) interface</li> <li>● 1× General-Purpose Memory Controller (GPMC) up to 133 MHz</li> <li>● OSPI/QSPI with 166-MHz DDR / 200-MHz SDR</li> <li>●</li> </ul>
General Connectivity	<ul style="list-style-type: none"> <li>● 9x Universal Asynchronous Receiver-Transmitters (UART)</li> <li>● 5x Serial Peripheral Interface (SPI) controllers</li> <li>● 6x Inter-Integrated Circuit (I2C) ports</li> <li>● 3x Multichannel Audio Serial Ports (McASP)</li> <li>● 3x enhanced PWM modules (ePWM)</li> <li>● 3x enhanced Quadrature Encoder Pulse modules (eQEP)</li> <li>● 3x enhanced Capture modules (eCAP)</li> <li>● General-Purpose I/O (GPIO), All LVCMOS I/O can be configured as GPIO</li> <li>● 3x Controller Area Network (CAN) modules with CAN-FD support</li> </ul>
Technology / Package	<ul style="list-style-type: none"> <li>● 16-nm technology</li> <li>● 13 mm x 13 mm, 0.5-mm pitch, 425-pin FCCSP BGA (ALW)</li> </ul>

**Table 2-1 TI AM62x resources**

Refer to the chip manual for details.



## 2.2. Core Board Features

Item	Features
CPU series	AM62x
CPU Chip type	AM6254, AM6252, AM6231
DDR storage	Single DDR4, standard with 1GB / 2GB
eMMC	EMMC: 8GB (other capacity optional) EEPROM: 32KB
CPU Processor	AM6254, 4*Cortex-A53@1.4GHz+Cortex-M4F@400MHz AM6252, 2*Cortex-A53@1.4GHz+Cortex-M4F@400MHz AM6231, 1*Cortex-A53@1GHz+Cortex-M4F@400MHz
Core board size	43mm x 45mm
Interface type	Stamp hole+LGA, 222PIN
PCB board specifications	10 layer plate design, gold sinking process production

**Table 2-2 Core board features**



## 2.3. Block Diagram

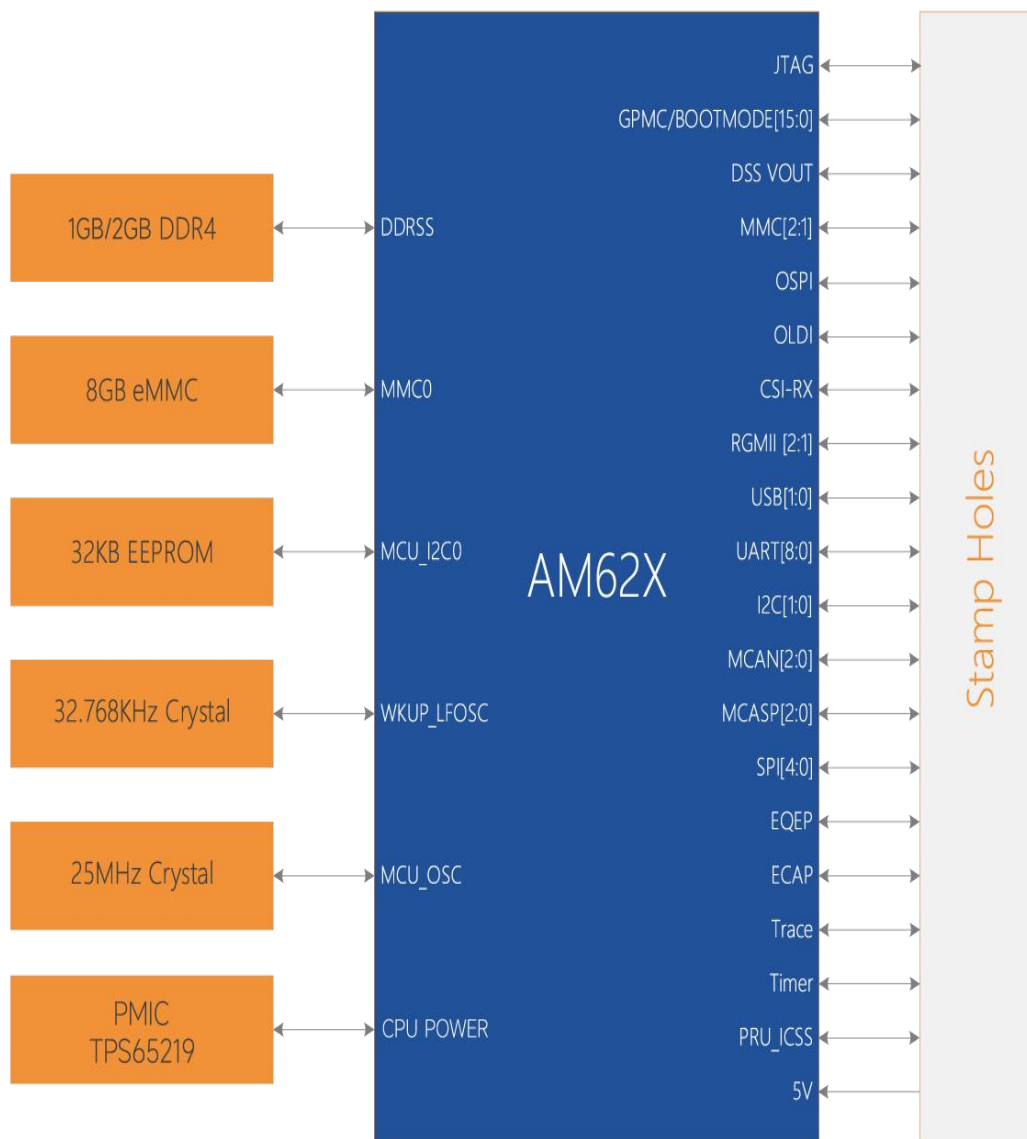


Figure 2-2 Core board block diagram



## 2.4. Core Board Ordering Information

MYC-YM62X series core board includes 3 standard product models: they have some differences in operating temperature parameters, customers can choose the appropriate model according to their needs. For batch requirements, MYIR provides customized services, you can choose the core board parameters.

Part Item	MYC-YM6254-8E2D-140-I	MYC-YM6252-8E1D-140-I	MYC-YM6231-8E1D-100-I
CPU	AM6254ATCGGAALW	AM6252ATCGGAALW	AM6231ASGGGAALW
CPU series	AM62x	AM62x	AM62x
DDR	2GB	1GB	1GB
eMMC	8GB eMMC	8GB eMMC	8GB eMMC
Core	4*Cortex-A53	2*Cortex-A53	1*Cortex-A53
Frequency	1.4GHz	1.4GHz	1GHz
Video output	2*LVDS 1*RGB	2*LVDS 1*RGB	2*LVDS 1*RGB
Audio	3*MCASP	3*MCASP	3*MCASP
Parallel CSI	1* MIPI CSI	1* MIPI CSI	1* MIPI CSI
uSDHC	2	2	2
USB	2*USB2.0	2*USB2.0	2*USB2.0
Ethernet	2* RGMII	2* RGMII	2* RGMII
UART	9*URAT	9*URAT	9*URAT
CAN	3*CAN FD	3*CAN FD	3*CAN FD
SPI	5*SPI	5*SPI	5*SPI
I2C	6*I2C	6*I2C	6*I2C
GPMC	1*GPMC	1*GPMC	1*GPMC
JTAG	1*JTAG	1*JTAG	1*JTAG
System	Linux 6.1.33, Ubuntu 22.04	Linux 6.1.33 , Ubuntu 22.04	Linux 6.1.33, Ubuntu 22.04
Power Supply	+5V	+5V	+5V



Mechanical size	43mmx45mm	43mmx45mm	43mmx45mm
Operating temperature	-40°C-85°C	-40°C-85°C	-40°C-85°C
Connector	Stamp hole+LGA, 222PIN	Stamp hole+LGA, 222PIN	Stamp hole+LGA, 222PIN
Certification	CE ROHS	CE ROHS	CE ROHS

**Table 2-3 MYC-YM62X core board ordering information**

*Note: The blue background represents the interface type supported by the core board module; The gray background represents the others. The selection table is the maximum resource extracted from the core board, and there may be a reuse relationship.*



## 3. Pin Description

### 3.1. Pin Out

The MYC-YM62X core board is soldered to the bottom plate in the form of an SMD patch and the pins are stamp holes. For the package design of baseboard, refer to the instructions in Section 7.2.

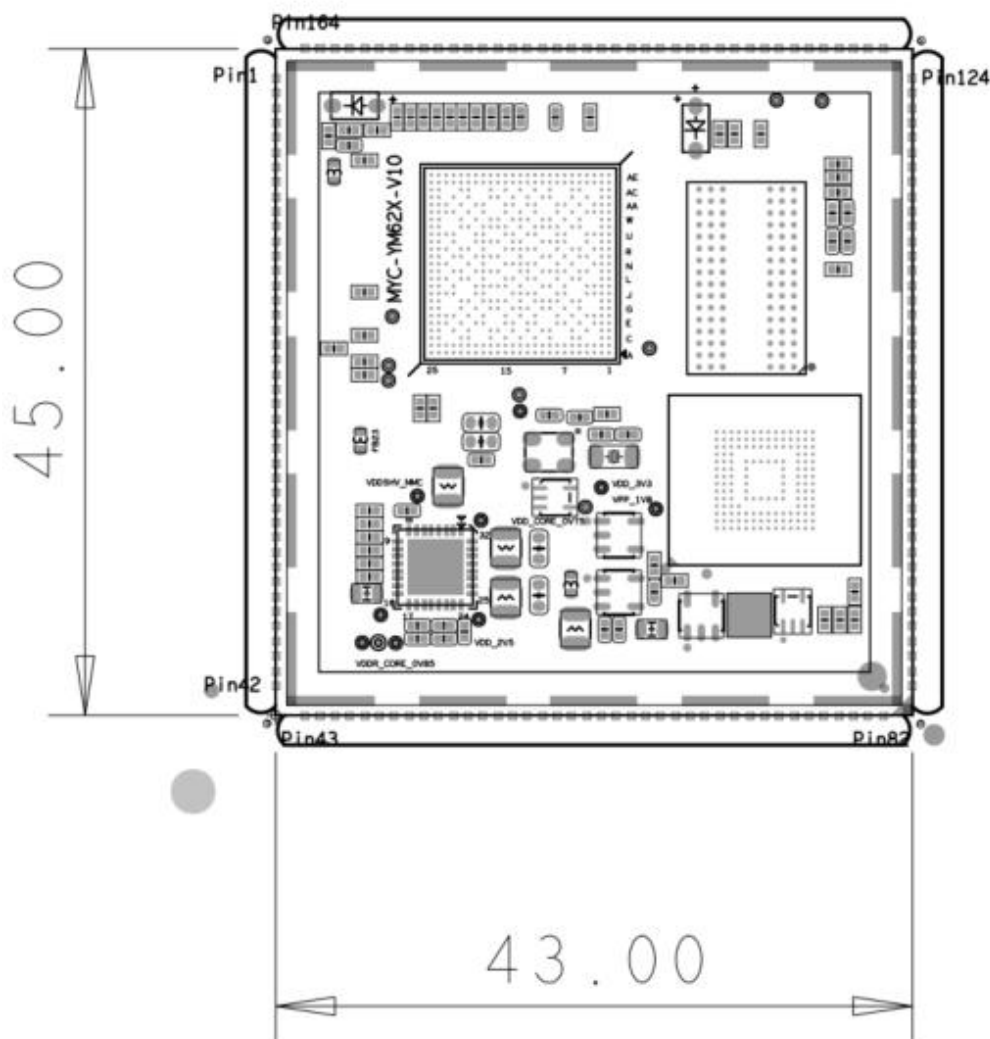


Figure 3-1 Module Pin map (Top side)



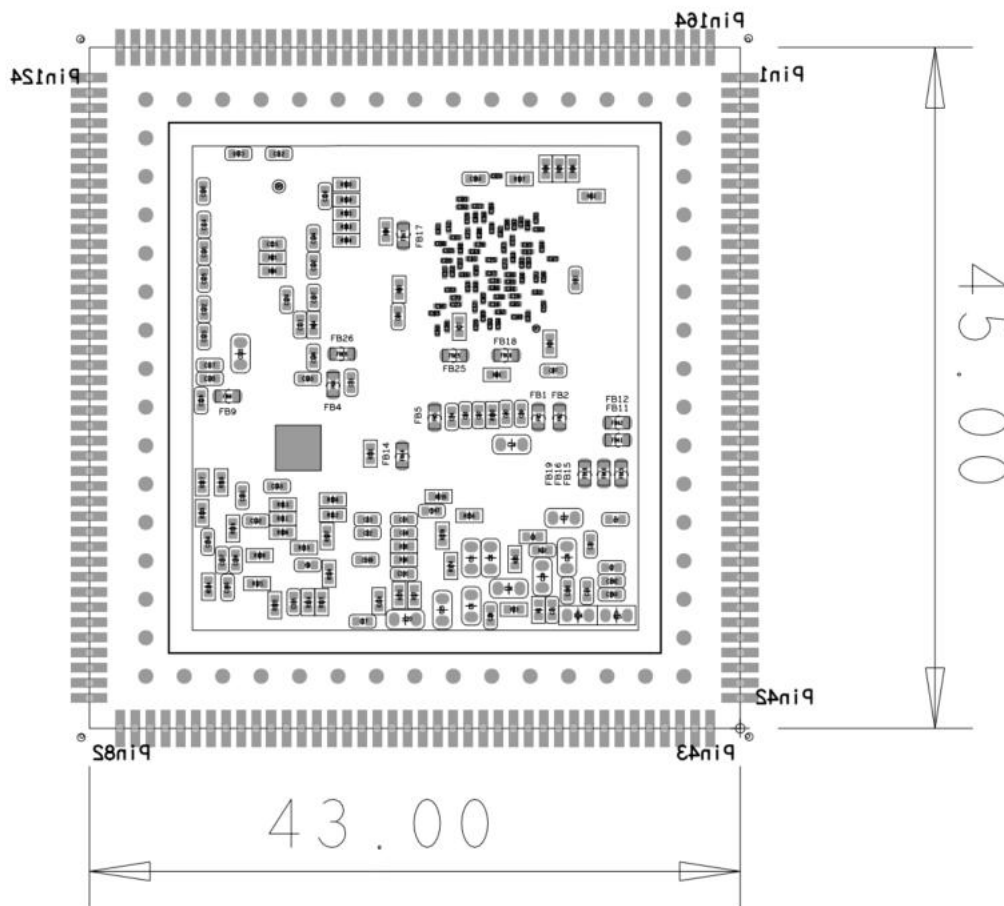


Figure 3-2 Module pin map (Bottom side)





## 3.2. Pin List

The following table shows the definition of the interface pins of the MYC-YM62X core board. The pin functions of the BSP development kit are configured according to "Default functions" in the following table. If you need to change the default pin functions, please modify the related driver configuration code.

Item	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	1	GND			0V		
	2	GND			0V		
	3	GND			0V		
	4	SOC_JTAG_TDI	JTAG	JTAG Test Data Input	3V3	I	
	5	SOC_JTAG_TRSTN	JTAG	TAG Reset	3V3	I	
	6	SOC_JTAG_TCK	JTAG	JTAG Test Clock Input	3V3	I	
	7	SOC_JTAG_TDO	JTAG	JTAG Test Data Output	3V3	O	
	8	SOC_JTAG_TMS	JTAG	JTAG Test Mode Select Input	3V3	I	
	9	GND			0V		
	10	SOC_LVDS0_A0P	LVDS0	OLDI Differential Data +	1V8	IO	
	11	SOC_LVDS0_A0N	LVDS0	OLDI Differential Data -	1V8	IO	
	12	GND			0V		
	13	SOC_LVDS0_A1P	LVDS0	OLDI Differential Data +	1V8	IO	
	14	SOC_LVDS0_A1N	LVDS0	OLDI Differential Data -	1V8	IO	
	15	GND			0V		
	16	SOC_LVDS0_A2P	LVDS0	OLDI Differential Data +	1V8	IO	
	17	SOC_LVDS0_A2N	LVDS0	OLDI Differential Data -	1V8	IO	
	18	GND			0V		
	19	SOC_LVDS0_A3P	LVDS0	OLDI Differential Data +	1V8	IO	
	20	SOC_LVDS0_A3N	LVDS0	OLDI Differential Data -	1V8	IO	
	21	GND			0V		
	22	SOC_LVDS0_CLK0P	LVDS0	OLDI Differential Clock +	1V8	IO	
	23	SOC_LVDS0_CLK0N	LVDS0	OLDI Differential Clock -	1V8	IO	
	24	GND			0V		
	25	SOC_LVDS1_A0P	LVDS1	OLDI Differential Data +	1V8	IO	
	26	SOC_LVDS1_A0N	LVDS1	OLDI Differential Data -	1V8	IO	
	27	GND			0V		
	28	SOC_LVDS1_A1P	LVDS1	OLDI Differential Data +	1V8	IO	
	29	SOC_LVDS1_A1N	LVDS1	OLDI Differential Data -	1V8	IO	
	30	GND			0V		
	31	SOC_LVDS1_A2P	LVDS1	OLDI Differential Data +	1V8	IO	
	32	SOC_LVDS1_A2N	LVDS1	OLDI Differential Data -	1V8	IO	
	33	GND			0V		
	34	SOC_LVDS1_A3P	LVDS1	OLDI Differential Data +	1V8	IO	
	35	SOC_LVDS1_A3N	LVDS1	OLDI Differential Data -	1V8	IO	
	36	GND			0V		
	37	SOC_LVDS1_CLK0P	LVDS1	OLDI Differential Clock +	1V8	IO	
	38	SOC_LVDS1_CLK0N	LVDS1	OLDI Differential Clock -	1V8	IO	



39	GND			0V		
40	SOC_USB0_DP	USB0	USB 2.0 Differential Data +	1V8	IO	
41	SOC_USB0_DM	USB0	USB 2.0 Differential Data -	1V8	IO	
42	SOC_EXTINT_GPIO1_31			3V3		
43	SOC_USB1_DP	USB1	USB 2.0 Differential Data +	1V8	IO	
44	SOC_USB1_DM	USB1	USB 2.0 Differential Data -	1V8	IO	
45	JTAG_EMU_RSTN		JTAG_EMU_RSTN	3V3	I	
46	SOC_CSI0_RXCLKP	CSI0	CSI0 Differential Receive Clock Input +	1V8	I	
47	SOC_CSI0_RXCLKN	CSI0	CSI0 Differential Receive Clock Input -	1V8	I	
48	GND			0V		
49	SOC_CSI0_RXP0	CSI0	CSI0 Differential Receive Input +	1V8	I	
50	SOC_CSI0_RXN0	CSI0	CSI0 Differential Receive Input -	1V8	I	
51	GND			0V		
52	SOC_CSI0_RXP1	CSI0	CSI0 Differential Receive Input +	1V8	I	
53	SOC_CSI0_RXN1	CSI0	CSI0 Differential Receive Input -	1V8	I	
54	GND			0V		
55	SOC_CSI0_RXP2	CSI0	CSI0 Differential Receive Input +	1V8	I	
56	SOC_CSI0_RXN2	CSI0	CSI0 Differential Receive Input -	1V8	I	
57	GND			0V		
58	SOC_CSI0_RXP3	CSI0	CSI0 Differential Receive Input +	1V8	I	
59	SOC_CSI0_RXN3	CSI0	CSI0 Differential Receive Input -	1V8	I	
60	GND			0V		
61	SOC_RGMII1_TD2	RGMII1	RGMII Transmit Data 2	1V8		
62	SOC_RGMII1_TD3	RGMII1	RGMII Transmit Data 3	1V8	O	
63	SOC_RGMII1_TXC	RGMII1	RGMII Transmit Clock	1V8	IO	
64	SOC_RGMII1_TX_CTL	RGMII1	RGMII Transmit Control	1V8	O	
65	SOC_RGMII1_TD0	RGMII1	RGMII Transmit Data 0	1V8	O	
66	SOC_RGMII1_TD1	RGMII1	RGMII Transmit Data 1	1V8	O	
67	SOC_RGMII1_RD2	RGMII1	RGMII Receive Data 2	1V8	I	
68	SOC_RGMII1_RX_CTL	RGMII1	RGMII Receive Control	1V8	I	
69	GND			0V		
70	SOC_RGMII1_RXC	RGMII1	RGMII Receive Clock	1V8	I	
71	SOC_RGMII1_RD3	RGMII1	RGMII Receive Data 3	1V8	I	
72	SOC_RGMII1_RD0	RGMII1	RGMII Receive Data 0	1V8	I	
73	SOC_RGMII1_RD1	RGMII1	RGMII Receive Data 1	1V8	I	
74	SOC_RGMII2_TD3	RGMII2	RGMII Transmit Data 3	1V8	O	
75	SOC_RGMII2_TD0	RGMII2	RGMII Transmit Data 0	1V8	O	
76	SOC_RGMII2_TD1	RGMII2	RGMII Transmit Data 1	1V8	O	
77	SOC_RGMII2_TX_CTL	RGMII2	RGMII Transmit Control	1V8	O	
78	GND			0V		
79	SOC_RGMII2_TXC	RGMII2	RGMII Transmit Clock	1V8	IO	
80	SOC_RGMII2_TD2	RGMII2	RGMII Transmit Data 2	1V8	O	
81	SOC_RGMII2_RXC	RGMII2	RGMII Receive Clock	1V8	I	
82	SOC_RGMII2_RD0	RGMII2	RGMII Receive Data 0	1V8	I	



83	SOC_RGMII2_RX_CTL	RGMII2	RGMII Receive Control	1V8	I	
84	SOC_RGMII2_RD3	RGMII2	RGMII Receive Data 3	1V8	I	
85	SOC_RGMII2_RD2	RGMII2	RGMII Receive Data 2	1V8	I	
86	SOC_RGMII2_RD1	RGMII2	RGMII Receive Data 1	1V8	I	
87	SOC_VOUT0_DE	VOUT0	Video Output Data Enable	3V3	O	
88	SOC_VOUT0_HSYNC	VOUT0	Video Output Horizontal Sync	3V3	O	
89	SOC_VOUT0_PCLK	VOUT0	Video Output Pixel Clock Output	3V3	O	
90	SOC_VOUT0_VSYNC	VOUT0	Video Output Vertical Sync	3V3	O	
91	GND			0V		
92	SOC_VOUT0_DATA6	VOUT0	Video Output Data 6	3V3	O	
93	SOC_VOUT0_DATA8	VOUT0	Video Output Data 8	3V3	O	
94	SOC_VOUT0_DATA14	VOUT0	Video Output Data 14	3V3	O	
95	SOC_VOUT0_DATA0	VOUT0	Video Output Data 0	3V3	O	
96	SOC_VOUT0_DATA20/BOOTMODE12	VOUT0	Video Output Data 20	3V3	O	
97	SOC_VOUT0_DATA12	VOUT0	Video Output Data 12	3V3	O	
98	SOC_VOUT0_DATA7	VOUT0	Video Output Data 7	3V3	O	
99	SOC_VOUT0_DATA4	VOUT0	Video Output Data 4	3V3	O	
100	GND			0V		
101	SOC_VOUT0_DATA2	VOUT0	Video Output Data 2	3V3	O	
102	SOC_VOUT0_DATA23/BOOTMODE15	VOUT0	Video Output Data 23	3V3	O	
103	SOC_VOUT0_DATA21/BOOTMODE13	VOUT0	Video Output Data 21	3V3	O	
104	SOC_GPMC0_AD4/BOOTMODE04	GPMC0	GPMC Data 4	3V3	IO	
105	SOC_VOUT0_DATA5	VOUT0	Video Output Data 5	3V3	O	
106	SOC_VOUT0_DATA3	VOUT0	Video Output Data 3	3V3	O	
107	SOC_VOUT0_DATA1	VOUT0	Video Output Data 1	3V3	O	
108	SOC_VOUT0_DATA22/BOOTMODE14	VOUT0	Video Output Data 22	3V3	O	
109	GND			0V		
110	SOC_GPMC0_AD1/BOOTMODE01	GPMC0	GPMC Data 1	3V3	IO	
111	SOC_GPMC0_AD2/BOOTMODE02	GPMC0	GPMC Data 2	3V3	IO	
112	SOC_VOUT0_DATA18/BOOTMODE10	VOUT0	Video Output Data 18	3V3	O	
113	SOC_VOUT0_DATA17/BOOTMODE09	VOUT0	Video Output Data 17	3V3	O	
114	SOC_GPMC0_AD3/BOOTMODE03	GPMC0	GPMC Data 3	3V3	IO	
115	SOC_VOUT0_DATA16/BOOTMODE08	VOUT0	Video Output Data 16	3V3	O	
116	SOC_VOUT0_DATA19/BOOTMODE11	VOUT0	Video Output Data 19	3V3	O	



117	SOC_VOUT0_DATA10	VOUT0	Video Output Data 10	3V3	O	
118	SOC_GPMC0_AD0/B OOTMODE00	GPMC0	GPMC Data 0	3V3	IO	
119	GND			0V		
120	SOC_GPMC0_CLK	GPMC0	GPMC clock	3V3	O	
121	SOC_I2C1_SDA	I2C1	IIC bus data	3V3	IO	
122	SOC_I2C1_SCL	I2C1	IIC bus clock	3V3	IO	
123	SOC_UART0_RTSEN	UART0	UART Request to Send	3V3	O	
124	SOC_UART0_CTSEN	UART0	UART Clear to Send	3V3	I	
125	SOC_UART0_RXD	UART0	UART Data receive	3V3	I	
126	SOC_UART0_TXD	UART0	UART Data transmit	3V3	O	
127	SOC_OSPI0_LBCLK	OSPI0	OSPI Loopback Clock Output	1V8	IO	
128	SOC_OSPI0_CSN0	OSPI0	OSPI Chip Select 0	1V8	O	
129	SOC_OSPI0_CSN1	OSPI0	OSPI Chip Select 1	1V8	O	
130	SOC_OSPI0_RESETO UT1	OSPI0	OSPI Reset1	1V8	O	
131	SOC_OSPI0_ECC_FAIL	OSPI0	OSPI ECC Status	1V8	I	
132	SOC_OSPI0_CLK	OSPI0	OSPI Clock	1V8	O	
133	SOC_OSPI0_DQ5	OSPI0	OSPI Data 5	1V8	IO	
134	GND			0V		
135	SOC_OSPI0_DQS	OSPI0	OSPI Data Strobe	1V8	I	
136	SOC_OSPI0_DQ6	OSPI0	OSPI Data 6	1V8	IO	
137	SOC_OSPI0_DQ2	OSPI0	OSPI Data 2	1V8	IO	
138	SOC_OSPI0_DQ1	OSPI0	OSPI Data 1	1V8	IO	
139	SOC_OSPI0_DQ0	OSPI0	OSPI Data 0	1V8	IO	
140	SOC_OSPI0_DQ3	OSPI0	OSPI Data 3	1V8	IO	
141	SOC_OSPI0_DQ4	OSPI0	OSPI Data 4	1V8	IO	
142	SOC_OSPI0_DQ7	OSPI0	OSPI Data 7	1V8	IO	
143	GND			0V		
144	SOC_MMC2_CLK	MMC2	MMC/SD/SDIO Clock	3V3	IO	
145	SOC_MMC2_DAT1	MMC2	MMC/SD/SDIO Data1	3V3	IO	
146	SOC_MMC2_DAT0	MMC2	MMC/SD/SDIO Data0	3V3	IO	
147	SOC_MMC2_CMD	MMC2	MMC/SD/SDIO Command	3V3	IO	
148	SOC_MMC2_SDCD	MMC2	SD Card Detect	3V3	I	
149	SOC_MMC1_CLK	MMC1	MMC/SD/SDIO Clock	3V3	IO	
150	SOC_JTAG_EMU1	JTAG	Emulation Control 1	3V3	IO	
151	SOC_MMC2_DAT3	MMC2	MMC/SD/SDIO Data3	3V3	IO	
152	GND			0V		
153	SOC_MMC2_DAT2	MMC2	MMC/SD/SDIO Data2	3V3	IO	
154	SOC_MMC1_DAT1	MMC1	MMC/SD/SDIO Data1	3V3	IO	
155	SOC_MMC1_DAT0	MMC1	MMC/SD/SDIO Data0	3V3	IO	
156	SOC_MMC1_CMD	MMC1	MMC/SD/SDIO Command	3V3	IO	
157	SOC_MMC1_DAT3	MMC1	MMC/SD/SDIO Data3	3V3	IO	
158	SOC_MMC1_DAT2	MMC1	MMC/SD/SDIO Data2	3V3	IO	
159	SOC_MMC1_SDCD	MMC1	SD Card Detect	3V3	I	



160	SOC_JTAG_EMU0	JTAG	Emulation Control 0	3V3	IO	
161	VDD_SYS_5V0			5V		
162	VDD_SYS_5V0			5V		
163	VDD_SYS_5V0			5V		
164	VDD_SYS_5V0			5V		
L1	SOC_MCU_UART0_RXD	UART0	UART Receive Data	3V3	I	
L2	SOC_MCU_SPI0_CS0	SPI0	SPI Chip Select 0	3V3	IO	
L3	SOC_MCU_SPI0_D0	SPI0	SPI Data 0	3V3	IO	
L4	SOC_MCU_SPI0_D1	SPI0	SPI Data 1	3V3	IO	
L5	SOC_UART1_DCDN	UART1	UART Clear to Send	3V3	I	
L6	SOC_UART1_DSRN	UART1	UART Data Set Ready	3V3	I	
L7	SOC_UART1_RXD	UART1	UART Receive Data	3V3	I	
L8	SOC_UART1_TXD	UART1	UART Transmit Data	3V3	O	
L9	SOC_UART1_RIN	UART1	UART Ring Indicator	3V3	I	
L10	SOC_UART1_DTRN	UART1	UART Data Terminal Ready	3V3	O	
L11	SOC_UART1_RTSN	UART1	UART Request to Send	3V3	O	
L12	SOC_UART1_CTSN	UART1	UART Clear to Send	3V3	I	
L13	SOC_MCASP0_ACLKX	MCASP0	MCASP Transmit Bit Clock	3V3	IO	
L14	SOC_MCASP0_AFSX	MCASP0	MCASP Transmit Frame Sync	3V3	IO	
L15	SOC_MCASP0_AXR0	MCASP0	MCASP Serial Data	3V3	IO	
L16	SOC_MCASP0_AXR1	MCASP0	MCASP Serial Data	3V3	IO	
L17	SOC_RESET_REQZ	RESET	Main Domain external warm reset request input	3V3	I	
L18	SOC_RESETSTATZ	RESET	Main Domain warm reset status output	3V3	O	
L19	SOC_PORZ_OUT	PORZ_OUT	Main Domain POR status output	3V3	O	
L20	SOC_WKUP_UART0_RXD	UART0	UART Receive Data	3V3	I	
L21	SOC_MCU_RESETZ	RESET	MCU Domain warm reset	3V3	I	
L22	SOC_EXT_REFCLK1	EXT_REFCLK1	External clock input to Main Domain	3V3	I	
L23	SOC_RGMII_MDC	RGMII	MDIO Clock	1V8	O	
L24	SOC_RGMII_MDIO	RGMII	MDIO Data	1V8	IO	
L25	SOC_UART4_RXD	UART4	UART Receive Data	3V3	I	
L26	SOC_UART4_TXD	UART4	UART Transmit Data	3V3	O	
L27	SOC_VOUT0_DATA11	VOUT0	Video Output Data 11	3V3	O	
L28	SOC_VOUT0_DATA15	VOUT0	Video Output Data 15	3V3	O	
L29	SOC_VOUT0_DATA9	VOUT0	Video Output Data 9	3V3	O	
L30	SOC_VOUT0_DATA13	VOUT0	Video Output Data 13	3V3	O	
L31	SOC_WKUP_UART0_TXD	UART0	UART Transmit Data	3V3	O	
L32	SOC_GPMC0_WAIT1	GPMC0	GPMC External Indication of	3V3	I	



				Wait			
L33	SOC_GPMC0_DIR	GPMC0	GPMC Data Bus Signal Direction Control	3V3	O		
L34	SOC_GPMC0_BE0N_CLE	GPMC0	GPMC Lower-Byte Enable	3V3	O		
L35	SOC_GPMC0_WAIT0	GPMC0	GPMC External Indication of Wait0	3V3	I		
L36	SOC_GPMC0_AD7/B OOTMODE07	GPMC0	GPMC Data 7	3V3	IO		
L37	SOC_GPMC0_AD5/B OOTMODE05	GPMC0	GPMC Data 5	3V3	IO		
L38	SOC_GPMC0_AD6/B OOTMODE06	GPMC0	GPMC Data 6	3V3	IO		
L39	SOC_GPMC0_BE1N	GPMC0	GPMC Upper-Byte Enable	3V3	O		
L40	SOC_GPMC0_OEN_R EN	GPMC0	GPMC Output Enable	3V3	O		
L41	SOC_GPMC0_WPN	GPMC0	GPMC Flash Write Protect	3V3	O		
L42	SOC_GPMC0_WEN	GPMC0	GPMC Write Enable	3V3	O		
L43	VDD_3V3			3V3			
L44	SOC_SPI0_CS1	SPI0	SPI Chip Select 1	3V3	IO		
L45	SOC_SPI0_D1	SPI0	SPI Data 1	3V3	IO		
L46	SOC_USB0_DRVVBU S	USB0	USB VBUS control output	3V3	O		
L47	SOC_GPMC0_CSN0	GPMC0	GPMC Chip Select 0	3V3	O		
L48	SOC_GPMC0_ADV_N ALE	GPMC0	GPMC Address Valid	3V3	O		
L49	SOC_USB1_DRVVBU S	USB1	USB VBUS control output	3V3	O		
L50	SOC_SPI0_CS0	SPI0	SPI Chip Select 0	3V3	IO		
L51	SOC_SPI0_CLK	SPI0	SPI_Clock	3V3	IO		
L52	SOC_SPI0_D0	SPI0	SPI Data 0	3V3	IO		
L53	SOC_MCU_SPI0_CLK	SPI0	SPI Clock	3V3	IO		
L54	SOC_MCU_MCAN0_T X	CAN0	CAN transmit Data	3V3	O		
L55	SOC_MCU_MCAN1_ RX	CAN1	CAN receive Data	3V3	I		
L56	SOC_MCU_MCAN1_T X	CAN1	CAN transmit Data	3V3	O		
L57	SOC_MCU_MCAN0_ RX	CAN0	CAN receive Data	3V3	I		
L58	SOC_MCU_UART0_T XD	UART0	UART transmit Data	3V3	O		

**Table 3-1 MYC-YM62X Core board Pin List**



## 4. Electrical Characteristics

### 4.1. Primary System Power (VDD\_5V)

The main power supply of the MYC-YM62X core board is VDD\_5V, which corresponds to the PIN161-164 pin of the stamp hole SMD pad. In order to ensure normal operation, the carried board must provide a voltage of  $5V \pm 5\%$ , a current of about 1A, and ensure that the output capacity of the supply circuit can meet the power consumption of the core board. This section lists the power consumption and current of the core board under various conditions. Please reserve an appropriate margin when designing the power supply circuit.

Name	Description	Recommended Voltage
VDD_5V	Main supply voltage, 5V input, 2A	5V
VDD_3V3	3.3V output, 0.2A	3.3V

Table 4-1 External input / output voltage

### 4.2. Power Consumption

Conditon	Voltage(V)	Average Current(A)	Power Consumption (W)
no-load	5	0.21	1.05
Full-load (ENET*1+USB*2+Type-C* 1+SD Card*1+aging)	5	0.298	1.49
mem (echo mem)	-	-	-
freeze (echo freeze)	5	0.16	0.8

Table 4-2 Power consumption parameters





## 4.3. GPIO DC Parameters

Parameter	Symbol	Min	Typical	Max	Units	description
High-lever DC input voltage	$V_{IH}$	2	—	$VDD+0.3$	V	—
Low-lever DC input voltage	$V_{IL}$	0.8	—	$0.3 \times VDD$	V	—
High-lever DC output voltage	$V_{OH}$	2.4	—	VDD	V	—
Low-lever DC output voltage	$V_{OL}$	0.4	—	$0.2 \times VDD$	V	—

**Table 4-3 GPIO DC Parameters**



## 5. System necessary circuit design

### 5.1. Boot

Using the MYC-YM62X core board, the base board can be designed to start the circuit board from the corresponding start item (OSPI, MMCSD, EMMC), The dial-up code in the bottom board adopts the 3V3 of the core board.

B3	B4	B5	B6	B7	B8	B9	BOOTDEVICE
0	1	1	1	0	0	1	OSPI
0	0	0	1	0	0	1	MMCSD BOOT
1	0	0	1	0	0	0	EMMC BOOT

图 5-1 boot 配置电路

### 5.2. Burning firmware

Micro SD card circuit is recommended for the core board of MYC-YM62X to burn and update the firmware of the core board, and MMC1 is recommended for signal interface. Please refer to Section 6.1.

### 5.3. Debug

It is recommended that the core board of MYC-YM62X use UART interface circuit to debug the software program of the core board. It is recommended that the signal interface use UART0, MCU-UART to TYPE-C. For details, please refer to Section 6.2.

### 5.4. Reset

With the MYC-YM62X core board, the SYS-RST-IN signal is drawn from the PIN L21 pin of the core board, the hardware system used for the core board resets the input signal, 3.3V level logic.



## 6. Interfaces

### 6.1. SD

MYC-YM62X core board is equipped with two SD/MMC interfaces, MMC1 is commonly used to design MicroSD card signals; MMC2 in the core board has been used to WIFI connect.

#### 6.1.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	155	SOC_MMC1_DAT0	MMC1	MMC/SD/SDIO Data0	3V3	IO	
	154	SOC_MMC1_DAT1	MMC1	MMC/SD/SDIO Data1	3V3	IO	
	158	SOC_MMC1_DAT2	MMC1	MMC/SD/SDIO Data2	3V3	IO	
	157	SOC_MMC1_DAT3	MMC1	MMC/SD/SDIO Data3	3V3	IO	
	156	SOC_MMC1_CMD	MMC1	MMC/SD/SDIO Command	3V3	IO	
	149	SOC_MMC1_CLK	MMC1	MMC/SD/SDIO Clock	3V3	IO	
	159	SOC_MMC1_SDCD	MMC1	SD Card Detect	3V3	I	
	144	SOC_MMC2_CLK	MMC2	MMC/SD/SDIO Clock	3V3	IO	
	146	SOC_MMC2_DAT0	MMC2	MMC/SD/SDIO Data0	3V3	IO	
	145	SOC_MMC2_DAT1	MMC2	MMC/SD/SDIO Data1	3V3	IO	
	153	SOC_MMC2_DAT2	MMC2	MMC/SD/SDIO Data2	3V3	IO	
	151	SOC_MMC2_DAT3	MMC2	MMC/SD/SDIO Data3	3V3	IO	
	147	SOC_MMC2_CMD	MMC2	MMC/SD/SDIO Command	3V3	IO	
	148	SOC_MMC2_SDCD	MMC2	SD Card Detect	3V3	I	

Table 6-1 SD/MMC PIN description



## 6.2. UART

MYC-YM62X core board processor has up to 9 serial ports. Due to the pin reuse of the chip, the core board is configured with four serial ports by default, UART0 and MCU\_UART0 use to UART to TYPE-C, UART4 and UART6 use to RS485.

The other 5 channels due to pin multiplexing into other functions.

### 6.2.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	125	SOC_UART0_RXD	UART0	UART Data receive	3V3	I	
	126	SOC_UART0_TXD	UART0	UART Data transmit	3V3	O	
	L1	SOC_MCU_UART0_RXD	UART0	UART Receive Data	3V3	I	
	L58	SOC_MCU_UART0_TXD	UART0	UART transmit Data	3V3	O	
	L25	SOC_UART4_RXD	UART4	UART Receive Data	3V3	I	
	L26	SOC_UART4_TXD	UART4	UART Transmit Data	3V3	O	
	L32	SOC_GPMC0_WAIT1	GPMC0	GPMC External Indication of Wait	3V3	I	multiplex UART6_TXD
	L41	SOC_GPMC0_WPN	GPMC0	GPMC Flash Write Protect	3V3	O	multiplex UART6_RXD

**Table 6-2 UART PIN description**



## 6.3. USB

The MYC-YM62X core board provides two USB2.0 devices. all supports HOST and Device modes.

### 6.3.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	40	SOC_USB0_DP	USB0	USB 2.0 Differential Data +	1.8 V	IO	
	41	SOC_USB0_DM	USB0	USB 2.0 Differential Data -	1.8 V	IO	
	43	SOC_USB1_DP	USB1	USB 2.0 Differential Data +	1.8 V	IO	
	44	SOC_USB1_DM	USB1	USB 2.0 Differential Data -	1.8 V	IO	

**Table 6-3 USB PIN description**



## 6.4. CAN

The MYC-YM62X core board has a maximum of three CAN ports. Due to Pin reuse, two CAN0 CAN1 bus interface is configured on the core board by default. If you want to use more CAN bus interfaces, please consult the chip manual or Pin List and modify the pin configuration in the driver.

### 6.4.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	L54	SOC_MCU_MCAN0_TX	CAN0	CAN transmit Data	3V3	O	
	L57	SOC_MCU_MCAN0_RX	CAN0	CAN receive Data	3V3	I	
	L55	SOC_MCU_MCAN1_RX	CAN1	CAN receive Data	3V3	I	
	L56	SOC_MCU_MCAN1_TX	CAN1	CAN transmit Data	3V3	O	

**Table 6-4 CAN PIN description**



## 6.5. Ethernet

MYC-YM62X core board leads to two RGMII signal. When the user designs the carried board circuit, the Ethernet PHY circuit, transformer isolation circuit and RJ45 part of the circuit can be designed. CPU Ethernet interfaces support only RGMII and RMII.

### 6.5.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	65	SOC_RGMII1_TD0	RGMII1	RGMII Transmit Data 0	1.8 V	O	
	66	SOC_RGMII1_TD1	RGMII1	RGMII Transmit Data 1	1.8 V	O	
	61	SOC_RGMII1_TD2	RGMII1	RGMII Transmit Data 2	1.8 V		
	62	SOC_RGMII1_TD3	RGMII1	RGMII Transmit Data 3	1.8 V	O	
	72	SOC_RGMII1_RD0	RGMII1	RGMII Receive Data 0	1.8 V	I	
	73	SOC_RGMII1_RD1	RGMII1	RGMII Receive Data 1	1.8 V	I	
	67	SOC_RGMII1_RD2	RGMII1	RGMII Receive Data 2	1.8 V	I	
	71	SOC_RGMII1_RD3	RGMII1	RGMII Receive Data 3	1.8 V	I	
	63	SOC_RGMII1_TXC	RGMII1	RGMII Transmit Clock	1.8 V	IO	
	70	SOC_RGMII1_RXC	RGMII1	RGMII Receive Clock	1.8 V	I	
	64	SOC_RGMII1_TX_CTL	RGMII1	RGMII Transmit Control	1.8 V	O	
	68	SOC_RGMII1_RX_CTL	RGMII1	RGMII Receive Control	1.8 V	I	
	75	SOC_RGMII2_TD0	RGMII2	RGMII Transmit Data 0	1.8 V	O	
	76	SOC_RGMII2_TD1	RGMII2	RGMII Transmit Data 1	1.8 V	O	
	80	SOC_RGMII2_TD2	RGMII2	RGMII Transmit Data 2	1.8 V	O	
	74	SOC_RGMII2_TD3	RGMII2	RGMII Transmit Data 3	1.8 V	O	
	82	SOC_RGMII2_RD0	RGMII2	RGMII Receive Data 0	1.8 V	I	
	86	SOC_RGMII2_RD1	RGMII2	RGMII Receive Data 1	1.8 V	I	
	85	SOC_RGMII2_RD2	RGMII2	RGMII Receive Data 2	1.8 V	I	
	84	SOC_RGMII2_RD3	RGMII2	RGMII Receive Data 3	1.8 V	I	
	79	SOC_RGMII2_TXC	RGMII2	RGMII Transmit Clock	1.8 V	IO	
	81	SOC_RGMII2_RXC	RGMII2	RGMII Receive Clock	1.8 V	I	
	77	SOC_RGMII2_TX_CTL	RGMII2	RGMII Transmit Control	1.8 V	O	
	83	SOC_RGMII2_RX_CTL	RGMII2	RGMII Receive Control	1.8 V	I	
	L23	SOC_RGMII_MDC	RMII	MDIO Clock	1.8 V	O	
	L24	SOC_RGMII_MDIO	RMII	MDIO Data	1.8 V	IO	

**Table 6-5 Ethernet PIN description**





## 6.6. LVDS

The MYC-YM62X core board has two LVDS display and output interfaces. LVDS0 supports double LVDS interface display. Support double display. The resolution is 1920x1080.

### 6.6.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	10	SOC_LVDS0_A0P	LVDS0	OLDI Differential Data +	1V8	IO	
	11	SOC_LVDS0_A0N	LVDS0	OLDI Differential Data -	1V8	IO	
	13	SOC_LVDS0_A1P	LVDS0	OLDI Differential Data +	1V8	IO	
	14	SOC_LVDS0_A1N	LVDS0	OLDI Differential Data -	1V8	IO	
	16	SOC_LVDS0_A2P	LVDS0	OLDI Differential Data +	1V8	IO	
	17	SOC_LVDS0_A2N	LVDS0	OLDI Differential Data -	1V8	IO	
	19	SOC_LVDS0_A3P	LVDS0	OLDI Differential Data +	1V8	IO	
	20	SOC_LVDS0_A3N	LVDS0	OLDI Differential Data -	1V8	IO	
	22	SOC_LVDS0_CLK0P	LVDS0	OLDI Differential Clock +	1V8	IO	
	23	SOC_LVDS0_CLK0N	LVDS0	OLDI Differential Clock -	1V8	IO	
	25	SOC_LVDS1_A0P	LVDS1	OLDI Differential Data +	1V8	IO	
	26	SOC_LVDS1_A0N	LVDS1	OLDI Differential Data -	1V8	IO	
	28	SOC_LVDS1_A1P	LVDS1	OLDI Differential Data +	1V8	IO	
	29	SOC_LVDS1_A1N	LVDS1	OLDI Differential Data -	1V8	IO	
	31	SOC_LVDS1_A2P	LVDS1	OLDI Differential Data +	1V8	IO	
	32	SOC_LVDS1_A2N	LVDS1	OLDI Differential Data -	1V8	IO	
	34	SOC_LVDS1_A3P	LVDS1	OLDI Differential Data +	1V8	IO	
	35	SOC_LVDS1_A3N	LVDS1	OLDI Differential Data -	1V8	IO	
	37	SOC_LVDS1_CLK0P	LVDS1	OLDI Differential Clock +	1V8	IO	
	38	SOC_LVDS1_CLK0N	LVDS1	OLDI Differential Clock -	1V8	IO	

**Table 6-6 LVDS PIN description**



## 6.7. I2C

The MYC-YM62X core board processor supports a maximum of Six I2C buses, in which I2C0, I2C1 and I2C3 are respectively signal expansion, CSI, LCD and AUDIO bus connection, and LVDS, RTC and USB bus connection.

If you want to use more I2C bus interfaces, consult the chip manual or Pin List and modify the pin configuration in the driver.

### 6.7.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	121	SOC_I2C1_SDA	I2C1	IIC bus data	3V3	IO	
	122	SOC_I2C1_SCL	I2C1	IIC bus clock	3V3	IO	
	123	SOC_UART0_RTSEN	UART0	UART Request to Send	3V3	IO	I2C3_SDA
	124	SOC_UART0_CTSEN	UART0	UART Clear to Send	3V3	IO	I2C3_SCL
	L5	SOC_UART1_DCDN	UART1	UART Clear to Send	3V3	IO	I2C0_SCL
	L6	SOC_UART1_DSRN	UART1	UART Data Set Ready	3V3	IO	I2C0_SDA

**Table 6-7 I2C PIN description**



## 6.8. Audio

The MYC-YM62X core board contains analog audio internally, connected to the other side via the chip SGTL5000XNAA3.

### 6.8.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	L13	SOC_MCASP0_ACLKX	MCASP0	MCASP Transmit Bit Clock	3V3	IO	
	L14	SOC_MCASP0_AFSX	MCASP0	MCASP Transmit Frame Sync	3V3	IO	
	L15	SOC_MCASP0_AXR0	MCASP0	MCASP Serial Data	3V3	IO	
	L16	SOC_MCASP0_AXR1	MCASP0	MCASP Serial Data	3V3	IO	
	L5	SoC_UART1_DCDn	UART1	UART Clear to Send	3V3	IO	multiplex AUDIO_I2C_SCL
	L6	SoC_UART1_DSRn	UART1	UART Data Set Ready	3V3	IO	multiplex AUDIO_I2C_SDA

**Table 6-8 Audio PIN description**



## 6.9. CSI

The MYC-YM62X core board supports 1channel CSI。Support for virtual channels (up to 16), Support 1,2,3 or 4 data channel modes, up to 2.5 Gbps.

### 6.9.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	46	SOC_CSI0_RXCLKP	CSI0	CSI0+	1V8	I	
	47	SOC_CSI0_RXCLKN	CSI0	CSI0-	1V8	I	
	49	SOC_CSI0_RXP0	CSI0	CSI0+	1V8	I	
	50	SOC_CSI0_RXN0	CSI0	CSI0-	1V8	I	
	52	SOC_CSI0_RXP1	CSI0	CSI0+	1V8	I	
	53	SOC_CSI0_RXN1	CSI0	CSI0 -	1V8	I	
	55	SOC_CSI0_RXP2	CSI0	CSI0+	1V8	I	
	56	SOC_CSI0_RXN2	CSI0	CSI0-	1V8	I	
	58	SOC_CSI0_RXP3	CSI0	CSI0+	1V8	I	
	59	SOC_CSI0_RXN3	CSI0	CSI0 -	1V8	I	
	L5	SOC_UART1_DCDN	UART1	UART Clear to Send	3V3	IO	Multiplex I 2 C _ SCL _ CSI, requiring a change between levels
	L6	SOC_UART1_DSRN	UART1	UART Data Set Ready	3V3	IO	Multiplex I 2 C _ SDA _ CSI, requiring a change between levels

**Table 6-9 CSI PIN description**



## 6.10. HDMI

The MYC-YM62X core board supports 1channel LCD,The output from RGB to HDMI .

### 6.10.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	87	SOC_VOUT0_DE	VOUT0	Video Output Data Enable	3V3	O	
	88	SOC_VOUT0_HSYNC	VOUT0	Video Output Horizontal Sync	3V3	O	
	89	SOC_VOUT0_PCLK	VOUT0	Video Output Pixel Clock Output	3V3	O	
	90	SOC_VOUT0_VSYNC	VOUT0	Video Output Vertical Sync	3V3	O	
	95	SOC_VOUT0_DATA0	VOUT0	Video Output Data 0	3V3	O	
	107	SOC_VOUT0_DATA1	VOUT0	Video Output Data 1	3V3	O	
	101	SOC_VOUT0_DATA2	VOUT0	Video Output Data 2	3V3	O	
	106	SOC_VOUT0_DATA3	VOUT0	Video Output Data 3	3V3	O	
	99	SOC_VOUT0_DATA4	VOUT0	Video Output Data 4	3V3	O	
	105	SOC_VOUT0_DATA5	VOUT0	Video Output Data 5	3V3	O	
	92	SOC_VOUT0_DATA6	VOUT0	Video Output Data 6	3V3	O	
	98	SOC_VOUT0_DATA7	VOUT0	Video Output Data 7	3V3	O	
	93	SOC_VOUT0_DATA8	VOUT0	Video Output Data 8	3V3	O	
	L29	SOC_VOUT0_DATA9	VOUT0	Video Output Data 9	3V3	O	
	117	SOC_VOUT0_DATA10	VOUT0	Video Output Data 10	3V3	O	
	L27	SOC_VOUT0_DATA11	VOUT0	Video Output Data 11	3V3	O	
	97	SOC_VOUT0_DATA12	VOUT0	Video Output Data 12	3V3	O	
	L30	SOC_VOUT0_DATA13	VOUT0	Video Output Data 13	3V3	O	
	94	SOC_VOUT0_DATA14	VOUT0	Video Output Data 14	3V3	O	
	L28	SOC_VOUT0_DATA15	VOUT0	Video Output Data 15	3V3	O	
	115	SOC_VOUT0_DATA16/ BOOTMODE08	VOUT0	Video Output Data 16	3V3	O	
	113	SOC_VOUT0_DATA17/ BOOTMODE09	VOUT0	Video Output Data 17	3V3	O	
	112	SOC_VOUT0_DATA18/ BOOTMODE10	VOUT0	Video Output Data 18	3V3	O	
	116	SOC_VOUT0_DATA19/ BOOTMODE11	VOUT0	Video Output Data 19	3V3	O	
	96	SOC_VOUT0_DATA20/ BOOTMODE12	VOUT0	Video Output Data 20	3V3	O	
	103	SOC_VOUT0_DATA21/ BOOTMODE13	VOUT0	Video Output Data 21	3V3	O	
	108	SOC_VOUT0_DATA22/ BOOTMODE14	VOUT0	Video Output Data 22	3V3	O	



	Pin	Signal	Default Function	Description	Voltage	IO	Comments
	102	SOC_VOUT0_DATA23/ BOOTMODE15	VOUT0	Video Output Data 23	3V3	O	
	L5	SOC_UART1_DCDN	UART1	UART Clear to Send	3V3	IO	Multiplexing I2C
	L6	SOC_UART1_DSRN	UART1	UART Data Set Ready	3V3	IO	Multiplexing I2C
	L13	SOC_MCASP0_ACLKX	MCASP0	MCASP Transmit Bit Clock	3V3	IO	Multiplexing
	L14	SOC_MCASP0_AFSX	MCASP0	MCASP Transmit Frame Sync	3V3	IO	Multiplexing
	L15	SOC_MCASP0_AXR0	MCASP0	MCASP Serial Data	3V3	IO	Multiplexing

**Table 6-10 HDMI PIN description**



## 6.11. GPMC

The MYC-YM62X core board supports 1 universal memory controller (GPMC), up to 133 MHz.

### 6.11.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	118	SOC_GPMC0_AD0/BOOTMODE00	GPMC0	GPMC Data 0	3V3	IO	
	110	SOC_GPMC0_AD1/BOOTMODE01	GPMC0	GPMC Data 1	3V3	IO	
	111	SOC_GPMC0_AD2/BOOTMODE02	GPMC0	GPMC Data 2	3V3	IO	
	114	SOC_GPMC0_AD3/BOOTMODE03	GPMC0	GPMC Data 3	3V3	IO	
	104	SOC_GPMC0_AD4/BOOTMODE04	GPMC0	GPMC Data 4	3V3	IO	
	L37	SOC_GPMC0_AD5/BOOTMODE05	GPMC0	GPMC Data 5	3V3	IO	
	L38	SOC_GPMC0_AD6/BOOTMODE06	GPMC0	GPMC Data 6	3V3	IO	
	L36	SOC_GPMC0_AD7/BOOTMODE07	GPMC0	GPMC Data 7	3V3	IO	
	120	SOC_GPMC0_CLK	GPMC0	GPMC clock	3V3	O	
	L33	SOC_GPMC0_DIR	GPMC0	GPMC Data Bus Signal Direction Control	3V3	O	
	L34	SOC_GPMC0_BE0N_CLE	GPMC0	GPMC Lower-Byte Enable	3V3	O	
	L35	SOC_GPMC0_WAIT0	GPMC0	GPMC External Indication of Wait0	3V3	I	
	L40	SOC_GPMC0_OEN_REN	GPMC0	GPMC Output Enable	3V3	O	
	L42	SOC_GPMC0_WEN	GPMC0	GPMC Write Enable	3V3	O	
	L47	SOC_GPMC0_CSN0	GPMC0	GPMC Chip Select 0	3V3	O	
	L48	SOC_GPMC0_ADV_N_ALE	GPMC0	GPMC Address Valid	3V3	O	

**Table 6-11 GPMC PIN description**





## 6.12. JTAG

The MYC-YM62X core board Lead out a road JTAG to transmit debugging information.

### 6.12.1. Pin Description

	Pin	Signal	Default Function	Description	Voltage	IO	Comments
-	4	SOC_JTAG_TDI	JTAG	JTAG Test Data Input	3V3	I	
	5	SOC_JTAG_TRSTN	JTAG	TAG Reset	3V3	I	
	6	SOC_JTAG_TCK	JTAG	JTAG Test Clock Input	3V3	I	
	7	SOC_JTAG_TDO	JTAG	JTAG Test Data Output	3V3	O	
	8	SOC_JTAG_TMS	JTAG	JTAG Test Mode Select Input	3V3	I	

**Table 6-12 JTAG PIN description**



# 7. Package Information

## 7.1. Package Dimensions

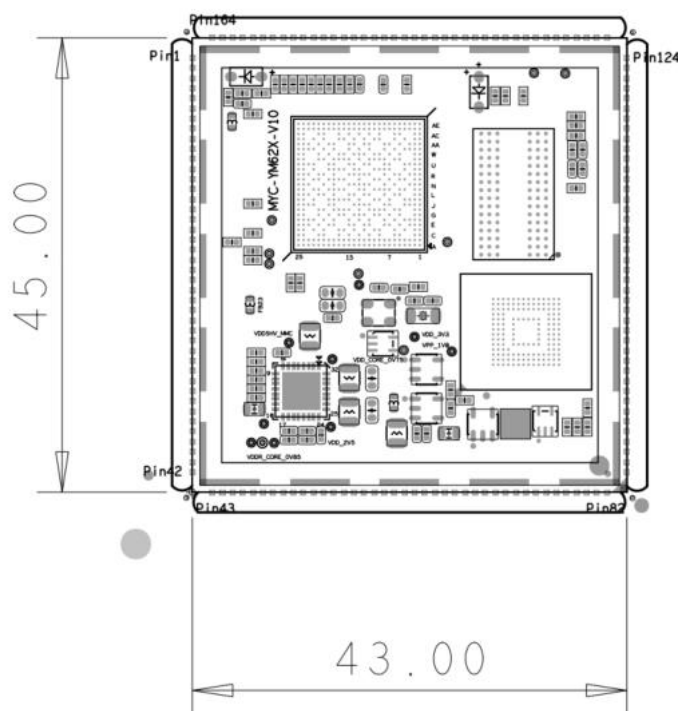


Figure 7-1 MYC-YM62X Top View

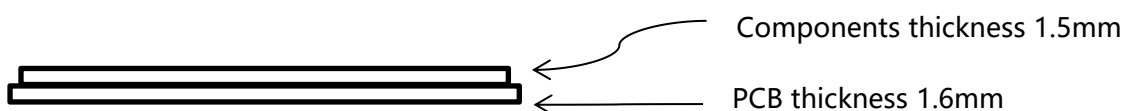


Figure 7-2 MYC-YM62X Side View



## 7.2. Carrier Board PCB Design

- a. PCB thickness is recommended to be at least 1.6mm. Pay attention to the balance of copper coating. If PCB deformation occurs in the over furnace, it is recommended to use a carrier to fix the over furnace.
- b. To ensure the quality of mounting and tinning, ensure that the PCB module is at least 3mm away from other components.
- c. PCB packaging provided by MYIR Electronics is recommended.



## 8. Mount and storage requirements

### 8.1. Steel mesh design

- 1) It is recommended to open holes at a ratio of 1:1 for the circular pad with a thickness of 0.15mm tin; With a thickness of 0.18mm, the opening ratio is 1:0.8.

### 8.2. Storage requirement

Modules are shipped in vacuum sealed form, and the following conditions are required for storage:

- 1) The vacuum-sealed bag can be stored for 12 months when the ambient temperature is lower than 40°C and the air humidity is less than 90%.
- 2) After opening the vacuum sealing bag, reflow welding can be carried out directly within 72 hours when the ambient temperature is lower than 30°C and the air humidity is less than 10%.

Note: If the above conditions are not met, baking should be carried out before applying.

### 8.3. Baking method

Because the module packaging material cannot withstand high temperature, if necessary, please choose one of the following two methods to bake, to avoid affecting the welding quality of the module.

- 1) Baking in the original package: baking temperature is 40 ~ 60°C and time is 5 ~ 7 days.
- 2) Transfer to high temperature resistant dish baking: baking temperature is 100 ~ 120, baking time is more than 48 hours.

### 8.4. Welding technology

- 1) If the plate to be mounted is double-sided device layout, it is recommended to put the core plate mounting process in the last stage.
- 2) It is recommended to set the preheating time of 160 ~ 200°C to 60 ~ 120 seconds.
- 3) It is recommended that the temperature of reflow welding should be 235 ~ 245°C, and the maximum temperature should not exceed 250°C, and the reflow time should be controlled within 40 ~ 60 seconds.
- 4) The recommended temperature rise rate is 1-3 °C/ s, and the temperature drop rate is 2-4 °C/ s.



# Appendix A

## Warranty & Technical Support Services

**MYIR Electronics Limited** is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

### Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

### Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

### Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

### Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

### After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

### Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;



- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;
- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
  - Hardware or software problems occurred during customers' own development;
  - Problems occurred when customers compile or run the OS which is tailored by themselves;
  - Problems occurred during customers' own applications development;
  - Problems occurred during the modification of MYIR's software source code.

## After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

## Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

## Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service



but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

## Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

## Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

## Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

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