



FE1.1

USB 2.0 HIGH SPEED 4-PORT HUB CONTROLLER

Data Sheet



INTRODUCTION

The FE1.1 is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 High Speed 4-Port Hub.

It adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special Build-In-Self-Test mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using 0.18μm technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

FEATURES

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
 - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
 - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 5V to 3.3V and 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resistor, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- *Multiple Transaction Translators (MTT)* –
 - One TT for each downstream port;
 - Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT;
 - Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;
- Automatic self-power status monitoring;



- ☐ Automatic re-enumeration when Self-Powered switching to Bus-Powered;
- Board configured options –
 - ☐ *Ganged or Individual Power Control Mode* select;
 - ☐ *Global or Individual Over-Current Detection Mode* select;
 - ☐ *Removable or Non-Removable Downstream Devices* configuration;
- Comprehensive Port Indicators support:
 - ☐ Standard downstream port status indicators (Green and Amber LED control for each downstream port);
 - ☐ Hub active LED support;

ORDER INFORMATION

P/N-Order Code	Description	Package Type	Packing	Minimum Order Quantity
FE1.1-AQFP48A	USB 2.0 4-Port MTT Hub Controller	48-pin LQFP (7mm x 7mm)	Tray	15000
FE1.1-AQFN48A		48-pin QFN (6mm x 6mm)	Tape & Reel	12500
FE1.1-AQFP48AT ^(Note)		48-pin LQFP (7mm x 7mm)	Tray	2500

Note: Product of order code AQFP48AT is final tested in Room Temperature, 85°C, and -40°C, respectively.

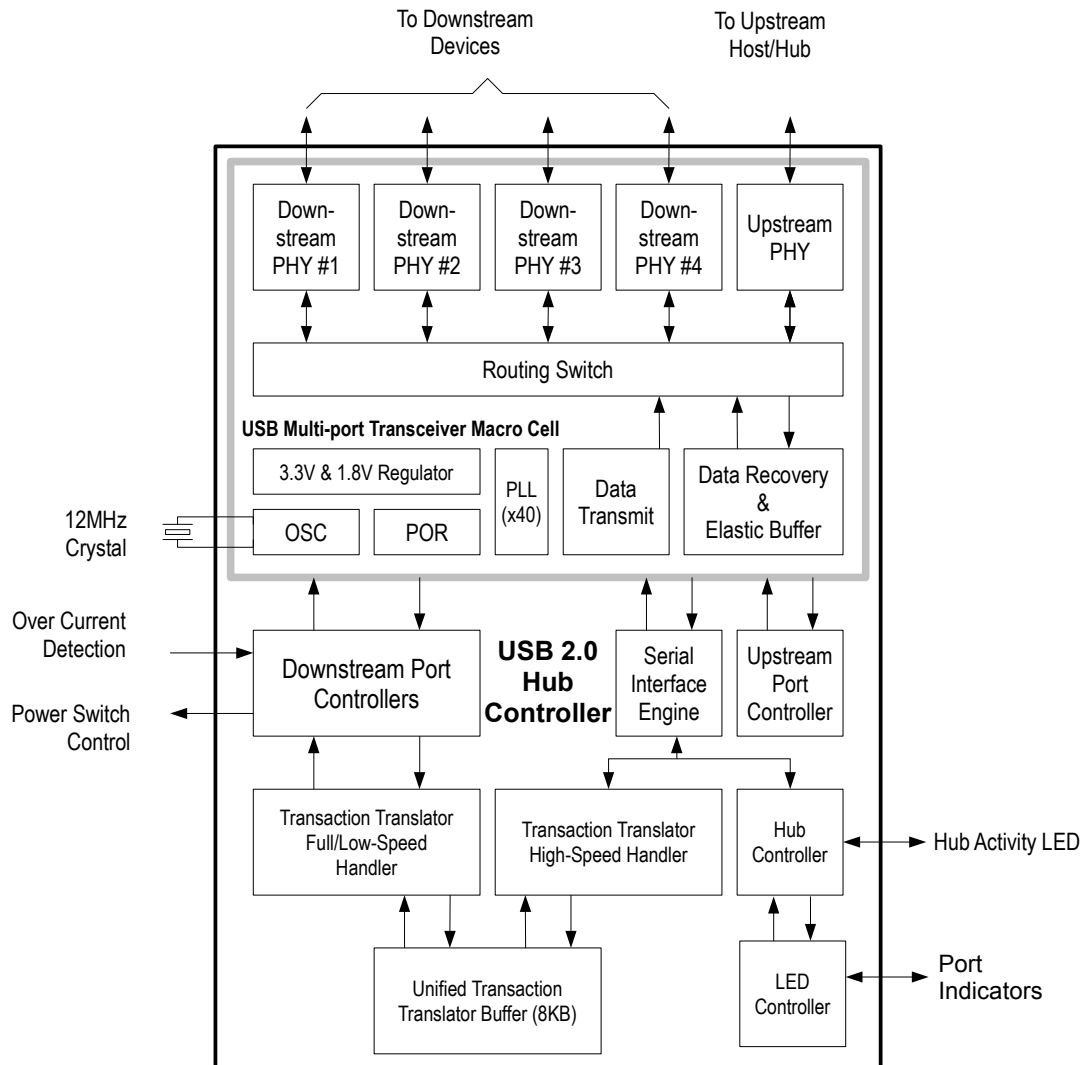


Fig. 1: Block Diagram

PACKAGE I – 48-PIN LQFP

(Body Size: 7mm x 7mm)

PIN ASSIGNMENT

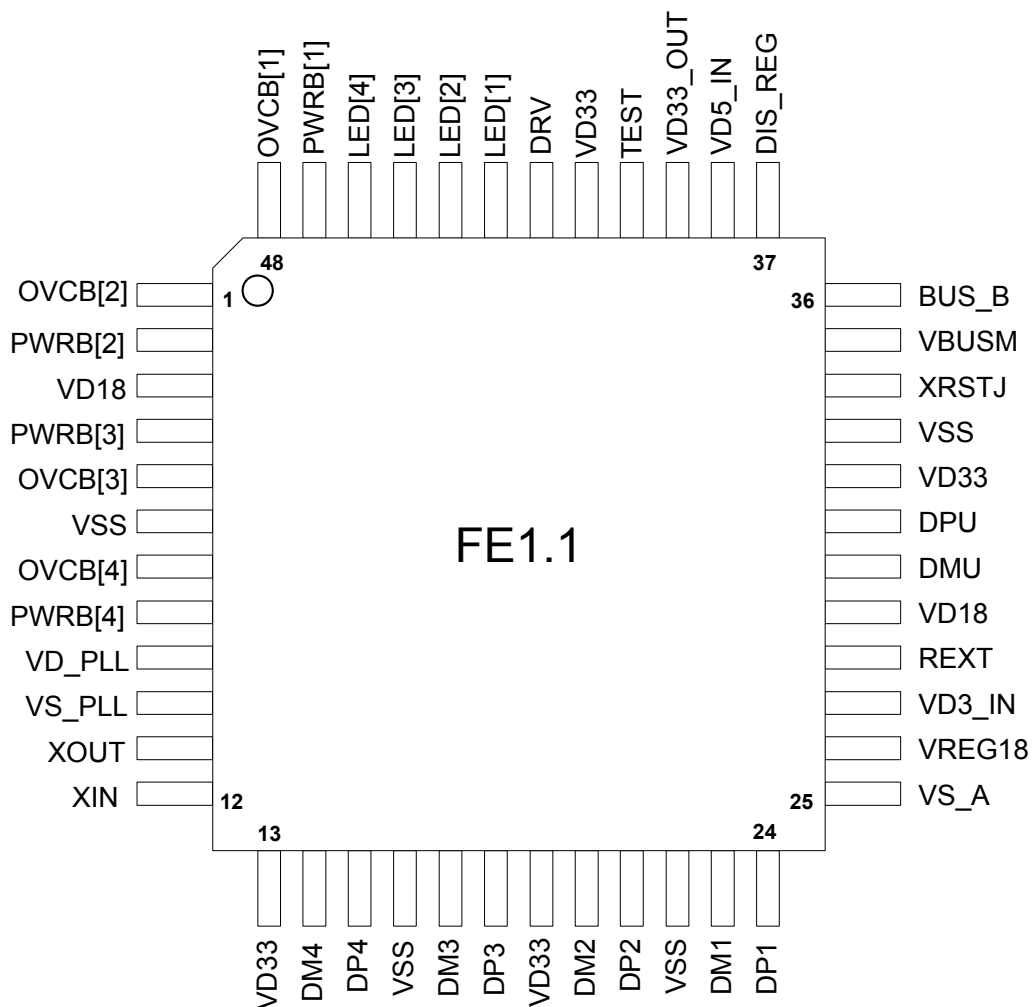


Fig. 2: 48-Pin LQFP Pin Assignment

PACKAGE II— 48-PIN QFN

(Body Size: 6mm x 6mm, 0.4pitch)

PIN ASSIGNMENT

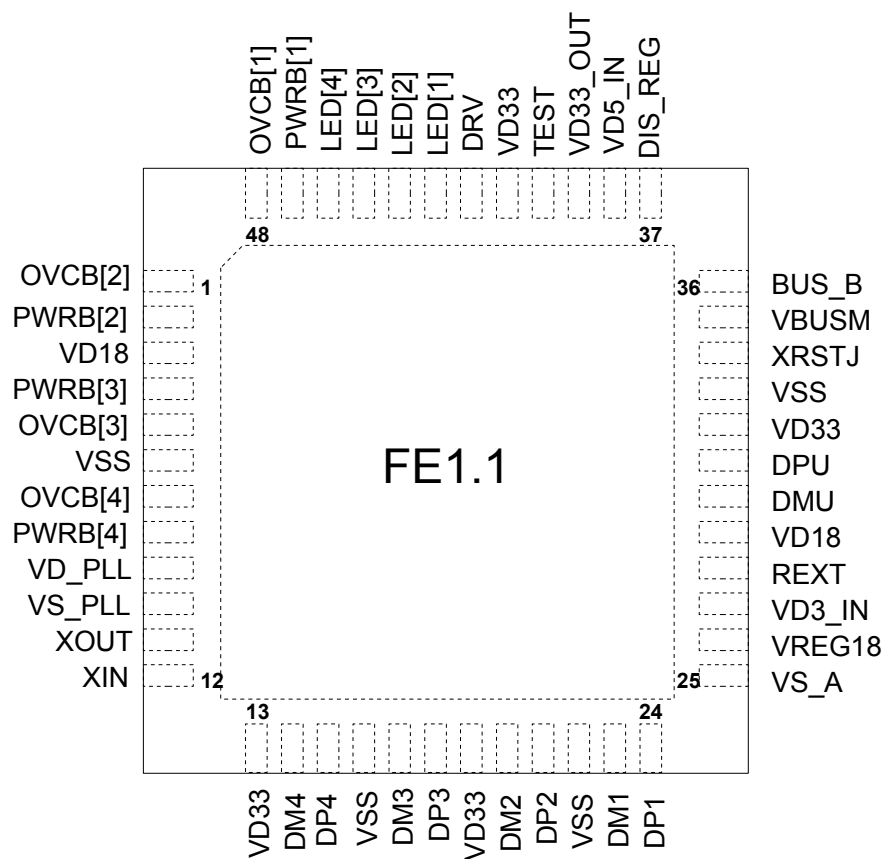


Fig. 3: 48-Pin QFN Pin Assignment

PIN DESCRIPTION TABLE

Pin Name	Pin No.	Type	Function	Note
OVCB[4:1]	7, 5, 1, 48	I	Over Current Indicators, active low, for each corresponding downstream facing port. When <i>Global Over-Current Protection</i> mode being selected with PWRB[4] tied to ground, only OVCB[1] is used, and all the other pins should be tied to ground.	2
PWRB[3:1]	4, 2, 47	O	Downstream Device Power Enable, active low, for each corresponding downstream device. When <i>Ganged Power Switching</i> mode being selected, with PWRB[4] tied to ground, only PWRB[1] is used.	2
PWRB[4]	8	I/O	When this pin been tied to ground, the <i>Global Over-Current Protection</i> and <i>Ganged Power Control</i> mode is selected. In this mode, only OVCB[1] and PWRB[1] are effective. Otherwise, it is Downstream Device Power Enable, active low, for the 4 th downstream facing port.	2
VD_PLL	9	P	1.8V power for PLL.	
VS_PLL	10	P	Ground for PLL.	
XOUT	11	OSC	12 MHz Crystal Oscillator output	1
XIN	12	OSC	12 MHz Crystal Oscillator input.	1
VD33	13, 19, 32, 41	P	3.3V Power	
DM4	14	UT	The D- pin for the 4 th Downstream Facing Port.	
DP4	15	UT	The D+ pin for the 4 th Downstream Facing Port.	
VSS	6, 16, 22, 33	P	Ground	
DM3	17	UT	The D- pin for the 3 rd Downstream Facing Port.	
DP3	18	UT	The D+ pin for the 3 rd Downstream Facing Port.	
DM2	20	UT	The D- pin for the 2 nd Downstream Facing Port.	
DP2	21	UT	The D+ pin for the 2 nd Downstream Facing Port.	
DM1	23	UT	The D- pin for the 1 st Downstream Facing Port.	
DP1	24	UT	The D+ pin for the 1 st Downstream Facing Port.	
VS_A	25	P	Analog Ground.	
VREG18	26	P	1.8V power output from integrated 3.3V→1.8V regulator – a 10μF decoupling capacitor is required.	
VD3_IN	27	P	3.3V power input for 3.3V→1.8V integrated regulator.	
REXT	28		A 2.7KΩ (± 1%) resister should be connected to VS_A to provide internal bias reference.	
VD18	3, 29	P	1.8V Power	

DMU	30	UT	The D- pin of the Upstream Facing Port.	
DPU	31	UT	The D+ pin of the Upstream Facing Port.	
XRSTJ	34	I	External Reset, active low, is an optional source of chip reset signal, beside the build-in Power-On-Reset. The minimum low pulse width is 10 μ s.	
VBUSM	35	I	The V _{BUS} Monitor of upstream facing port.	
BUS_B	36	I	Bus power indicator, active low, when no local power presented.	
DIS_REG	37	I	Disable Built-In 5V→3.3V Regulator – tie to 3.3V to disable the embedded 5V→3.3V regulator.	
VD5_IN	38	P	5V power input for integrated 5V→3.3V regulator.	
VD33_OUT	39	P	3.3V power output from integrated 5V→3.3V regulator – a 10 μ F decoupling capacitor is required.	
TEST	40	I	Test Mode Enable should be tied to ground for normal operation.	
DRV	42	I/O	LED Drive Control – when tied to ground, the support of PORT_INDICATOR (LED) is disabled; otherwise, together with LED[4:1], it controls the illumination of LED's.	3
LED[4:1]	46, 45, 44, 43	I/O	Port Indicator (LED) Control – one pin for each downstream port. If tied to ground, it indicates the device attached to the corresponding port is a <i>Non-Removable</i> device and no LED is supported. If connected to the Green LED and Amber LED, it controls their illumination according to the Hub Class Specification.	3

Type Abbreviation –

I : Input; O : Output; I/O : Input/Output; P : Power/Ground; UT: USB Transceiver.

Note 1 – Crystal Requirements

- Frequency accuracy: 12MHz \pm 50ppm
- Load capacitance: 16pF ~ 20pF

Note 2 – Power Control Switch And Over-Current Protection Configuration

Both the power control mode and over-current protection mode are configured by the PWRB[4] pin. To select *Ganged Power Control Mode* and *Global Over-Current Protection Mode*, the PWRB[4] should be tied to ground, as shown on the left part of Fig. 4. In this case, the over-current indicator is sampled by OVCB[1] and the power switch for downstream ports is controlled by PWRB[1]. The rest of the OVCB, 4 to 2, must be tied to ground and the PWRB, 3



and 2, left unconnected. The power switch of the left part of Fig. 4 is not really necessary, unless power-off downstream devices during hub reset is required. It is only placed here to demonstrate how the PWRB[1] works in this mode.

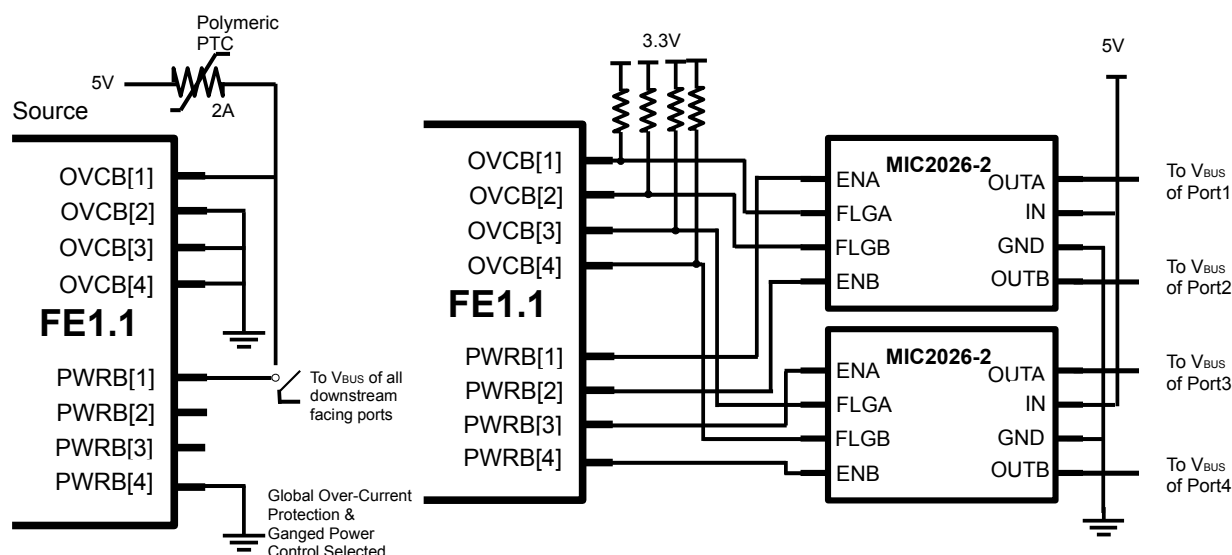


Fig. 4: Power Control & Over-Current Protection Configuration

For more delicate power management of downstream devices, the *Individual Power Control Mode* and *Individual Over-Current Protection Mode* could be implemented. As depicted by the right part of Fig. 4, two Dual-Channel Power Distribution Switch with current sensing and limiting capability are used. In this configuration, the FE1.1 will automatic recognize that the Individual mode is selected and report to the host as such in the Hub Descriptor Table.

Note 3 – LED Configuration

The supporting of *Port Indicators* – one Green LED and one Amber LED for each downstream port, is optional and could be configured by the DRV pin. If LED is not required, the DRV should be tied to ground to disable this option, as shown in the left part of the following fig. 5. The LED[n] pins could be either left unconnected to denote removable downstream devices, or tied to ground to identify that the corresponding port is attached by a non-removable device, as shown by port 4.



To fully support PORT_INDICATOR as USB Specification Rev. 2.0 defined, the LED's should be connected as the right part of the fig. 5. It is important that the direction of all the LED's must be connected as shown. Otherwise, the Green/Amber light would not function as defined by the USB 2.0 specifications. The maximum load current of each LED is 3mA. The LED[n] pin could also be tied to ground to indicate that the device attached to port n is a non-removable device. If this be case, no LED could be connected to that pin – as demonstrated by port 4.

An optional *Hub Active* LED could be implemented between DRV pin and ground. This light would go on whenever the hub is configured by the host driver, or wake-up from suspend mode. It will go off whenever the hub switch into suspend mode or unconfigured by the host.

The LED[1] of the right part of fig. 4 demonstrate that the LED could be omitted without affecting the normal function. That is, the host would still identify this hub as supporting port indicators, the Hub Active LED would illuminate as normal, and the port 1 would not be considered as non-removable.

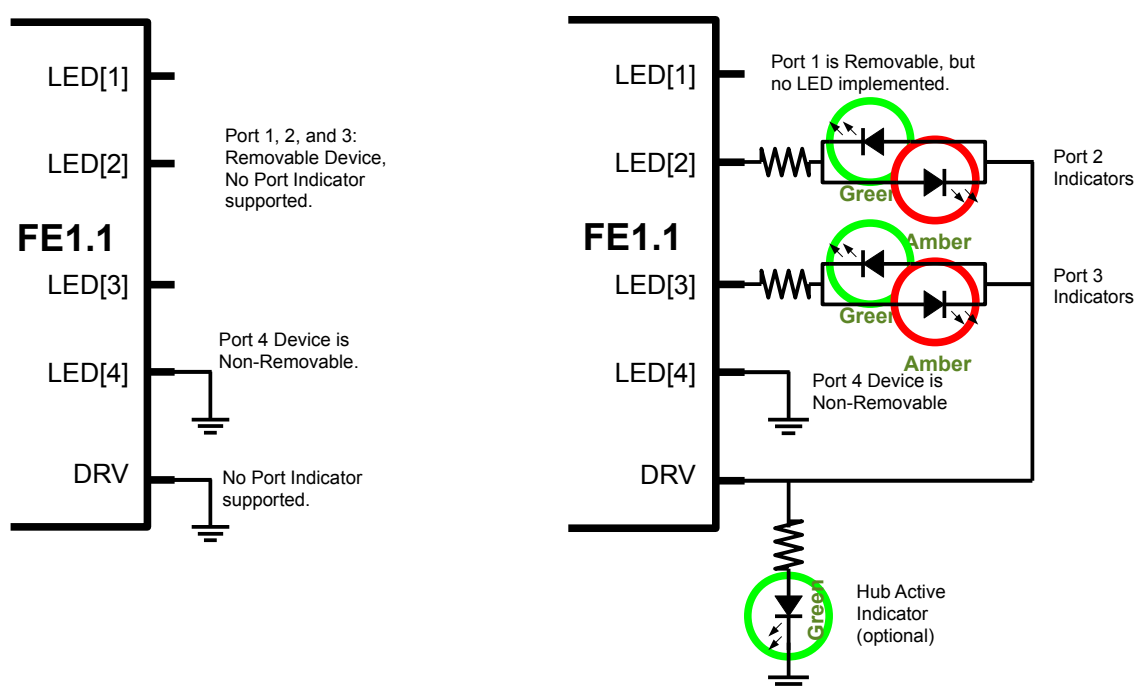


Fig. 5: Port Indicators And Removable Device Configurations

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	+150	°C
Power Supply Voltage	VD5_IN VD33 & VD3_IN VD18 & VD_PLL	-0.5 -0.5 -0.5	+6.0 +4.0 +2.5	V
ESD Human Body Mode		-2000	2000	V
ESD Machine Mode		-200	200	V
ESD Charged Device Mode		-500	500	V
Latch Up		-200	200	mA

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	0		70	°C
Case Temperature (LQFP-48 package)	TC _{LQFP}	0		95	°C
Case Temperature (QFN-48 package)	TC _{QFN}	0		80	°C
Operating voltage	VD5_IN VD33 & VD3_IN VD18 & VD_PLL	4.5 3.0 1.62	5.0 3.3 1.8	5.5 3.6 1.98	V
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
Threshold voltage of digital input	VTH	1.45	1.58	1.74	V
Low-to-High level of Schmitt-trigger input	VT+	1.44	1.5	1.56	V
High-to-Low level of Schmitt-trigger input	VT-	0.89	0.94	0.99	V
LOW level voltage of digital output@4mA	VOL			0.4	V
HIGH level voltage of digital output@4mA	VOH	2.4			V
XIN input capacitance	Cin		32		pF
Internal Pull-Up Resister Range	RPU	39	65	116	KΩ

***EXTENDED OPERATING RANGES***

Product with order code of AQFP48AT is Final Tested (FT) at *Room Temperature, 85°C, and -40°C.*

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	-40	25	85	°C

POWER CONSUMPTION

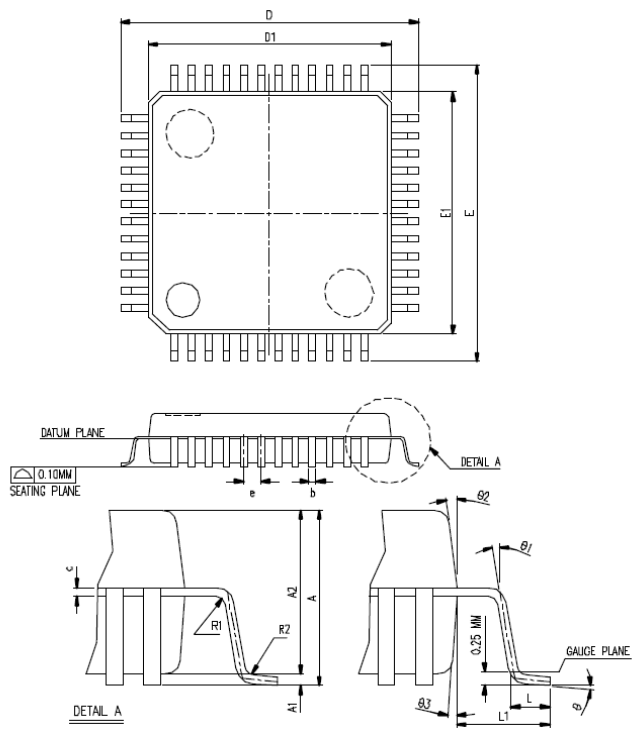
DC SUPPLY CURRENT

Symbol	Condition			Typical	Unit
	Active	Host	Devices		
I_suspend	Suspend			620	uA
I _{cc}	4	Full-Speed	4x Full-Speed	26	mA
		High-Speed	4x High-Speed	84	mA
		High-Speed	4x Full-Speed	40	mA
	3	Full-Speed	3x Full-Speed	26	mA
		High-Speed	3x High-Speed	73	mA
		High-Speed	3x Full-Speed	40	mA
	2	Full-Speed	2x Full-Speed	26	mA
		High-Speed	2x High-Speed	62	mA
		High-Speed	2x Full-Speed	39	mA
	1	Full-Speed	1x Full-Speed	26	mA
		High-Speed	1x High-Speed	51	mA
		High-Speed	1x Full-Speed	39	mA
	No active	Full-Speed	None	26	mA
		High-Speed	None	39	mA

Note: The power consumption is measured when the bus is in IDLE state – there is no activities other than the Start-Of-Frame (SOF) and INTERRUPT-IN packets for the hub itself on the bus. The peak power consumption varies depending upon the system configuration, type of operations, and over-all bus utilization.



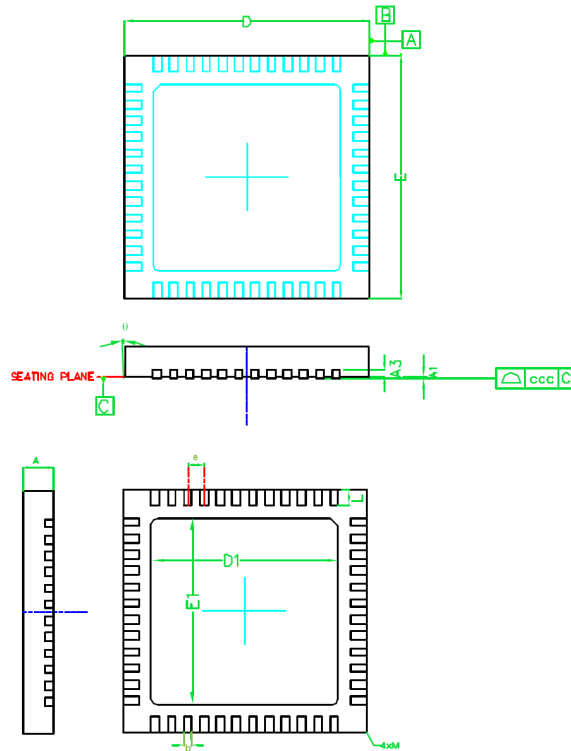
PACKAGE DRAWING I – 48-PIN LQFP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
e	0.50 BASIC			0.020 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R2	0.08		0.20	0.003		0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBC)					

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE.
" D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

PACKAGE DRAWING I – 48-PIN QFN



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.010	0.030
A3	---	0.20REF.	---
b	0.15	0.20	0.25
D	5.95	6.00	6.03
D1	---	4.60BSC	---
E	5.95	6.00	6.03
E1	---	4.60BSC	---
e	---	0.40BSC	---
L	0.35	0.40	0.45
θ	-12	---	0
ccc	---	0.08	---
M	---	---	0.05
Burr	0	0.030	0.060

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